Scheme – I

Sample Question Paper

Program Name	: Electronics and Computer Engineering Program Group
Program Code	: CO/CM/CW/DE/EJ/ET/EN/EX/IE/IS/IC/MU
Semester	: Third
Course Title	: Digital Techniques
Marks	: 70

22320

Time: 3 Hrs.

Instructions:

(1) All questions are compulsory.

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data if necessary.

(5) Preferably, write the answers in sequential order.

Q.1) Attempt any FIVE of the following.   **10 Marks**

a) Write the base of the following number systems: Decimal, Binary, Octal, and Hexadecimal.

b) Draw symbol and write the truth table of JK flip flop.

c) State the necessity of multiplexer.

d) Write excitation table of D flip flop.

e) List any two specifications of IC- DAC 0808.

f) Draw three variable K-map format.

g) Define modulus of a counter? Write down the number of flip flops required for mod-5 counter?

Q.2) Attempt any THREE of the following.   **12 Marks**

a) For the given figure No. 1, derive the Boolean expression of Y.
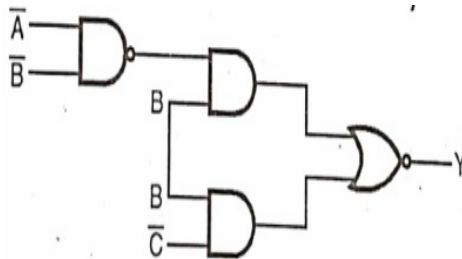

Figure No. 1

b) Draw the circuit diagram of BCD to 7 segment decoder and write its truth table.

c) Draw the block diagram of Programmable Logic Array.

d) Minimize the following expression using K-map.

$f (P, Q, R, S) = \Sigma\, m\, (0, 1, 4, 5, 7, 8, 9, 12, 13, 15)$.

Q.3) Attempt any THREE of the following.   **12 Marks**

a) Realize the following logic operations using only NAND gates: AND, OR, NOT.

b) Compare TTL and CMOS logic families on the basis of following:

    i) Propogation delay ii) Power dissipation iii) Fan-out iv) Basic gate

c) Describe the operation of 4- bit universal shift register with the help of block diagram.

d) Calculate analog output of 4 bit DAC for digital input is 1011. Assume $V_{FS} = 5V$.

Q.4) Attempt any THREE of the following.   **12 Marks**

a) Draw the symbol and write logic expression and truth table of the two input universal logic gates.

b) Describe function of full subtractor circuit with its truth table, K-map simplification and logic diagram.

c) Design 1: 16 demultiplexer using 1: 4 demultiplexers.

d) Describe the working of Master-Slave JK Flip-Flop with Truth Table and Logic diagram.

e) The output of 8 bit DAC varies between +10V and -10V. Calculate the following:

    i) Resolution   ii) Percentage resolution.

Q.5) Attempt any TWO of the following.   **12 Marks**

a) Design 3-bit synchronous counter and draw output waveform.

b) Compare the following (Any three points)   .

    (i) Volatile with Non-Volatile memory.

    (ii) SRAM with DRAM memory.

c) Convert the following :

    i) $(5C7)_{16} = (?)_{10}$

    ii) $(2598)_{10} = (?)_{16}$

    iii) $(10110)_2 = (?)_{10} = (?)_{16}$

Q.6) Attempt any TWO of the following.   **12 Marks**

    a)   Describe the procedure to design MOD-6 counter using IC 7490 in brief.

    b)   Design a four bit BCD adder using IC 7483 and NAND gates only.

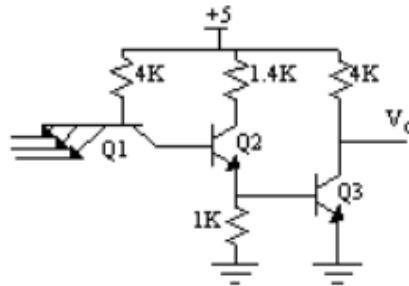   c)   Identify the circuit shown as figure no.2 and explain its working.

Figure No.2.

Scheme – I

Sample Test Paper - I

Program Name	: Electronics and Computer Engineering Program Group	
Program Code	: CO/CM/CW/DE/EJ/ET/EN/EX/IE/IS/IC/MU	**22320**
Semester	: Third	
Course Title	: Digital Techniques	
Marks	: 20	**Time: 1 Hour**

Instructions:

    (1) All questions are compulsory.
    (2) Illustrate your answers with neat sketches wherever necessary.
    (3) Figures to the right indicate full marks.
    (4) Assume suitable data if necessary.
    (5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR.   **08 Marks**

    a) Convert the following Binary number into Gray code.

        (i) 1111   (ii) 1101001

    b) Draw the Symbol and write the Truth Table of Universal Gates.

    c) Define following characteristics of logic families :

           i) Fan in   ii)Fan out

    d) State commutative and associative laws for the binary numbers.

    e) Draw the block diagram and write the Truth Table of Half Subtractor.

    f) Define 1's and 2's Complement of Binary Number with example.

Q.2 Attempt any THREE.   **12 Marks**

    a) Perform the following subtraction using 1's and 2's complement method:

        i) $(52)_{10} - (65)_{10}$ ii) $(101011)_2 - (11010)_2$

    b) State and prove De Morgan's Theorems.

    c) Reduce the following Boolean expression using Boolean laws.

        $Y=AB+\overline{A}B+A\overline{B}+\overline{AB}$

    d) Compare the parameters of TTL, ECLand CMOS logic families (any 4 points).

    e) Describe the operation of TTL logic circuit working as NAND gate.

    f) Design Full Adder using K-map and Truth Table.

Scheme – I

Sample Test Paper – II

Program Name	: **Electronics and Computer Engineering Program Group**	
Program Code	: **CO/CM/CW/DE/EJ/ET/EN/EX/IE/IS/IC/MU**	
Semester	: **Third**	**22320**
Course Title	: **Digital Techniques**	
Marks	: **20**	**Time:1 Hour**

Instructions:

    (1) All questions are compulsory.
    (2) Illustrate your answers with neat sketches wherever necessary.
    (3) Figures to the right indicate full marks.
    (4) Assume suitable data if necessary.
    (5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR.   **08 Marks**

    a) Draw Block diagram of 4:1 Multiplexer and write its truth table.
    b) Explain the triggering methods used for digital circuits.
    c) Identify function of following ICs. (i) 74151(ii) 74155
    d) Draw symbol and write the truth table of JK flip flop.
    e) State any two applications of PLA's.
    f) Compare Static RAM and Dynamic RAM.

Q.2 Attempt any THREE.   **12 Marks**

    a) Realize the following function using demultiplexer :
            $F1 = \Sigma \, m \, (1, 2, 5, 6, 7, 11, 14)$
            $F2 = \pi \, M \, (0, 1, 2, 5, 6, 7, 8, 11, 12, 15)$
    b) Describe the operation of 4 bit SISO shift register with the help of block diagram, truth table and timing diagram.
    c) Describe the operation of 3 bit synchronous up counter with Truth Table and Logic diagram
    d) Describe the working principle of Successive approximation type ADC with the help of block diagram.
    e) Design a four bit BCD adder using IC 7483 and NAND gates.
    f) Give the function of the following terminals of IC 7447.
      i) LT ii) RBI   iii) BI   iv) RBO

Scheme – I

Sample Question Paper

Program Name	: Electronics and Computer Engineering Program Group	
Program Code	: CO/CM/CW/DE/EJ/ET/EN/EX/IE/IS/IC/MU	
Semester	: Third	**22320**
Course Title	: Digital Techniques	
Marks	: 70	Time: 3 Hrs.

Instructions:

    (1) All questions are compulsory.

    (2) Illustrate your answers with neat sketches wherever necessary.

    (3) Figures to the right indicate full marks.

    (4) Assume suitable data if necessary.

    (5) Preferably, write the answers in sequential order.

Q.1) Attempt any FIVE of the following.   **10 Marks**

    a)   Write the base of the following number systems: Decimal, Binary, Octal, and Hexadecimal.

    b)   Draw symbol and write the truth table of JK flip flop.

    c)   State the necessity of multiplexer.

    d)   Write excitation table of D flip flop.

    e)   List any two specifications of IC- DAC 0808.

    f)   Draw three variable K-map format.

    g)   Define modulus of a counter? Write down the number of flip flops required for mod-5 counter?

Q.2) Attempt any THREE of the following.   **12 Marks**

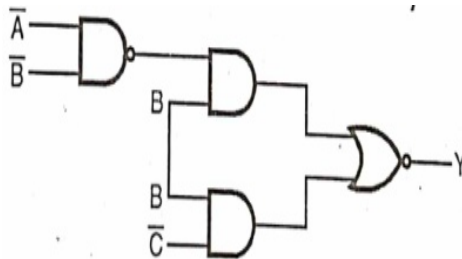   a)   For the given figure No. 1, derive the Boolean expression of Y.

Figure No. 1

b) Draw the circuit diagram of BCD to 7 segment decoder and write its truth table.

c) Draw the block diagram of Programmable Logic Array.

d) Minimize the following expression using K-map.

$f (P, Q, R, S) = \Sigma m (0, 1, 4, 5, 7, 8, 9, 12, 13, 15)$.

Q.3) Attempt any THREE of the following.   **12 Marks**

a) Realize the following logic operations using only NAND gates: AND, OR, NOT.

b) Compare TTL and CMOS logic families on the basis of following:

   i) Propogation delay ii) Power dissipation iii) Fan-out iv) Basic gate

c) Describe the operation of 4- bit universal shift register with the help of block diagram.

d) Calculate analog output of 4 bit DAC for digital input is 1011. Assume $V_{FS}= 5V$.

Q.4) Attempt any THREE of the following.   **12 Marks**

a) Draw the symbol and write logic expression and truth table of the two input universal logic gates.

b) Describe function of full subtractor circuit with its truth table, K-map simplification and logic diagram.

c) Design 1: 16 demultiplexer using 1: 4 demultiplexers.

d) Describe the working of Master-Slave JK Flip-Flop with Truth Table and Logic diagram.

e) The output of 8 bit DAC varies between +10V and -10V. Calculate the following:

   i) Resolution   ii) Percentage resolution.

Q.5) Attempt any TWO of the following.   **12 Marks**

a) Design 3-bit synchronous counter and draw output waveform.

b) Compare the following (Any three points)   .

   (i) Volatile with Non-Volatile memory.

   (ii) SRAM with DRAM memory.

c) Convert the following :

   i) $(5C7)_{16} = (?)_{10}$

   ii) $(2598)_{10} = (?)_{16}$

   iii) $(10110)_2 = (?)_{10} = (?)_{16}$

Q.6) Attempt any TWO of the following.   **12 Marks**

    a)   Describe the procedure to design MOD-6 counter using IC 7490 in brief.

    b)   Design a four bit BCD adder using IC 7483 and NAND gates only.

    c)   Identify the circuit shown as figure no.2 and explain its working.
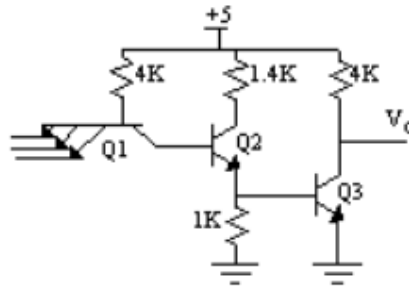
Figure No.2.

Scheme – I

Sample Test Paper - I

Program Name	: Electronics and Computer Engineering Program Group
Program Code	: CO/CM/CW/DE/EJ/ET/EN/EX/IE/IS/IC/MU
Semester	: Third
Course Title	: Digital Techniques
Marks	: 20

22320

Time: 1 Hour

Instructions:

(1) All questions are compulsory.
(2) Illustrate your answers with neat sketches wherever necessary.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary.
(5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR.   **08 Marks**

   a) Convert the following Binary number into Gray code.

      (i) 1111   (ii) 1101001

   b) Draw the Symbol and write the Truth Table of Universal Gates.

   c) Define following characteristics of logic families :

        i) Fan in   ii)Fan out

   d) State commutative and associative laws for the binary numbers.

   e) Draw the block diagram and write the Truth Table of Half Subtractor.

   f) Define 1's and 2's Complement of Binary Number with example.

Q.2 Attempt any THREE.   **12 Marks**

   a) Perform the following subtraction using 1's and 2's complement method:

      i) $(52)_{10} - (65)_{10}$ ii) $(101011)_2 - (11010)_2$

   b) State and prove De Morgan's Theorems.

   c) Reduce the following Boolean expression using Boolean laws.

      $Y=AB+\overline{A}B+A\overline{B}+\overline{A}\overline{B}$

   d) Compare the parameters of TTL, ECLand CMOS logic families (any 4 points).

   e) Describe the operation of TTL logic circuit working as NAND gate.

   f) Design Full Adder using K-map and Truth Table.

Scheme – I

Sample Test Paper – II

Program Name	: Electronics and Computer Engineering Program Group
Program Code	: CO/CM/CW/DE/EJ/ET/EN/EX/IE/IS/IC/MU
Semester	: Third
Course Title	: Digital Techniques
Marks	: 20

22320

Time:1 Hour

Instructions:

    (1) All questions are compulsory.
    (2) Illustrate your answers with neat sketches wherever necessary.
    (3) Figures to the right indicate full marks.
    (4) Assume suitable data if necessary.
    (5) Preferably, write the answers in sequential order.

Q.1 Attempt any FOUR.   **08 Marks**

    a) Draw Block diagram of 4:1 Multiplexer and write its truth table.
    b) Explain the triggering methods used for digital circuits.
    c) Identify function of following ICs. (i) 74151(ii) 74155
    d) Draw symbol and write the truth table of JK flip flop.
    e) State any two applications of PLA's.
    f) Compare Static RAM and Dynamic RAM.

Q.2 Attempt any THREE.   **12 Marks**

    a) Realize the following function using demultiplexer :
            $F1 = \Sigma\ m\ (1, 2, 5, 6, 7, 11, 14)$
            $F2 = \pi\ M\ (0, 1, 2, 5, 6, 7, 8, 11, 12, 15)$
    b) Describe the operation of 4 bit SISO shift register with the help of block diagram, truth table and timing diagram.
    c) Describe the operation of 3 bit synchronous up counter with Truth Table and Logic diagram
    d) Describe the working principle of Successive approximation type ADC with the help of block diagram.
    e) Design a four bit BCD adder using IC 7483 and NAND gates.
    f) Give the function of the following terminals of IC 7447.
       i) LT ii) RBI iii) BI iv) RBO

22320

Seat No.

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1.   **Attempt any FIVE of the following:**   **10**

a) Write the radix of binary, octal, decimal and hexadecimal number system.

b) Draw the circuit diagram for AND and OR gates using diodes.

c) Write simple examples of boolean expression for SOP and POS.

d) State the necessity of multiplexer.

e) Draw logic diagram of T flip-flop and give its truth table.

f) Define modulus of a counter. Write the numbers of flip flops required for Mod-6 counter.

g) State function of preset and clear in flip flop.

Marks

2. **Attempt any THREE of the following:** **12**

a) Draw the block diagram of Programmable Logic Array.

b) Convert -

(i) $(255)_{10} = (?)_{16} = (?)_8$

(ii) $(157)_{10} = (?)_{BCD} = (?)_{Excess3}$

c) Draw the symbol, truth table and logic expression of any one universal logic gate. Write reason why it is called universal gate.

d) Minimize the following expression using K-Map.

$f(A, B, C, D) = \Sigma m (0, 1, 2, 4, 5, 7, 8, 9, 10)$

3. **Attempt any THREE of the following:** **12**

a) Compare TTL and CMOS logic families on the basis of following:

(i) Propagation delay

(ii) Power Dissipation

(iii) Fan-out

(iv) Basic gate

b) Describe the function of Full Adder Circuit using its truth table, K-Map simplification and logic diagram.

c) Realize the basic logic gates, NOT, OR and AND gates using NOR gates only.

d) Describe the working of JK flip-flop with its truth table and logic diagram.

4. **Attempt any THREE of the following:** **12**

a) Draw and explain working of 4 bit serial Input parallel Output shift register.

b) Draw 16:1 MUX tree using 4:1 MUX.

c) Calculate analog output of 4 bit DAC for digital input 1101. Assume $V_{FS} = 5V$.

d) State De Morgan's theorem and prove any one.

e) Design one digit BCD Adder using IC 7483.

Marks

5. **Attempt any TWO of the following:** **12**

a) Subtract using 2's compliment method

$(35)_{10} - (5)_{10}$

b) Design a 4 bit synchronous counter and draw its logic diagram.

c) Describe the working of successive Approximation ADC. Define Resolution and conversion time associated with ADC.

6. **Attempt any TWO of the following:** **12**

a) Design 4 bit Binary to Gray code converter.

b) Compare the following (Any three points)

    (i) Volatile with Non-volatile memory

    (ii) SRAM with DRAM memory

c) Give block schematic of decade counter IC 7490. Design Mod-7 counter using this IC.

_____

22320

Seat No.

Instructions – (1) All Questions are *Compulsory*.

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Use of Non-programmable Electronic Pocket Calculator is permissible.

(7) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1.   **Attempt any FIVE of the following:**   **10**

a) List the binary, octal and hexadecimal numbers for decimal no. 0 to 15.

b) Define fan-in and fan-out of a gate.

c) Compare between synchronous and asynchronous counter (any two points).

d) State two specification of DAC.

e) Write the gray code to given no. $(\perp\perp0\perp)_2$ = (?) Gray.

f) Define encoder, write the IC number of IC used as decimal to BCD encoder.

g) Draw the logical symbol of EX-OR and EX-NOR gate.

Marks

2.   **Attempt any THREE of the following:**   **12**

a) Convert:

(i) $(AD92 \cdot BC\ A)_{16}$ = $(?)_{10}$ = $(?)_8$ = $(?)_2$

b) Simplify the following and realize it

$$Y = A + \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}\,\overline{C} + ABC + \overline{A}\,\overline{B}$$

c) Explain the flowing characteristics w.r.t logic families:

(i)   Noise margin

(ii)   Power dissipation

(iii) Figure of merit

(iv) Speed of operation

d) Draw logic diagram of half adder circuit.

3.   **Attempt any THREE of the following:**   **12**

a) Draw the circuit of successive approximation type ADC and explain it's working.

b) Describe the operation of R-5 flip-flop using NAND gates only.

c) Give classification of memory and compare RAM and ROM (any four points).

d) State the applications of shift register.

4.   **Attempt any THREE of the following:**   **12**

a) Subtract the given number using 2's complement method:

(i) $(\perp\perp 0\perp\perp)_2 - (\perp\perp\perp 00)_2$

(ii) $(\perp 0\perp 0)_2 - (\perp 0\perp)_2$

b) State De-Morgan's theorem and prove any one.

c) Compare between PLA and PAL.

d) Reduce the following expression using K-map and implement it

$$F\ (A,\ B,\ C,\ D) = \pi\ M\ (1,3,5,7,8,10,14)$$

e) Describe the working of J-K flip-flop and state the race around condition.

Marks

5. **Attempt any <u>TWO</u> of the following:** **12**

   a) Design BCD to seven segment decoder using IC 7447 with its truth table.

   b) Describe the working of 4 bit universal shift register.

   c) Design basic logic gates using NAND and NOR gate.

6. **Attempt any <u>TWO</u> of the following:** **12**

   a) Design a mod-6 Asynchronous counter with truth-table and logic.

   b) Design $\perp$:8 demultiplexer using 1:4 demultiplexer.

   c) Draw the circuit diagram of 4 bit R-2R ladder DAC and obtain its output voltage expression.

————

22320

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1.   **Attempt any FIVE of the following:**   **10**

a) Convert $(D8F)_{16}$ into binary and octal.

b) Draw Symbol, Truth Table and logic equation of Ex-OR gate.

c) State the DeMorgan's Theorems.

d) Convert the following expression into standard SOP form.
    $Y = AB + A\overline{C} + BC$

e) Draw symbol and write truth table of D and T Flip Flop.

f) Write down number of flip flops are required to count 16 clock pulses.

g) List the types of DAC

Marks

2. Attempt any THREE of the following: **12**

a) Perform the subtraction using 2'S Complement methods.

$(52)_{10} - (65)_{10}$

b) Simplify the following Boolean Expression and Implement using logic gate.

$AB\overline{C}\,\overline{D} + AB\overline{C}D + ABC\overline{D} + ABCD$

c) Minimize the four variable logic function using K map.

$f(A,B,C,D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

d) Implement the following functions using demultiplexer.

$f_1 = \Sigma m\ (0, 2, 4, 6)$

$f_2 = \Sigma m\ (1, 3, 5)$

3. Attempt any THREE of the following: **12**

a) Realize the following logic expressions using only NAND gates.

(i) OR

(ii) AND

(iii) NOT

b) Draw binary to gray converter and write its truth table.

c) Describe the working of JK flip flop with truth table and logic diagram.

d) Describe the working of 4 bit SISO (serial in serial out) Shift Register with diagram and waveform if input is 01101.

4. Attempt any THREE of the following: **12**

a) Design a full Adder using Truth Table and K-map.

b) Describe the working of ring counter using D flip flop with diagram and waveforms.

c) Draw block diagram of programmable logic Array.

d) Compare the following:

(i) Volatile with Non Volatile.

(ii) EPROM with EEPROM.

e) Describe the working principle of successive approximation ADC.

Marks

5. Attempt any TWO of the following: **12**

  a) (i) Convert the following binary number $(11001101)_2$ into Gray Code and Excess-3 Code.

     (ii) Perform the BCD Addition.

         $(17)_{10} + (57)_{10}$

     (iii) Perform the binary addition.

         $(10110 \cdot 110)_2 + (1001 \cdot 10)_2$

  b) Design a 4bit ripple counter using JK flip flop, with truth table and waveforms.

  c) Calculate the analog output for 4 bit weighted register type DAC for inputs

     (i) 1011

     (ii) 1001

     Assume (V_{fs}) full scale range of voltage is 5V

6. Attempt any TWO of the following: **12**

  a) Compare TTL, CMOS and ECL logic family on the following points.

     (i) Basic Gates

     (ii) Propogation delay

     (iii) Fan out

     (iv) Power Dissipation

     (v) Noise immunity

     (vi) Speed Power Product.

  b) Design a BCD adder using IC 7483.

  c) Design a 3 bit synchronous counter using JK FlipFlop.

————

11920

3 Hours / 70 Marks

17320

Instructions –   (1) All Questions are *Compulsory.*

     (2) Answer each next main Question on a new page.

     (3) Illustrate your answers with neat sketches wherever necessary.

     (4) Figures to the right indicate full marks.

     (5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1.   a)   **Attempt any <u>SIX</u> of the following:**   12

     (i)   Represent the decimal no. 27 in binary form using -

       (1) BCD code

       (2) Gray code

     (ii)   Draw the logic diagram of half subtractor and write its truth table.

     (iii)   Draw the symbol of Ex-OR gate along with truth table.

     (iv)   What is meant by modulas of a counter?

     (v)   Define the following specifications of DAC.

       (1) Resolution

       (2) Linearity

     (vi)   Compare EPROM and flash memory. (any two points)

     (vii)   Draw the logical diagram of bit memory cell using NAND gates only.

     (viii)   List the types of ADC's and DAC's.

Marks

b) **Attempt any TWO of the following:** 8

    (i) Perform the binary subtraction using 1's and 2's compliment method.

$$(52)_{10} - (65)_{10}$$

    (ii) Define priority encoder. Draw the truth table of decimal to BCD encoder.

    (iii) Write the difference between combinational and sequential logic circuit.

2. **Attempt any FOUR of the following:** 16

a) Perform the following BCD operation

    (i) $(37)_{10} + (65)_{10}$

    (ii) $(46)_{10} - (73)_{10}$ [use 10's compliment method]

b) Draw and explain the circuit diagram of 1:4 demultiplexer using logic gates.

c) Why NOR gate is called as Universal gate? Implement basic gates using NOR gate.

d) Explain full adder with its truth table, K-map specification and logic diagram.

e) Explain the working of 4 bit ring counter with a neat diagram.

f) Compare between R-2R ladder DAC and weighted resistor DAC. (any four points)

3. **Attempt any FOUR of the following:** 16

a) Convert the following:

    (i) $(5C7)_{16} = (?)_{10}$

    (ii) $(1011.110)_2 = (?)_{10}$

    (iii) $(43)_8 = (?)_{10}$

    (iv) $(6AC)_{16} = (?)_2$

b) Simplify the following equations with Boolean Law.

    (i) $y = A\overline{B} + \overline{A}B + AB + \overline{A}\overline{B}$

    (ii) $y = A\overline{B}C + \overline{A}BC + ABC$

c) Minimize the following expression using K-map.

(i) $f(A, B, C) = \Sigma m (0, 1, 3, 4, 5, 7)$

(ii) $f(A, B, C, D) = \pi M (0, 2, 7, 8, 9, 10, 13)$

d) Identify the following circuit as combinational circuit OR sequential circuit.

(i) 3 bit ring counter

(ii) Full Adder

(iii) Clocked J-K FF

(iv) 4:1 Mux

e) Describe the working of single slope ADC with block diagram.

f) State different types of ROM and explain any one in detail.

4. **Attempt any FOUR of the following:** **16**

a) Convert the following numbers into binary and add them.

$(173)_8 + (741)_8$

b) Compare Totem pole and Open Collector outputs. (any four points)

c) Describe the working of BCD to 7 segment decoder with truth table and circuit diagram.

d) Draw 3 bit asynchronous up counter with truth table and timing diagram.

e) Describe the working of Dual Slope ADC.

f) Compare Volatile and Non-volatile Memory. (any four points)

5. **Attempt any FOUR of the following:** **16**

a) State and prove first and second De-morgan's theorem.

b) Compare TTL and CMOS logic families on the basis of size, power consumption, speed, and fan out.

c) Design 32:1 multiplexer using 16:1 multiplexer and one 2:1 multiplexer.

Marks

d) Draw logic diagram of 4 bit SISO shift register and its output waveform.

e) What is race-around condition in J-K Flip Flop? How is it avoided using MS JK - Flip Flop?

f) Explain R-2R ladder network method of D\A conversion with neat circuit diagram.

6. **Attempt any FOUR of the following:** 16

a) Realize the following Boolean expression using Basic gates.

(i) $y = AB + BC + \overline{A}\overline{B}$

(ii) $y = AB + AC$

b) Draw the block diagram of ALU IC 74181 and also write its operation.

c) Realize the following function using De-multiplexer.

(i) $F_1 = \Sigma m \ (0,1,3,7,11,13,15)$

(ii) $F_2 = \Sigma m \ (2,4,8,10,12)$

d) How IC 7490 can be used as a decade counter, explain with neat block diagram.

e) Calculate the analog output of a 4 bit DAC if the digital input is 1101. Assume $V_{FS} = 5V$.

f) Compare static RAM and Dynamic RAM (any four points).

_____

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Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1.   **Attempt any FIVE of the following:**   **10**

a) Convert $(1101011)_2 = ($ $)_{16}$ and

$(1111011)_2 = ($ $)_8$

b) List triggering methods used for triggering flip flops.

c) Define Minterm and Maxterm w.r.t. K-map.

d) Define shift register and list its types.

e) List any two specifications of IC-DAC 0808.

f) Draw logical circuit diagram of half adder circuit.

g) Write truth table of D type flip-flop.

                                                                              Marks

2.   Attempt any THREE of the following: **12**

a) Convert $(43)_{10}$ = (BCD)

                $(34)_{10}$ = (Excess-3)

                $(110111)_2$ = (Gray)

                $(11101)_2$ = (2's complement)

b) Draw logical diagram of full adder using K-map simplification and write truth table.

c) Draw the block diagram of programmable logic Array with proper labels.

d) Draw the circuit diagram of BCD to 7 - segment decoder and write truth table.

3.   Attempt any THREE of the following: **12**

a) State and prove two De-Morgan's Theorems.

b) Draw basic gates AND, OR and NOT using NAND gate only.

c) Draw 4 bit ring counter with truth table and its waveform.

d) Compare the following: (Any two points each)

    (i)   Volatile - Non volatile memory

    (ii) SRAM - DRAM memory

4.   Attempt any THREE of the following: **12**

a) Realize given boolean expression using basic gates and simplify same.

    y = AB + BC (B+C)

b) Design 4 bit binary to gray code converter. Using truth table.

c) Realize given expression using K-map

    $f(A, B, C, D = \Sigma m(3, 5, 7, 8, 10, 11, 12, 13)$

d) Draw JK master slave flip flop and explain its operations.

e) Calculate analog o/p of 4 bit DAC for digital input is 1100. Assume V_{FS} = 5 V

Marks

5. **Attempt any TWO of the following:** **12**

a) Draw and explain operation 4 bit universal shift register. Draw necessary waveforms.

b) Draw block diagram of Dual slope ADC and explain its working.

c) Subtract following using Two's complement method.

$(15)_{10} - (32)_{10}$

6. **Attempt any TWO of the following:** **12**

a) Design MOD-12 ripple counter. Write its truth table with waveform.

b) Design 16:1 MUX using 4:1 MUX.

c) Compare TTL and CMOS with following points.

(i) Fan IN

(ii) FAN OUT

(iii) Propogation delay

(iv) Power dissipation

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22320

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Use of Non-programmable Electronic Pocket Calculator is permissible.

(7) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1.   **Attempt any FIVE of the following :**   **10**

a) Write radix of binary, octal, hexadecimal number system.

b) State necessity of demultiplexer.

c) Draw symbol and write the truthtable for T-flipflop.

d) Compare between synchronous and asynchronous counter.

e) Write gray code to given number $(11111)_2 = (?)_{Gray}$

f) State two features of ADC IC0809.

g) Draw four variable K-map.

Marks

2. **Attempt any THREE of the following :** **12**

a) Sketch the given Boolean expression; use one AND gate one OR gate only $Y = AB + AC$.

b) Draw circuit diagram of BCD to seven segment decoder and write its truth table.

c) Draw the block diagram of programmable array logic.

d) Minimize following expression using K-map.

$f(A,B,C,D) = \Sigma m\,(1,5,6,7,11,12,13,15)$

3. **Attempt any THREE of the following :** **12**

a) Realize the following logic operation using only NOR gates : AND, OR, NOT.

b) Describe the operation of 4 bit serial in serial out shift register.

c) Calculate the analog output of 4 bit DAC if the digital input is 1101. Assume $V_{FS} = 5\,V$

d) Describe the working of SR flipflop with its truth table and logic diagram.

4. **Attempt any THREE of the following :** **12**

a) Draw symbol, truth table and logical output equation of OR and EX-OR gate.

b) Describe function of full adder circuit with its truth table and logical diagram.

c) Design 16:1 multiplexer using 4:1 multiplexer.

d) Describe working of Master-slave JK flipflop with truth table and logic diagram.

e) Compare between R-2R ladder DAC and weighted resistor DAC (Four points).

Marks

5. Attempt any TWO of the following : 12

a) Explain 3 bit asynchronous counter with output waveforms.

b) Compare following (Any three points)

i) RAM with ROM memory.

ii) EPROM with EEPROM memory.

c) Convert the following.

i) $(6AC)_{16} = (?)_{10}$

ii) $(2003)_{10} = (?)_{16}$

iii) $(228)_{10} = (?)_{BCD}$

6. Attempt any TWO of the following : 12

a) Give the block schematic of decade counter IC 7490. Design mod-7 counter using IC.

b) Design a four bit BCD adder using IC-7483 and NAND gate only.

c) Draw the circuit and explain the principle of TTL gate with totempole output

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Seat No.

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Figures to the right indicate full marks.

(4) Assume suitable data, if necessary.

(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. a) **Attempt any SIX of the following:** 12

   (i) Convert (AC) H into binary and octal.

   (ii) Draw symbol, Truth table and logical equation of Ex-OR gate.

   (iii) Draw logic diagram of half adder and write its logical equation.

   (iv) Draw symbol of positive edge triggered and negative.

   (v) Specify the function of –

   1) IC 74245

   2) IC 74151

   (vi) What is Flash memory?

   (vii) Write applications of DAC and ADC.

   (viii) List advantages of TTL logic family.

b) **Attempt any TWO of the following:**   8

    (i)   Perform binary subtraction using 2's complement method.

        $(12)_{10} - (08)_{10}$

    (ii)   Convert following expression into canonical SOP form

          $Y = A + BC + ABC$

    (iii) Draw excitation table for RS Flip-flop and JK filp-flop.
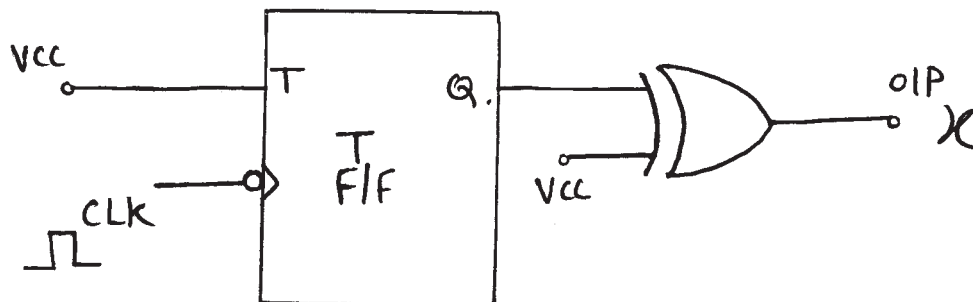
2.   **Attempt any FOUR of the following:**   16

   a) Compare TTL, ECL and CMOS logic family on following points:

    (i)   Basic gates

    (ii)   Component used

    (iii) Propagation delay

    (iv) Power dessipation

   b) Design half subtractor using truth table and k-map.

   c) Draw 4 bit left shift SISO register, truth table and waveforms for data 1011.

   d) Study the following circuit and draw waveforms for Q and x. consider last value of Q = 1.

last value of Q = 1.

Fig. No. 1

Marks

    e) Differentiate between weighted resistor method DAC and R-2R ladder DAC. (any four points)

    f) Find out Gray code and excess-3 code of given numbers.

        (i) $(28)_{10}$

        (ii) $(64)_{10}$

3.   **Attempt any <u>FOUR</u> of the following:**   **16**

    a) Minimize the following expression using k-map and realize it using basic logic gates.

$$Y = \sum m \ (1, 3, 4, 5, 6, 7)$$

    b) What is race around condition? How it can be avoided?

    c) Draw and explain the operation of 2 input totem pole TTL NAND gate with circuit diagram.

    d) (i)   Perform BCD addition.

$$(983)_{10} + (274)_{10}$$

        (ii) State the rules of BCD additions

    e) Draw and explain working of single slope ADC.

    f) Differentiate between

        (i)   Static RAM and dynamic RAM

        (ii) Volatile and Non-Volatile memory

4.   **Attempt any <u>FOUR</u> of the following:**   **16**

    a) (i)   Add binary numbers.

$$(10110 \cdot 110)_2 + (1001 \cdot 1)_2$$

        (ii) Multiply

$$(1110)_2 \times (101)_2$$

    b) Realize the following expression using only NOR gate.

$$Y = (ABC + \overline{B} + \overline{C}) \cdot C$$

Marks

c) Draw and explain working of single digit BCD adder using IC 7483.

d) Design a 3 bit synchronous up counter and draw it.

e) Draw single digit memory cell using NAND gates and explain working with truth table.

f) Identify function of IC 7481 and 2716 and draw its pin diagram.

5. **Attempt any FOUR of the following:** 16

a) Compare single slope ADC and dual slope ADC (any four points).

b) How are memories classified ? Explain any two types of memories.

c) Why NAND and NOR gates are called as universal gates. Derive basic gates using NOR gates only.

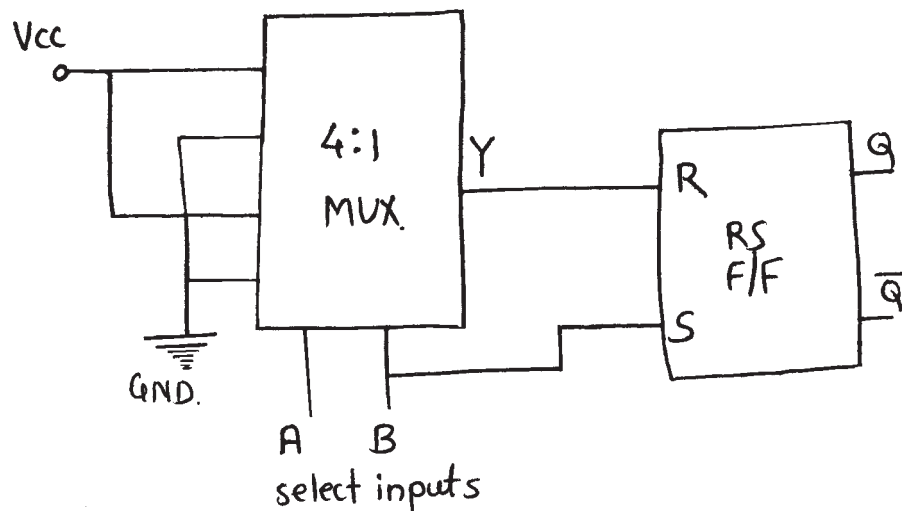d) Write a truth table for given circuit if A B changes from 00 to 11.

Fig. No. 2

e) Draw binary to gray code converter and write its truth table.

f) Draw 4 - bit twisted ring counter and explain working with truth table and waveforms.

6.   **Attempt any <u>FOUR</u> of the following:**   **16**

a) Draw the pinout configuration for

   (i)   IC 7402

   (ii) IC 7404

b) Implement 1:16 Demux using 1:4 Demux write a truth table.

c) Draw pin diagram of IC PCF 8591 and list four features.

d) Design and draw MOD-6 counter using IC 7490.

e) Draw block diagram of ALU 74181 and explain.

f) Calculate output voltage for 4 bit binary weighted resistor DAC for binary inputs and V_{ref} = 5V.

   (i)   1010

   (ii) 1100

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Instructions – (1) All Questions are *Compulsory*.

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. a) **Attempt any <u>SIX</u> of the following:**   12

   (i) Draw symbol of EXOR gate and also write its truth table.

   (ii) Identify the function of IC 0800 and IC 0809.

   (iii) Convert the following binary number to gray code:

   1) 1101001

   2) 11111

   (iv) What is the role of Preset and clear terminal of flip-flop?

   (v) Compare TTL and CMOS Logic families. (2 points)

   (vi) What is Tristate buffer? Draw its symbol.

   (vii) Define modulus of counter? How many flip flops are required for mod 5 counter?

   (viii) State the necessity of multiplexer.

Marks

b) **Attempt any <u>TWO</u> of the following:**   8

    (i)   Convert the following into Binary and Add them $(A96)_{16} + (28B)_{16}$

    (ii)   Differentiate between Synchronous and Asynchronous counter.

    (iii)   Draw circuit diagram of 1:4 Demux using logic gate. Write its truth table.

2.   **Attempt any <u>FOUR</u> of the following:**   16

a) Compare EPROM and flash memory.

b) Describe operation of full adder with proper truth table and logical diagram.

c) Convert the following number into Binary:

    (i) $(736.6)_8$

    (ii) $(2F9.25)_{16}$

d) State and prove De Morgan's Theorems.

e) Draw the diagram of 3-bit twisted ring counter using JK F/F. Also write its truth table. Draw waveforms.

f) Draw the block diagram of successive approximation type ADC and explain its working.

3.   **Attempt any FOUR of the following:**   **16**

a) Convert the following expression into their standard SOP form $Y = A + BC + ABC + B$

b) What is Race around condition and how it is eliminated?

c) Solve the following using 1^s and 2^s complement method.

   (i) $(42)_{10} - (63)_{10}$

   (ii) $(11010)_2 - (11100)_2$

d) What is priority encoder? Draw the truth and symbol table of decimal to BCD encoder.

e) Draw 4 bit weighted resistor DAC and give expression for output voltage.

f) Reduce the following Boolean expression using Boolean laws.

   $Y = A\overline{B} + \overline{A}B + AB + \overline{A}\,\overline{B}$

   $Y = A\overline{B}C + \overline{A}BC + ABC$

4.   **Attempt any FOUR of the following:**   **16**

a) Draw the internal diagram of IC 7490. Design mod 8 counter using IC 7490.

b) Explain with circuit diagram, the principle of TTL gate (NAND) with totem pole.

c) Calculate analog output of 4 bit DAC and digital input is 1011. Assume $V_{fs} = 5V$

d) Compare sequential and combinational logic circuit. (Four points)

e) Implement OR gate and AND gate using NAND gate.

f) Compare single slope and dual slope ADC.

Marks

5. **Attempt any FOUR of the following:** **16**

a) Compare R-2R and binary weighted register.

b) Define memory? Write down types of memory.

c) Draw PIPO shift register. State applications of shift register.

d) Design 16:1 MUX using 8:1 MUX

e) Give any four characteristics of CMOS and ECL logic families.

f) Convert the following decimal numbers into excess-3 code

   (i) $(5)_{10}$

   (ii) $(25)_{10}$

   (iii) $(46)_{10}$

   (iv) $(144.4)_{10}$

6. **Attempt any FOUR of the following:** **16**

a) Draw block diagram and explain working of dual slope ADC.

b) Describe working of SR latch using NAND gates with proper truth table.

c) Draw the block diagram of ALU IC 74181 and also write its operation.

d) Mention any eight Boolean laws.

e) Draw 3 bit synchronous counter with truth table and explain working.

f) Draw and explain static RAM cell (TTL).

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Instructions –   (1) All Questions are *Compulsory.*

   (2) Answer each next main Question on a new page.

   (3) Illustrate your answers with neat sketches wherever necessary.

   (4) Figures to the right indicate full marks.

   (5) Assume suitable data, if necessary.

   (6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

   (7) Use of Steam tables, logarithmic, Mollier's chart is permitted.

Marks

1.   **Attempt any <u>TEN</u> of the following:**   **20**

   a) Convert the following hexadecimal number to decimal number

   (i) $(EF)_{16}$

   (ii) $(DAD)_{16}$

   b) Convert the following decimal number to octal.

   (i) $(28)_{10}$

   (ii) $(62)_{10}$

c) Draw the symbol of EX-OR and EX-NOR gate along with its logical equation

d) Draw symbol of AND gate and write its truth table.

e) Draw the symbol of D-FlipFlop and T-FlipFlop.

f) Define Bidirectional Shift Register and Universal Shift Register.

g) State different triggering methods in digital circuits.

h) State DeMorgan's theorems.

i) Convert the following:

    (i) $(111011)_2 = (?)$ gray code

    (ii) $(46)_{10} = (?)$ excess-3 code

j) What is Modulus of counter? How many FlipFlops are required for MOD-11 counter.

k) What is Flash Memory?

l) Define Resduction and Linearity of DAC.

m) Implement given logical equation using gates $Y = AB + C$

n) Define Accuracy and settling time w.r.t. to DAC.

2.   **Attempt any <u>FOUR</u> of the following:**   **16**

a) Perform the following:

    $(11011)_2 \times (11011)_2$

b) State the rules for BCD Addition explain with example.

c) Draw and explain the working CMOS inverter with circuit diagram.

d) Design Half adder using K-map and implement using gates.

e) Realize

$F_1 = \Sigma m \ (0, \ 2, \ 4, \ 6)$

$F_2 = \Sigma m \ (1, \ 3, \ 5)$

using Demultiplexer.

f) Draw and explain S.R. and FlipFlop using NAND gate along with truth table.

3. Attempt any FOUR of the following: **16**

a) Draw and explain working of R-2R DAC.

b) State different types of ROM and explain any one.

c) Draw circuit diagram of TTL NAND gate and explain its working.

d) Subtract using 2's complement method

(i) $(1110)_2 - (1001)_2$

(ii) $(1000)_2 - (1001)_2$

e) Draw Master Salve JF FlipFlop and write its truth table.

f) Design MOD-6 Counter using IC 7490 and write its truth table.

4. Attempt any FOUR of the following: **16**

a) Describe working of SISO shift Register with proper circuit diagram.

b) Compare combinational and sequential circuit. (Four points)

c) Compare :

(i) Volatile with Non-Volatile memory.

(ii) SRAM with DRAM memory.

d) Explain working of single slope ADC with diagram.

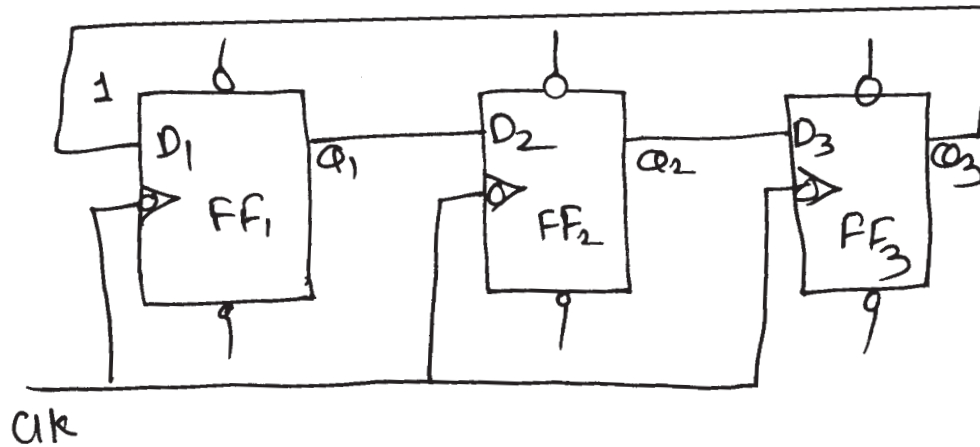e) Identity the given circuit and explain its working. (Refer Figure No.1)

Fig. No. 1

f) Draw and explain working of 4-bit Weighted Register DAC. circuit.

5. **Attempt any FOUR of the following:** 16

a) Compare TTL logic family with CMOS w.r.t. to

  (i) Propogation delay

  (ii) Power dissipation

  (iii) Fan-out

  (iv) Basic gate

b) Prove :

  (i) $A + AB = A$

  (ii) $\overline{\overline{A} + \overline{B} + \overline{C}} = ABC$

c) Classify memories and Identify the IC

  (i) IC 2716

  (ii) IC 7481

d) Design and draw 16:1 MUX using 8:1 MUX (Multiplex).

e) What is priority encodes? How is Demultiplex used as Decoder?

f) Draw block diagram of successive approximation type ADC and write its advantages.

6. **Attempt any FOUR of the following:** 16

a) Compare weighted resistor and R-2R methods of ADC.

b) Write std SOP equation of given logical equation
   (i) $y = AB + BC$
   (ii) $y = \overline{A}BC + B$

c) Minimize $y = \Sigma m$ (0, 5, 2, 8, 7, 10, 15, 13) using k-map.

d) Write Advantages of MUX and DEMUX state their applications.

e) Identify the given circuit and write its truth table -
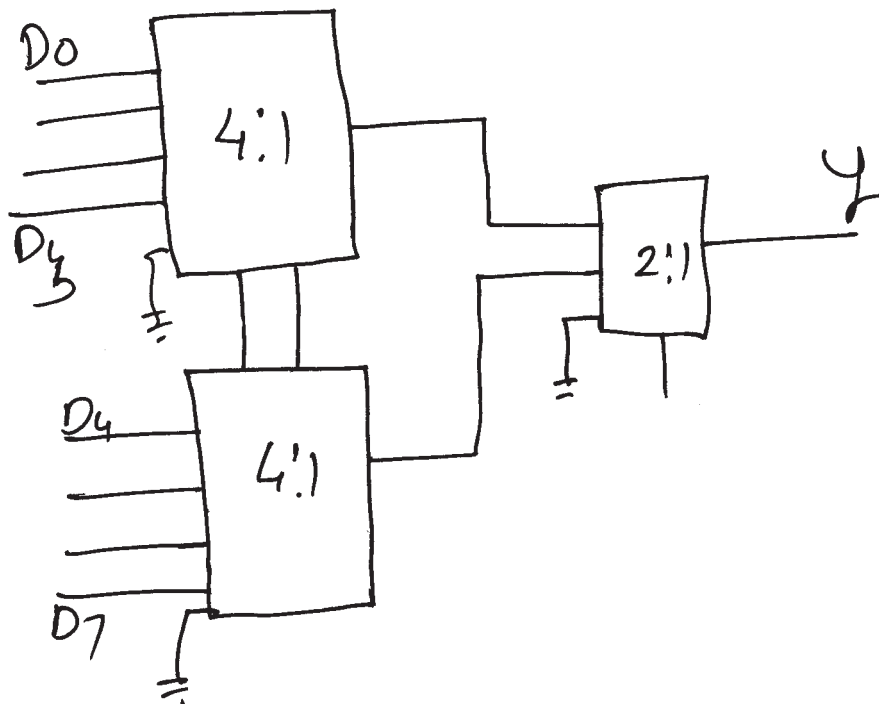   Diagram below (Refer Figure No.2)

Fig. No. 2

f) (i) Draw circuit diagram of MOD-10 counter using T-FF.

   (ii) Identify the function of
        1) IC – 0800
        2) IC – 0809

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3 Hours / 100 Marks   Seat No.

Instructions :   (1)   All Questions are *compulsory*.

(2)   Answer each next main Question on a new page.

(3)   Illustrate your answers with neat sketches wherever necessary.

Marks

1.   **Attempt any TEN :**   **20**

(a)   Convert (i) $(28.56)_{10} = (?)_2$ (ii) $(372)_8 = (?)_{10}$

(b)   Draw logic diagram of tristate buffer with active low enable and active high enable.

(c)   Draw truth table for logic gates represented by following IC's :

(i)   IC7400

(ii)   IC7402

(d)   State triggering methods in digital circuits (any two)

(e)   Identify SOP and POS equations :

(i)   AB + CD

(ii)   (A + B) (C + D)

(f)   Differentiate between RAM & ROM (2 points)

(g)   List any two non-weighted codes.

(h)   Add the binary numbers (1011) & (1100)

(i)   Find Y_1 & Y_2 for Fig. 1 & Fig. 2 respectively.

Fig. 1   **Fig. 2**

(j) Define universal shift register.

(k) Draw symbol of TFF & write its truth table.

(l) Implement given logic equation using basic gates $Y = A\overline{B} + \overline{A}B$.

(m) Prove that $AB + A\overline{B} = A$, using laws of Boolean Algebra.

(n) Draw 3 variable K-map format.

2. Attempt any FOUR : 16

(a) Subtract $(1101)_2$ from $(1110)_2$ using 1's & 2's complement method.

(b) Two square waves of 4 kHz & 8 kHz are applied as the inputs of AND gate & NAND gate. Draw the output waveform in each case.

(c) Design 1 : 32 De MUX using 1 : 8 De MUX.

(d) Write down excitation table of JK & DFF.

(e) Describe 3 bit R-2R ladder DAC with neat diagram.

(f) Compare Static RAM & Dynamic RAM (any 4 points)

3. Attempt any FOUR : 16

(a) Perform the following operations :

   (i) $(1001)_2 \times (1101)_2$

   (ii) $(1001)_2 / (11)_2$

(b) Compare TTL, ECL & CMOS logic families (any 4 points)

(c) Realize following expression using MUX :

   $f = \Sigma_m (0, 3, 5, 9, 11, 15)$

(d) Describe operation of PISO shift register with neat circuit diagram.

(e) Compare single slope ADC with dual slope ADC w.r.t.

(f) Draw organization of 4×4 memory and lable it.

4. **Attempt any FOUR :** 16

   (a) Perform BCD addition :

      (i) $(45)_{10} + (33)_{10}$

      (ii) $(57)_{10} + (26)_{10}$

   (b) Define following characteristics of logic families :

      (i)   fan in

      (ii) fan out

      (iii) Propagation delay

      (iv) Power dissipation

   (c) Design 32 : 1 MUX using 16 : 1 MUX.

   (d) Draw logic diagram for 3 bit up-down counter.

   (e) Simplify given SOP equation using K map

$$Y = \Sigma_m (0, 1, 2, 3, 5, 7, 8, 9, 11)$$

   (f) Write advantages (any 3) and disadvantage (any 1) of dual slope ADC.

5. **Attempt any FOUR :** 16

   (a) Define priority encoder. Draw the generalised block diagram of priority encoder.

   (b) Compare R-2R ladder DAC with weighted resistor DAC (any 4 points)

   (c) Explain the operation of TTL logic NAND gate. Draw the circuit diagram.

   (d) Design MOD-6 counter using IC 7490.

   (e) Compare combinational circuit with sequential circuit (any 4 points)

   (f) Compare EPROM and EEPROM (any four points).

6. **Attempt any FOUR :** 16

(a) Implement Y = f (A, B, C) = Σ_m (0, 1, 2, 6, 7) using suitable DeMUX & logic gates.

(b) State the use of preset and clear terminal in a Flip-flop.

(c) Draw 3 bit synchronous up counter. Write its truth table.

(d) Draw 4 bit weighted resistor DAC and give expression for output voltage.

(e) Describe successive approximation ADC with neat diagram.

(f) Describe the operation of 1 dig it BCD adder using IC 7483.

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17320

Instructions –   (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. a) Attempt any <u>SIX</u> of the following: **12**

i)   List any two nonweighted code.

ii) Write the functions of following ICS :

1) 74151

2) 74155

iii) Define modulus of counter. How many flip flops are required for mod 5 counter.

iv) List the types of shift registers

v)   List the types of ADCs and DACs

vi) Compare RAM and ROM (any two points)

vii) State De Morgan's theorems.

viii) Why NAND and NOR are called as universal gates?

Marks

b) **Attempt any <u>TWO</u> of the following:**   **08**

    i)   Write down rules for binary addition and subtraction.

    ii)   Design half adder using K Map

    iii)   Design 16:1 MUX using 4:1 MUX only

2.   **Attempt any <u>FOUR</u> of the following:**   **16**

    a)   Subtract using 2's complement

      i) $(1101)_2 - (1001)_2$

      ii) $(1000)_2 - (1010)_2$

    b)   Realise Y=AB+AC using one OR gate and one AND gate only.

    c)   Convert the given expressions into standard form

      i) $Y = A + BC + ABC$

      ii) $Y = (A + B)\ (A + \overline{C})$

    d)   Draw clocked SR flip flop with preset and clear using gates. What is the drawback of SR flip flop.

    e)   Draw 3 bit asynchronous up counter with truth table and timing diagram.

    f)   Draw 4 bit weighted Resistor DAC and give expression for output voltage. What is the advantage of this type of DAC.

3.   **Attempt any <u>FOUR</u> of the following:**   **16**

    a)   Perform BCD addition

      i) $(37)_{10} + (65)_{10}$

      ii) $(45)_{10} + (24)_{10}$

    b)   Compare TTL and CMOS with respect to propagation delay, power dissipation, fanout and basic gate.

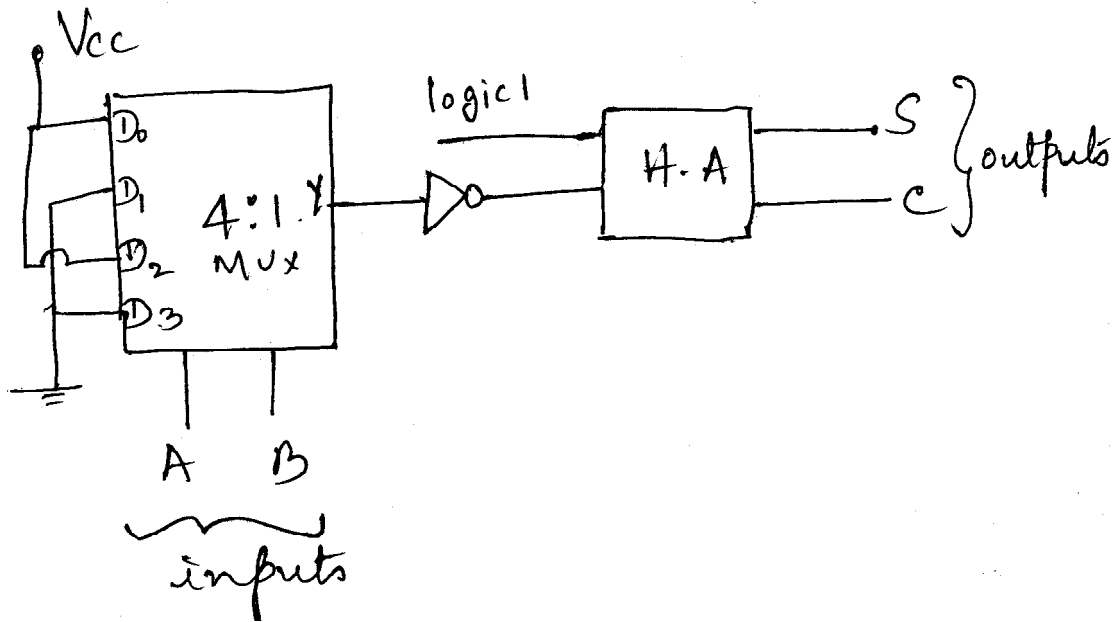c) Write down the truth table for the given diagram.
Refer Figure No.1.

Fig. No. 1

d) Draw D and T flip flop using JK flip flop.

e) Describe the working of single slope ADC with block diagram.

f) Draw 4 × 4 memory organisation of ROM array and list the types of ROM

4.   Attempt any <u>FOUR</u> of the following: **16**

a) Define tristate logic. Draw the symbol of tristate inverter.

b) Realise using 8:1 MUX $f = \Sigma(0, 3, 4, 7)$

c) What is race around condition in JK flip flop? How it is avoided using MSJK flip flop.

d) Draw 3 bit twisted ring counter using D flip flop. Give its timing diagram.

e) Draw and explain dual slope ADC

f) Compare static RAM and dynamic RAM, volatile and non volatile.

Marks

5. **Attempt any <u>FOUR</u> of the following:** **16**

a) Draw and explain TTL NAND gate with totempole output

b) Define priority encoder. Draw the truth table of decimal to BCD encoder

c) Write down excitation table for SR flip flop and T flip flop.

d) Design mode 6 counter using IC 7490

e) Draw and explain SAR ADC with block diagram.

f) Give classification of memory compare EPROM and Flash memory (3 points)

6. **Attempt any <u>FOUR</u> of the following:** **16**

a) Convert the given number into octal, binary, hexadecimal and BCD $(64.75)_{10}$

b) Two square waves of 2KHZ and 4KHZ are applied as the inputs of AND and OR gates. Draw the output waveform in each case.

c) Prove :

i) $A + \overline{A}B = A + B$

ii) $(A + B)(A + \overline{B}) = A$ using Boolean theorems.

d) Design 1:32 demux using 1:8 demux

e) Draw 3 bit synchronous counter with truth table and timing diagram

f) Derive the expression for output voltage in 3 bit R-2R ladder DAC

13141

3 Hours / 100 Marks

21314

3 Hours/100 Marks   Seat No.

Instructions :   (1) **All** questions are **compulsory**.

           (2) Illustrate your answers with **neat** sketches **wherever** necessary.

           (3) Figures to the **right** indicate **full** marks.

           (4) Use of Non-programmable Electronic Pocket Calculator is **permissible**.

           (5) Mobile Phone, Pager and any other Electronic Communication devices are **not permissible** in Examination Hall.

MARKS

1. Attempt **any ten** of the following :   **20**

    a) Convert given numbers :

       i) $(110100)_2 = (...)_{Gray}$ ii) $(1111)_{Gray} = ..._B$

    b) Draw the logic circuit diagram of 1 bit memory cell using NAND gate.

    c) State the necessity of multiplexers.

    d) Differentiate between RAM and ROM (any 2 points).

    e) Subtract $(32)_{10}$ from $(85)_{10}$ using 2's complement binary arithmetic.

    f) Give two applications of A/D converter.

    g) Draw OR and AND gate using NAND gate only.

    h) Classify memories on the basis of principle of operation.

    i) Write truth table and the expressions of half subtractor.

    j) Perform $(52)_{10} - (89)_{10}$ using 9's and 10's complement method.

    k) Draw the truth table of following IC's

       i) IC – 7432   ii) IC – 7486

    l) Draw circuit diagram of 4 : 1 multiplexer.

    m) Give various methods of D/A converter.

    n) State the applications of Flip-Flops.

2. Attempt **any four** of the following :   **16**

   a) Perform the following operations :

     i) $(11100)_2 \div (100)_2$ ii) $(1010.11)_2 \times (11)_2$

   b) Design 32 : 1 multiplexer using 16 : 1 multiplexer and 2 : 1 multiplexer.

   c) Draw the circuit diagram of S – R Flip-Flop using NAND gate and describe its working.

   d) Simplify the following expression using Boolean laws.

     i) $y = (A + B)(A + C)$ ii) $y = ABC + A\overline{B}C + AB\overline{C}$

   e) How many bits are required for a resolution of 5 mV and full scale voltage in 15 V ?

   f) Identify the following circuit as combinational circuit or sequential circuit.

     i) 3 – bit ring counter   ii) Full adder

     iii) Clocked J-K F/F   iv) 4 : 1 MUX

3. Attempt **any four** of the following :   **16**

   a) State and prove De-Morgan's 1st and 2nd theorem.

   b) Describe the operation of single digit BCD adder using IC – 7483 with circuit diagram.

   c) State the working principle of J–K Flip-Flop with neat diagram.

   d) Minimize the following expression using K-map.

     i) $f(w, x, y) = \Sigma m (0, 1, 2, 4, 6, 7)$

     ii) $f(A, B, C, D) = \Pi M (0, 2, 7, 8, 9, 10, 13)$

   e) Describe with circuit diagram the working operation of static RAM cell.

   f) Study the given circuit as shown in fig. no. 1 initial o/p condition is $Q_A Q_B Q_C = 010$, write truth table of output $Q_A Q_B Q_C$.
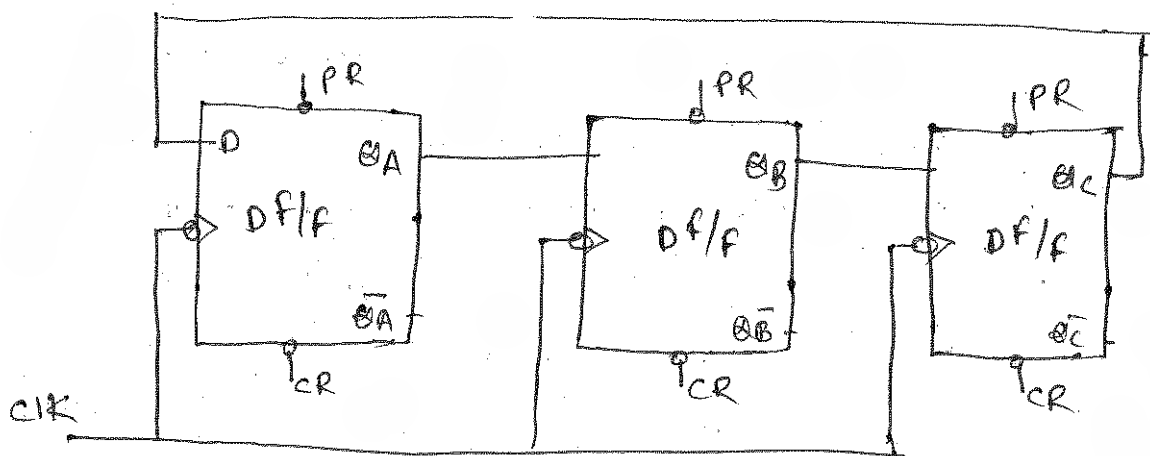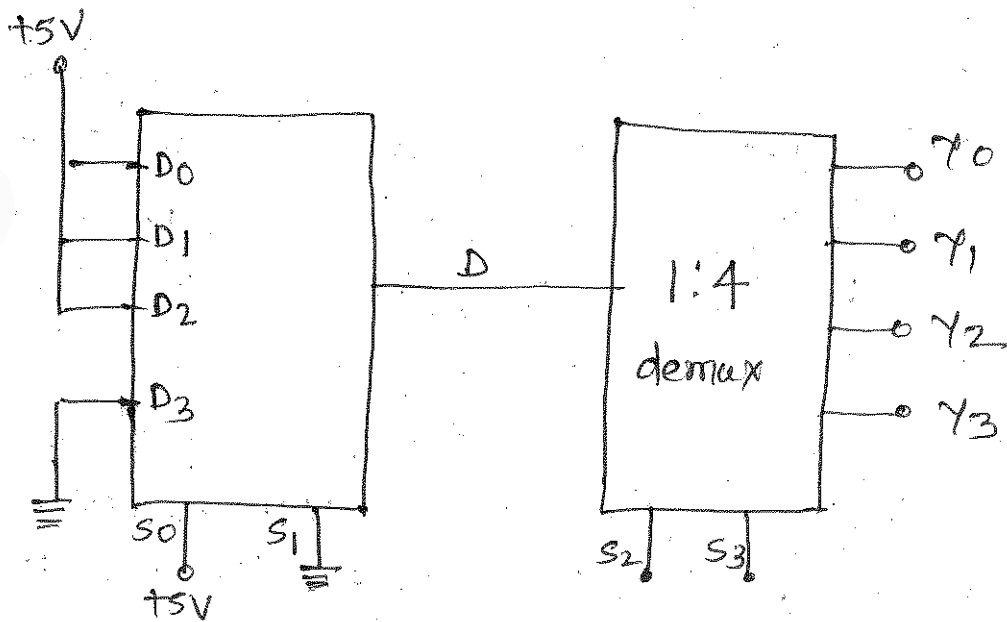

Fig No. 1

4. Attempt **any four** of the following :   **16**

   a) Encode the following decimal number in BCD code and excess-3 code.

      i) $(48)_{10}$ ii) $(228)_{10}$

   b) Describe R-2R ladder network method of D/A conversion with neat circuit diagram.

   c) Explain the operation of TTL logic using NAND gate.

   d) Design a full subtractor circuit using K-map with truth tables.

   e) For 3 bit synchronous up-counter.

      i) Draw circuit diagram (use T-Flip Flop)

      ii) Write truth table

   f) Draw block diagram of decimal to BCD encoder with its truth table.

5. Attempt **any four** of the following :   **16**

   a) Compare combinational and sequential logic circuits. (any four points)

   b) Draw pinout diag. of 2716 EPROM and state its operation.

   c) Explain race around condition in J-K Flip-Flop.

   d) Describe the working of dual slope A/D converter.

   e) Compare TTL and CMOS logic families.

   f) In the given fig. 2, the control signal S_2S_3 of 1 : 4 demux changes from 00 through 11. Write its truth table.

Fig. No. 2

6. Attempt **any four** of the following : **16**

a) Add $(147)_{10}$ and $(284)_{10}$ in BCD code.

b) Explain the operation of 1 : 4 de-multiplexer using logic gate.

c) Describe operation of SIPO shift register with circuit diagram.

d) A RAM IC has 12 address lines and 8 data lines. If its first location has address 9000H what will be the address of the last location ?

e) Describe the working principle of successive approximation method ADC with block diagram.

f) For a given logical diagram, derive Boolean expression for output Y by simplifying it as much as possible.
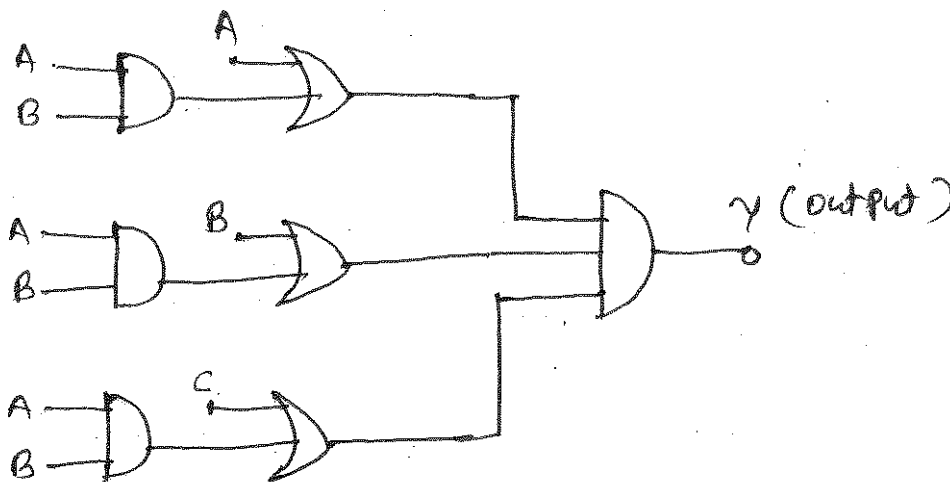

Fig. No. 3

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3 Hours/100 Marks

Seat No.

Instructions : (1) **All** questions are **compulsory**.
(2) Illustrate your answers with **neat** sketches **wherever** necessary.
(3) Figures to the **right** indicate **full** marks.
(4) Assume suitable data, if **necessary**.

MARKS

1. A) Attempt **any six**.   **12**

    a) Convert the following binary number to gray code

      i) 1101001   ii) 11111.

    b) Write any two advantages of MUX.

    c) What is meant by modulus of a counter ?

    d) Define bi-directional shift register.

    e) Write any two applications of analog to digital converter.

    f) Write the types of RAM memory with its definitions.

    g) Draw symbol of IC 7400 and also write the truth table and boolean expression.

    h) Draw the given boolean expression use one AND gate and one OR gate.

      $y = AB + BC$.

   B) Attempt **any two** :   **8**

    a) Add the binary number

      i) 1011.11 and 1100.01

      ii) 0101.1 and 1111.01

    b) Convert the following expression into their standard SOP form

      $y = A + BC + ABC$

    c) Draw the general block diagram of MUX and write its operation.

2. Attempt **any four** :   **16**

   a) Convert following numbers into binary and add them $(173)_8 + (741)_8$.

   b) Why NAND gate is called universal gate ? Implement basic gates using NAND gate only.

   c) Draw the block diagram of ALU IC 74181 and also write its operation.

   d) Write the difference between combinational and sequential logic circuit. (any four points).

   e) Design 4 bit asynchronous up-counter also write the truth table and draw the waveform.

   f) Compare between R-2R ladder DAC and weighted resistor DAC (4 points).

3. Attempt **any four** :   **16**

   a) Convert the following decimal number into excess-3 code,

      i) $(6)_{10}$ ii) $(35)_{10}$ iii) $(46)_{10}$ iv) $(142.2)_{10}$.

   b) Compare totem pole and open collector outputs. (any four points)

   c) Implement the following using 16 : 1 multiplexer,

      $y = \Sigma m\ (1, 2, 5, 6, 8, 12)$.

   d) Write the use of preset and clear terminal in a flip-flop.

   e) Draw the block diagram of successive approximation type ADC and write the function of each block.

   f) Compare EPROM and EEPROM with any four points.

4. Attempt **any four** :   **16**

   a) What is priority encoder ? Draw the block diagram of priority encoder.

   b) Realize the following function using De-multiplexer.

      i) $F_1 = \Sigma m\ (0, 1, 3, 7, 11, 13, 15)$

      ii) $F_2 = \Sigma m\ (2, 4, 8, 10, 11)$.

MARKS

c) What is the Race-around condition ? How it will be eliminated in J-K flip-flop ?

d) Draw the diagram of 3-bit twisted ring counter using J-K F/F. Also write its truth table.

e) Write any three advantages and one disadvantage of dual slope Analog to Digital Converter (ADC).

f) Compare SRAM and DRAM with any four points.

5. Attempt **any four** :   **16**

a) Write the four specifications of TTL logic family.

b) Draw the logic diagram of bi-directional buffer IC 74245.

c) With neat diagram write the working of serial in serial out shift register.

d) Write any four features of IC PCF 8591.

e) Compare between EPROM and Flash Memory.

f) Study the given circuit as shown in figure initial output condition is $Q_A Q_B Q_C$ = o/o. Write truth table of output $Q_A Q_B Q_C$.
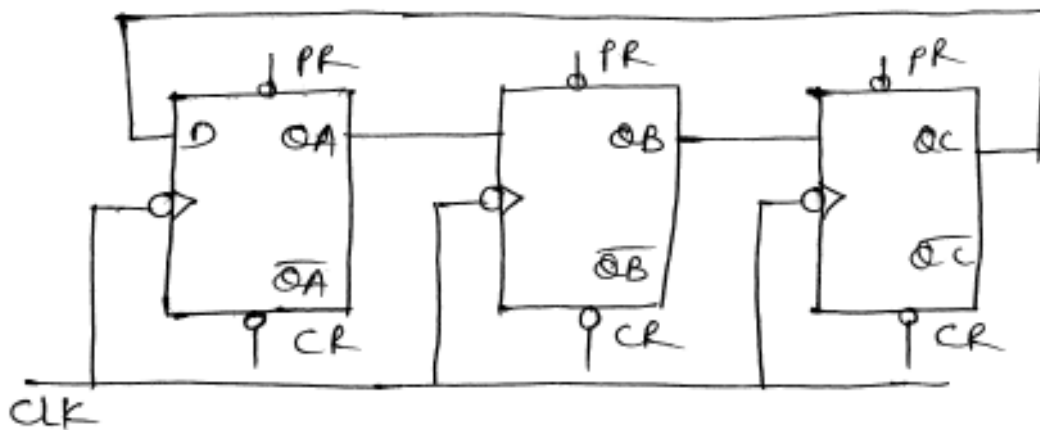
6. Attempt **any four** : **16**

a) Convert the number into its decimal equivalent

$(1011.01)_2$

b) Draw the logical diagram of

i) OR gate

ii) NAND gate

using only NOR gate.

c) Write the De-Morgan's theorem and prove it.

d) Design 16 : 1 MUX using 8 : 1 MUX.

e) Draw S-R latch using NAND gates only, also write about the received output for each condition using truth table of S-R flip-flop.

f) Draw the circuit diagram of 3-bit binary weighted Digital to Analog Converter (DAC) also write its mathematical derivation.

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3 Hours/100 Marks

Seat No.

Instructions :
(1) **All** questions are **compulsory**.
(2) Illustrate your answers with **neat** sketches **wherever** necessary.
(3) Figures to the **right** indicate **full** marks.
(4) Assume **suitable data**, if necessary.

MARKS

1. A) Attempt **any six** :   **12**

   a) Convert the decimal no. 46 into BCD code and in excess 3 code.

   b) Give the two advantages of multiplexer.

   c) State the different triggering methods in digital circuit.

   d) State the various types of shift registers.

   e) Identify the IC 0800 and IC 0809.

   f) Compare EPROM and EEPROM (any two pts.).

   g) Write associative and commutative Boolean laws.

   h) Draw the logic symbol and truth table for two input NAND gate.

   B) Attempt **any two** :   **8**

   a) Solve the following subtraction using 1's and 2's complement method.

      i) $(52)_{10} - (65)_{10}$

      ii) $(101011)_2 - (11010)_2$.

   b) Explain Full adder with its truth table, K-map simplification and logic diagram.

   c) Design a 4 : 1 MUX using 2 : 1 MUX and write truth table.

2. Attempt **any four** : **16**

   a) Perform the following multiplication in binary number system $(15)_{10} \times (8)_{10}$.

   b) State and prove the both De-Morgan's theorems with logic diagram.

   c) Explain the concept of Minterm and Maxterm with example.

   d) Draw and explain OR flip flop using NAND gate with its truth table.

   e) Draw the circuit diagram of 3 bit synchronous up counter with its truth table and explain its working.

   f) Define the following specifications of DAC :

      i) Resolution

      ii) Linearity

      iii) Accuracy

      iv) Settling time.

3. Attempt **any four** : **16**

   a) State the rules for BCD addition.

   b) Compare CMOS and TTL logic family on following points : propagation delay, fan out, power dissipation, Noise immunity.

   c) Design 1 : 16 demultiplexer using 1 : 4 demultiplexer.

   d) Compare combinational circuit with sequential circuit (any 4 points).

   e) Draw the block diagram of dual slope ADC and explain its working with waveforms.

   f) State the different types of ROMs and explain any one type of ROM.

4. Attempt **any four** : 16

   a) Design a 3 : 8 line decoder with truth table and logic diagram and give IC No. for the same.

   b) Draw and explain decimal to BCD priority encoder using IC 74147.

   c) What is race around condition in JKFF ? How it can be avoided ?

   d) Explain the working of 4 bit ring counter with a neat diagram.

   e) Describe successive approximation ADC with neat circuit diagram.

   f) Compare Static RAM with Dynamic RAM (any 4 pts.).

5. Attempt **any four** : 16

   a) Draw the circuit of TTL totem pole two input NAND gate and explain its working.

   b) Draw and explain the circuit diagram of 1 : 4 demultiplexer using logic gates.

   c) Explain with neat diagram. How to convert JK flip flop into TFF ? Write truth table.

   d) How can IC 7490 be used as a decade counter with neat block diagram ?

   e) How many bits are required for a resolution of 5 mV and full scale voltage is 15 V ?

   f) Compare volatile and non-volatile memory (any 4 pts.).

6. Attempt **any four** : 16

   a) Convert the following :

      i) $(5C7)_{16} = (?)_{10}$

      ii) $(2598)_{10} = (?)_{16}$

      iii) $(10110)_2 = (?)_{10} = (?)_{16}$.

   b) Why NAND & NOR gates are called as an universal gates ? Realise OR gate using NAND gate.

c) Reduce the following Boolean expression using Boolean laws :

   i) $Y = A\overline{B} + \overline{A}B + AB + \overline{A}\overline{B}$

   ii) $Y = A\overline{B}C + \overline{A}BC + ABC$.

d) Realize the following function using demultiplexer :

   i) $F_1 = \Sigma m\,(0, 1, 3, 7, 11, 13, 15)$

   ii) $F_2 = \Sigma m\,(2, 4, 8, 10, 12)$.

e) Design MOD 10 asynchronous up counter, with its truth table and timing diagram.

f) Calculate the analog output of a 4 bit DAC, if the digital input is 1011. Assume VFS = 5 V.

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15116

3 Hours / 100 Marks   Seat No.

Instructions :   (1)   All Questions are *compulsory*.

(2)   Illustrate your answers with neat sketches wherever necessary.

(3)   Figures to the right indicate full marks.

(4)   Assume suitable data, if necessary.

(5)   Use of Non-programmable Electronic Pocket Calculator is permissible.

(6)   Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. **Attempt any TEN :**   **20**

(a)   Convert following binary numbers to decimal :

(i)   101011   (ii)   110011

(b)   Convert following hexadecimal numbers to decimal :

(i)   2CH   (ii)   A9DH

(c)   Convert following decimal numbers to octal :

(i)   26   (ii)   44

(d)   Draw symbol and truth table of :

(i)   AND gate   (ii)   NOR gate

(e)   State commutative and associative laws.

(f)   Prove : $A (1 + \bar{A}) = A$

(g)   Draw the symbol and write logical equation of output for 'EX-OR' and 'EX-NOR' gates.

(h)   Implement given logical equation using logic gates – $Y = AB + CD$

(i)   Convert given SOP equation in standard SOP equation :

$Y = \bar{A}BC + B\bar{C} + AC$

(j)   Draw the logic diagram of half subtractor and write its truth table.

(k)   Define :   (i) MUX (ii) De-MUX

P.T.O.

(l) Draw the diagram of one bit memory cell using NAND gates only.

(m) State drawback of S-R flip-flop. How is it overcome ?

(n) Draw the symbol of D flip-flop and write its truth table.

2. **Attempt any FOUR :** **16**

(a) Perform following binary operations :

(i) 1011   (ii) 1101

  $\times 101$ -110

(using 2's complement method)

(b) Draw the circuit diagram of CMOS inverter. Explain its operation.

(c) Design full adder using K-map technique.

(d) Draw the logical diagram of clocked S-R flip-flop using NAND gate only. Write its truth table.

(e) With the help of circuit diagram, describe the operation of weighted resistor DAC.

(f) Compare EPROM and FLASH memory.

3. **Attempt any FOUR :** **16**

(a) Perform following BCD operations :

(i) $+\begin{matrix}16\\27\end{matrix}$ (ii) $-\begin{matrix}35\\19\end{matrix}$

(b) State and prove DeMorgan's theorems.

(c) Simplify given SOP equation using K-map technique –

Y = Σm (0, 1, 2, 3, 4, 5, 7, 12, 13, 15)

(d) Draw the circuit diagram of master-slave J-K flip-flop using NAND gates and explain its operation.

(e) Draw the block diagram of single slope ADC. State its disadvantage.

(f) Draw organization of 8 × 8 memory and label it.

4. **Attempt any FOUR :** **16**

(a) Obtain :
(i) 2's complement of 110011
(ii) Gray code of 1101

    (b)   Compare TTL and CMOS logic families.

    (c)   Draw and write truth table of 8:1 MUX tree using 4:1 MUX.

    (d)   Describe application of shift register as ring counter.

    (e)   Draw the block diagram of SAR ADC and write its operation in brief.

    (f)   Compare :

        (i)   static and dynamic memory (two points)

        (ii)   volatile and non-volatile memory (two points)

5.   **Attempt any FOUR :**   **16**

    (a)   Draw TTL NAND gate and write its truth table.

    (b)   How is Demux used as Decoder ? Write truth table of 3:8 decoder.

    (c)   Draw the diagram of 3 bit ripple counter and write its operation.

    (d)   Draw logic diagram of 4 bit serial-in serial-out shift register and its output waveform.

    (e)   Describe the working principle of dual slope ADC with its block diagram.

    (f)   Explain classification of memories. What is flash memory ?

6.   **Attempt any TWO :**   **16**

    (a)   Draw internal block schematic of 7490 decade counter. Describe its operation. Draw output waveform.

    (b)   Identify function of following IC numbers :

        (i)   74244   (ii)   74245

        (iii)   74151   (iv)   74155

        Describe any two of the above IC with its truth table.

    (c)   Draw the diagram of 3 bit R-2R ladder DAC. Derive the mathematical expression for digital input 101.

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17320

3 Hours / 100 Marks   Seat No.

Instructions : (1) **All** questions are **compulsory**.
(2) Illustrate your answers with **neat** sketches **wherever** necessary.
(3) Figures to the **right** indicate **full** marks.
(4) Assume suitable data, if **necessary**.
(5) Use of Non-programmable Electronic Pocket Calculator is **permissible**.
(6) Mobile Phone, Pager and any other Electronic Communication devices are **not** permissible in Examination Hall.

Marks

1. Attempt **any five** :   **20**

a) Convert the following decimal numbers into excess – 3 code.

i) $(7)_{10}$ ii) $(45)_{10}$ iii) $(232.8)_{10}$

b) Draw the logical diagram of OR gate and NOR gate using NAND gate only.

c) Convert the following expression in standard SOP form. $Y = AB + AC + BC$.

d) Compare between combinational and sequential logic circuits. (any 04 points).

e) State any four features of PCF 8591.

f) State different types of ROM and explain any one in detail.

g) State the number of Flip Flops required to construct the following modulus of counter :

i) 7   ii) 85   iii) 98   iv) 11

2. Attempt **any four** :   **16**

a) Perform binary subtraction using 2's complement method $(11001)_2 - (1010)_2$.

b) State DeMorgan's theorems and prove by Truth-table method for two variables.

c) Give the expression of Grey code equivalent of 4-bit binary using K-map.

d) Draw the circuit diagram of 3-bit asynchronous up/down counter using T-FF.

e) Describe any four specifications of DAC.

f) Compare volatile and non-volatile memories (any 4 pts.)

Marks

3. Attempt **any four** :   **16**

   a) Add $(532)_{10}$ and $(248)_{10}$ in BCD.

   b) Compare TTL and CMOS logic families on the basis of size, power, cost and speed.

   c) Minimize following expression using K-map $f(P, Q, R, S) = \sum m(0, 1, 4, 5, 7, 8, 9, 12, 13, 15)$.

   d) Describe the working of 4-bit ripple counter with logic diagram and waveforms.

   e) State advantages and disadvantages of single slope ADC.

   f) Describe the working of Flash-memory.

4. Attempt **any four** :   **16**

   a) State the rules for BCD addition.

   b) Draw two input OR gate, using ECL logic family (only diagram).

   c) Realize full subtractor using K-map.

   d) Describe positive and negative edge triggering methods of clock with their logic symbol.

   e) Calculate the analog output of 4-bit DAC if the digital input is 1101. Assume VFS = 5V.

   f) Draw the logic diagram of 4-bit SIPO shift register and explain its working principle.

5. Attempt **any four** :   **16**

   a) Realize the following expression using K-map.

      $Y = f(A, B, C, D) = \sum m(0, 2, 3, 5, 6, 7, 10, 11) + d(8, 14, 15)$ and implement it.

   b) Simplify the following expression using Boolean laws.

      $Y = (A + B) (A + C)$

      $Y = ABC + A\overline{B}C + AB\overline{C}$

   c) Draw the circuit of master slave JK FF using NAND gate and list its advantages.

   d) Draw and explain the block diagram of successive approximation method ADC.

   e) Convert the given binary number into decimal, hexadecimal, octal and grey code $(10111101)_2$.

   f) Implement the following function using demultiplexer.

      $F_1 = \sum m(1, 2, 5, 6, 7, 11, 14)$

      $F_2 = \pi M(0, 1, 2, 5, 6, 7, 8, 11, 12, 15)$

6. Attempt **any four** :   **16**

   a) Describe CMOS inverter with diagram.

   b) Design 32 : 1 multiplexer using 16 : 1 multiplexer and one 2 : 1 multiplexer.

   c) Describe the working of BCD to 7 segment decoder with truth table and circuit diagram.

   d) Design 3-bit synchronous counter and draw O/P waveform (only logic diagram, truth table and waveforms expected).

   e) Draw the circuit diagram of 4-bit R-2R ladder DAC and obtain its output voltage expression.

   f) Design 3 : 8 line decoder and give IC number for the same.

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