17659

21415

3 Hours / 100 Marks **Seat No.** | | | | | | | | |

Instructions : (1) All Questions are *compulsory*.

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

Marks

1. (A) Attempt any THREE : **12**

(a) Define the terms :

(i) Metastability

(ii) Noise Margin

(iii) Power Fanout

(iv) Skew

(b) Compare BJT and CMOS. (any 4 points)

(c) State the use and syntax of :

(i) signal

(ii) variable in VHDL

(d) Compare software and hardware description languages.

(e) Write the VHDL program for 3-bit up-counter.

(B) Attempt any ONE : **6**

(a) List and explain the main steps carried in typical n-well, CMOS fabrication process with neat sketches.

(b) Describe the following statements with example :

(i) assert statement

(ii) wait statement

(iii) case statement

P.T.O.

2. Attempt any FOUR : **16**

(a) Define the terms :

(i) Oxidation

(ii) Epitaxy

(iii) Deposition

(iv) Ion-implantation

(b) State the datatypes used in VHDL.

(c) Design the following logic gates using CMOS :

(i) NOR gate

(ii) NAND gate with Truth table showing ON-OFF action.

(d) Compare concurrent and sequential statement. (Any 4 points)

(e) State and explain delta delay.

3. Attempt any FOUR : **16**

(a) Explain Moore and Mealy Machine with block diagram.

(b) Explain the process of estimation of the channel resistance and how it is calculated.

(c) Write the abbreviation of VLSI and VHDL. What is VHDL ?

(d) Design the Boolean equation using CMOS

$$Y = \overline{\overline{A + B}} + \overline{A} \cdot \overline{C}$$

(e) State and explain coding styles in VHDL :

4. (A) Attempt any THREE : **12**

(a) Explain the terms w.r.t. VHDL :

(i) Entity,

(ii) architecture (with one example)

(b) Write VHDL program to implement 4:1 Multiplexer using case statement.

(c) Draw HDL design flow for synthesis and explain.

(d) Draw internal block diagram of CPLD Xilinx series and state the function of each block.

(B) Attempt any ONE : **6**

(a) Write the VHDL program to implement 9:4 encoder.

(b) Design a sequence detector of 011 using JK flip-flop. Use mealy machine.

5. Attempt any FOUR : **16**

(a) Explain the architecture of SPARTAN-3 FPGA Family with neat diagram.

(b) Compare CPLD and FPGA. (8 points)

(c) Compare synchronous and asynchronous sequential circuit on the basis of :

(i) Definition

(ii) Clock requirement

(iii) Output affected by

(iv) Memory element

(d) List operators and their operations used in VHDL.

(e) State Event scheduling and sensitivity list.

(f) Explain : CMOS Transmission gate with diagram.

6. Attempt any FOUR : **16**

(a) Explain with neat diagram wafter processing by C-Z method.

(b) State and explain :

(i) Zero Modeling

(ii) Simulation cycle

(c) State the test bench and write its application.

(d) What is simulation ? Explain event based and cycle based simulator.

(e) Draw and explain ASIC design flow.

(f) Write the VHDL program for D-flip-flop.

———————

17659

15116

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. a) **Attempt any <u>THREE</u> of the following:** **12**

(i) Define the following terms.

1) Metastability

2) Noise Margin

(ii) Compare BJT and CMOS.

(iii) What is VHDL? State VHDL flow elements.

(iv) Explain flattening and structuring with example.

(v) Explain the estimation of resistance of channel for MOSFET (Sheet Resistance).

Marks

b) **Attempt any ONE of the following:** **6**

(i) Design Melay sequence detector circuit for detecting sequence of '110' using D flip-flop.

(ii) Write VHDL program to Implement JK flip-flop with + ve edge trigger.

(iii) Explain the basic architecture of SPARTAN - 3 FPGA series.

2. Attempt any FOUR of the following: **16**

a) Compare software and hardware description language.

b) Compare FPGA and CPLD.

c) Explain Twin-Tub process in CMOS fabrication.

d) State and explain different operators used in VHDL.

e) Explain different types of simulators.

3. Attempt any FOUR of the following. **16**

a) Design clocked sequential circuit using Toggle flip-flop to count from 00 to 11 (2 bit counter).

b) List the features of FPGA.

c) Write the VHDL code for 3:8 decoder.

d) Explain event scheduling and sensitivity list.

e) Implement the logic circuit using CMOS.

$\gamma = ([A \cdot B] + [C \cdot D])$

Marks

4. a) **Attempt any THREE of the following:** **12**

(i) Explain with syntax.

1) Entity

2) Architecture

(ii) Compare Mealy Machine with Moore Machine.

(iii) Explain sharing of complex operators in VHDL with suitable example.

(iv) Draw and explain working of CMOS Transmission gates.

b) **Attempt any ONE of the following:** **6**

(i) Explain the architecture of Xilinx family of CPLD.

(ii) Write the VHDL code for 8:1 MUX.

(iii) Explain the steps involved in fabrication of n-well process.

5. **Attempt any FOUR of the following:** **16**

a) Draw and Implement the T flip-flop using Moore machine.

b) Define following terms related to fabrication process.

(i) Oxidation

(ii) Diffusion

(iii) Ion - implantation

(iv) Deposition

c) Describe following statement with syntax

(i) Process statement

(ii) Case statement

Marks

d) List the advantages and disadvantages of VHDL.

e) State different coding styles in VHDL and explain any one.

f) Draw the general FPGA chip architecture and explain the same.

6. Attempt any FOUR of the following: **16**

a) Explain product term allocator of Xilinx CPLD family.

b) Write VHDL code for FULL ADDER.

c) State the following data types.

(i) scalar data types

(ii) composite data types

d) Draw HDL design flow for synthesis.

e) Draw and explain working of CMOS Inverter.

17659

15162

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory*.

(2) Illustrate your answer with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data, if necessary.

(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Attempt any TEN of the following : **(10 × 2) = 20**

(a) Define the term 'Noise Margins'.

(b) Draw the block diagram of Mealy Machine.

(c) Define 'skew' w.r.t. sequential logic.

(d) State applications of finite state machines.

(e) Draw two input NOR Gate using CMOS technology.

(f) List different capacitances related to CMOS transistor.

(g) List different Data types used in VHDL.

(h) Give the syntax of signal used in VHDL.

(i) Write the syntax of CASE statement.

(j) List the different sequential statements used in VHDL.

(k) What do you mean by 'simulation' ?

(l) List the different softwares related to VHDL.

(m) State the advantages of PLD's.

(n) State any four features of XILINX.

P.T.O.

2. Attempt any FOUR of the following : **16**

(a) Distinguish asynchronous sequential circuit and synchronous sequential circuits.

(b) Explain estimation of channel resistance of CMOS.

(c) Draw CMOS AND Gate and write it with Truth Table. (2 input)

(d) State the various features of VHDL.

(e) Write VHDL code for half adder.

(f) List different levels of simulation and explain in brief.

3. Attempt any FOUR of the following : **16**

(a) Compare Mealy machine with Moore Machine.

(b) Explain fabrication using N-well process.

(c) Design $Z = \overline{XY + UV}$ using CMOS logic.

(d) Give the syntax of Entity and Architecture using in VHDL programming.

(e) Draw 3 : 8 decoder and write VHDL code for it.

(f) Explain event scheduling with suitable example.

4. Attempt any FOUR of the following : **16**

(a) Define the following terms :

(i) Meta stability

(ii) Set-up time

(iii) Hold time

(iv) Fan-out

(b) Explain Twin-tube process with suitable diagram.

(c) Explain various operators used in VHDL.

(d) Explain, how to write test bench for any VHDL code.

(e) Explain Event based and cycle based simulator.

(f) Explain sensitivity list and zero modelling.

5. Attempt any FOUR of the following : **16**

(a) Write various steps of well process.

(b) List different concurrent statements and explain any two.

(c) Draw full Adder using gates and write VHDL code for it.

(d) Write the various steps of synthesis and explain in short.

(e) Explain efficient coding styles.

(f) Draw design flow of ASIC and explain it.

6. Attempt any FOUR of the following : **16**

(a) Compare CMOS and BJT Technology.

(b) Explain the shift operations and logical operations.

(c) Write VHDL programme for 1 : 4 Demux using when-else statement.

(d) Draw FPGA configurable logic block diagram.

(e) Write various factors for selection of FPGA.

(f) Draw architecture of CPLD and explain in brief.

17659

16117

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Use of Non-programmable Electronic Pocket Calculator is permissible.

(7) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

(8) Use of Steam tables, logarithmic, Mollier's chart is permitted.

Marks

1. a) **Attempt any THREE of the following:** **12**

(i) Explain the process of estimation of resistance of the channel and how it is calculated.

(ii) Draw NAND and NOR gates using NMOS.

(iii) Explain Latch-up in CMOS and how it is minimized.

(iv) Explain any three operators used in VHDL.

b) **Attempt any ONE of the following:** **6**

(i) Explain CZ process for wafer fabrication, with neat diagram.

(ii) Define the terms:

1) Metastability

2) Noise margins

3) Skew

Marks

2. Attempt any FOUR of the following: **16**

a) Differentiate between Xiliv and Atmel series architecture of CPLD. (four points)

b) Compare Moore and Mealy machines. (four points)

c) Write VHDL code for 3-bit up-counter.

d) What are the advantages of twin-tub process of CMOS fabrication?

e) List the types of FSM. Draw labelled diagram of each.

f) Write the advantages and purpose of VHDL.

3. Attempt any FOUR of the following: **16**

a) Explain basic architecture of sparton 3 FPGA series.

b) What is Test bench and write down a typical test bench format.

c) Write VHDL code to implement 4:1 multiplexer.

d) Draw NAND gate using CMOS transistors.

e) Explain P well process with suitable diagram.

f) Write the output equation of Moore and Mealy machines. List any two examples of FSM.

4. a) Attempt any THREE of the following: **12**

(i) Write VHDL code to implement 4-bit adder.

(ii) Explain the following terms

1) Event scheduling

2) Simulation cycle

(iii) Draw CMOS transistor fabrication using n-well process.

(iv) Explain the following terms

1) Architecture

2) Configuration

b) Attempt any ONE of the following: **6**

(i) Draw architecture of XC9500 CPLD.

(ii) Design a sequence detector to detect the sequence 101.

Marks

5. Attempt any FOUR of the following: **16**

a) Differentiate FPGA and CPLD.

b) List and explain data types used in HDL.

c) Explain in cycle based simulation.

d) Draw the CMOS inverter characteristic and explain it.

e) Explain shift operators with example.

f) What is event scheduling and zero modelling.

6. Attempt any FOUR of the following: **16**

a) Explain oxidation and diffusion process in fabrication process.

b) Define the following terms related to VHDL

(i) Package

(ii) Entity

c) Explain HDL design flow for synthesis.

d) Explain the following terms

(i) Delta Delay

(ii) Sensitivity list

e) Execute the following equation by the circuit with CMOS logic.

$D = [(A \cdot B) + (C \cdot D)]$

f) What is meant by efficient coding style? How arithmetic expressions are optimized?

17659

16172

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Answer ***each*** *Section on* ***same/separate*** *answer sheet.*
(3) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(4) Figures to the ***right*** *indicate* ***full*** *marks.*
(5) Assume suitable data, ***if necessary****.*
(6) Use of Non-programmable Electronic Pocket Calculator is ***permissible****.*
(7) Mobile Phone, Pager and any other Electronic Communication devices are ***not*** *permissible in Examination Hall.*

Marks

1. A) Attempt **any three**: **12**

i) Define :
1) Asynchronous sequential circuit
2) Noise margin
3) Fan out
4) Skew.

ii) Write any two pro's and any two con's of VHDL.

iii) What do you mean by event based and cycle based simulator ?

iv) List any four features of Spartan 3 series FPGA.

B) Attempt **any one**: **6**

i) Describe the twin tub process for CMOS fabrication.

ii) Write the VHDL program to implement 4 bit adder.

2. Attempt **any four**: **16**

a) Design a sequence detector '10' using D-FF. If the sequence is valid, it gives the output z = '1' else 'z' = 0.

b) Realize the equation $y = \overline{(u + v)(w + x)}$ using CMOS logic.

c) What do you mean by enumerated data types ? Give the suitable example.

d) What do you mean by test bench ? State its applications.

e) Draw the HDL design flow for synthesis. Write the steps in the flow.

f) Compare FPGA and CPLD (any four).

P.T.O.

Marks

3. Attempt **any four** : **16**

a) What is metastability ? Give the example.

b) Compare BJT and CMOS (any four).

c) Define 1. Entity 2. Architecture in VHDL.

d) What are the different measures should be taken to write the efficient code ?

e) Draw the ASIC design flow and explain it.

4. A) Attempt **any three** : **12**

i) Draw the Moore machine and write its o/p equation.

ii) List the any four logical operators in VHDL.

iii) What do you mean by delta delay ? Give the example.

iv) Describe the following statement with syntax :

i) wait

ii) assert.

B) Attempt **any one** : **6**

i) Describe the resistance estimation of conducting material of uniform sheets with 'L' length. ' ρ ' resistivity, 'w' width and 't' thickness.

ii) Write the VHDL program to implement 8 : 3 encoder.

5. Attempt **any four** : **16**

a) Draw the state diagram and state table for 3 bit binary counter.

b) Explain with the syntax : 1. Signal 2. Variable.

c) Describe the transmission gate with neat sketch.

d) Write the VHDL program for 4 : 1 Mux.

e) Differentiate software programming language and hardware descriptive language.

f) Draw the functional block architecture of Xilinx CPLD.

6. Attempt **any four** : **16**

a) Describe the process of oxidation.

b) Define sensitivity list. State any two VHDL syntax in which sensitivity list is defined.

c) Draw the simulation cycle and label it.

d) Draw the FPGA configurable logic block with neat label.

e) Write two examples of CPLD and FPGA. Write one application of CPLD and FPGA.

17659

11718

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(3) Figures to the ***right*** *indicate* ***full*** *marks.*
(4) Use of Non-programmable Electronic Pocket Calculator is ***permissible****.*

Marks

1. A) Solve **any three** : **12**
a) Write VHDL program for 3 bit up counter. **4**
b) Define the terms : **4**
i) Noise margin
ii) Skew.
c) State the use and syntax of : **4**
i) Signal
ii) Constant.
d) Draw two input NAND gate using CMOS technology. Write its truth table. **4**
e) Explain efficient coding style. **4**
B) Solve **any one** : **6**
a) Explain different level of simulation in brief. **6**
b) Explain following statement with example : **6**
i) Process statement
ii) Wait statement.

2. Solve **any four** : **16**
a) Differentiate between BJT and CMOS. **4**
b) List the data types and explain any one. **4**
c) Draw and explain HDL design flow for synthesis. **4**
d) Draw ASIC design flow and explain it. **4**
e) Draw block diagram of Melay and Moore machine and explain it. **4**

3. Solve **any four** : **16**
a) Explain fabrication of N-well process. **4**
b) Define the terms with syntax : **4**
i) Entity
ii) Architecture.

P.T.O.

Marks

c) Write VHDL code for D flip-flop. **4**

d) State and explain : **4**
   i) Event scheduling
   ii) Simulation cycle.

e) Differentiate between CPLD and FPGA. **4**

4. A) Solve **any three** : **12**

a) Define the term : **4**
   i) Fan out
   ii) Metastability
   iii) Asynchronous sequential circuit
   iv) Synchronous sequential circuit.

b) Design boolean equation using CMOS : $Z = \overline{AB} + \overline{(C + D)}$. **4**

c) Draw transmission gate. Explain it. **4**

d) Draw neat diagram of architecture of SPARTAN-3 FPGA family and explain it. **4**

B) Solve **any one** : **6**

a) Explain twin tube process with suitable diagram. **6**

b) Draw architecture of CPLD. Explain in brief. **6**

5. Solve **any four** : **16**

a) State the pro's and con's of VHDL. **4**

b) Compare concurrent and sequential statement. **4**

c) Explain estimation of channel resistance of CMOS. **4**

d) Write various factor of selection of FPGA. **4**

e) Design a sequence detector to detect 011 using JK flip-flop using Melay machine. **4**

f) State and explain Delta delay. **4**

6. Solve **any four** : **16**

a) Write VHDL program to implement 4 : 1 mux using case statement. **4**

b) Write VHDL code for full adder. Draw the neat diagram. **4**

c) Differentiate software and hardware description language. **4**

d) Explain CZ method for water processing with neat diagram . **4**

e) Compare between asynchronous and synchronous sequential circuit. **4**

f) Explain zero modelling and sensitivity list. **4**

17659

16172

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Answer ***each*** *Section on* ***same/separate*** *answer sheet.*
(3) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(4) Figures to the ***right*** *indicate* ***full*** *marks.*
(5) Assume suitable data, ***if necessary****.*
(6) Use of Non-programmable Electronic Pocket Calculator is ***permissible****.*
(7) Mobile Phone, Pager and any other Electronic Communication devices are ***not*** *permissible in Examination Hall.*

Marks

1. A) Attempt **any three**: **12**

i) Define :
1) Asynchronous sequential circuit
2) Noise margin
3) Fan out
4) Skew.

ii) Write any two pro's and any two con's of VHDL.

iii) What do you mean by event based and cycle based simulator ?

iv) List any four features of Spartan 3 series FPGA.

B) Attempt **any one**: **6**

i) Describe the twin tub process for CMOS fabrication.

ii) Write the VHDL program to implement 4 bit adder.

2. Attempt **any four**: **16**

a) Design a sequence detector '10' using D-FF. If the sequence is valid, it gives the output z = '1' else 'z' = 0.

b) Realize the equation $y = \overline{(u + v)(w + x)}$ using CMOS logic.

c) What do you mean by enumerated data types ? Give the suitable example.

d) What do you mean by test bench ? State its applications.

e) Draw the HDL design flow for synthesis. Write the steps in the flow.

f) Compare FPGA and CPLD (any four).

P.T.O.

Marks

3. Attempt **any four** : **16**

a) What is metastability ? Give the example.

b) Compare BJT and CMOS (any four).

c) Define 1. Entity 2. Architecture in VHDL.

d) What are the different measures should be taken to write the efficient code ?

e) Draw the ASIC design flow and explain it.

4. A) Attempt **any three** : **12**

i) Draw the Moore machine and write its o/p equation.

ii) List the any four logical operators in VHDL.

iii) What do you mean by delta delay ? Give the example.

iv) Describe the following statement with syntax :

i) wait

ii) assert.

B) Attempt **any one** : **6**

i) Describe the resistance estimation of conducting material of uniform sheets with 'L' length. ' ρ ' resistivity, 'w' width and 't' thickness.

ii) Write the VHDL program to implement 8 : 3 encoder.

5. Attempt **any four** : **16**

a) Draw the state diagram and state table for 3 bit binary counter.

b) Explain with the syntax : 1. Signal 2. Variable.

c) Describe the transmission gate with neat sketch.

d) Write the VHDL program for 4 : 1 Mux.

e) Differentiate software programming language and hardware descriptive language.

f) Draw the functional block architecture of Xilinx CPLD.

6. Attempt **any four** : **16**

a) Describe the process of oxidation.

b) Define sensitivity list. State any two VHDL syntax in which sensitivity list is defined.

c) Draw the simulation cycle and label it.

d) Draw the FPGA configurable logic block with neat label.

e) Write two examples of CPLD and FPGA. Write one application of CPLD and FPGA.

17659

21718

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(3) Figures to the ***right*** *indicate* ***full*** *marks.*
(4) Assume suitable data, if ***necessary****.*
(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. A) Attempt **any three** : **12**

i) Draw the AND gate and NOR gate using CMOS.
ii) Write VHDL code for 3-bit up counter.
iii) What is instantiation in VHDL ? Write one example.
iv) Draw the diagram of Moore machine and Mealy machine. Write expression for its output.

B) Attempt **any one** : **8**

i) Write any six features of spartan-3.
ii) Draw the diagram of Cz process for water fabrication. List the steps involved in water fabrication.

2. Attempt **any four** of the following : **(4×4=16)**

a) Design a mealy sequence detector circuit for detecting sequence 101 using J-K flipflop.
b) Explain how to estimate the channel resistance of CMOS transistor.
c) Compare BJT and CMOS technology.
d) Write the syntax of entity and architecture in VHDL programming.
e) Explain the sharing of complex operators.
f) Write the VHDL code for full adder.

3. Attempt **any four** of the following : **(4×4=16)**

a) State the any four features of VHDL.
b) Design the boolean expression r = (A + B). C using CMOS logic.
c) Compare synchronous and asynchronous sequential circuits. (any four points).
d) Write the VHDL code for 3 : 8 decoder.
e) Explain efficient coding styles.
f) Compare FPGA and CPLD.

P.T.O.

Marks

4. Attempt **any four** of the following : **(4×4=16)**

a) Write two advantages and disadvantages of VHDL.

b) Define the following terms related to fabrication process.

i) Oxidation

ii) Ion-implantation

iii) Diffusion

iv) Deposition.

c) Write the VHDL code for D-flipflop.

d) Design parity generator using moore machine.

e) Compare hardware and software description language.

f) Draw FPGA's configurable logic block diagram and write the function of it.

5. Attempt **any four** of the following : **(4×4=16)**

a) State the applications of test bench and write down the typical format of test bench.

b) Design 2-bit sequential counter using mealy machine.

c) Explain n-well CMOS fabrication process with neat sketches.

d) List the datatypes used in HDL and explain.

e) Explain event scheduling.

f) Draw the design flow of ASIC and explain.

6. Attempt **any four** of the following : **(4×4=16)**

a) Write the VHDL code for 3-bit right shift register.

b) Draw HDL design flow for synthesis and explain.

c) Explain CMOS transmission gate with neat diagram.

d) Draw the architecture of XC9500 CPLD.

e) Explain event based simulator.

f) Differentiate between Xilinx and Atmel series architecture of CPLD (four points).

11819

17659

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Answer ***each*** *next main question on a* ***new*** *page.*
(3) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(4) Figures to the ***right*** *indicate* ***full*** *marks.*
(5) Assume suitable data, if ***necessary****.*

Marks

1. A) Attempt **any three** : **(3×4=12)**

1) Compare Asynchronous sequential and synchronous sequential circuits.
2) Explain estimation of channel capacitance of CMOS.
3) Draw CMOS two input NOR gate and write it's truth table.
4) State any 4 features of VHDL.

B) Attempt **any one** : **(1×6=6)**

1) Compare FPGA and CPLD (any six pts.)
2) State any one process for wafer fabrication with diagram.

2. Attempt **any four** : **(4×4=16)**

1) Explain fabrication using N-well process.
2) Design $Y = \overline{AB}.\ \overline{CD}$ using CMOS logic.
3) What do you mean by simulation ? Why it is necessary ?
4) Compare Mealy M/C with Moore M/C.
5) Write VHDL code for half adder.

3. Attempt **any four** : **(4×4=16)**

1) Write the syntax of entity and architecture used in VHDL and explain it.
2) Draw 2 : 4 decoder and write VHDL code for it.
3) Describe Twin-tube process with diagram.
4) What do you meant by sensitivity list and zero modeling ?
5) Compare signals and variables in VHDL.

P.T.O.

Marks

4. A) Attempt **any three** : **(3×4=12)**

1) Define the following terms :
   i) Noise margin
   ii) Power fanout
   iii) Skew
   iv) Meta stability
2) Explain event scheduling with suitable example.
3) What is test bench ? Write its applications.
4) List different concurrent statements and give the example of any two.

B) Attempt **any one** : **(1×6=6)**

1) Draw architecture of XC9500 CPLD.
2) Design a sequence detector to detect the sequence 110. Use D F/F to design the circuit.

5. Attempt **any four** : **(4×4=16)**

1) Draw the HDL design flow for synthesis.
2) State the function of each step elements of VHDL.
3) Draw CMOS inverter characteristic and explain it.
4) Write VHDL code for 4 : 1 MUX.
5) List the types of FSM. Draw labelled diagram of each.

6. Attempt **any four** : **(4×4=16)**

1) Explain basic architecture of Spaston-3 FPGA series.
2) Write VHDL code for 3-bit down counter.
3) Draw design flow of ASIC and explain it.
4) Explain the shift and logical operations.
5) State different modeling styles used in VHDL and write VHDL code for 1 : 4 DEMUX using any one style.

17659

21819

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Answer each next main Question on a new page.

(3) Figures to the right indicate full marks.

Marks

1. Attempt any FIVE : **5 × 4 = 20**

(a) Draw AND gate and NOR gate using NMOS.

(b) Define : (i) Metastability

(ii) Noise Margin

(c) Compare Moore and Mealy machine.

(d) What is VHDL ? Write two advantages of VHDL.

(e) Explain : (i) Sensitivity list.

(ii) Wait statement.

(f) Explain the wafer processing with C-Z method.

(g) Design Mealy sequence detector circuit for detecting sequence of "001".

2. Attempt any FOUR : **4 × 4 = 16**

(a) Compare synchronous & asynchronous sequential circuits.

(b) Draw the architecture of sparatan-3 FPGA series. Explain any two blocks.

(c) Explain : (i) Flattening

(ii) Structuring

(d) Write VHDL program for 3 : 8 decoder.

(e) List and explain data types used in VHDL.

(f) Draw and explain CMOS AND gate.

3. Attempt any FOUR : **16**

(a) List and explain features of CPLD.

(b) State and explain delta delay.

(c) Write VHDL code for Full ADDER.

(d) Explain N-well process with diagram.

(e) Explain Resistance Fabrication.

(f) Design parity checker using Moore logic or Mealy logic.

4. Attempt any FOUR : **4 × 4 = 16**

(a) Compare FPGA and CPLD.

(b) Explain cycle based and event based simulators.

(c) Describe verification using Test Bench.

(d) Write VHDL code for 2 : 1 MUX using if… else statements.

(e) Explain Twin-Tab process in CMOS fabrication with diagram.

(f) Explain HDL design flow for synthesis.

5. Attempt any FOUR : **4 × 4 = 16**

(a) Explain : (i) Sensitivity list

(ii) Zero modeling

(b) Draw the architecture of Xilinx 9500 family CPLD. Explain any two blocks.

(c) What is instantiation in VHDL ? Write one example.

(d) List and explain different types of operators in VHDL.

(e) State and explain efficient coding styles.

(f) Write the VHDL code for 4-bit adder without instantiation.

6. Attempt any FOUR : **4 × 4 = 16**

(a) Explain the following process :

(i) Oxidation process

(ii) Diffusion process

(b) Draw ASIC design flow.

(c) Compare software & hardware description language.

(d) Write VHDL program for 4 : 1 MUX using case statement.

(e) Explain Entity and Architecture with suitable example.

(f) Design the following function using CMOS :

$Y = (A \cdot B) + C$

17659

11920

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Solve any FIVE : **20**

(a) List the types of FSM. Draw labelled diagram for each.

(b) Define the following terms :

(i) Metastability

(ii) Noise margin

(iii) Fan out

(iv) Skew

(c) Explain (i) Event scheduling (ii) zero modeling.

(d) Design the NAND Gate using CMOS and write its truth table.

(e) Explain the HDL terms entity and Architecture with syntax.

(f) Compare Software and Hardware description language.

(g) Write the VHDL code to implement 2 I/P NOR gate.

2. Solve any FOUR : **16**

(a) Write a VHDL code for 3 : 8 decoder.

(b) Write a VHDL code for 16 : 1 MUX.

(c) Explain the main steps carried out in a p-well process.

(d) Draw state diagram of a sequence detector to detect a sequence of '1101'.

(e) Explain different Data Types in VHDL.

(f) Explain the silicon gate process for N-MOS transistor.

3. Solve any FOUR : **16**

(a) Write VHDL code for four bit binary to array code converter.

(b) Explain different types of sequential constructs in VHDL.

(c) State the features of VHDL (any four).

(d) Describe oxidation in CMOS fabrication.

(e) Explain resistance estimation of MOSFET.

(f) Design a CMOS logic gate for the function

$f = \overline{A \cdot B + C \cdot D}$

4. Solve any FOUR : **4 × 4 = 16**

(a) Draw and explain design flow of ASIC.

(b) Compare Moore and Melay type of state machine (any four points)

(c) Write steps for designing clocked synchronous state machine.

(d) Compare BJT with CMOS.

(e) Explain architecture of Xilinx 9500 family CPLD.

(f) Explain sharing of complex operator in HDL.

5. Solve any TWO : **16**

(a) List the steps carried out in the twin tub fabrication. Also state the advantages.

(b) Explain simulation deltas with an example.

(c) Draw and explain basic architecture of Spartan-3 FPGA series.

6. Solve any TWO : **16**

(a) Draw the functional blocks of XC4000 FPGA series and differentiate between FPGA and CPLD (any four points).

(b) Explain HDL design flow for synthesis in detail.

(c) Write test bent for 2 input AND Gate and state applications of test bench.
