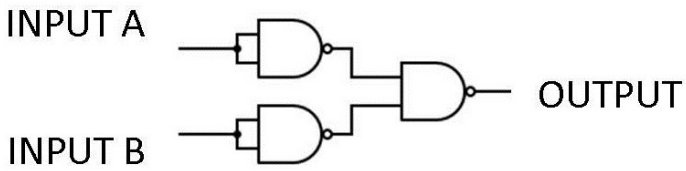
Important suggestions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more importance. (Not applicable for subject English and communication skills)
4) While assessing figures, examiner may give credit for principle components indicated in a figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case some questions credit may be given by judgment on part of examiner of relevant answer based on candidate understands.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q.1 **Attempt any FIVE of the following** **5x2= 10 Marks**

a) **Construct OR gate using NAND gate.**

Ans: **OR gate using NAND gate:** **(2 Marks)**

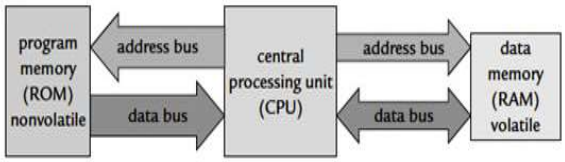
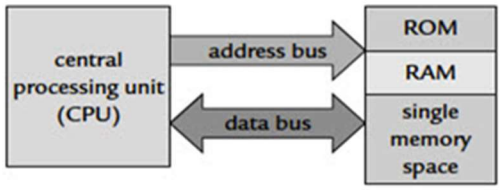


or equivalent

b) **Compare Harward and Von-Neuman architecture. (any two points)**

Ans: **(Any Two point expected: 1 Mark each, Total 2 Marks)**

S.No	Harward architecture	Von-Neumann architecture
1	The computer has two separate memories for storing data and program. e.g. 8051 microcontroller	The computer has single storage system(memory) for storing data as well as program to be executed e.g. 8085 microprocessor
2	Faster Execution of program	Slower execution of program
3	Requires more hardware because of separate bus-structure	Requires less hardware because of single bus structure

	4	 
c)	**Write the excitation table for T-FF.**	
Ans:	**Excitation table for T-FF:** **(2 Marks)**	

Q(t)	Q(t+1)	T	Operation
0	0	0	No change
0	1	1	Complement
1	0	1	Complement
1	1	0	No Change

d)	**Define : (i) Address bus (ii) Data bus.**
Ans:	**Address bus:** **(1 Mark)** It is the bunch of wires which carry binary address of the peripheral that is connected to CPU **Data Bus:** **(1 Mark)** It is the bunch of wires which carry binary data that is exchanged between CPU and peripheral
e)	**List the different addressing modes of 8051.**
Ans:	**Following addressing modes of 8051:** **(Any Two point expected: 1 mark each, Total 2 Mark)** 1) Immediate addressing mode 2) Direct Addressing mode 3) Register addressing mode 4) Register indirect addressing mode 5) Indexed addressing mode
f)	**Define : (i) Assembler (ii) Compiler**
Ans:	**(i) Assembler:** **(1 Mark)** Assembler converts assembly language program into object code or machine code **(ii) Compiler:** **(1 Mark)** Compiler converts higher level language programs (C language) into machine codes

g) Find the number of address lines required for (i) 4K RAM (ii) 8K ROM

Ans: (i) For 4K RAM : - 12 address line as 2^{12}=4096 **(1 Mark)**

(ii) For 8K ROM : - 13 address lines as 2^{13}=8192 **(1 Mark)**

Q. 2 Attempt any THREE of the following 3x4= 12 Marks

a) State & explain De-Morgan's first theorem.

Ans: De-Morgan's first theorem: (4 Marks)

DeMorgan's Theorem is mainly used to solve the various Boolean algebra expressions. The **Demorgan's theorem** defines the uniformity between the gate with same inverted input and output. It is used for implementing the basic gate operation likes NAND gate and NOR gate.

It states that "when OR sum of two variables is inverted, it is equivalent to ANDing of NOT output of each variable"

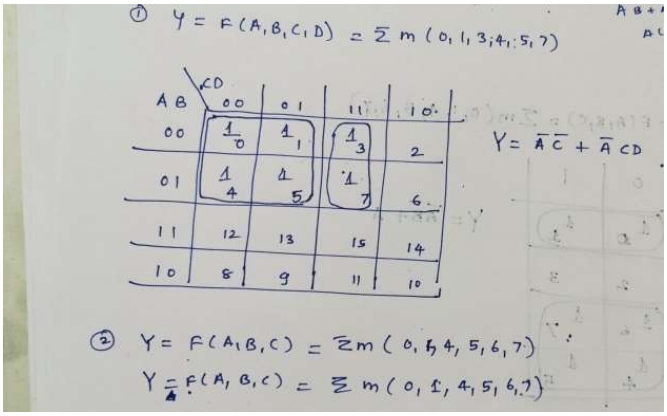
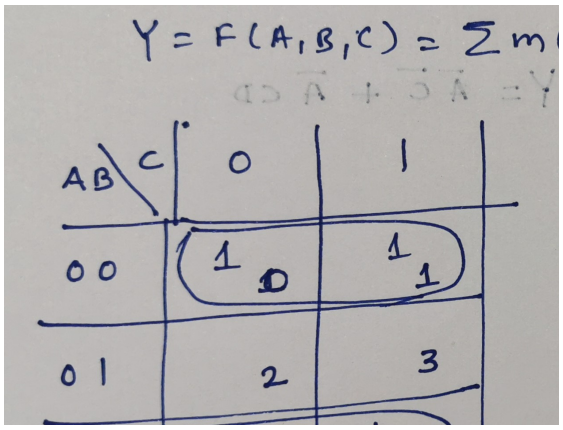
$$\overline{A+B} = \overline{A}.\overline{B}$$

b) Compare microprocessor & microcontroller. (any four points)

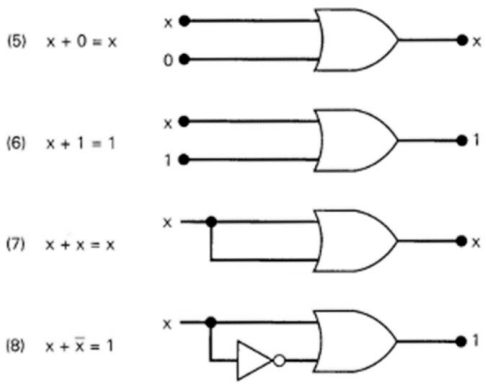
(Any four point expected: 1 mark each, total 4 Mark)

Ans:

S.No	Microprocessor	Microcontroller
1	It is just a CPU i.e. central processing unit with address and data bus. It requires memory and other peripherals to make a computer	It is a computer on single chip. It consists of CPU memory and peripherals in a single chip.
2	It does not have digital input output ports. Needs to be externally connected	It has several digital input output lines 8051 has 32 I/O lines
3	It is mainly used for information processing, multimedia and for making desktop computer.	It is mainly used for digital control in industrial applications or in home appliances
4	It can have large external memory	Memory capacity is small
5	It is based on VonNeumann architecture	It is based on Harward architecture
6	Cost and size of hardware is large	It is cheaper in cost and compact in size
7	Example: 8085 microprocessor, Pentium processor	Example: 8051, 8052 microcontroller

c)	**Solve the following SOP expressions with the help of K-map :** **(i) F(A, B, C, D) = Σm (0, 1, 3, 4, 5,7) (ii) F(A, B, C) = Σm (0, 1, 4, 5, 6, 7)**
Ans:	**(i) F(A, B, C, D) = Σm (0, 1, 3, 4, 5,7) :** **(2 Mark)**  **(ii) F(A, B, C) = Σm (0, 1, 4, 5, 6, 7):** **(2 Mark)** 
d)	**Write any two laws of Boolean algebra. Justify with the help of truth table.**

Ans:	**(4 Marks)**
	The basic Laws of Boolean Algebra can be stated as follows**: (Any Two expected)**
	1. **Commutative Law** states that the interchanging of the order of operands in a Boolean equation does not change its result. For example:
	  1. OR operator → A + B = B + A
	  2. AND operator → A * B = B * A
	2. **Associative Law** of multiplication states that the AND operation are done on two or more than two variables. For example:
	A * (B * C) = (A * B) * C
	3. **Distributive Law** states that the multiplication of two variables and adding the result with a variable will result in the same value as multiplication of addition of

	the variable with individual variables. For example: A + BC = (A + B) (A + C). **OR** 1. Annulment law: A.0 = 0 A + 1 = 1 2. Identity law: A.1 = A A + 0 = A 3. Idempotent law: A + A = A A.A = A 4. Complement law: A + A' = 1 A.A'= 0 5. Double negation law: ((A)')' = A 6. Absorption law: A.(A+B) = A A + AB = A **OR**  or equivalent table
Q.3	**Attempt any THREE of the following** **12 Marks**
a)	**List any eight features of microcontroller 8051.**
Ans:	**Following features of microcontroller 8051.** **(Any four point expected: 1 mark each, total 4 Mark)**

1) 4kbytes of Program memory
2) 128 bytes of data memory
3) 1 serial port
4) 2 internal timers of 16bit
5) 40 pin device
6) Power supply voltage 5V
7) 5 interrupt sources
8) Harward architecture
9) 32 bidirectional IO lines divided in 4 IO ports
10) 16 address and 8 data lines available on port P0 and P2

b) Compare TTL, CMOS & ECL families on the following : (i) Power dissipation (ii) Noise Margin (iii) Speed of Operation (iv)Fan-in

Ans: **(Each point : 1 Mark, Total 4 Mark)**

S.No	Point	TTL	CMOS	ECL
1	Power dissipation	10mW	0.001mW	175mW
2	Noise margin	Very good 0.5V	Excellent,1.5V	Good 0.16V
3	Speed of operation	fast	Moderate	fastest
4	Fan-in	12-14	>10	>10

c) Describe the function of following pins of 8051 : (i) PSEN (ii) RESET (iii) ALE (iv) ĒA

Ans:

PSEN- **(1 Mark)**

It is an output control signal used to enable external program memory. It is to be connected to /RD pin of external program memory.

RESET: **(1 Mark)**

It is active high input signal to 8051 used to reset 8051. When it is HIGH, 8051 program counter is reset to 0000h.

ALE: **(1 Mark)**

Address latch enable. It is output control signal to indicate presence of address on lower 8 bit address lines AD0-AD7 on port P0.

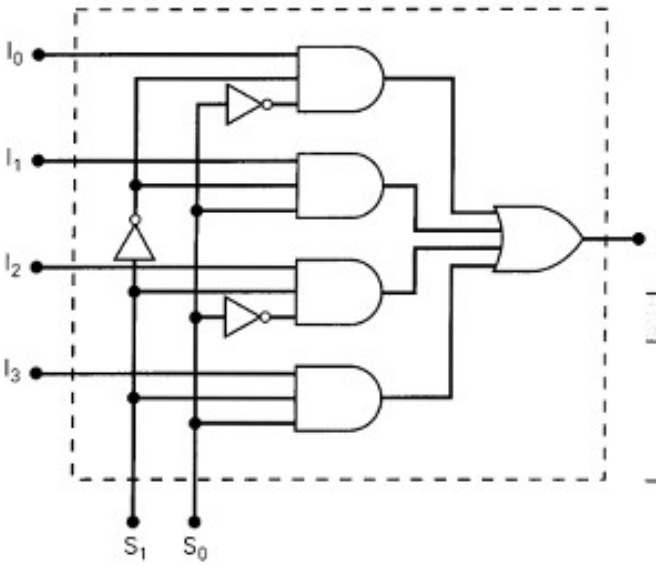
ĒA- **(1 Mark)**

It is active low control input signal. When /EA is at logic 0, external program memory is used. When /EA is at logic 1, internal program memory is used for address range 0000-0FFF.

d) Draw logic diagram of 4 : 1 multiplexer & give it's truth table.

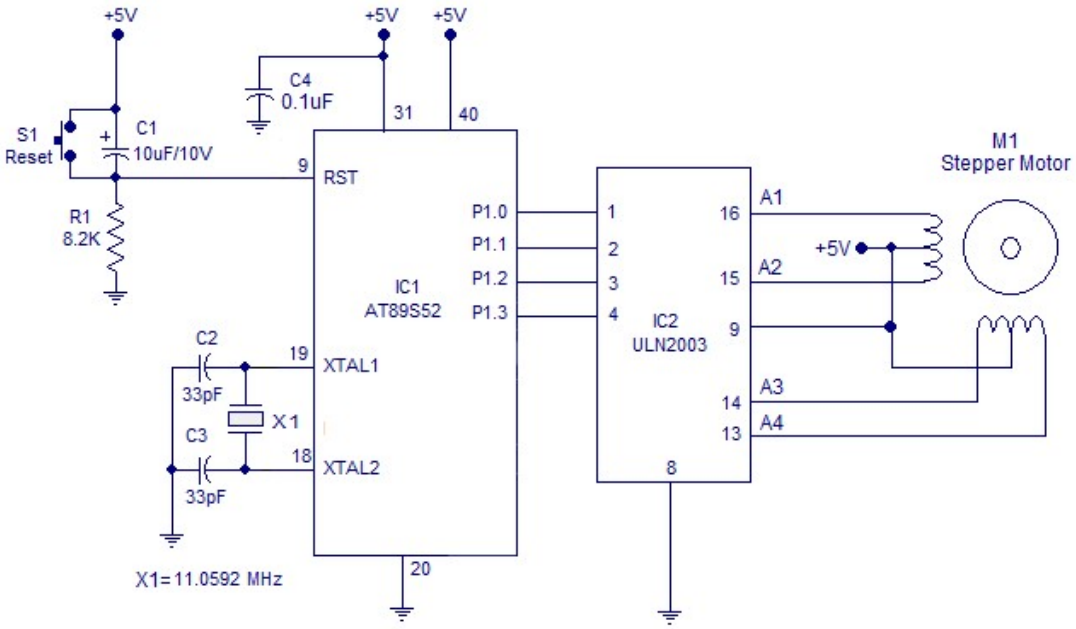
Ans: logic diagram of 4 : 1 multiplexer & give it's truth table :

(Diagram: 2 Mark, Truth table: 2 Mark, Total 4 Mark)



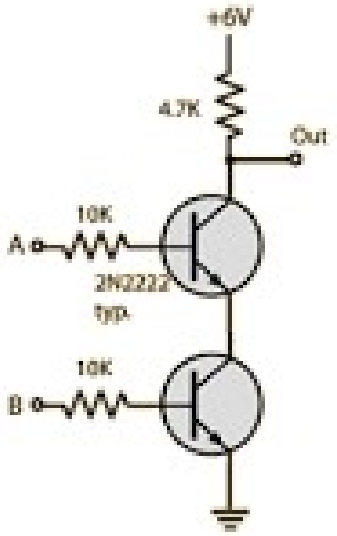
S_1	S_0	Output
0	0	$Z = I_0$
0	1	$Z = I_1$
1	0	$Z = I_2$
1	1	$Z = I_3$

Q.4	Attempt any THREE of the following	12 Marks
a)	**Draw a neat labelled interfacing diagram of 8051 with stepper motor.**	
Ans:	**labelled interfacing diagram of 8051 with stepper motor:**	**(4 Mark)**



or equivalent figure

b)	**Implement OR gate using transistor.**	
Ans:	**OR gate using transistor:**	**(4 Mark)**



or equivalent figure

c) Write the alternative function of Port-3 pins.

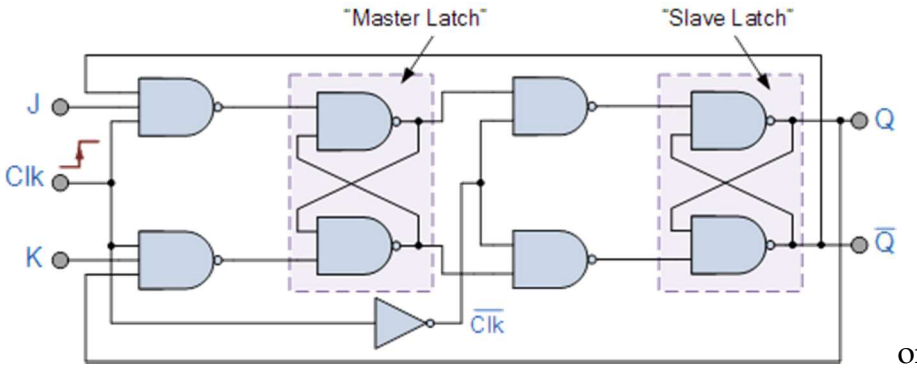
Ans: **Alternative function of Port-3 pins:** **(4 Marks)**

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

d) Draw master-slave JK FF & write it's truth table.

Ans: **Master-slave JK FF & write it's truth table:**

(Diagram: 2 Mark & truth table : 2 Marks)



or equiavlet figure

J	K	CLK	Q	Q'	
0	0	⊓	Q_0	Q_0'	Hold
0	1	⊓	0	1	Reset
1	0	⊓	1	0	Set
1	1	⊓	Q_0'	Q_0	Toggle (opposite state)

e) Explain Boolean processor of 8051.

Ans: **Explanation: Boolean processor of 8051:** **(4 Marks)**

The Boolean processor of 8051 offers single bit operations.

The internal RAM contains 128 bit addressable bits.

All port lines are bit addressable
Many SFRs are bit addressable. E.g. Accumulator, PSW register, TCON, IE register.
Different Boolean instructions are

Mnemonic		Description	Byte	Cyc
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
MOV	C.bit	Move direct bit to Carry flag	2	1
MOV	bit.C	Move Carry flag to direct bit	2	2
ANL	C.bit	AND direct bit to Carry flag	2	2
ANL	C.bit	AND complement of direct bit to Carry flag	2	2
ORL	C.bit	OR direct bit to Carry flag	2	2
ORL	C.bit	OR complement of direct bit to Carry flag	2	2
JC	rel	Jump if Carry is flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit.rel	Jump if direct Bit set	3	2
JNB	bit.rel	Jump if direct Bit Not set	3	2
JBC	bit.rel	Jump if direct Bit is set & Clear bit	3	2

Q.5 **Attempt any TWO of the following** **12 Marks**

a) **Execute the following program & specify the contents of Accumulator & status of PSW after execution. Also draw the format of PSW**

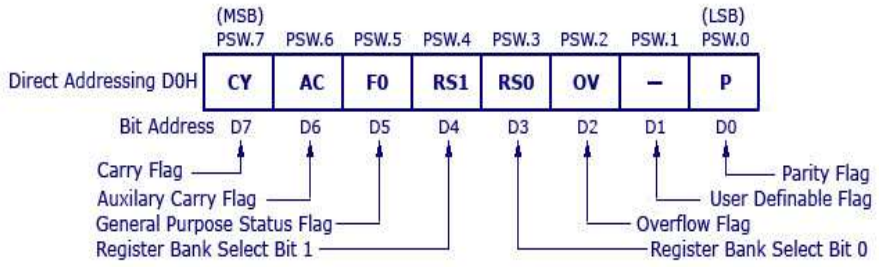
```
MoV A, #OFH
MoV B, #03H
Div AB
End
```

Ans: **(6 Marks)**

1) ACC will be loaded with number 0Fh (15 decimal)
2) B register will be loaded with 03h (03 decimal)
3) Division instruction will be executed
4) Contents of A = 05H , B= 00h,

Carry flag =0, OV flag =0

Processor Status Word



b) Develop an ALP to generate square wave of 1kHz at port pin P1.3. Draw flowchart for it.

Ans: **(6 Marks)**

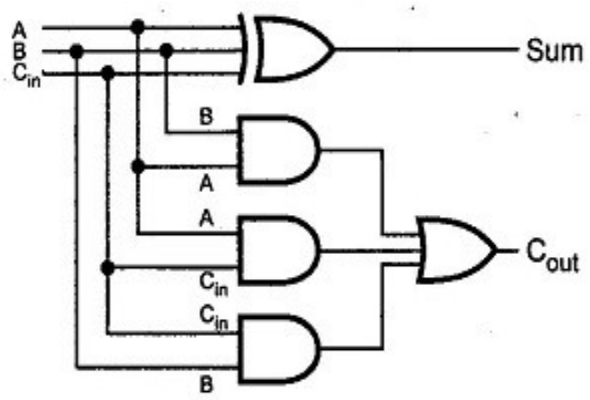
```
        //assume clock input 12Mhz
        //required counts = 65536-500=FE0Ch
        MOV P1,#00000000B
        MOV TMOD,#00000001B
MAIN:   SETB P1.0
        ACALL DELAY
        CLR P1.0
        ACALL DELAY
        SJMP MAIN

DELAY:  MOV TH0,#0FEH
        MOV TL0,#00CH
        SETB TR0
HERE:   JNB TF0,HERE
        CLR TR0
        CLR TF0
        RET
        END
```

A suitable flow chart may be given credit.

c) Explain full adder with it's logic diagram & truth table.

Ans: **full adder with it's logic diagram & truth table:**

(Diagram: 3 Mark & Truth table: 3 Mark, Total 6 Marks)



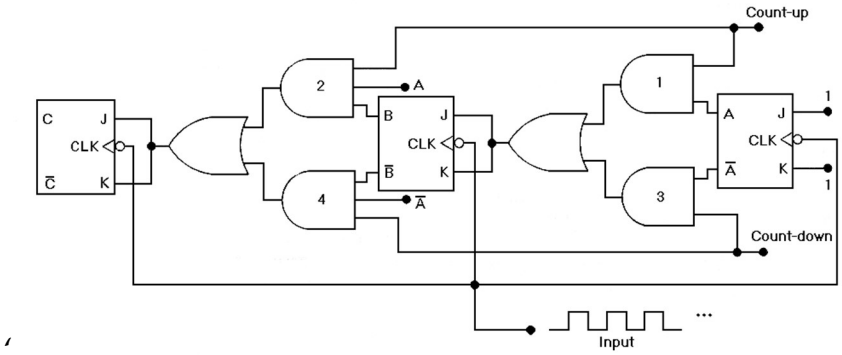
Inputs			Outputs	
A	B	C_{in}	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

or equivalent figure

Q.6	Attempt any TWO of the following	12 Marks
a)	Construct 3-bit synchronous UP counter using flip-flop. Also draw it's timing diagram.	

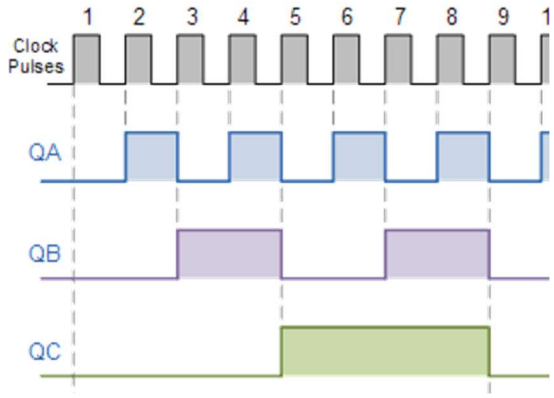
Ans:

3-bit synchronous UP counter using flip-flop : **(3 Marks)**



or Equivalent diagram

Timing diagram: **(3 Marks)**



or Equivalent diagram

b)	**Describe the following assembler directives with one example of each :** **(i) ORG (ii) DB (iii) EQU (iv) END (v) CODE (vi) DATA**

Ans:

(Each assembler directives : 1 Mark, Total 6 Marks)

i) **ORG:** (Origin) It is the assembler directive to indicate starting address of program.

Example:

ORG 0000h

LJMP MAIN

ii) DB – Define Byte It is the directive used to define 8 bit data

example: DATA1 DB 39H

iii) EQU : Equate It is the directive used to define constant without occupying memory location.

Example: COUN T EQU 25

iv) END: end of program. It is the directive used to indicate end of assembly program

v) CODE: It is the directive used to indicate assembler to start CODE segment

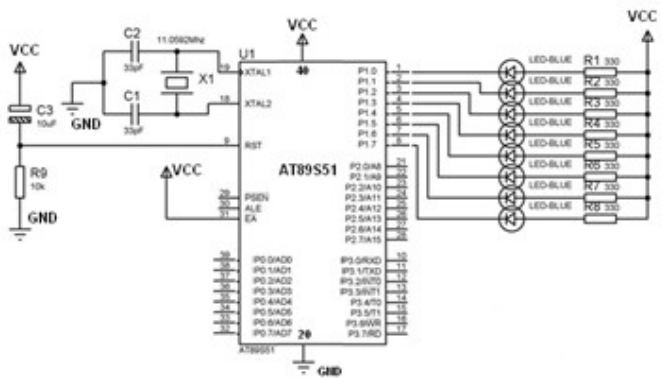
vi) DATA: It is the directive used before variable declarations.

c) Develop an ALP for interfacing of LED's with Port 1 of 8051. Draw interfacing diagram for the same.

Ans: **Developing an ALP for interfacing of LED's with Port 1 of 8051**: **(3 Marks)**

```
        MOV P1,#00h ;configure all lines of port P1 in output mode
AGAIN:  MOV P1,#00h
        ACALL DELAY
        MOV P1,#0FFh
        ACALL DELAY
        SJMP AGAIN

DELAY:  MOV R0,#0FFh
BACK2:  MOV R1,#05H
BACK1:  DJNZ R1,BACK1
        DJNZ R0,BACK2

        END
```

Interfacing diagram : **(3 Marks)**



or equivalent diagram

----------END----------