MODEL ANSWER

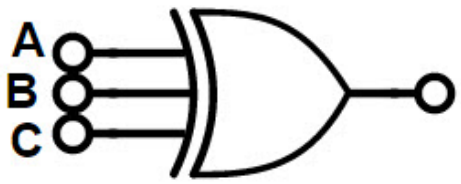
SUMMER – 2018 EXAMINATION

Subject: Digital Techniques **Subject Code:** **17333**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
1.	**A)** **a)** **Ans.**	**Attempt any six:** **State any two advantages and disadvantages of digital circuits.** **Advantages of digital circuits:** 1. Digital Electronic circuits are relatively easy to design. 2. It has higher accuracy, programmability. 3. Transmitted signals are not degraded over long distances. 4. Digital Signals can be stored easily. 5. Digital Electronics is comparatively more immune to 'error' and 'noise'. But in case of high speed designs a small noise can induce error in signal. 6. More Digital Circuits can be fabricated on integrated chips; this helps us obtain complex systems in smaller size. **Disadvantages of digital circuits:** 1. Digital Circuits operate only with digital signals hence, encoders and decoders are required for the process. This increases the cost of equipment. 2. Energy consumption in digital circuit is more than analog circuit	**12** **2M** ***Any two advantages and disadvantages ½ M each***

		for same calculation or signal processing. 3. Production of heat is more due to higher energy consumption. 4. For smaller circuits Digital Circuits are comparatively expensive. 5. Real world is analogue in nature, all quantities such as light, temperature, sound etc. For Digital Systems it is required to translate a continuous signal to discrete which leads to small quantization errors. To reduce quantization errors large amount of data needs to be stored in Digital Circuit. 6. Portability of digital circuit is difficult.	
	b) Ans.	**Define Fan-out and Power Dissipation.** **Fan-out:** Fan out is the maximum number of similar gates which can be driven by a gate. A fan out of 6 indicates that the gate can drive maximum 6 inputs of gates having same IC family. **Power Dissipation:** Power dissipation is the amount of power dissipated in an IC. Due to applied voltage V_{ee} and current flowing through the $I_{c,}$ some power is dissipated in it in the form of heat. It is determined by the current I_{cc} that it draws from the V_{cc} supply. The power dissipated is given by $P = V_{cc} X I_{cc}$ This power is in milliwatts.	**2M** ***Fan-out 1M*** ***Power dissipation 1M***
	c) Ans.	**Draw symbol and truth table of 3-i/p Ex-OR gate.** **Symbol of 3-i/p Ex-OR gate:**  **Truth table of 3-i/p Ex-OR gate:** For XOR gates, we can have the HIGH input when odd numbers of inputs are at HIGH level. The 3-input X-OR gate is called as 'Odd functioned OR gate'.	**2M** ***Symbol 1M***

		<table><tr><th colspan="3">Inputs</th><th>outputs</th></tr><tr><th>W</th><th>X</th><th>Y</th><th>Q = A⊕B⊕C</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>	***Truth Table 1M***
	d) **Ans.**	**Convert $(10110)_2 = (?)_6, (?)_8$.** ***(Note: Calculation based on base 16).*** • **$(10110)_2 = (?)_{16}$:** Step 1: Split the given binary number into groups from right, each containing 4 bits. 1 0110 Group 2 Group 1 Step 2: Add 0 or 0s to the left side if any group is lack of 4 bits. Group 2 containing only 1 bit so add three zeros to the left. 0001 0110 Step 3: Find the Hex equivalent for each group. 0001 0110 ⇩ ⇩ 1 6 **$(10110)_2 = (16)_{16}$** • **$(10110)_2 = (?)_8$** Find out Octal Equivalent for Binary 10110 Convert the binary number into groups from right side, each containing 3 bits 10 110 group 2 group 1 group 2 contains only 2 bits, so add 0 to the left	**2M** ***Each calculation 1M***

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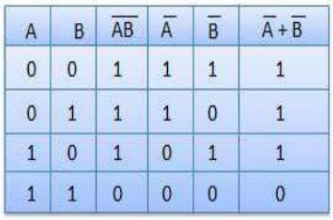
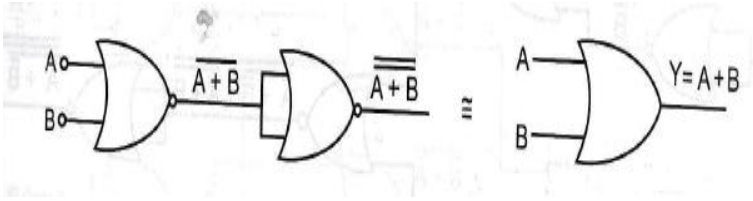
		0 1 0 1 1 0 ⇩ ⇩ 2 6 Arrange the numbers in same order So the Octal equivalent is 26 **$(10110)_2 = (26)_8$**	
	e) **Ans.**	**State any four Boolean Laws.** **Boolean laws:** A + 1 = 1 A + 0 = A A . 1 = A A . 0 = 0 A + A = A A . A = A A+B = B+A A.B = B.A (A + B) + C = A + (B + C) (A B) C = A (B C) A (B + C) = A B + A C A + (B C) = (A + B) (A + C)	**2M** ***Any 4 Boolean laws ½ M each***
	f) **Ans.**	**Explain the rules to simplify Boolean equation using K-map (any two).** **Rules to simplify Boolean equation using K-map:** 1. Enter a '1' on the K-map for each fundamental product that produces a '1' in the truth table. Enter 'o' case 'o' else where. 2. Encircle the octet, quads, pairs remember to roll and overlap to get the largest group possible. 3. If any isolated '1' remains encircle each. 4. Eliminate any redundant group. 5. Write the Boolean expression by 'o' ring the product corresponding to encircled groups.	**2M** ***Any 2 rules 1M each***
	g) **Ans.**	**Compare RAM and ROM memories (any two point)** **Comparison** | **RAM** | **ROM** Data | The data is not permanent and it can be altered any | The data is permanent it can be altered but only a limited number of times	**2M**

			number of times.	that too at slow speed.	***Any 2 points 1M each***
			Speed	It is high-speed memory.	It is much slower than the RAM
			CPU Interaction	The CPU can access the data stored on it.	The CPU can not access the data stored on it. In order to do so, the data is first copied to the RAM.
			Size and capacity	Large size with higher capacity.	Small size with less capacity.
			Usage	Primary memory (DRAM DIMM modules), CPU Cache	Firmware like BIOS or UEFI, RFID tags, microcontrollers, medical devices, and at places where a small and permanent memory solution.
	h) Ans.	**State two specification of DAC.** **1. Resolution: Resolution** is defined as the ratio of change in analog output voltage resulting from a change of 1 LSB at the digital input V_{FS} is defined as the full scale analog output voltage i.e. the analog output voltage when all the digital input with all digits 1. $$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$ **2. Accuracy:** Accuracy indicates how close the analog output voltage is to its theoretical value. It indicates the deviation of actual output from the theoretical value. Accuracy depends on the accuracy of the resistors used in the ladder, and the precision of the reference voltage used. Accuracy is always specified in terms of percentage of the full scale output that means maximum output voltage **3. Linearity:** • The relation between the digital input and analog output should be linear. • However practically it is not so due to the error in the values of resistors used for the resistive networks. **4. Temperature sensitivity:**	**2M** ***Any two specification of DAC 1M each***

		• The analog output voltage of D to A converter should not change due to changes in temperature. • But practically the output is a function of temperature. It is so because the resistance values and OPAMP parameters change with changes in temperature. **5. Settling time**: • The time required to settle the analog output within the final value, after the change in digital input is called as settling time. • The settling time should be as short as possible. **6. Long term drift** • Long term drift are mainly due to resistor and semiconductor aging and can affect all the characteristics. • Characteristics mainly affected are linearity, speed etc. **7. Supply rejection** • Supply rejection indicates the ability of DAC to maintain scale, linearity and other important characteristics when the supply voltage is varied. • Supply rejection is usually specified as percentage of full scale change at or near full scale voltage at 25^{o}e **8. Speed:** • It is defined as the time needed to perform a conversion from digital to analog. It is also defined as the number of conversions that can be performed per second	
1.	**B)** **a)** **Ans.**	**Attempt any two:** **State and prove DeMorgan's theorem.** **Theorem1**: It state that the, complement of a sum is equal to product of its complements $\overline{A+B} = \overline{A}.\overline{B}$ NOR = Bubbled AND A B $\overline{A+B}$ $\overline{A}$ $\overline{B}$ $\overline{A}.\overline{B}$ 0 0 1 1 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 0 0 0 0	**8** **4M** ***Theorem 1M each*** ***Prove 1M each***

		Theorem2: It states that, the complement of a product is equal to sum of the complements. $\overline{A.B} = \overline{A} + \overline{B}$ NAND = Bubbled OR  A B $\overline{AB}$ $\overline{A}$ $\overline{B}$ $\overline{A}+\overline{B}$ 0 0 1 1 1 1 0 1 1 1 0 1 1 0 1 0 1 1 1 1 0 0 0 0	
	b) **Ans.**	**Perform the following BCD subtraction using 9's complement** **i) $(47)_{10} - (31)_{10}$ ii) $(52)_{10} - (67)_{10}$** **i) $(47)_{10} - (31)_{10}$:** Step 1: Take 9's compliment of 31 99 – 31 68 ⟶ 0110 1000 Step 2: 0 1 0 0 0 1 1 1 + 0 1 1 0 1 0 0 0 1 0 1 0 1 1 1 1 (Invalid BDC No.> 9) Step 3: 1 0 1 0 1 1 1 1 Add 6 0 1 1 0 0 1 1 0 1 0 0 0 1 0 1 0 1 Carry …….. 1 0 0 0 1 0 1 1 0 1 6 **$(47)_{10} - (31)_{10} : (16)_{10}$** **ii) $(52)_{10} - (67)_{10}$** Step 1: Take 9's compliment of 67	**4M** ***2M*** ***2M***

		99 – 67 32 ⟶ 0011 0010 Step 2: 0 1 0 1 0 0 1 0 + 0 0 1 1 0 0 1 0 1 0 0 0 0 1 0 0 ↓ ↓ 8 4 (Valid BCD No carry Answer is –ve & in 9's compliment from) Take 9's compliment 99 – 84 15 **$(52)_{10} – (67)_{10} = - (15)_{10}$**	
	c) Ans.	**Implement OR and AND gets using NOR gate only.** **OR gate using NOR gate:** Expression for OR gate is $Y = A + B = \overline{\overline{A + B}}$  **AND gate using NOR gate:** Expression for AND gate is $Y = AB = \overline{\overline{AB}}$ $\left(\text{as } \overline{\overline{A}} = A\right)$ Applying De Morgan's second theorem, $Y = \overline{\overline{A} + \overline{B}}$, we can implement using NOR gates at this stage.	**4M** ***OR gate using NOR gate 2M*** ***AND gate using NOR gate 2M***

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		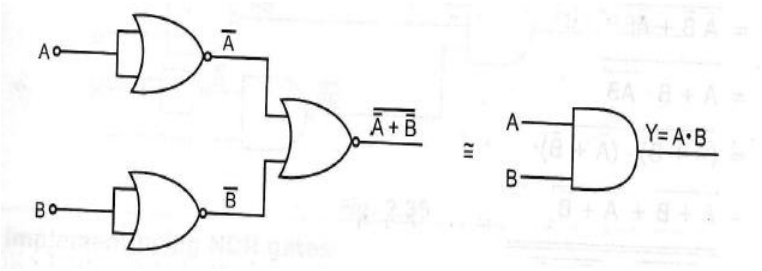	
2.	**a)**	**Attempt any four of the following:** **Simplify the following Boolean expression** **i) Y = AB + ABC + $\overline{A}$B + A$\overline{B}$C** **ii) Y = (A + B) (A + $\overline{B}$) ($\overline{A}$ + B)**	**16** **4M**
	Ans.	**i) Y = AB + ABC + $\overline{A}$B + A$\overline{B}$C** = AB + ABC + A$\overline{B}$C + $\overline{A}$B = AB + AC (B + $\overline{B}$) + $\overline{A}$B = AB + AC + $\overline{A}$B [B+$\overline{B}$ = 1] = B[A+ $\overline{A}$] + AC [A+ $\overline{A}$ = 1] = B + AC	***2M***
		ii) Y = (A + B) (A + $\overline{B}$) ($\overline{A}$ + B) = (A .A + A$\overline{B}$ + AB +B$\overline{B}$) . ($\overline{A}$ + B) = (A + A$\overline{B}$ + AB + 0) . ($\overline{A}$ + B) = [A(1+B) + A$\overline{B}$]. ($\overline{A}$ + B) 1 + B = 1 = [A + A$\overline{B}$]. [$\overline{A}$ + B] = A (1 + $\overline{B}$). ($\overline{A}$ + B) 1 + $\overline{B}$ = 1 = A. ($\overline{A}$ + B)	***2M***

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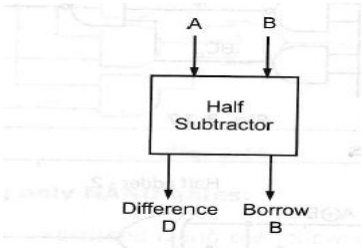
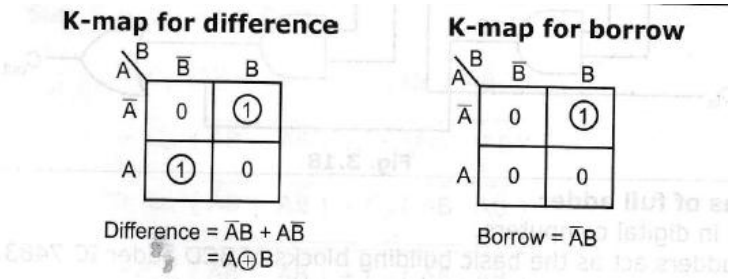
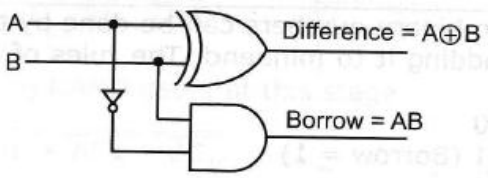
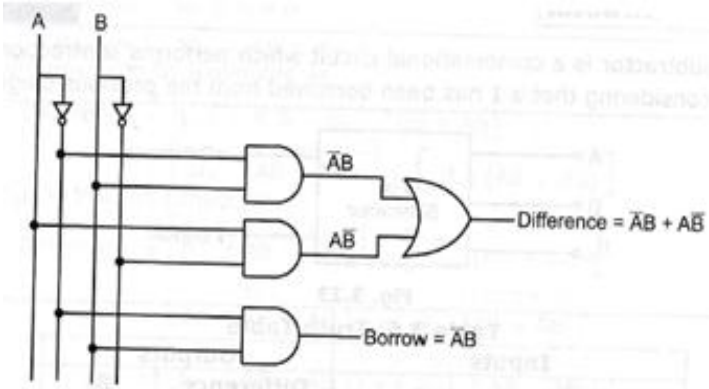
		= A . $\overline{A}$ + AB A $\overline{A}$ = 0 **Y = AB**	
	b) **Ans.**	**Subtract the given number using 2's complement** **i) $(11011)_2 - (11100)$ ii) $(1010)_2 - (101)_2$** **i) $(11011)_2 - (11100)$:** Step 1: 2's compliment of 2nd no, 1 1 1 0 0 ↓ ↓ ↓ ↓ ↓ 0 0 0 1 1 (1's compliment of 2nd no.) + 1 0 0 1 0 0 (2's compliment) Step 2: Add first no of the 2's compliment of 2nd no 1 1 0 1 1 + 0 0 1 0 0 1 1 1 1 1 ⟶ No carry Take 2's compliment of Answer 1 1 1 1 1 ↓ ↓ ↓ ↓ ↓ 0 0 0 0 0 + 1 0 0 0 0 1 with –ve sign **$(11011)_2 - (11100)$: -$(00001)_2$** **ii) $(1010)_2 - (101)_2$:** Make 2nd no as 04 digits by adding '0' to left side ⟶ 0 1 0 1 Step 1: 2's compliment of 2nd no	**4M** ***2M***

		0 1 0 1 ↓ ↓ ↓ ↓ 1 0 1 0 + 1 1 0 1 1 Step 2: Add 1st number to the 2's compliment of 2nd no. 1 0 1 0 + 1 0 1 1 1 0 1 0 1 carry Step 3: Carry is there discard the carry Step 4 : Answer is in true form **$(1010)_2 – (101)_2$: +$(0101)_2$**	***2M***
	c) Ans.	**Design Half subtracter using K-map.** **Half subtractor:** Half subtractor is a combinatonal circuit with two inputs and two outputs (difference and borrow) **Truth Table** Inputs: A, B; Outputs: Difference A – B, Borrow B 0 0 | 0 0 0 1 | 1 1 1 0 | 1 0 1 1 | 0 0 	**4M** ***Truth table 1M*** ***1M for difference***

		 **Logic implementation of half subtractor:**  **Logic implementation using basic gates:** 	***1M for Borrow*** ***Any one circuit 1M***
	d) **Ans.**	**Simplify the following equation using K-map and realize it using logic gates Y = *Σ*m(1, 5, 7, 9, 11, 13, 15).**	**4M**

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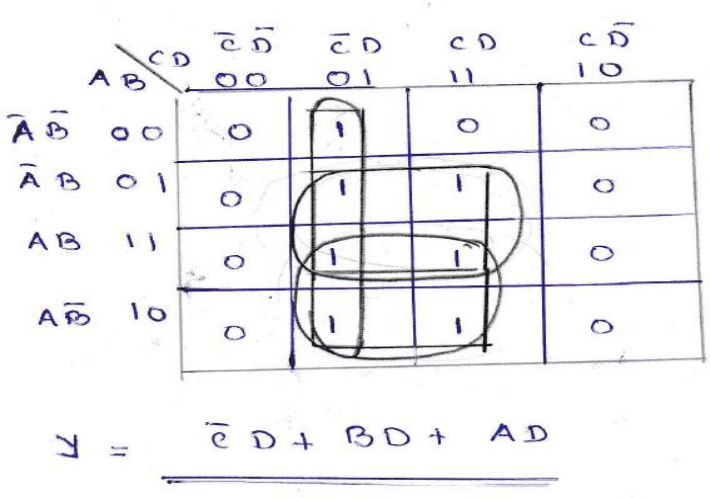
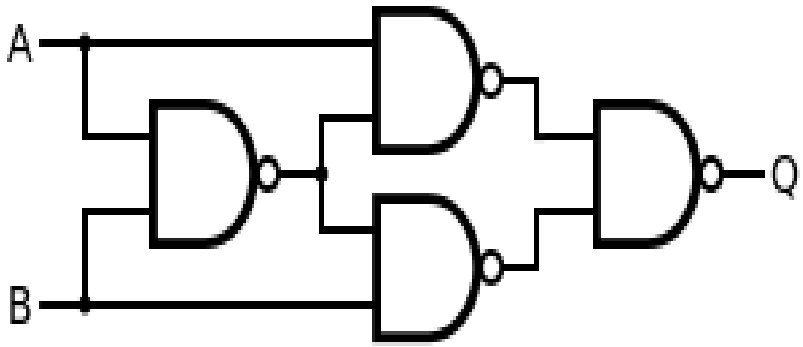
			***K-map 2M*** ***Simplification 2M***
	e) Ans.	**Draw X-OR gate using NAND gate only.** 	**4M** ***Diagram 4M***
	f) Ans.	**Design 1:4 demultiplexer using 1:2 demultiplexer.** **1:4 demultiplexer using 1:2 demultiplexer:**	**4M**

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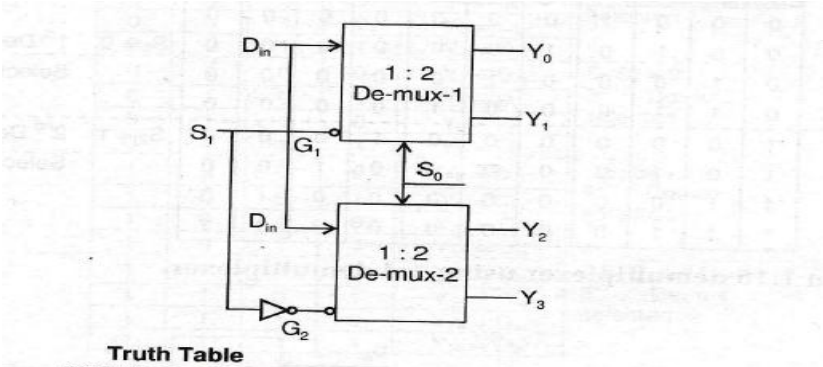
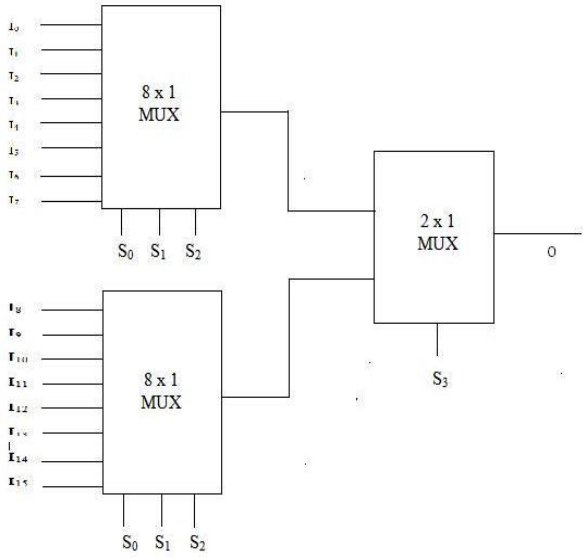
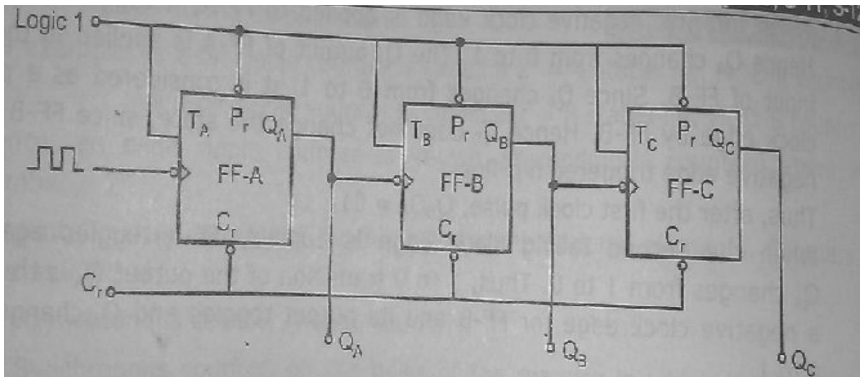
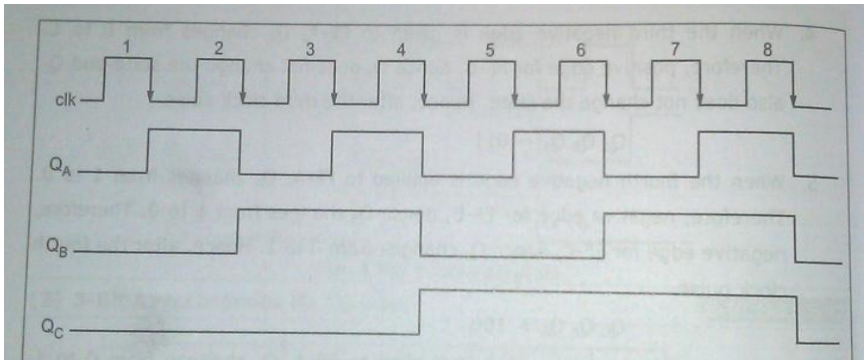
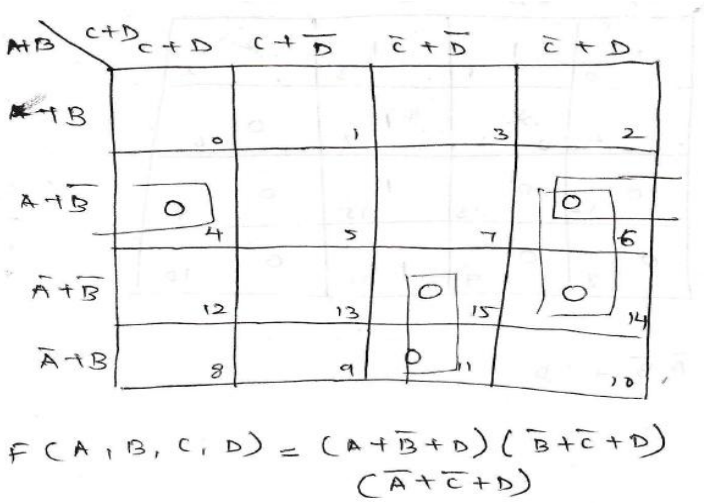
		 **Truth Table** Inputs: S_1 S_0 — Outputs: Y_0 Y_1 Y_2 Y_3 0 0 1 0 0 0 — $S_1 = 0$ 1st demultiplexer 0 1 0 1 0 0 1 0 0 0 1 0 — $S_1 = 1$ 2nd demultiplexer 1 1 0 0 0 1 Select lines S_0 of demultiplexer-1 and demultiplexer-2 are connected together but select line S_1 is connected directly to enable input of demultiplexer-1 and it is connected to demultiplexer-2 through inverter.	***Circuit diagram 2M*** ***Truth table 1M*** ***Explanation 1M***
3.		**Attempt any four of the following:**	**16**
	a)	**Simplify the following expression using Boolean Laws and De-morgan's theorems.**	**4M**
	Ans.	**If student has attempted to solve the question award appropriate marks.**	***4M***
	b)	**Design 16 : 1 multiplexer using 8 : 1 multiplexer** ***(Note: Any other correct diagram may also be considered)***	**4M**
	Ans.		

			***Correct diagram 4M***
	c) Ans.	**Describe different types of triggering methods for a flip-flop.** 1. **Level triggering**: The latch or flip-flop circuits which respond to their inputs, only if their enable input (E) or clock input held at an active HIGH or LOW level are called as level triggered latches or flip flops. **Positive level triggered:** If the outputs of S-R flip flop response to the input changes, for its clock input at high (1), level then it is called as the positive level triggered S-R flip flop. **Negative level triggered FF:** If the outputs of an S-R flip-flop respond to the input changes, for its clock input at low (0) level, then it is called as the negative level triggered S-R flip-flop. **2. Edge Triggering:** The flip-flop which changes their outputs only corresponding to the positive or negative edge of the clock input are called as edge triggered flip-flops. **Types of edge triggered flip-flops:** There are two types of edge triggered flip flops: **Positive edge triggered flip flops**: Positive edge triggered flip flops, will allow its outputs to change only at the instants corresponding to the rising edges of clock (or positive spikes). Its outputs will not	**4M** ***2M each for each type of triggering***

		respond to change in inputs at any other instant of time. **Negative edge triggered flip flops**: Negative edge triggered flip-flops will respond only to the going edges (or spikes) of the clock.	
	d) **Ans.**	**Draw and explain 3-bit asynchronous up counter with timing diagram.** Following figure shows 3-bit asynchronous counter. It uses 3 flip-flops, i.e. it has 23 = 8 states The clock pulse is applied to flip-flop A and QA output of flip-flop A acts as a clock input for Flip-flop B and QB output of flip-flop B acts as a clock input for Flip-flop C.   Using 3-bit ripple counter we can count 0-7. Because we know by 3 bit we can represents minimum 0 (000) and maximum 7 (111). The clock inputs of the three flip flops are connected in cascade. The T input of each flip flop is connected to a constant 1, which means that the state of the flip flop will toggle at each negative edge of its clock. Thus the clock input of the first flip flop is connected to the *Clock* line. The other two flip flops have their clock inputs driven	**4M** ***Diagram of Counter 1M*** ***Timing Diagram 1M*** ***Explanation 2M***

		by the Q output of the preceding flip flop. Therefore, they toggle their state whenever the preceding flip flop changes its state from Q = 1 to Q = 0, which results in a negative edge of the Q signal. So as we take the output from Q_C,Q_B,Q_A	
	e) **Ans.**	**Minimize the following equation using K-map** **i) F(A,B,C,D) = π M (4,6,11,14, 15)** **ii) F(A,B,C,D) = $\sum$m (1.3,7,11, 15)+d(0,2,5)** **i) F(A,B,C,D) = π M (4,6,11,14, 15)**  $F(A,B,C,D) = (A+\bar{B}+D)(\bar{B}+\bar{C}+D)(\bar{A}+\bar{C}+D)$ **ii) F(A,B,C,D) = $\sum$m (1.3,7,11, 15)+d(0,2,5)**	**4M** ***2M***

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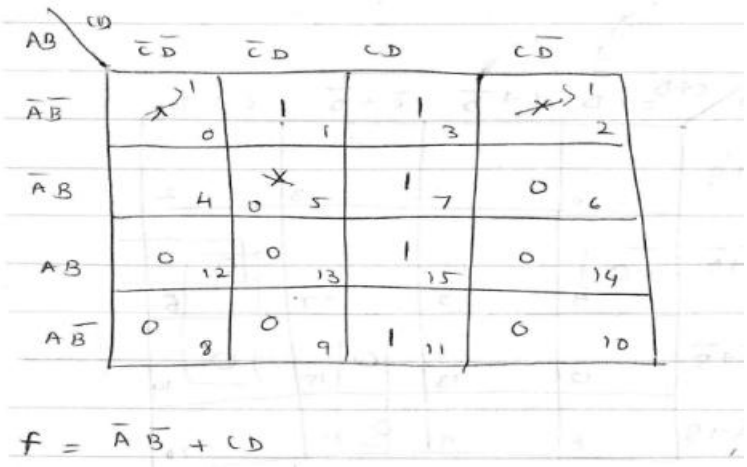
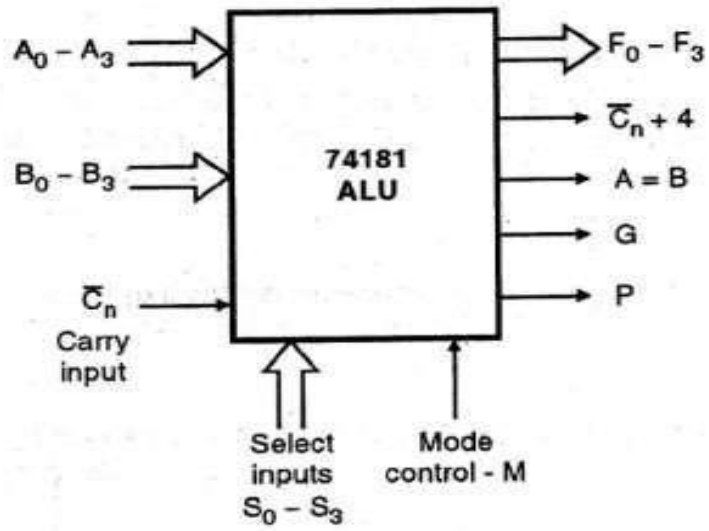
			***2M***
	f) **Ans.**	**Draw block diagram of ALU and describe any four function performed by ALU.**  **Functions performed by ALU:**	**4M** ***Block Diagram 2M***

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C_n}$ = H (no carry)	$\overline{C_n}$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

Any four function s 2M

4. **a)** **Ans.**

Attempt any four of the following: **16**

Describe working of JK Flip-Flop and write its truth table. **4M**

(Note: Diagram of J K flip flop optional)

Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

Truth Table 2M

MODEL ANSWER

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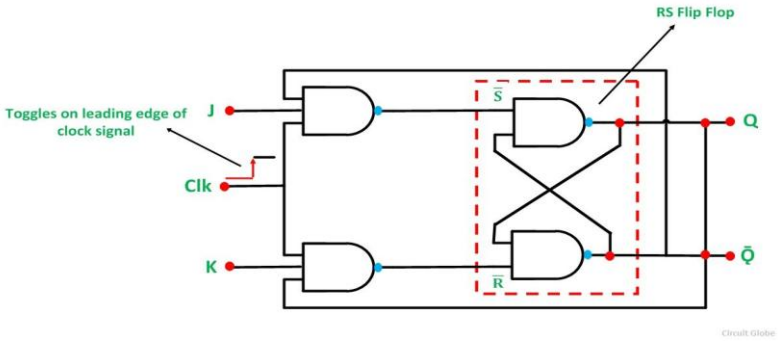
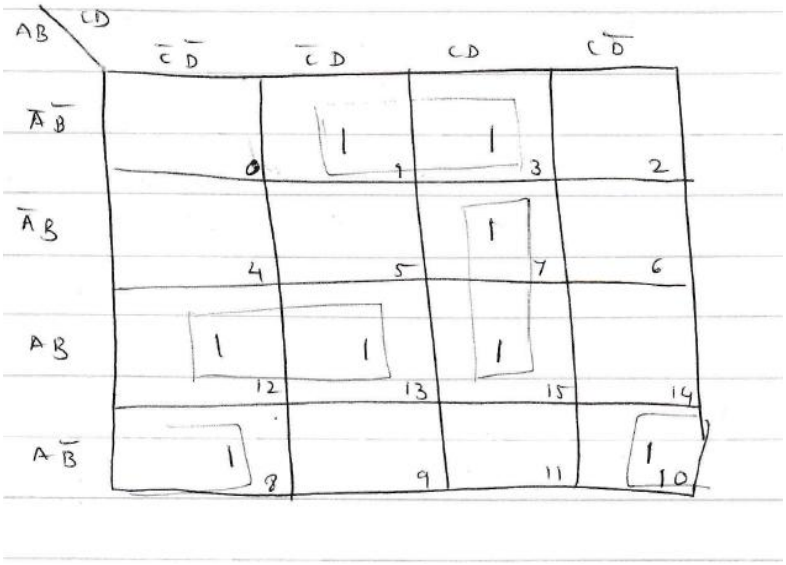
Subject: Digital Techniques **Subject Code:** **17333**

		 **Working:** 1. When J & K are both low, then no change occurs. 2. If J and K are both high at the clock edge then the output will toggle from one state to the other. 3. If J = 1, K = 0, at the clock edge, the flip flop will reset 4. If J = 0, K = 1, the flip flop will set.	***Explanation 2M***
	b) **Ans.**	**Simplify the following equation using K-map and realize it using basic gates only** **F (A, B, C, D) = ∑ m (1, 3, 7, 8, 10, I2, 13, L5)** 	**4M** ***K-map 1M*** ***Simplification 1M***

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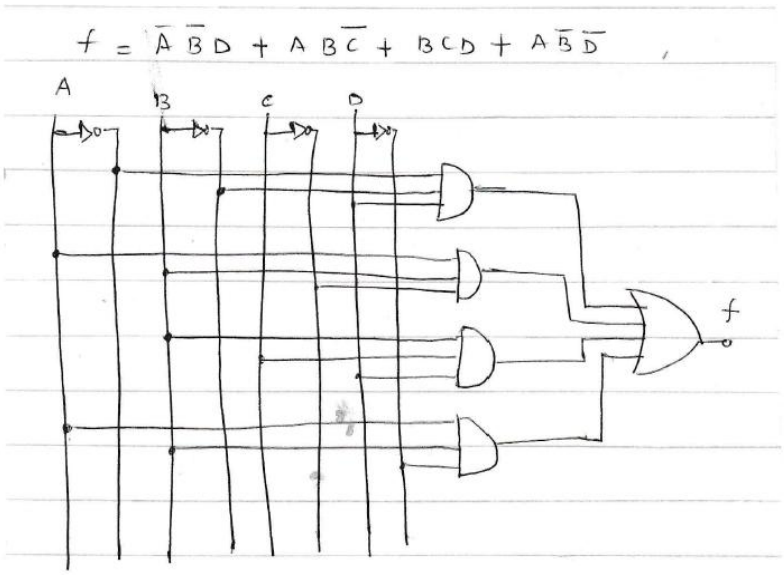
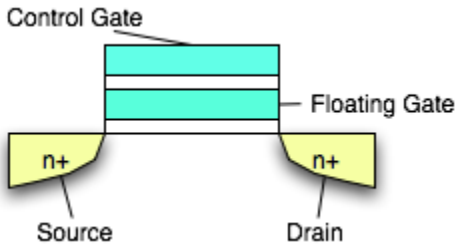
			***Circuit diagram 2M***
	c) **Ans.**	**Explain the working of EPROM.** ***(Note: Any other answer shall be considered)*** An EPROM, or erasable programmable read-only memory, is a type of memory chip that retains its data when its power supply is switched off. Computer memory that can retrieve stored data after a power supply has been turned off and back on is called non-volatile. It is an array of floating-gate transistors individually programmed by an electronic device that supplies higher voltages than those normally used in digital circuits. Once programmed, an EPROM can be erased by exposing it to strong ultraviolet light source .  Each storage location of an EPROM consists of a single field-effect transistor. Each field-effect transistor consists of a channel in the	**4M** ***Explanation 4M***

		semiconductor body of the device. Source and drain contacts are made to regions at the end of the channel. An insulating layer of oxide is grown over the channel, then a conductive (silicon or aluminum) gate electrode is deposited, and a further thick layer of oxide is deposited over the gate electrode. The floating-gate electrode has no connections to other parts of the integrated circuit and is completely insulated by the surrounding layers of oxide. A control gate electrode is deposited and further oxide covers it.[2] To retrieve data from the EPROM, the address represented by the values at the address pins of the EPROM is decoded and used to connect one word (usually an 8-bit) of storage to the output buffer amplifiers. Each bit of the word is a 1 or 0, depending on the storage transistor being switched on or off, conducting or non-conducting. The switching state of the field-effect transistor is controlled by the voltage on the control gate of the transistor. Presence of a voltage on this gate creates a conductive channel in the transistor, switching it on. In effect, the stored charge on the floating gate allows the threshold voltage of the transistor to be programmed. The programming process is not electrically reversible. To erase the data stored in the array of transistors, ultraviolet light is directed onto the die. Photons of the UV light cause ionization within the silicon oxide, which allow the stored charge on the floating gate to dissipate. Since the whole memory array is exposed, all the memory is erased at the same time. The process takes several minutes for UV lamps.	
	d) **Ans.**	**Draw the circuit diagram of 3-bit R-2R ladder type DAC obtain its only output voltage expression.** **Consider Input/Output CBA = 100**	**4M**

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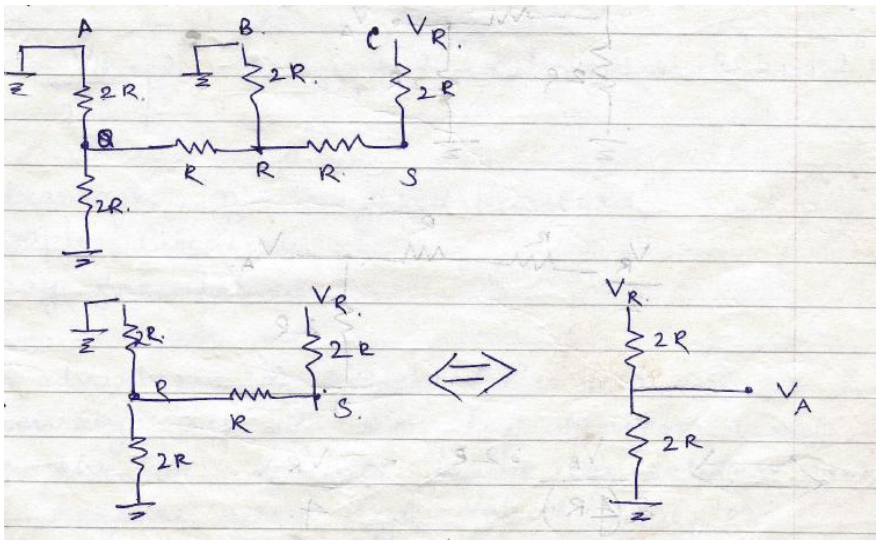


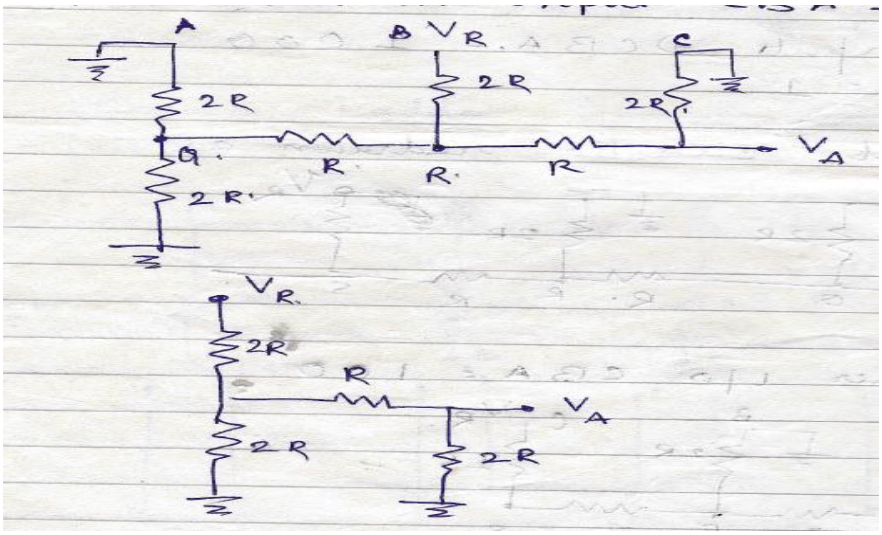
Diagram 2M

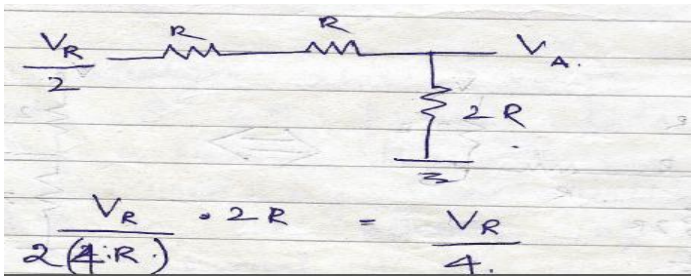
$$\therefore V_A = \frac{V_R}{4R} . 2R = \frac{V_R}{2}$$

Thus the output voltage contributed by the MSB is $V_R/2$

Derivation output voltage expression 2M

Consider the input CBA = 010





Thus the output voltage contributed by Next significant bit is $V_R/4$

Similarly, We can prove that output voltage contributed by bit A is $\frac{V_R}{8}$

Applying Super position theorem, we get

$$V_A = \frac{V_R}{2} + \frac{V_R}{4} + \frac{V_R}{8} \text{ for input CBA = 111.}$$

$$V_A = \frac{V_R}{2}[b_2] + \frac{V_R}{4} b_1 + \frac{V_R}{8} . b_0$$

$$= \frac{V_R}{8} [2^2 b_2 + 2^1 b_1 + 2^0 b_0]$$

e) **Define following terms with reference to A/D converters and list any four application of A/D converters.** — **4M**

i) Resolution

ii) Quantization error

Ans. **i) Resolution:**

It is define as the maximum number of digital output codes. Resolution= 2^n

Resolution is defined as the ratio of change in the value of the input analog voltage VA, required to change the digital output by 1 LSB. — ***Each Definition 1M***

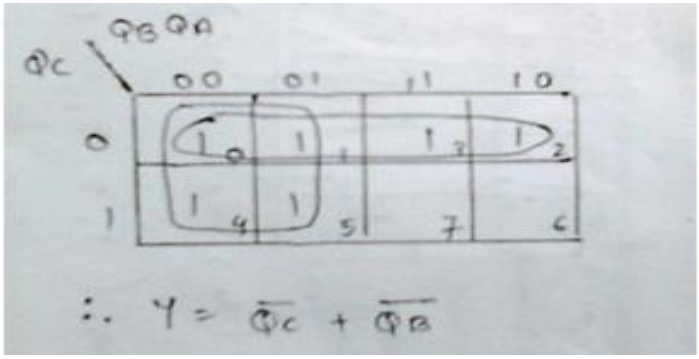
Resolution=$V_{FS}/(2^n-1)$

		ii) Quantization Error: An ADC, the whole range of analog voltage in an interval is represented by only one digital value. ∴, There is an error called Quantization error. Quantization error can be reduced by increasing the number of bits. **Applications of A/D converter:** 1. Computers use analog-to-digital converters in order to convert signals from analog to digital before they can be interpreted. For example, a modem will convert signals from digital to analog before transmitting them over telephone lines that carry only analog signals. These signals are then converted back into digital form at the receiving end so that the computer can interpret the data in digital format. 2. In a digital signal processing system, an ADC is required if the input signal is analog. For example, a fast video ADC is used in TV tuner cards. 8, 10, 12, or 16 bit analog to digital controllers are common in microcontrollers. 3. They are also needed in digital storage oscilloscopes. 4. Analog to digital converters are used in music reproduction technology when done using computers. In such an application, an ADC is needed when an analog recording is used in order to create the PCM data stream that goes onto a CD or a digital music file. 5. ADC is used in Cell phones 6. ADC is used in digital voltmeters 7. ADC is used in digital oscilloscope	***Any four Applications 2M***
	f) **Ans.**	**Design a mod-6 asynchronous counter with truth table and logic diagram.** ***(Note: K-map is optional)*** • MOD 6 asynchronous counter will require 3 flip flops and will count from 000 to 101. Rest of the states are invalid. To design the combinational circuit of valid states, following truth table and K-map is drawn:	**4M**

Q_C	Q_B	Q_A	Reset Logic
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Truth Table 2M

- From the above truth table, we draw the K-maps and get the expression for the MOD 6 asynchronous counter.



Logic Diagram 2M

Fig: K-map for above truth table

- Thus reset logic is OR of complemented forms of QC and QB. This will be given to the reset inputs of the counter so that as soon as count 110 reaches, the counter will reset. Thus the counter will count from 000 to 101. The implementation of the designed MOD 6 asynchronous counter is shown below:

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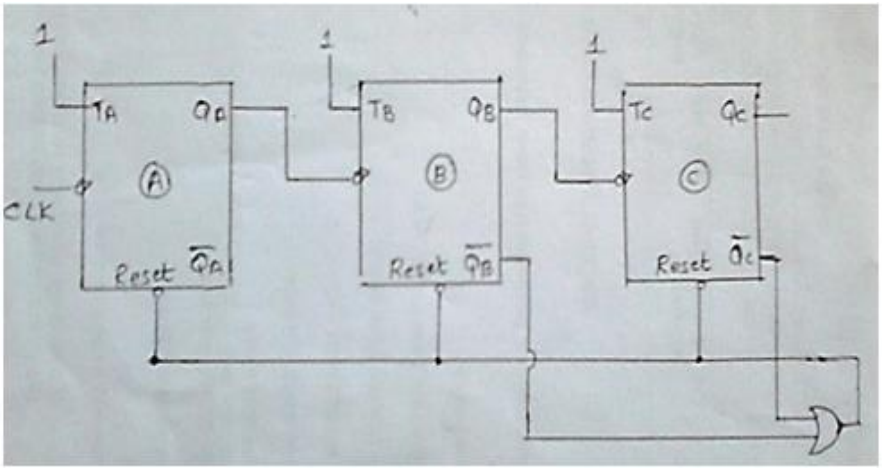
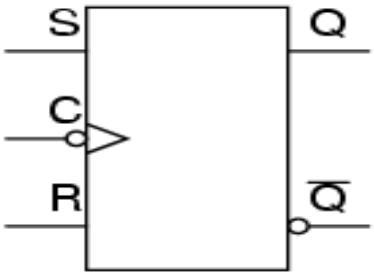
		 **Fig: Circuit diagram of MOD 6 asynchronous counter**	
5.	**a)**	**Attempt any four of the following:** **How many flip-flops are required to construct the following modulus counters?** **i) 27** **ii) 83** **iii) 95** **iv) 9**	**16** **4M**
	Ans.	The Number of flip flops are calculated from the formula**:** $2^n \geq m$ Where n= no of flip flops and m is the number of states**.** i) 27 = 5 ii) 83 = 7 iii) 95 = 7 iv) 9 = 4	***1M each***
	b)	**Draw logic diagram of S-R Flip-Flop with negative edge triggering and write its truth table.**	**4M**
	Ans.		***Diagram 2M***

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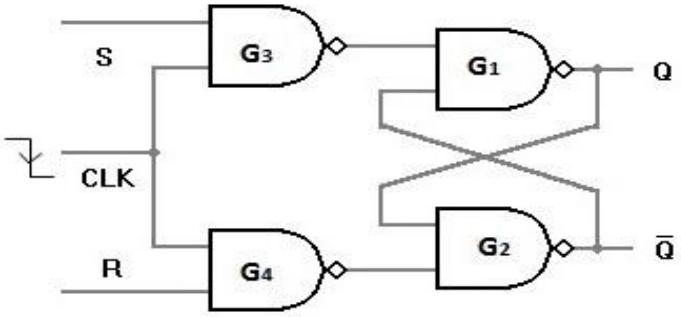
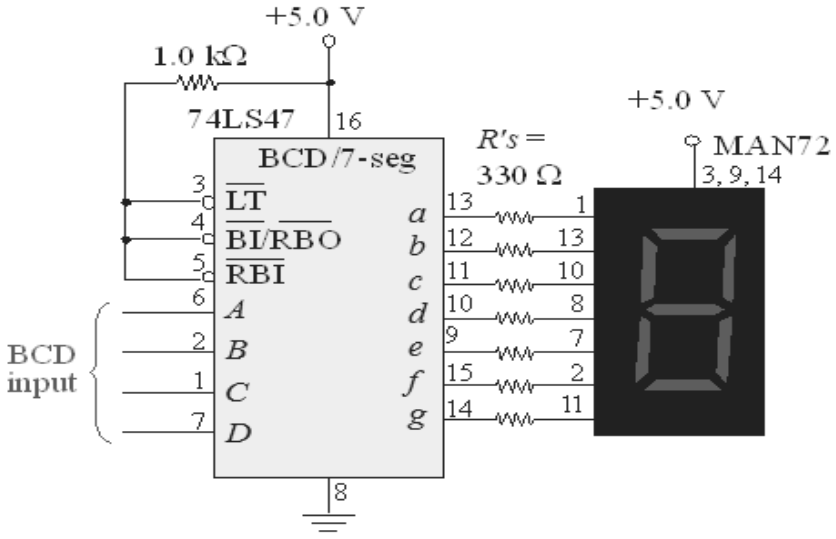


S	R	Q	State
0	0	Previous State	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden

Truth table 2M

c) **Ans.**

Draw BCD to seven segment decoder using IC 7447 and give function of each pin.



4M

Circuit diagram 2M

		The 74LS47 display decoder receives the BCD code and generates the necessary signals to activate the appropriate LED segments responsible for displaying the number of pulses applied. As the 74LS47 decoder is designed for driving a common-anode display, a LOW (logic-0) output will illuminate an LED segment while a HIGH (logic-1) output will turn it "OFF". For normal operation, the LT (Lamp test), BI/RBO (Blanking Input/Ripple Blanking Output) and RBI (Ripple Blanking Input) must all be open or connected to logic-1 (HIGH). **The functions of the pins are:** • **LT (Lamp test):** This is used to check the segments of LED. If it is connected to logic 0 all the segments of the display connected to the decoder will be ON. For normal decoding this terminal is to be connected to logic 1 level. • **RBI (Ripple Blanking Input):** It is to be connected to logic 1 for normal decoding operations. If it is connected to logic 0 the segment outputs will generate data for normal 7 segment decoding of all BCD inputs except zero. Whenever the BCD input correspond to zero, the 7 segment display switches off. This is used for blanking out leading zeros in multi digit displays. • **BI (Blanking input):** If it is connected to 0 level, the display is switched off irrespective of BCD inputs. That is used for conserving power in multiplexed displays. • **RBO (Ripple Blanking output):** This output which is normally at logic 1 goes to logic 0 during the zero blanking interval. This is used for cascading purpose and is connected to RBI of succeeding stages.	***Function of pins 2M***
	d) Ans.	**Implement using NOR gates only** $\mathbf{Y = (A + B).(\overline{A} + C)}$	**4M**

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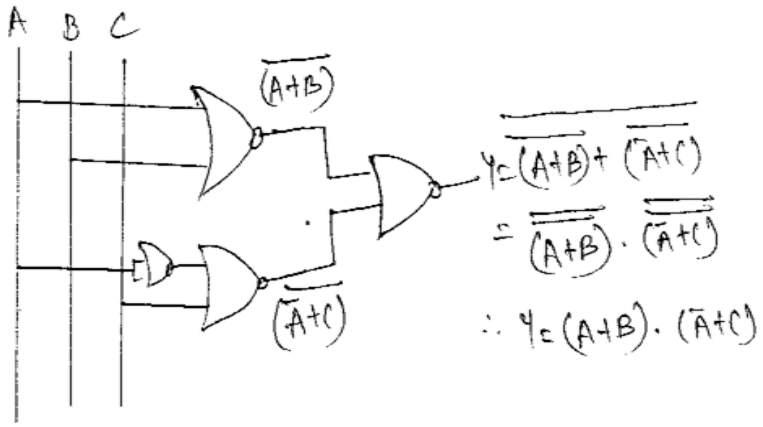
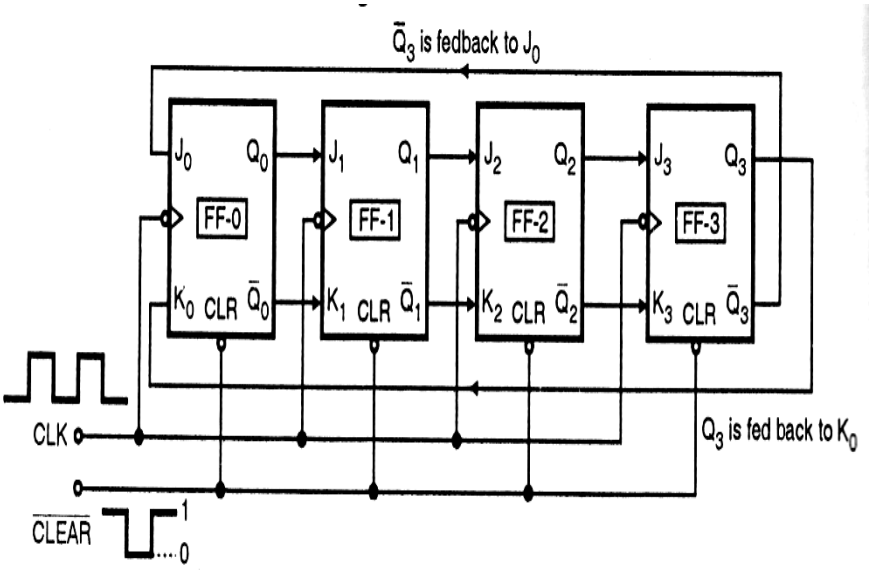
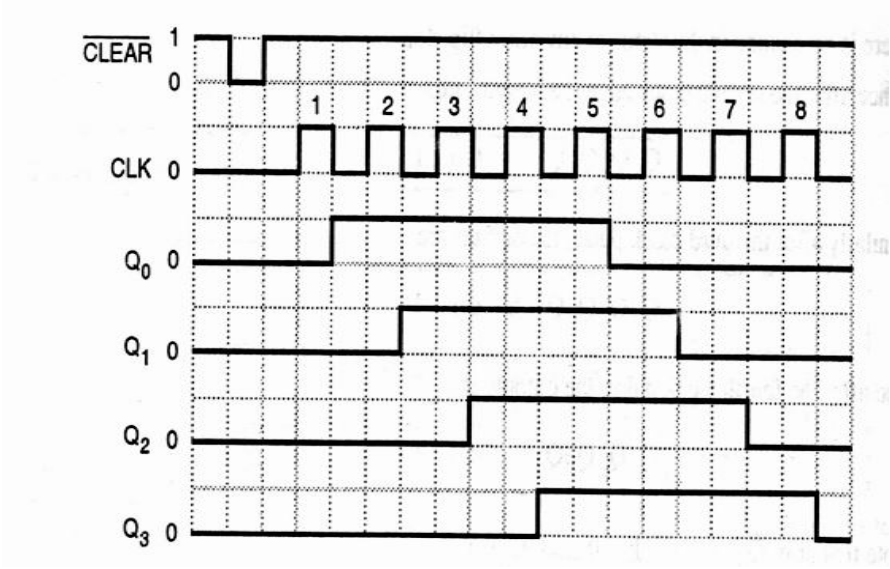
		$Y = (A+B).(\bar{A}+C)$ – Product of sum form:-  	***Circuit diagram 3M*** ***Output expression simplification 1M***
	e) **Ans.**	**Convert the following:** **i) $(429)_{10} = (?)_{BCD}$** **ii) $(2.45)_{10} = (?)_2$** **iii) $(AF)_{16} = (?)_8$** **iv) $(1011010)_2 = (?)_{16}$** i) $(429)_{10} = (0100\ 0010\ 1001)_{BCD}$ ii) $(2.45)_{10} = (10.01110)_2$ 2 | 2 | 0 ↑ 2 | 1 | 1 0 | 0.45 x 2 = 0.90 → 0 0.90 x 2 = 1.80 → 1 0.80 x 2 = 1.60 → 1 0.60 x 2 = 1.20 → 1 0.20 x 2 = 0.40 → 0	**4M** ***Each conversion 1M each***

		iii) $(AF)_{16} = (1010\ 1111)_2$ $(AF)_{16} = 0\,10\ 101\ 111 = (257)_8$ Implied Zero iv) $(1011010)_2 = (5A)_{16}$ $0101\ 1010 = 5A$ Implied Zero	
	f) **Ans.**	**Draw the circuit of Johnson counter and describe with timing diagram.** In a ring counter if the feedback connections are reversed i.e. J0=Q3' and K0=Q3 then the circuit becomes twisted ring counter.  	**4M** ***Circuit 2M***

		 The Johnson counter designed with D flip flop is shown below. It has four stages i.e. four flip flops connected in series type or cascaded. Initially zero / Null is fed to the Johnson counter and on applying the clock signal, outputs will change to "1000", "1100", "1110", "1111", "0111", "0011", "0001", "0000" in a sequence and the sequence will repeat for next clock signal. The Johnson counter produces a special pattern by passing four 0's and then four 1's and thus it produces a special pattern by counting up down.	***Timing diagram 1M*** ***Explanation 1M***
6.	**a)** **Ans.**	**Attempt any four of the following:** **Explain successive approximation method of ADC with neat diagram**.	**16** **4M**

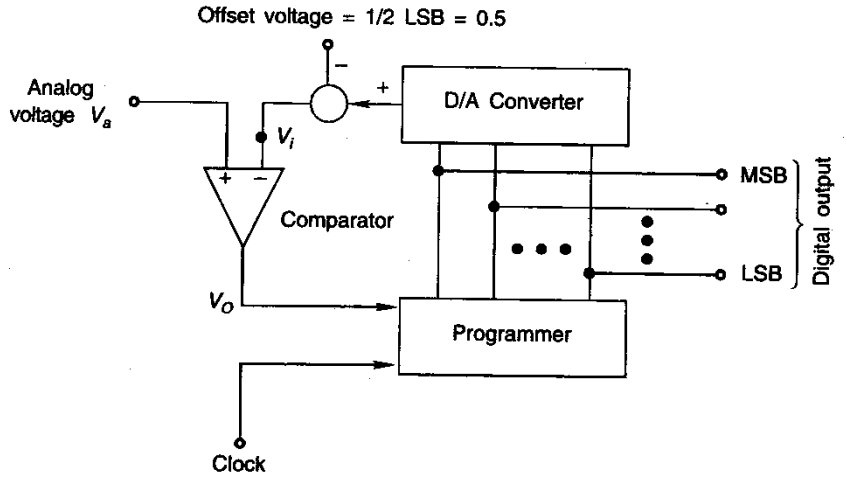


Diagram 2M

The successive approximation A/D converter is as shown in fig.

An analog voltage (Va) is constantly compared with voltage Vi, using a comparator. The output produced by comparator (Vo) is applied to an electronic Programmer.

- If Va=Vi, then Vo=0 & then no conversion is required. The programmer displays the value of Vi in the form of digital O/P.
- But if Va ≠ Vi, then the O/P is changed by the programmer.
  - If Va> Vi, then value of Vi is increased by 50% of earlier value.
  - But if Va< Vi, then value of Vi is decreased by 50% of earlier value.

This new value is converted into analog form, by D/A converter so as to compare it with Va again. This procedure is repeated till we get Va=Vi. As the value of Vi is changed successively, this method is called as successive-approximation A/D converter.

Explanation 2M

Advantages:

1. The conversion time is equal to n clock cycle period for an n-bit ADC. Thus the conversion time is very short. For a 10-bit ADC with a clock frequency of 1MHz, the conversion time will be $10x10^{-6}$ i.e., 10 μsec.
2. Conversion time is constant and independent of the amplitude of analog signal Va.

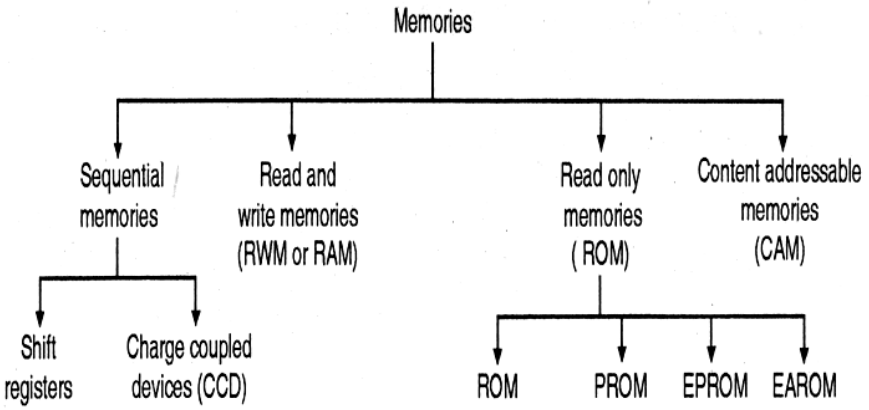
Dis-Advantages:
1. The circuit is complex.
2. The conversion time is more than flash type ADC.

b) Ans. **List four applications flip -flops.** — **4M**

Applications flip–flops:
a) It can be used as memory element.
b) It can be used to eliminate key debounce.
c) It is used as a building block in sequential circuits such as counters and registers.
d) It can be used as delay element.

Any 4 applications 1M each

c) Ans. **Give classification of memory and compare RAM and ROM (any 2 point).** — **4M**

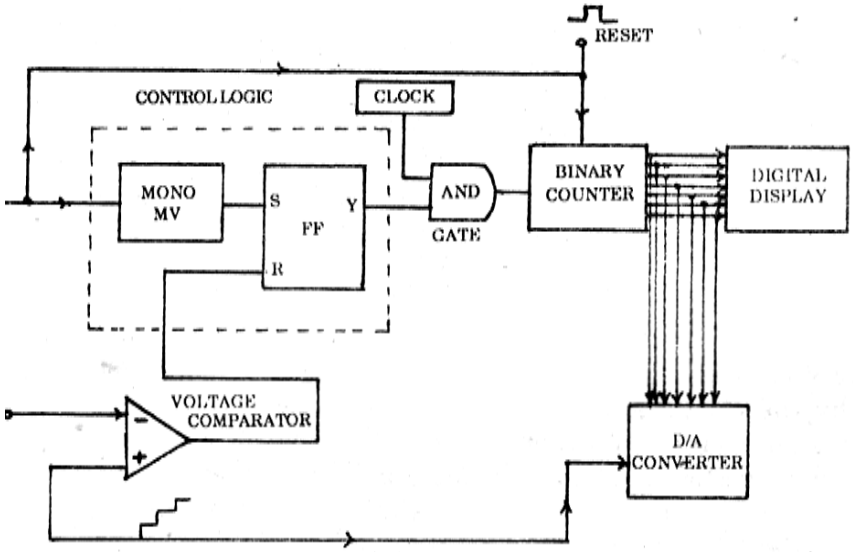


Classification 2M

Sr No	Parameters	RAM	ROM
1	Definition	From this memory data can be read, write, erase or modified.	From this memory data can only be read
2	Effect of power	Stored information is retained only as long as power is on. Information stored is lost if power is turned off	No effect of power on stored information. Information does not get lost

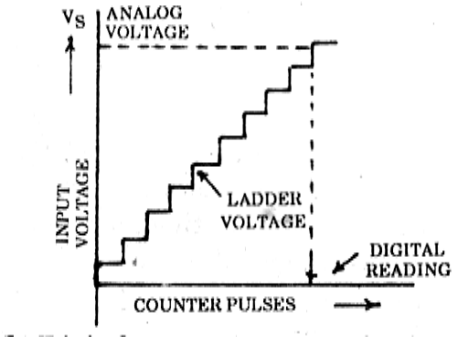
Any 2 points 1M each

		3	Applications	For temporary storage	For permanent storage of information	
	d) **Ans.**	**Compare combination circuit and sequential logic circuit. (any 4 pts).** **Sr No** / **Combinational circuits** / **Sequential circuits** 1 / In combinational circuits, the output variables depends on the combinational of input variables. / In sequential circuits , the output variables depends upon the present inputs as well as on the past output. 2 / Memory unit is not required in these circuits. / Memory unit is required in these circuits to store the previous output. 3 / These circuits are faster in speed because the delay between the input and output is due to the propogation delay. / Sequential circuits are slower than the combinational circuits. 4 / These are easy to design. / These are complex in designing. 5 / Ex: Parallel Adder. / Ex: Serial Adder.			**4M** ***Any 4 points 1M each***
	e) **Ans.**	**With suitable diagram explain the working of ramp type ADC.** ***(Note: Any other diagram shall be considered)***				**4M**



(a) Block diagram of a Ramp type ADC

Diagram 2M



This method of A/D conversion uses a binary counter, to count a continuous train of pulses. The pulses are produced from a clock. They pass through a gate, which is normally closed. It opens only when a start signal is applied to initiate a linear ramp. The gate remains open till the linear ramp voltage reaches a value equal to the input voltage to be measured. The counter thus records a number of clock pulses which is proportional to the input voltage. This method is also called counter method.

The fig. shows a schematic diagram of a staircase ramp or counter

Working 2M

		type A/D converter. This method uses a clock source, a counter and a D/A converter. An analog input is applied to one input of an OP AMP which is used as a voltage comparator. A start or convert pulse is applied to the set input of the flip-flop through a mono stable multivibrator (i.e. control logic) and also to the reset input of the binary counter. This pulse resets the binary counter and makes it ready for counting. As the counter resets, output of the D/A converter reduces to zero and thus with positive analog input to the voltage comparator, the output of the comparator goes low, which makes R = 0. The start pulse also triggers the mono stable multivibrator, which introduces the desired delay in the action of the other circuits. Thus the output of the mono stable multivibrator goes high. This makes S = 1, while R was already made 0. The RS flip-flop sets and the Y output goes high. The AND gate is enabled & the counter starts the counting the clock pulses. The output of the counter is fed to n D/A converter which produces an analog output in response to the digital signal as its input. This binary output starts increasing continuously with time. The output of the D/A converter also starts increasing in steps. The analog output is a staircase signal as shown in fig. This D/A output is fed to the reference voltage for the comparator. The staircase signal (i.e. digital output) is compared by the comparator with the analog voltage. So long as the input signal, Vs is greater than the digital output the gate remains enabled and clock pulses are counted by the counter, thus continuously raising the digital output. But as soon as the staircase digital output exceeds the given analog input, the output of the comparator changes from a low to a high level. This makes R = 1, while S is at 0. Thus, the flip-flop resets and Y output goes low. Hence the AND gate is disabled and no clock pulses can now reach the counter. This stops the counting and the binary output of the counter represents the final digital output. The staircase ramp or counter method is simple and least expensive. It is faster as compared to dual slope method. It needs longer time for conversion because of the following of the reasons (a) The counter starts after it is reset to zero, (b) The rate of clock pulses also decides the conversion time, and (c) Conversion time is different for analog voltages of different magnitudes.	

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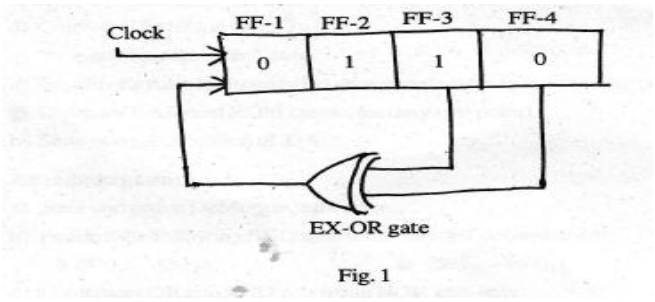
Subject: Digital Techniques **Subject Code:** **17333**

	f)	**In Fig. 1, if the 4-bit serial in parallel out right shift register has the initial contents 0110. After 3 clock pulses are applied what will be the contents of the shift register.**	**4M**
	Ans.	 Fig. 1 **Clock** | **0** | **1** | **1** | **0** 1 | 1 | 0 | 1 | 1 2 | 0 | 1 | 0 | 1 3 | 1 | 0 | 1 | 0	***Proper output at each step 4M***