MODEL ANSWER

SUMMER– 19 EXAMINATION

Subject Title: Principles of Digital Techniques Subject Code:17320

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
Q.1 a)		**Attempt any SIX of the following :**	**12M**
	i)	**Convert the following binary number to gray code.** **1)1101101** **2)101110**	**2M**
	Ans:	1) 1 1 0 1 1 0 1 → Binary number 1 0 1 1 0 1 1 → Graycode 2) 1 0 1 1 1 0 → Binary number 1 1 1 0 0 1 → Graycode	1M 1M
	ii)	**List any two applications of multiplexer.**	**2M**

	Ans:	1. It is used for simplification of Logic design. 2. Used in Data Acquisition system. 3.Used in Digital to Analog converters. 4. Used as Data selector. 5.Used in Designing combinational circuits.	**2M**
	iii)	**State the different triggering methods in digital circuit.**	**2M**
	Ans:	1. Level Triggering- a. Positive level triggering b. Negative level triggering 2. Edge Triggering- a. Positive edge triggering b. Negative edge triggering	**1M** **1M**
	iv)	**List any two applications of shift registers.**	**2M**
	Ans:	1. For temporary data storage. 2. As a delay line. 3. For serial data transmission. 4. Serial to parallel data converter. 5. Parallel to serial data converter. 6. As Ring counter.	**Any 2 points- 2 M**
	v)	**Identify following ICs** **1)IC 0800** **2)IC 0809**	**2M**
	Ans:	1. IC 0800- 8 bit Digital to Analog converter 2. IC 0809- 8 bit Analog to Digital converter	**1M for each IC**
	vi)	**Compare volatile memory and non-volatile memory(any two-points)**	**2M**
	Ans:		**Any 2 points- 2M**

Parameter	Volatile memory	Non-Volatile memory
definition	Information is lost if power is turned off	Information is not lost if power is turned off
classification	All RAMs	ROMs, EPROM, magnetic memories
Effect of power	Stored information is retained only as long as power is on.	No effect of power on stored information
applications	For temporary Storage	For permanent storage of information

	vii)	**State any four Boolean laws.**	**2M**

Ans:

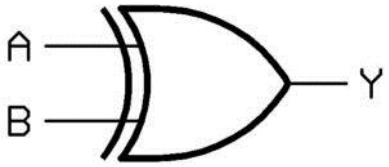
1.	Law of Identity	$\frac{A = A}{\overline{A} = \overline{A}}$
2.	Commutative Law	$A \cdot B = B \cdot A$ $A + B = B + A$
3.	Associative Law	$A \cdot (B \cdot C) = A \cdot B \cdot C$ $A + (B + C) = A + B + C$
4.	Idempotent Law	$A \cdot A = A$ $A + A = A$
5.	Double Negative Law	$\overline{\overline{A}} = A$
6.	Complementary Law	$A \cdot \overline{A} = 0$ $A + \overline{A} = 1$
7.	Law of Intersection	$A \cdot 1 = A$ $A \cdot 0 = 0$
8.	Law of Union	$A + 1 = 1$ $A + 0 = A$
9.	DeMorgan's Theorem	$\overline{AB} = \overline{A} + \overline{B}$ $\overline{A + B} = \overline{A}\,\overline{B}$
10.	Distributive Law	$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$ $A + (BC) = (A + B) \cdot (A + C)$
11.	Law of Absorption	$A \cdot (A + B) = A$ $A + (AB) = A$
12.	Law of Common Identities	$A \cdot (\overline{A} + B) = AB$ $A + (\overline{A}B) = A + B$

Note: Name of the law is optional

Any 4 Laws- each of 1/2M

viii) **Draw the logic symbol and truth table for two input EX-OR gate.** **2M**

Logic Symbol:



1M- symbol

Truth table:

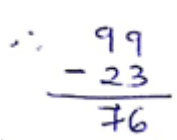
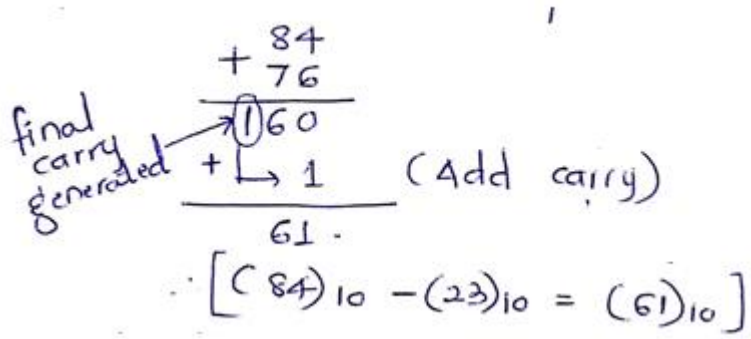
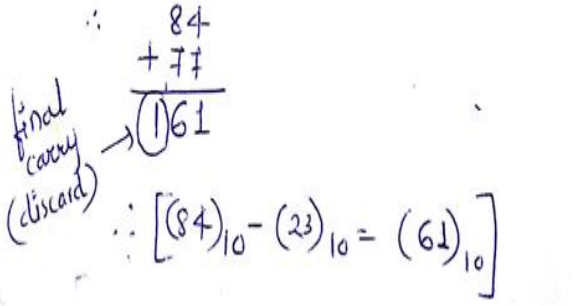
2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

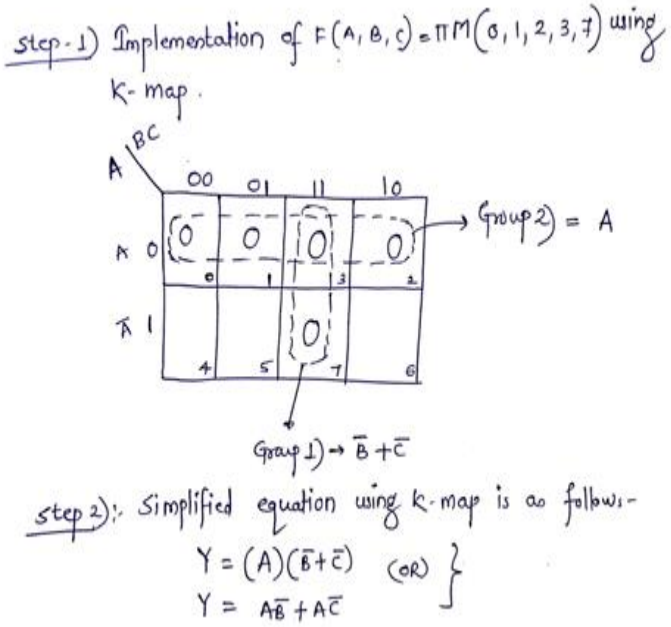
1M- truth table

b) **Attempt any TWO of the following :** **8M**

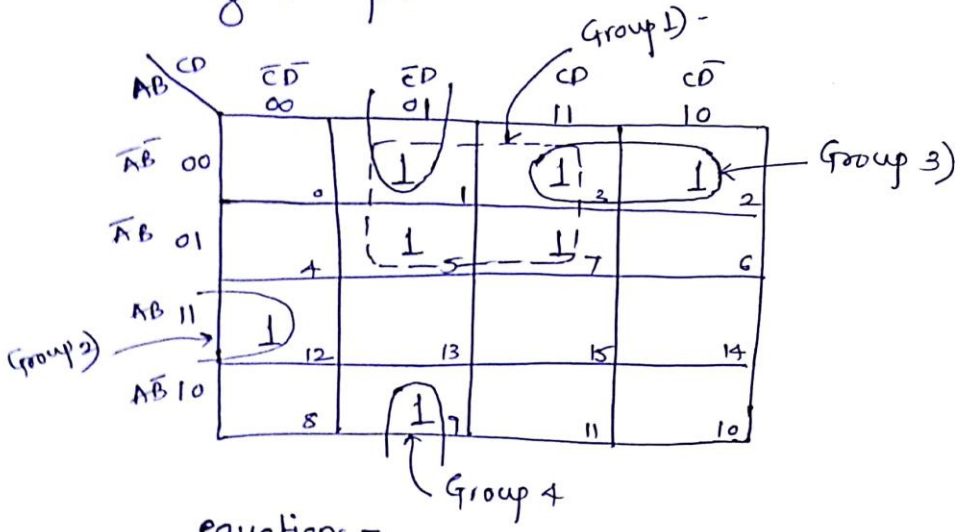
i) **Solve the following subtraction using 9's and 10's complement method.** **4M**

$(84)_{10}$-$(23)_{10}$

	Ans:	**Step 1: Take 9's complement of (23)10 i.e.**  Step 2: Add (84)10 and 9's complement of (23)10 i.e. 76  **Subtraction using 10's compliment:** **Step 1: Take 10's compliments of (23)10 = 9's compliment +1** **9's compliment of (23)10 =76** **Therefore** **10's compliment of (23)10 = 76+1=77** **Step 2:** Add (84)10 and 10's compliment of (23)10 i.e. 77 	Step 1-1M Each Step 2-1M Each
	ii)	**Minimize the following using K-map.** **1)F(A,B,C)=πM(0, 1,2,3,7)** **2)F(A,B,C,D)=∑m(1,2,3,5,7,9,12)**	**4M**

	Ans:	**1)F(A,B,C)=πM(0, 1,2,3,7)**  **2)F(A,B,C,D)=∑m(1,2,3,5,7,9,12)**	**2 M** **2M**

Step-1) Implementation of $F(A, B, C, D) = \Sigma m(1, 2, 3, 5, 7, 9, 12)$ using K-map.



equations –

Group 1) – $\bar{A}D$

Group 2) – $AB\bar{C}\bar{D}$

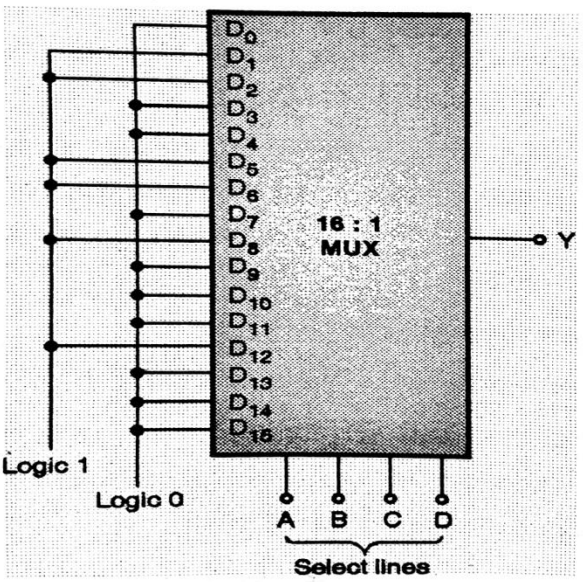
Group 3) – $\bar{A}\bar{B}C$

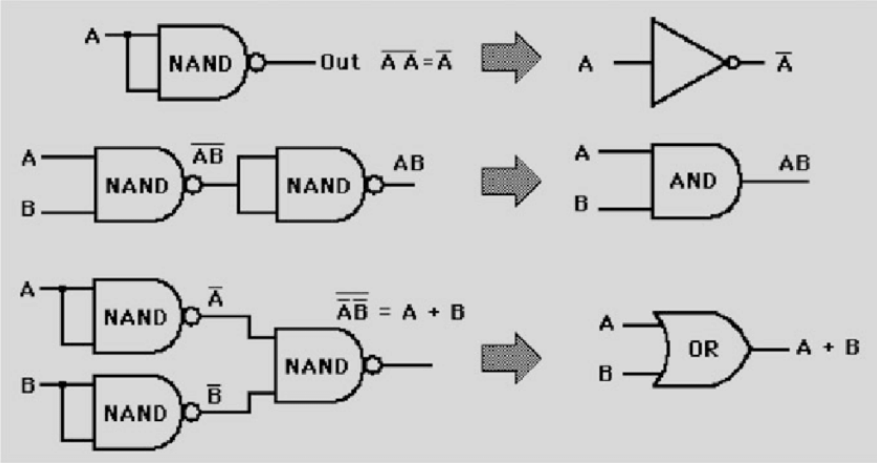
Group 4) – $\bar{B}\bar{C}D$

Step 2)- Simplified equation using K-map –

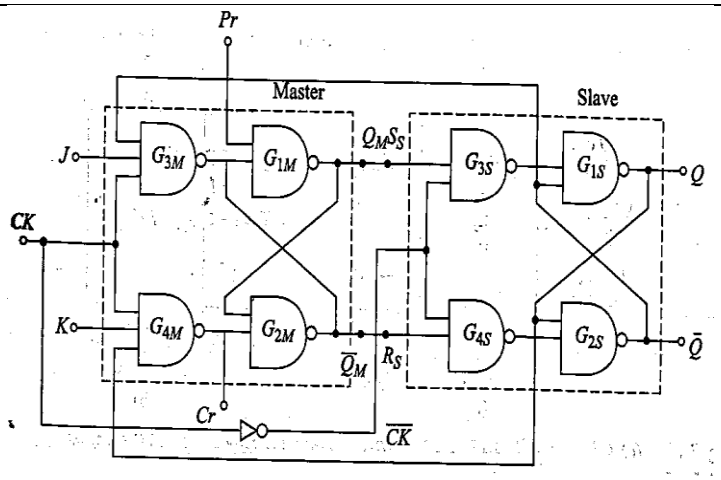
$Y = \bar{A}D + AB\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{B}\bar{C}D$

	iii)	**Implement the following function using 16:1 multiplexer.** **$Y=\sum m(1,2,5,6,8, 12)$**	**4M**

	Ans:		**4M**
Q.2		**Attempt any FOUR of the following:**	**16M**
	a)	**Convert the following numbers in binary and add them.** **$(l74)_8+(253)_8$**	**4M**
	Ans:	Step 1:- Binary of $(174)_8$ 1 7 4 001 111 100 → (1M) Step 2:- Binary of $(253)_8$ 2 5 3 010 101 011 → (1M) Step 3: Add binary of $(174)_8$ with $(253)_8$ ∴ 001 111 100 + 010 101 011 100 100 111 ---(2M) 4 4 7 ∴ $[(174)_8 + (253)_8 = (447)_8]$	

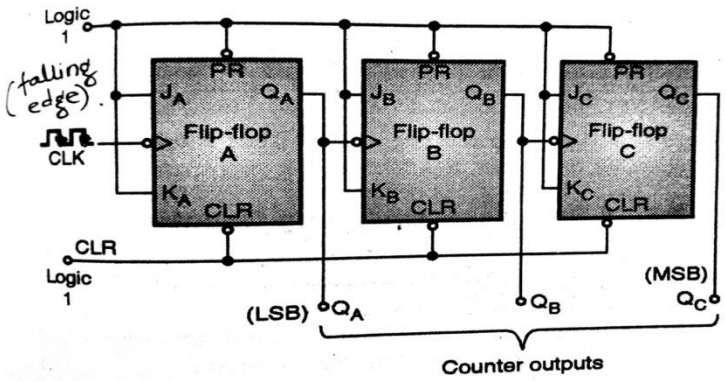
	b)	**Why NAND gate is called universal gate? Implement basic gates using NAND gate only.**	**4M**
	Ans:	**1.** With the help of NAND gate it is possible to implement all basic gates hence it is called as Universal gate**.** **2. Implementation of basic gates (NOT, AND OR) using NAND gate:**  	**1M for reason** **1M for each basic gate design**
	c)	**Convert the following expressions into their standard forms** **i)Y=A+BC+ABC** **ii)Y=(A+B)(A+C)**	**4M**

	Ans:	1) $Y = A + BC + ABC$ → step 1) - find the missing literals from each term - i.e. $Y = \underbrace{A}_{B\,\&\,C} + \underbrace{BC}_{A} + \underbrace{ABC}_{\text{All literals are present}}$ step 2) - ANDing each term (missing literals + complement of it) & solve to get canonical sop form. $\therefore Y = A(B+\bar{B})(C+\bar{C}) + BC(A+\bar{A}) + ABC$ $= (AB + A\bar{B})(C+\bar{C}) + ABC + \bar{A}BC + ABC$ $= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC + \bar{A}BC + ABC$ $= AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC + ABC$ (1M) $[\because ABC + ABC + ABC = ABC]$ $\therefore \boxed{Y = AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC + ABC}$ ..... (1M)	**2M**
		2) $Y = (A+B)(A+C)$ step 1) - find missing literals - $Y = \underbrace{(A+B)}_{C}\,\underbrace{(A+C)}_{B}$ step 2) - ORing each term (missing literal • complement of it) & solve to get canonical pos form $\therefore Y = (A+B+C\bar{C})(A+C+B\bar{B})$ $= (A+B+C)(A+B+\bar{C})(A+B+C)(A+\bar{B}+C)$ (1M) $\boxed{Y = (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)}$ $\{\because A \cdot A = A\}$ ... . (1M)	**2M**
	d)	**Draw the circuit diagram of master-slave J-K flip-flop with the help of NAND gates.**	**4M**
	Ans:	**Circuit diagram of master-slave J-K flip-flop :**	**4M**



e) **Design 3 bit asynchronous up counter, write its truth table and draw its output waveforms.** **4M**

Ans: **Circuit diagram:** **2M -**



Truth table: **1M**

Clock	Flip-flop outputs			State	Decimal equivalent
	Q_C (MSB)	Q_B	Q_A (LSB)		
Initially	0	0	0	1	0
1st (↓)	0	0	1	2	1
2nd (↓)	0	1	0	3	2
3rd (↓)	0	1	1	4	3
4th (↓)	1	0	0	5	4
5th (↓)	1	0	1	6	5
6th (↓)	1	1	0	7	6
7th (↓)	1	1	1	8	7
8th (↓)	0	0	0	1	0

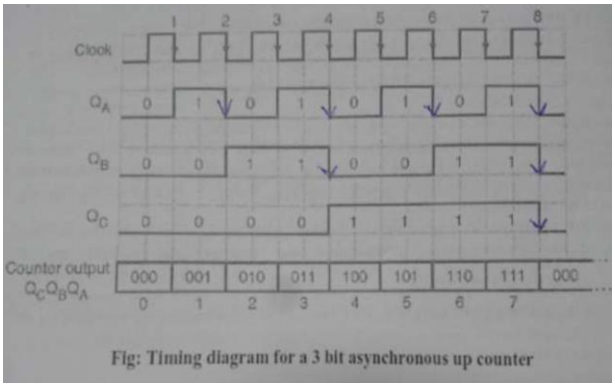
Fig: Truth Table.

Operation:

Initially all the flip flops are in reset state. i.e. QC QA QB =000

1st negative (falling) Clock pulse: FF-A toggles and QA becomes 1. it is treated as positive clock edge by FF-B so it does not change output state hence QB=0 so there is no change in QC, So QC=0, hence QC QB QA= 001 after 1st clock pulse.

2nd Clock pulse:- FF-A toggles and QA becomes 0.change in QA acts as negative clock edge

		for FF-B, hence it will toggle so QB becomes 1, which will acts as positive clock edge to FF-C hence QC remains unchanged so QC=0 therefore QC QB QA= 010 after 2nd clock pulse **3rd clock pulse:** After the 3rd clock pulse, the output are QCQBQA=011 accordingly. So all flip-flops will never trigger at the same time hence the counter is called as Asynchronous counter. **Timing (output) waveform:**  Fig: Timing diagram for a 3 bit asynchronous up counter	**1M**
	f)	**State and define any four specifications of DAC.**	**4M**
	Ans	**specifications of DAC** 1) Resolution 2) Accuracy 3) Setting time or DAC speed 4) Gain 5) Temperature sensitivity 6) Linearity 7) Môn tonicity 1) **Resolution**:- It is defined as the smallest possible change in the output voltage as a fraction or Percentage of the full scale output range it can be produced by a single step change in digital input. 2) **Accuracy**:- The accuracy of DAC is a measure of difference between the actual output as a percentage of full scale or maximum output voltage. 3) **Setting time or DAC speed**:- It is the time required for the DAC output to go from zero to full scale as the binary input is changed from 0 s to all 1s. Actually the setting time is measured as the time for the DAC output to settle within ±½ step size of its final value. 4) **Gain:-** It is defined as the ratio of the output voltage at DAC to the analogy equivalent of digital input. 5) **Temp sensitivity:** The parameters of active and passive devices varies with temp. These changes affects the	**Any 4 pont- 1M each point**

analogy output voltage of DACs. It is specified as ±pp m/oc.

6) **Linearity:** -
In DAC converters, equal increments in the numerical significance of the digital input should result in equal increment in the analogy output voltage.
The linearity of the converter is a measure of the precision with which the linear input output relationship is satisfied.

7) **Môn tonicity:-**
It is defined as the quality of DAC having no differential linearity problem. Thus monotonicity implies ±½ LSB accuracy.

Q.3 **Attempt any FOUR of the following :** **16M**

a) **Add $(248)_{10}$ and $(568)_{10}$ in BCD** **4M**

Ans:

$(248)_{10}$ 0010 0100 1000

$(568)_{10}$ + 0101 0110 1000 -------(1M)

0111 1011 0000
Valid Invalid In valid
BCD BCDBCD ----------(1M)

ADD 0110 TO INVALID BCD

111 11
0111 1011 0000
+ 0000 0110 0110

1000 0001 0110 ----------(1M)

8 1 6

$= (816)_{10}$ ----------(1M)

b) **Compare CMOS, TTL and ECL logic families. (any four points)** **4M**

Ans:

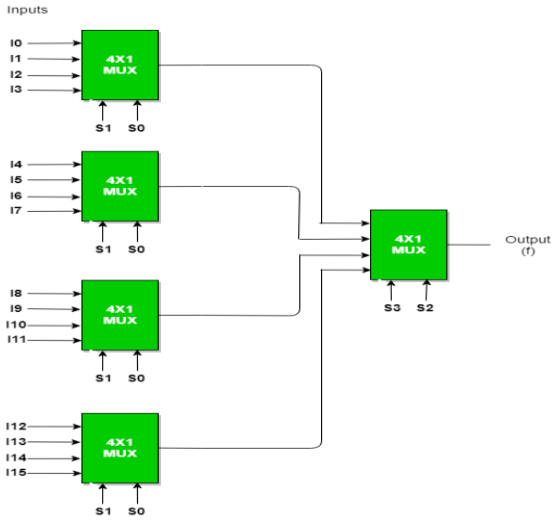
Parameter	CMOS	TTL	ECL
Basic gates	NOR/NAND	NAND	OR/NOR
Fan out	>50	10	25

Any four points- 1M each

Propagation delay(in ns)	**70-105**	**10**	**2**
Power dissipation(in mW)	**1.01mW**	**10mW**	**40-55**
Noise Immunity	**Excellent**	**Very good**	**Good**

c) **Design 16:1 multiplexer using 4:1 multiplexer.** **4M**

Ans:



Correct diagram 4M

d) **Write the use of preset and clear terminal in a flip-flop.** **4M**

Ans:

In the Flip-flop when the power is switched ON,the state of the circuit is uncertain.
It may be set(Q=1) or reset(Q=0)state.
In many applications it is desired to initially set or reset the flip flop ie. The initial state of the flip flop is to be assigned. This is done by preset(Pr)and clear(Cr) inputs.
Truth Table with Preset & Clear I/P

Input			Output(Q)	Operation Performed
CLK	Cr	Pr		
1	1	1	Qn+1	Normal FF
X	0	1	0	
X	1	0	1	

So ,the O/P of the flip-flop changes whenever a clock signal is applied, it is necessary to set the output or reset the output i e, to start with definite initial state, then two additional inputs Preset & Clear are used. These inputs sets or resets the flip-flop independent of clock.

(Role of each terminal 2 M each)

e) **State advantages and disadvantages of single slope ADC. (any two points each)** **4M**

Ans: **Any relevant Advantages of single slope AD** **:2M**

1.Single slope ADC's are appropriate for very high accuracy for very high resolution measurement where input signal bandwidth is relatively LOW

2.Be sides the accuracy these types of converters offer a low cost alternative to others.
Any relevant Disadvantages of Single slope ADC
1.It provide less speed as compared to dual slope.
2.Large errors possible due to noise.

:2M

f) Compare EPROM and EEPROM with any four points. **4M**

Ans:

SR.NO.	EPROM	EEPROM
1	Ultraviolet Light is used to erase the content of EPROM.	EEPROM contents are erased using electronic signal.
2	EPROM has a transparent quartz crystal window at the top.	EEPROM are totally encased in an opaque plastic case.
3	EPROM chip has to be removed from the computer circuit to erase and reprogram the computer BIOS.	EEPROM chip can be erased and reprogrammed in the computer circuit to erase and reprogram the content of computer BIOS.
4	EPROM is an older technology	EEPROM is a modern version over EPROM.

Any four points Each point 1M

Q.4 **Attempt any FOUR of the following :** **16M**

a) State and prove De' Morgan's theorems. **4M**

Ans:

i) $\overline{AB} = \overline{A} + \overline{B}$

It states that compliment of product is equal to sum of their compliments.

1	2	3	4	5	6
A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Column 03 = column 06
i.e. $\overline{AB} = \overline{A} + \overline{B}$
Hence proved

ii) $\overline{A+B} = \overline{A} \cdot \overline{B}$

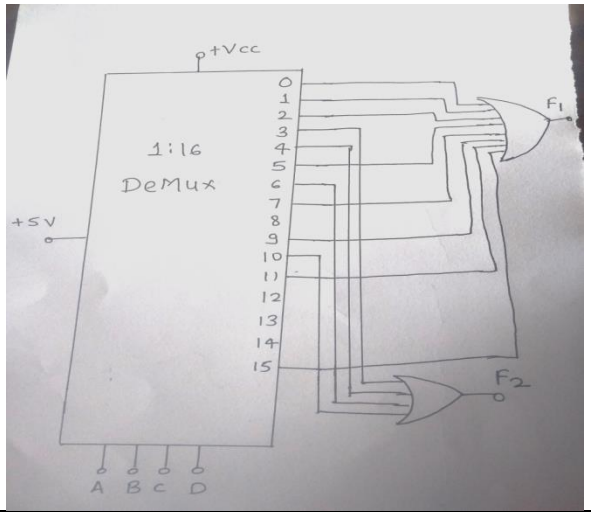
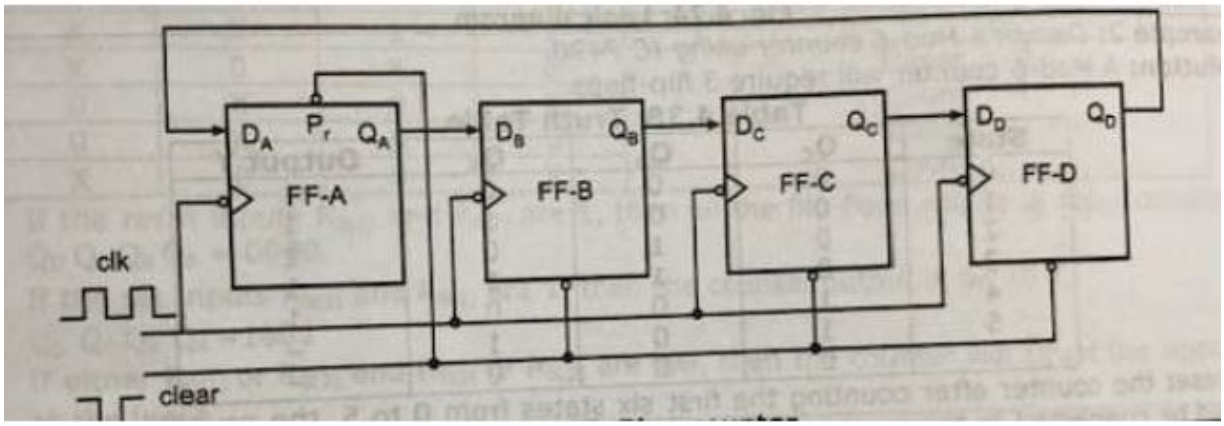
It states that complement of sum is equal to product of their complements.

1	2	3	4	5	6
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

Column 03 = column 06
$\therefore \overline{A+B} = \overline{A} \cdot \overline{B}$
Hence proved.

State 2M Proof 2M

b) Realize the following function using de multiplexer. **4M**
I) F1=∑m(0, 1,2,5,7,9, 11,15)

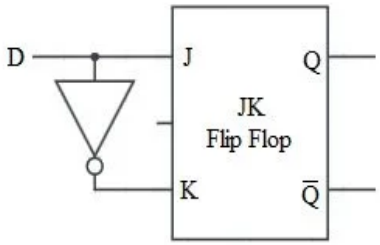
		(ii) F2=∑m(3,4,6, 10)	
	Ans:		**4M**
	c)	**Explain the working of 4 bit ring counter with neat diagram.**	**4M**
	Ans:	**Circuit Diagram :**  **Truth table** **calk** | **Q_A** | **Q_B** | **Q_C** | **Q_D** **X** | **1** | **0** | **0** | **0** **↓** | **0** | **1** | **0** | **0** **↓** | **0** | **0** | **1** | **0** **↓** | **0** | **0** | **0** | **1** **↓** | **1** | **0** | **0** | **0**	**Diagram-2M** **Explanation-2M**

4 bit ring counter:-As shown the 4 bit ring counter consists of 4 D flip flops (or SR or JK) where in the o/p of last flip flop is connected back to input of 1st flip flop. Clocks are applied simultaneously in serial output shift register manner. The working is as shown in truth table where 1 allowed to enter in 1st flip flop by activating preset terminal.
Therefore $Q_AQ_BQ_CQ_D$ =1000. Upon application of clock the data shifts from one flip flop to next in a circulating manner.
Therefore upon application of 1s t Click pulse status of $Q_AQ_BQ_CQ_D$ =0100.

2nd click pulse status of $Q_AQ_BQ_CQ_D$ =0010;
3rd click pulse status of $Q_AQ_BQ_CQ_D$ =0001.
And status of $Q_AQ_BQ_CQ_D$ will repeat after 4th click pulse as shown in truth

d) Convert J-K flip into 'D' and 'T' flip-flop. Write their truth tables. **4M**

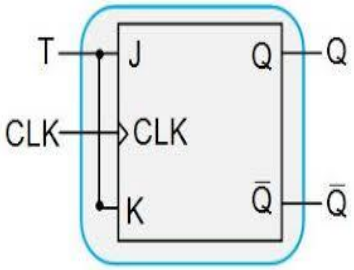
Ans: **D Flip flop :** **1M**



Truth Table : **1M**

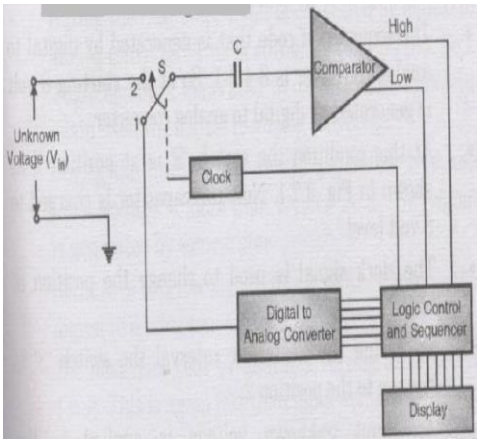
D	CLK	Qn+1	Comments
0	↑	**0**	**Reset**
1	↑	**1**	**Set**

T Flip flop : **1M**



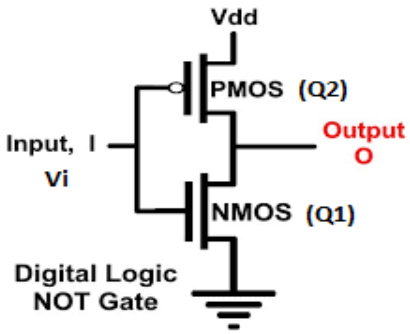
Truth table: **1M**

	Q_n+1
0	A_n
1	$\overline{Qn}$

	e)	**With the help of block diagram. Describe the working of successive approximation ADC.**	**4M**
	Ans:	 **Working Of Successive Approximation ADC :** DAC=Digital to Analog converter EOC=End of Conversion SAR=successive approximation register S/H=sample and hold circuit Vin=input voltage Verve=reference voltage The successive approximation Analog to digital converter circuit typically consists of four chief sub circuits: 1. A sample and hold circuit to acquire the input voltage (Vin). 2. An analog voltage comparator that compares Vin to the output of the internal DAC and outputs the result of the comparison to the successive approximation register(SAR). 3. A successive approximation register sub circuit designed to supply an approximate digital code of Vin to the internal DAC. 4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with Vin. The successive approximation register is initialized so that the most significant bit (MSB) is equal to digital 1.This code is fed into DAC, which then supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds Vin the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC). This code is fed into the DAC, which then supplies the analog equivalent.	**Block Diagram-2M Working-2M**
	f)	**Compare static RAM with Dynamic RAM, (any four points)**	**4M**
	Ans:	**Static RAM and dynamic RAM**	**Any four points-1M**

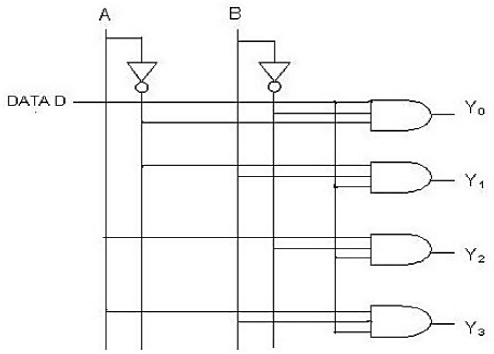
Parameter	Static RAM	Dynamic RAM
Circuit Configuration	Each SRAM cell is a flip flop	Each cell is one MOSFET & a capacitor
Bits stored	In the form of voltage	In the form of charges
No. of components per cell	More	Less
Storage capacity	Less	More

Each

Q5		**Attempt any FOUR of the following:**	**16**
	a)	**Draw the circuit diagram of CMOS NOT gate and explain its working.**	**4M**
	Ans:	**Circuit diagram of CMOS NOT gate:**  **Working:** 1. With $V_i = 0V$ (logic 0) • With $V_i = 0$, V_{GS} of Q_1 (NMOS) = 0V, So Q_1 OFF. But V_{GS} of Q_2 (PMOS) = V_{DD}. So Q_2 ON. • Hence $V_o = \pm V_{DD}$ i.e logic 1. 2. With $V_i = V_{DD}$ (logic 1) • With $V_i = + V_{DD}$, V_{GS} of Q_1 (NMOS) = V_{DD}, So Q_1 ON. But VGS of Q2 (PMOS) = 0V. So Q_2 OFF. • Hence, Vo is connected to ground i.e. Vo = 0 i.e logic 0. • Thus inversion takes place.	**2M** **2M**
	b)	**Draw and explain circuit diagram of 1 : 4 de multiplexer using logic gates.**	**4M**

Ans:

Circuit diagram of 1 : 4 de multiplexer using logic gates:



1 to 4 Demultiplexer

(dia – 2M

Working:

- A 1-to-4 de multiplexer has a single input (D), two selection lines (S_1 and S_0) and four outputs (Y_0 to Y_3).
- The input data goes to any one of the four outputs at a given time for a particular combination of select lines.
- The truth table of this type of de multiplexer is given below.
- From the truth table it is clear that, when S1=0 and S0= 0, the data input is connected to output Y0 and when S_1= 0 and s0=1, then the data input is connected to output Y_1.
- Similarly, other outputs are connected to the input for other two combinations of select lines.

Work 2M

Truth Table: (Optional)

Data Input	Select Inputs		Outputs			
D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

c)

In the Fig. No. 1 the control signals S_1,S_0 changes from 00 to

11. Write the truth table for outputs Q_A and $\overline{Q_A}$

Figure No. 1.

4M

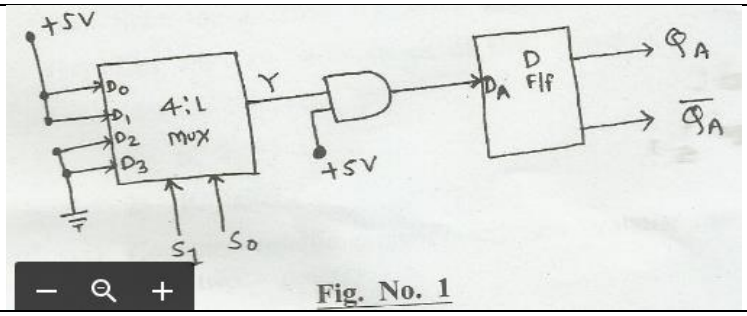


Fig. No. 1

Ans:

If the control signals S1S0 changes from 00 to 11 then the truth table for outputs QA and $\overline{Q_A}$ are as below.

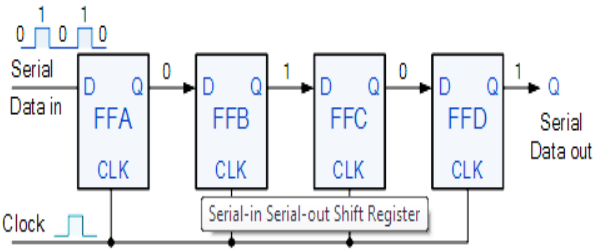
S1	S0	QA	$\overline{QA}$
0	0	1	0
0	1	1	0
1	0	0	1
1	1	0	1

4M

d) **Draw 4 bit SISO shift register using D-flip-flop. Explain its working in brief with waveforms.** **4M**

Ans: **2M**

Circuit Diagram:



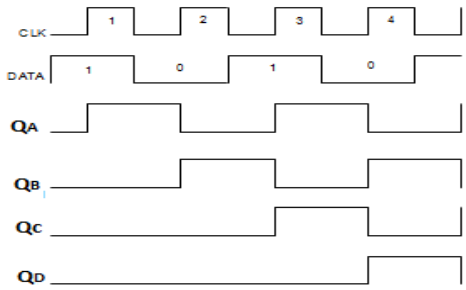
Working: **1M**

- In this serial in serial out shift register, when the clock signal is applied and the serial data is given; only one bit will be available at output at a time in the order of the input data.
- The data can be shifted either right or left. The right shift operation of 4 bit SISO is as below:

Operation of the Shift-right Register

Timing pulse	Q_A	Q_B	Q_C	Q_D	*Serial output at* Q_D
Initial value	0	0	0	0	0
After 1st clock pulse	1	0	0	0	0
After 2nd clock pulse	0	1	0	0	0
After 3rd clock pulse	1	0	1	0	0
After 4th clock pulse	0	1	0	1	1

Waveforms:



Output Waveforms of 4-bit Serial-in Serial-out Register

Note: Even 4 bit left shift SISO Register should be considered

Waveform-1M

e) **Calculate the analog output for 5 bit weighted resistor type DAC for inputs**

(i) 10110

(ii) 10001

Assume reference voltage = 1O$_V$

4M

Ans:

Given:
VR = 10V
Formula Used:
$V_o = - V_R (B1.2^{-1} + B2.2^{-2} + B3.2^{-3} + B4.2^{-4} + B5.2^{-5})$

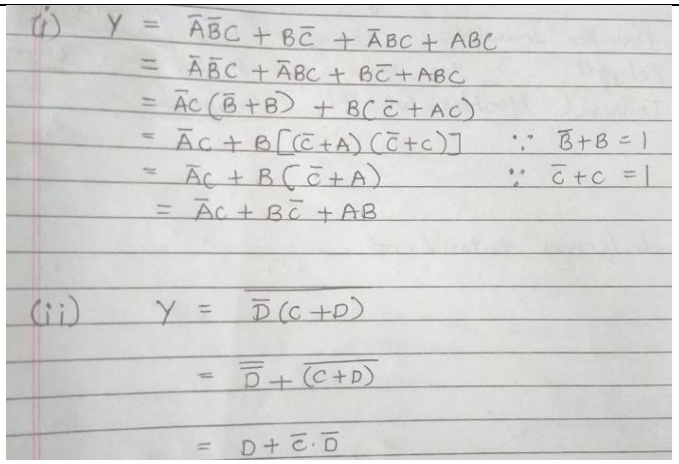
1. 10110
   $Vo = - V_R (B1.2^{-1} + B2.2^{-2} + B3.2^{-3} + B4.2^{-4} + B5.2^{-5})$
   $= - 10 (1*1/2 + 0 + 1*1/2^3 + 1 *1/2^4 + 0)$
   $= - 10 (1*1/2 + 1*1/8 + 1 *1/16)$
   $= - 10 (0.5 + 0.125 + 0.0625) = 6.875V$
   Vo = 6.875 V

2. 10001

(Each output 2mks)

		$Vo = - VR (B1.2^{-1} + B2.2^{-2} + B3.2^{-3} + B4.2^{-4} + B5.2^{-5})$ $= - 10 (1*1/2 + 0 + 0 + 0 + 1 *1/2^5)$ $= - 10 (1*1/2 + 1 *1/16)$ $= - 10 (0.5 + 0.03125) = 5.3125V$ $Vo = \underline{5.3125\ V}$	
	f)	**State any four advantages of semiconductor memories.**	**4M**
	Ans:	1. Occupy a small area. 2. Have a fast access time. 3. Operate with low power consumption. 4. They are non – volatile.	**(Each advantage 1mk)**
Q.6		**Attempt any FOUR of the following:**	**16M**
	a)	**Solve the following subtraction using l 's and 2's complement method $(10110)_2 - (10011)_2$**	**4M**
	Ans:	**1'sc complement:** $(10110)_2 – (10011)_2 = (00011)_2$ 1'sc of $(10011)_2 = (01100)_2$ 10110 + 01100 1 00010 Add Carry 1 00011	**2M**
		2'sc complement: $(10110)_2 – (10011)_2 = (00011)_2$ 2'sc of $(10011)_2 = (01100)_2 + (00001)_2 = (01101)_2$ 10110 + 01101 1 00011 Discard Carry	**2M**
	b)	**Simplify the following expressions using Boolean laws.** (i) $Y = \overline{A}\,\overline{B}\,C + B\overline{C} + \overline{A}BC + ABC$ (ii) $Y = \overline{\overline{D}(C + D)}$	**4M**

Ans:



$(D+\bar{C}).(D+\bar{D})$

$=(D+\bar{C})$

c) **Realize full adder circuit using K-map** **4M**

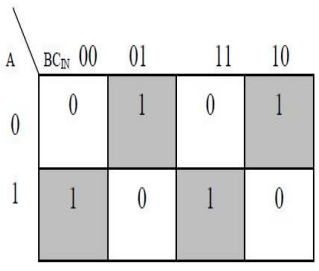
Ans: **(Truth table – 1M; Kmap for sum and Carry –2M Implementation – 1mk)**

The truth table for full adder is shown below.

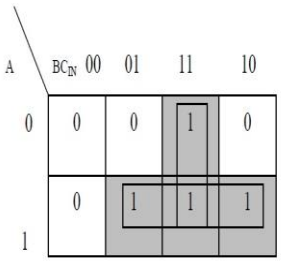
Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Based on the truth table, the Boolean functions for Sum (S) and Carry – out (COUT) can be derived using K – Map.

For Sum S,



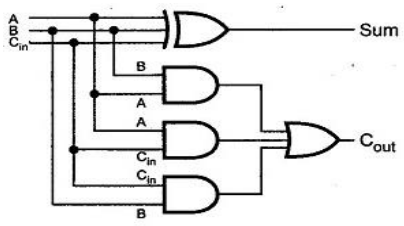
For Carry – out COUT,



The simplified equation for sum is

$sum=\bar{A}\bar{B}Cin + \bar{A}B\bar{C}in + A\bar{B}\bar{C}in + ABCin$

The simplified equation for COUT is COUT = AB + ACin + BCin



Implementation of full-adder

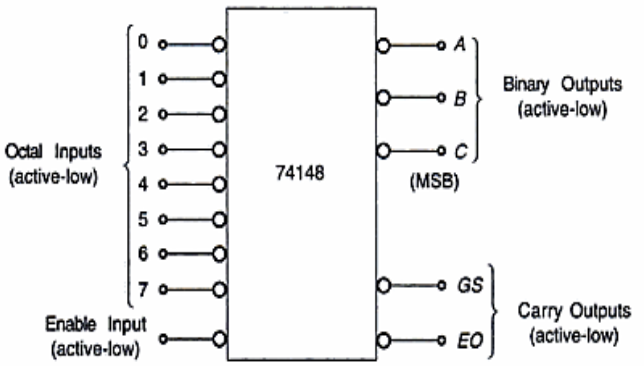
Note: Circuit diagram using universal gates also can be consider.

d) **Define priority encoder. Draw the block diagram of 8 : 3 priority encoder. Write its truth table.** **4M**

Ans: **Definition of priority encoder** **1M**

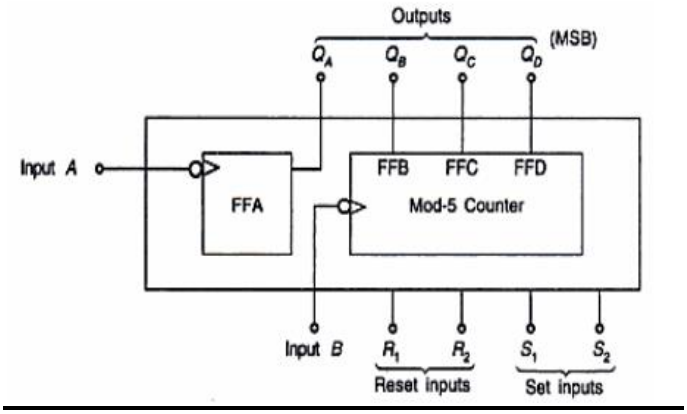
- Priority Encoder is a special type of encoder that responds to just one input in accordance with some priority system, among all those that may be simultaneously high.
- Priorities are given to the input lines. If two or more inputs are 1, at the same time, then input line with highest priority will be considered.

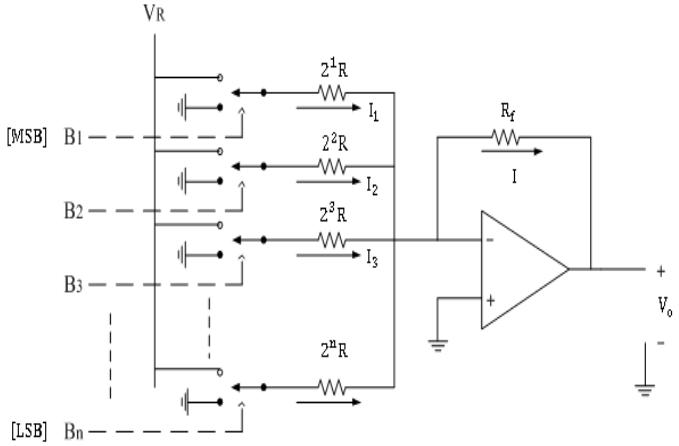
Block Diagram: 1 1/2M



Truth table of 74148

EI	Inputs								Outputs				
	0	1	2	3	4	5	6	7	C	B	A	GS	EO
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	x	0	1	1	1	1	1	1	1	1	0	0	1
0	x	x	0	1	1	1	1	1	1	0	1	0	1
0	x	x	x	0	1	1	1	1	1	0	0	0	1
0	x	x	x	x	0	1	1	1	0	1	1	0	1
0	x	x	x	x	x	0	1	1	0	1	0	0	1
0	x	x	x	x	x	x	0	1	0	0	1	0	1
0	x	x	x	x	x	x	x	0	0	0	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

			TT-1.5M
	e)	**Draw the block diagram of IC 7490 and specify it's working as decade counter.**	**4M**
	Ans:	**IC 7490 as decade counter:**  **Decade Counter Operation :** 1. The output of MOD-2 (Q_A) is externally connected to the input B which is the clock input of the internal MOD-5 counter. 2. Hence Q_A toggles on every falling edge of clock input whereas the output Q_D,Q_C,Q_B of the MOD-5 counter will increment from 000 to 100 on low going change of QA output. 3. Due to cascading of MOD-2 and MOD-5 counter, the overall configuration becomes a MOD-10 i.e. decade counter. 4. The reset inputs Ro(1), Ro(2) and preset inputs R9(1), R9(2) are connected to ground so as to make them inactive.	**2M** **2M**
	f)	**Draw the circuit diagram of 3-bit binary weighted resistor type DAC. Derive the expression for its output voltage.**	**4M**
	Ans	**Circuit diagram:**	**2M**



2M

Expression for its output voltage:

$$\therefore V_o = -IR_f$$

$$\therefore V_o = -[I_1 + I_2 + I_3 + \ldots\ldots\ldots + I_n]R_f$$

$$\therefore V_o = -\left[B_1 \frac{V_R}{2^1 R} + B_2 \frac{V_R}{2^2 R} + B_3 \frac{V_R}{2^3 R} + \ldots\ldots + B_n \frac{V_R}{2^n R}\right] R_f$$

$$V_o = -\frac{R_f}{R} V_R [B_1.2^{-1} + B_2.2^{-2} + B_3..2^{-3} + \ldots\ldots + B_n..2^{-n}]$$

$$If R_f = R$$

$$\therefore V_o = -V_R [B_1.2^{-1} + B_2.2^{-2} + B_3..2^{-3} + \ldots\ldots + B_n..2^{-n}]$$