LECTURE NOTES ON

INTEGRATED CIRCUIT APPLICATIONS

III B.Tech V semester

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UNIT I
INTEGRATED CIRCUITS

INTEGRATED CIRCUITS

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

Advantages of integrated circuits

1. Miniaturization and hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability due to the elimination of soldered joints.
4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Reduction in power consumption

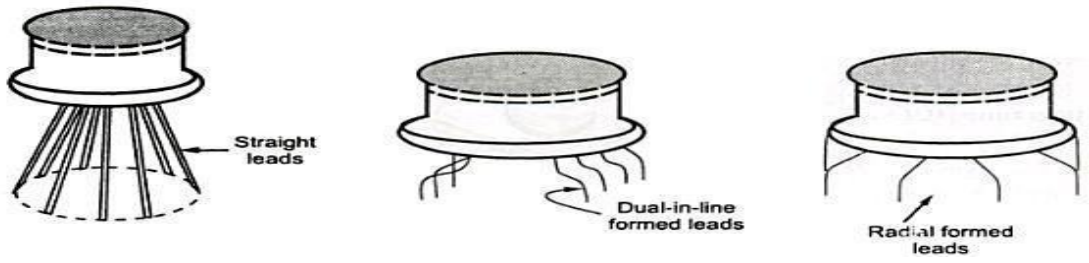
Depending upon the number of active devices per chip,there are different levels of integration

	Level of integration	Number of active devices per chip
1	Small scale integration(SSI)	Less then100
2	Medium Scale integration(MSI)	100-10000
3	Large scale integration(LSI)	1000-100,000
4	Very Large scale integration(VLSI)	Over 100,000
5	Ultra Large scale integration(ULSI)	Over 1 milloin

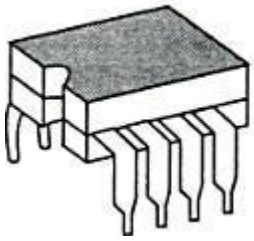
IC Package Types

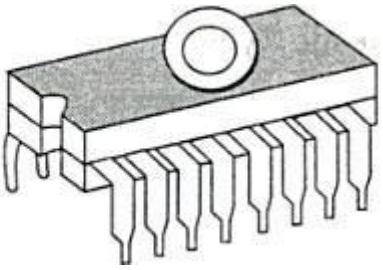
The op-amp ICs are available in various packages. The IC packages are classified as,
1.Metal Can
2.Dual In Line
3.Flat Pack

Metal Can package:

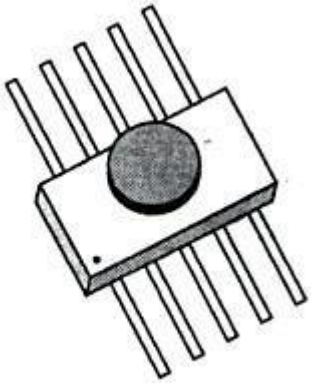


Dual- in- Line Package:





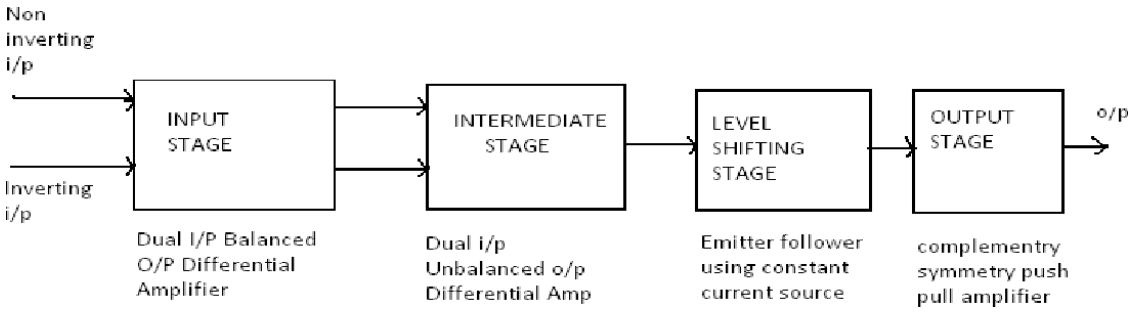
Flat Pack:



10 lead version

INTERNAL CIRCUIT :

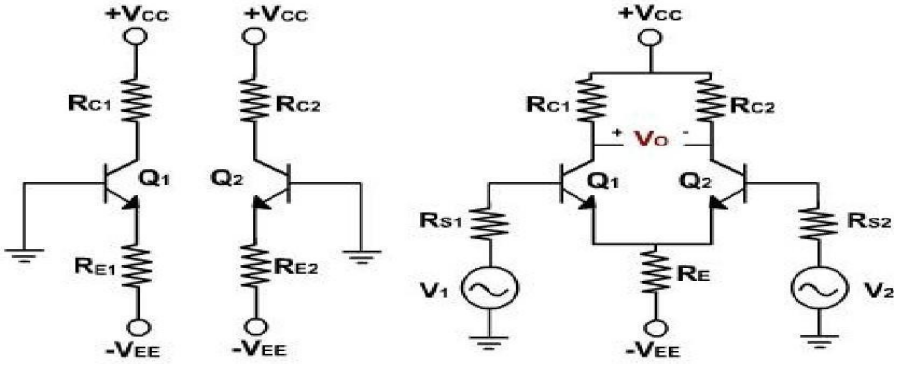
The operational amplifier is a direct-coupled high gain amplifier usable from 0 to over 1MHz to which feedback is added to control its overall response characteristic i.e. gain and bandwidth. The op-amp exhibits the gain down to zero frequency. The internal block diagram of an op-amp is shown in the fig The input stage is
the dual input balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp. The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. On most amplifiers, the intermediate stage is dual input, unbalanced output. Because of direct coupling, the dc voltage at the output of the intermediate stage is well above ground potential. Therefore, the level translator (shifting) circuit is used after the intermediate stage downwards to zero volts with respect to ground. The final stage is usually a push pull complementary symmetry amplifier output stage. The output stage increases the voltage swing and raises the ground supplying capabilities of the op-amp. A well designed output stage also provides low output resistance.



Block Diagram of OP-AMP

Differential amplifier:

Differential amplifier is a basic building block of an op-amp. The function of a differential amplifier is to amplify the difference between two input signals. The two transistors Q1 and Q2 have identical characteristics. The resistances of the circuits are equal, i.e. RE1 = R E2, RC1 = R C2 and the magnitude of +VCC is equal to the magnitude of -VEE. These voltages are measured with respect to ground.



Differential Amplifier

To make a differential amplifier, the two circuits are connected as shown in fig. 1.4. The two +VCC and -VEE supply terminals are made common because they are same. The two emitters are also connected and the parallel combination of RE1 and RE2 is replaced by a resistance RE. The two input signals v1& v2 are applied at the base of Q1 and at the base of Q2. The output voltage is taken between two collectors. The collector resistances are equal and therefore denoted by RC = RC1 = RC2.

Ideally, the output voltage is zero when the two inputs are equal. When v1 is greater then v2 the output voltage with the polarity shown appears. When v1 is less than v2, the output voltage has the opposite polarity.

The differential amplifiers are of different configurations.

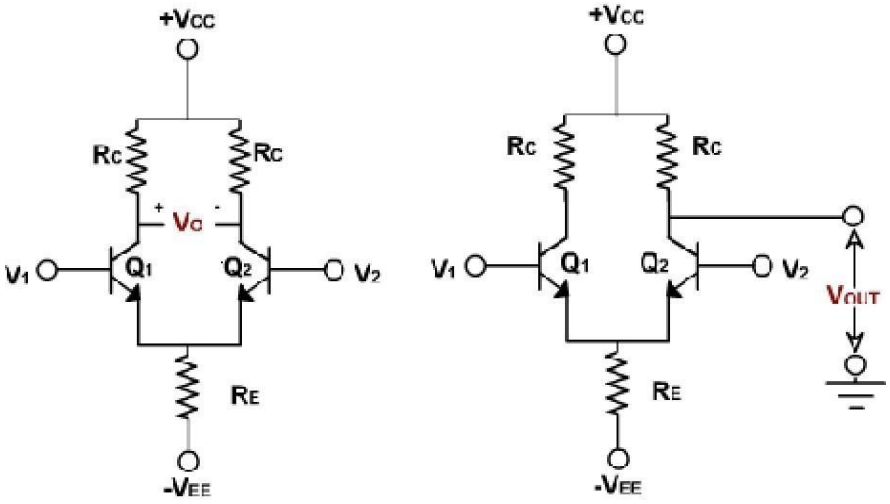


Fig. Dual input, balanced output differential amplifier.Fig.1.6. Dual input, unbalanced output differential amplifier.

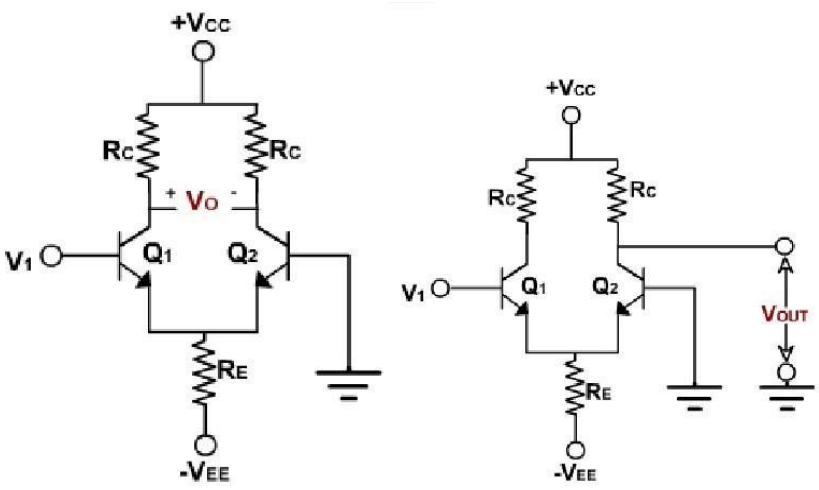


Fig..Single input, balanced output differential amplifierFig.1.8.Single input, unbalanced output differential amplifier.

The four differential amplifier configurations are following:

1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
3. Single input balanced output differential amplifier.
4. Single input unbalanced output differential amplifier.

These configurations are shown in fig and are defined by number of input signals used and the way an output voltage is measured. If use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration. On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground. If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output.

A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers. The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signals.

1.8.1 Dual Input, Balanced Output Differential Amplifier:

The circuit is shown in figV1 and V2 are the two inputs, applied to the bases of Q1 and Q2 transistors. The output voltage is measured between the two collectors C1 and C2, which are at same dc potentials.

D.C. Analysis:

To obtain the operating point (ICQ and VCEQ) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages V1 and V2 to zero as shown in fig

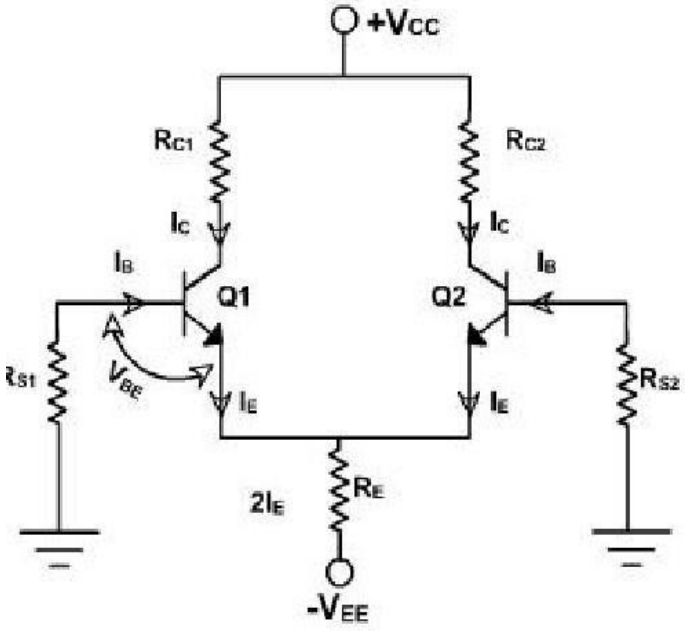


Fig.Differential Amplifier

The internal resistances of the input signals are denoted by RS because RS1= RS2. Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined. The same values of ICQ and VCEQ can be used for second transistor Q2. Applying KVL to the base emitter loop of the transistor Q1.

$$R_S\, I_B + V_{BE} + 2\, I_E\, R_E = V_{EE}$$

But $I_B = \dfrac{I_E}{\beta_{dc}}$ and $I_C \approx I_E$

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}} \qquad (E\text{-}1)$$

$V_{BE} = 0.6V$ for S_i and $0.2V$ for G_e.

Generally $\dfrac{R_S}{\beta_{dc}} << 2R_E$ because R_S is the internal resistance of input signal.

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

The value of RE sets up the emitter current in transistors Q1 and Q2 for a given value of VEE. The emitter current in Q1 and Q2 are independent of collector resistance RC. The voltage at the emitter of Q1 is approximately equal to -VBE if the voltage drop across R is negligible. Knowing the value of IC the voltage at the collector VCis given by

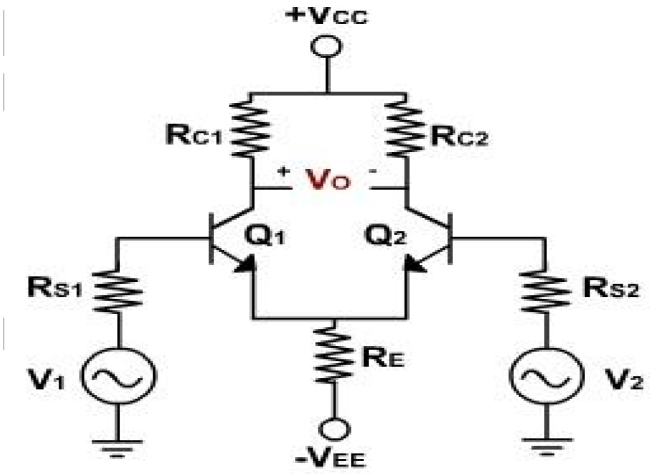


Fig Differential Amplifier

VC =VCC- IC RC and VCE = VC- VE

= VCC - IC RC + VBE

VCE = VCC + VBE -ICRC

From the two equations VCEQ and ICQ can be determined. This dc analysis is applicable for all types of differential amplifier.

A.C. Analysis :

The circuit is shown in fig. V1 and V2 are the two inputs, applied to the bases of Q1 and Q2 transistors. The output voltage is measured between the two collectors C1 and C2, which are at same dc potentials.

Dc analysis has been done to obtain the operating point of the two transistors. To find the voltage gain Ad and the input resistance Ri of the differential amplifier, the ac equivalent circuit is drawn using r-parameters as shown in fig. The dc voltages are reduced to zero and the ac equivalent of CE configuration is used.

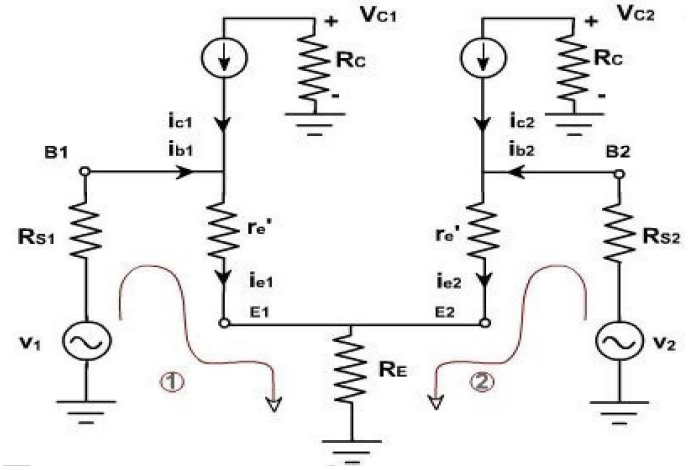


Fig. Differential Amplifier A/C Analysis

Since the two dc emitter currents are equal. Therefore, resistance r'e1 and r'e2 are also equal and designated by r'e . This voltage across each collector resistance is shown 180° out of phase with respect to the input voltages v1 and v2. This is same as in CE configuration. The polarity of the output voltage is shown in Figure. The collector C2 is assumed to be more positive with respect to collector C1 even though both are negative with respect to ground.

The output voltage VO is given by

$$\begin{aligned} V_o &= V_{c2} - V_{c1} \\ &= -R_C i_{C2} - (-R_c i_{c1} \\ &= R_C(i_{C1} - i_{c2}) \\ &= R_C(i_{e1} - i_{e2}) \end{aligned}$$

Substituting ie1, & ie2 in the above expression

$$V_o = R_C\left\{\frac{(r_e' + R_E)V_1 - R_E V_2}{(r_e' + R_E)^2 - R_E^2} - \frac{(r_e' + R_E)V_2 - R_E V_1}{(r_e' + R_E)^2 - R_E^2}\right\}$$

$$= \frac{R_C(V_1 - V_2)(r_e' - 2R_E)}{r_e'(r_e' + 2R_E)}$$

$$V_o = \frac{R_C}{r_e'}(V_1 - V_2) \ldots\ldots\ldots\ldots E(1)$$

Thus a differential amplifier amplifies the difference between two input signals. Defining the difference of input signals as Vd =V1 -V2 the voltage gain of the dual input balanced output differential amplifier can be given by (E-2)

Differential Input Resistance:

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance Ri1 seen from the input signal source V1 is determined with the signal source V2 set at zero.

$$R_{i1} = \left.\frac{v_1}{i_{b1}}\right|_{v_2 = 0}$$

$$= \left.\frac{v_1}{i_{e1}/\beta}\right|_{v_2 = 0}$$

$$R_{i1} = \frac{\beta r'_e (r'_e + 2R_E)}{r'_e + R_E}$$

Since $R_E >> r'_e$

$\therefore \quad r'_e + 2R_E >> 2R_E$

Similarly, the input signal V1 set at zero to determine the input resistance Ri2 seen from the input signal source V2. Resistance RS1 and RS2 are ignored because they are very small.

Subtuting ie 1,

Similarly

$$R_{i2} = \left.\frac{V_2}{i_{b2}}\right|_{v_1 = 0}$$

$$= \left.\frac{V_2}{i_{e2}/\beta}\right|_{v_1 = 0}$$

$$R_{i2} = 2\beta r'_e \qquad (E-4)$$

The factor of 2 arises because the re' of each transistor is in series. To get very high input impedance with differential amplifier is to use Darlington transistors. Another ways is to use FET.

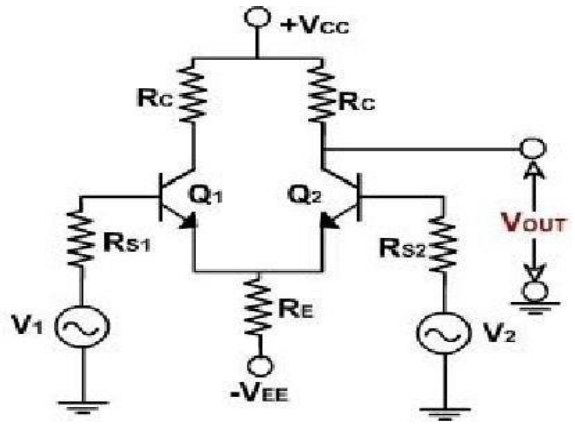
Output Resistance:

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance RO1 measured between collector C1 and ground is equal to that of the collector resistance RC. Similarly the output resistance RO2 measured at C2 with respect to ground is equal to that of the collector resistor RC.

RO1 = RO2 = RC (E-5)

The current gain of the differential amplifier is undefined. Like CE amplifier the differential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier.

Dual Input, Unbalanced Output Differential Amplifier:



Differential Amplifier

In this case, two input signals are given however the output is measured at only one of the two- collector w.r.t. ground as shown infig1.12. The output is referred to as an unbalanced output because the collector at which the output voltage is measured is at some finite dc potential with respect to ground.

In other words, there is some dc voltage at the output terminal without any input signal applied. DC analysis is exactly same as that of first case.

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + R_2 / \beta_{dc}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

AC Analysis:

The output voltage gain in this case is given by

$$A_d = \frac{V_0}{V_d} = \frac{R_C}{2r'_e}$$

The voltage gain is half the gain of the dual input, balanced output differential amplifier. Since at the output there is a dc error voltage, therefore, to reduce the voltage to zero, this configuration is normally followed by a level translator circuit.

DIFFERENTIAL AMPLIFIER:

The differential amplifier consists of two symmetrical common-emitter sections and is capable of amplifying the difference between two input signals. The differential amplifier can amplify ac as well as dc input signals because it employs direct coupling.

There are four types of differential amplifier configurations:

(a) The dual Input, Balanced output differential

amplifier DC Analysis $I_E = V_{EE} - V_{BE}/2R_E$,

$V_{CE} = Vcc + V_{BE} - R_c I_c$

AC Analysis ------- $A_d = R_C/r_e$

$R_{i1} = R_{i2} = 2\beta_{ac} r_e$

$R_{01} = R_{02} = R_c$

(b) The dual input, unbalanced output differential

Amplifier DC Analysis $I_E = V_{EE} - V_{BE}/(2R_E + R_{in}/\beta_{dc})$

$V_{CE} = Vcc + V_{BE} - R_c I_{CQ}$

AC Analysis ----------$A_d = R_C/2r_e$

$R_{i1} =$

$R_{i2} = 2\beta_{ac} r_e$

$R_0 = R_c$

(c) The single input, balanced output differential

Amplifier DC Analysis $I_E = V_{EE} - V_{BE}/(2R_E + R_{in}/\beta_{dc})$

$V_{CE} = Vcc + V_{BE} - R_c I_{CQ}$

AC Analysis ----------$I_E = V_{EE} - V_{BE}/(2R_E + R_{in}/\beta_{dc})$

$R_i = 2\beta$

$_{ac} r_e$

$R_{01} = R_0$

$_2 = R_c$

(d) The single input, unbalanced output differential

Amplifier DC Analysis $I_E = V_{EE} - V_{BE}/(2R_E + R_{in}/\beta_{dc})$

$V_{CE} = Vcc + V_{BE} - R_c I_{CQ}$

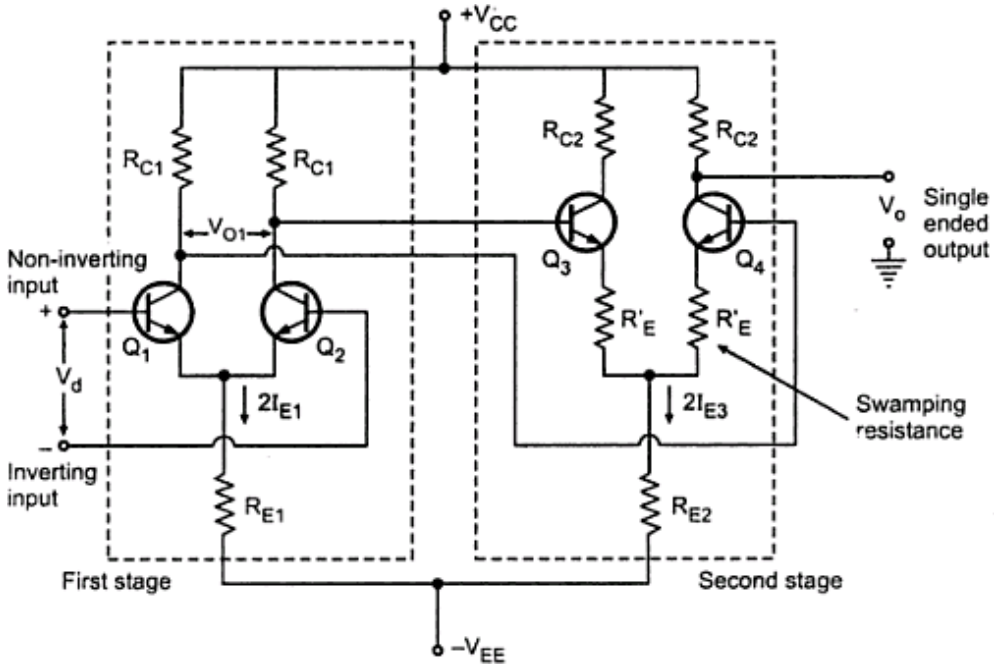
AC Analysis --------- $A_d = R_C/2r_e$

$R_{i=}2\beta_{ac}r_e$

$R_0= R_c$

Cascade Differential Amplifier Stages:

In cascaded differential amplifier, the output of the first stage is used as an input for the second stage, the output of the second stage is applied as an input to the third stage, and so on. Because of direct coupling between the stages, the operating point of succeeding stages changes



Level Translator:

Because of the direct coupling the dc level at the emitter rises from stages to stage. This increase in dc level tends to shift the operating point of the succeeding stages and therefore limits the output voltage swing and may even distort the output signal.

To shift the output dc level to zero, level translator circuits are used. An emitter follower with voltage divider is the simplest form of level translator as shown in fig Thus a dc voltage at the base of Q produces 0V dc at the output. It is decided by R1 and R2. Instead of voltage divider emitter follower either with diode current bias or current mirror bias as shown in fig may be used to get better results.

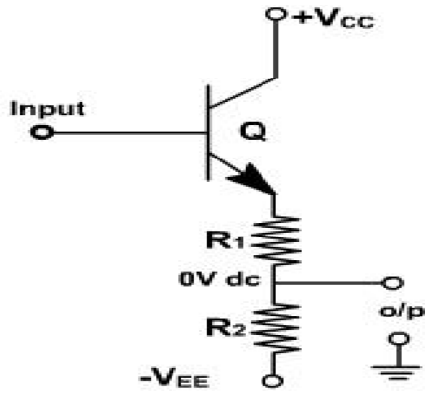


Fig Common collector Amplifier

In this case, level shifter, which is common collector amplifier, shifts the level by 0.7V. If this shift is not sufficient, the output may be taken at the junction of two resistors in the emitter leg.

Fig shows a complete op-amp circuit having input different amplifiers with balanced output, intermediate stage with unbalanced output, level shifter and an output amplifier.

characteristics Op-amp

DC characteristics:

a) Input offset voltage:

Input offset voltage Vio is the differential input voltage that exists between two input terminals of an op-amp without any external inputs applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero. Let us denote the output offset voltage due to input offset voltage Vio as Voo. The output offset voltage Voo is caused by mismatching between two input terminals. Even though all the components are integrated on the same chip, it is not possible to have two transistors in the input differential amplifier stage with exactly the same characteristics. This means that the collector currents in these two transistors are not equal, which causes a differential output voltage from the first stage. The output of first stage is amplified by following stages and possibly aggravated by more mismatching in them.

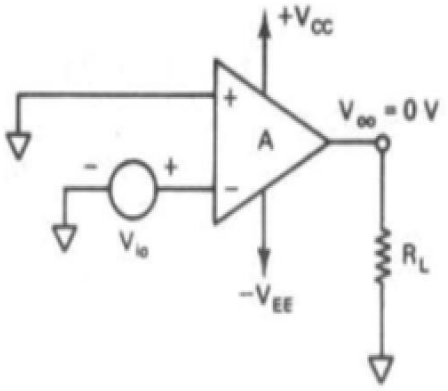


Fig Input offset voltage in op-amp

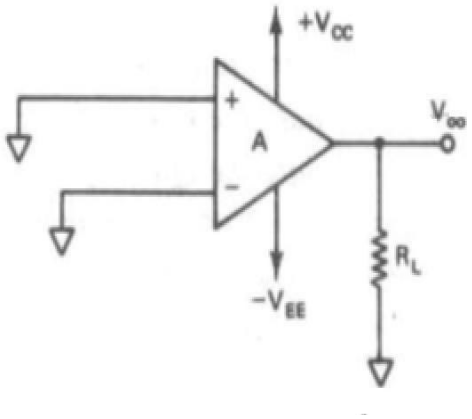


Fig Output offset voltage in op-amp

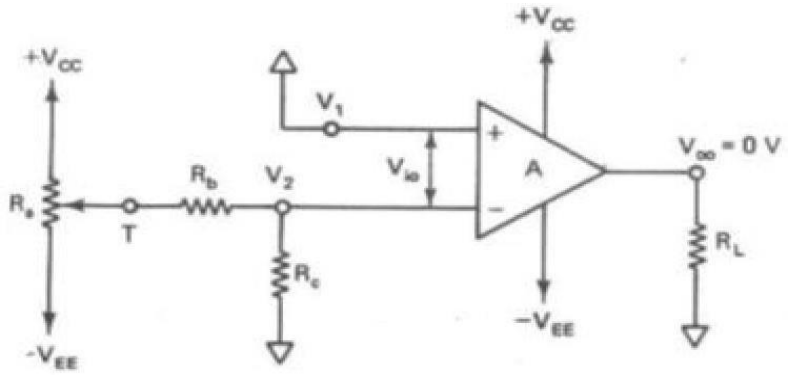


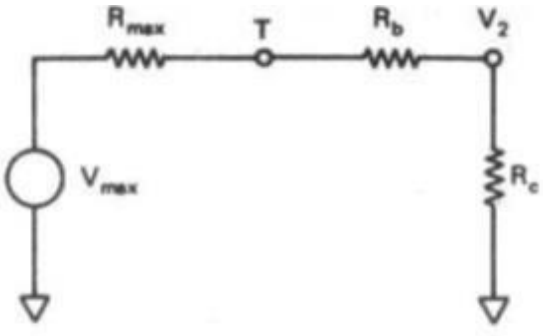
Fig .Op-Amp with offset voltage compensating network

The op-amp with offset-voltage compensating network is shown in Figure The Compensating network consists of potentiometer *Ra* and resistors *Rb* and *Re.* To establish a relationship between *Vio,* supply voltages, and the compensating components, first Thevenize the circuit, looking back into *Ra* from point *T.* The maximum Thevenin's equivalent resistance *Rmax,* occurs when the wiper is at the center of the Potentiometer, as shown in Figure.

$$R_{max} = (R_a/2) \| (R_a/2)$$

Supply voltages *VCC* and *–VEE* are equal *in* magnitude therefore; let us denote their magnitude by voltage *V.*

Thus $V_{max} = V$.



where *V2* has been expressed as a function of maximum Thevenin's voltage *Vmax* and maximum Thevenin's resistance, But the maximum value of *V2* can be equal to *Vio* since *V1— V2 = Vio*. Thus Equation becomes

$$V_2 = \frac{R_c}{R_{max} + R_b + R_c} V_{max}$$

$$V_{io} = \frac{R_c}{R_{max} + R_b + R_c} V_{max}$$

Assume Rb >Rmax >Rc, where Rmax = Ra/4. Using this assumption Rmax+Rb+Rc=Rb Therefore

$$V_{io} = \frac{R_c V_{max}}{R_b}$$

where

$$V_{max} = V = |V_{CC}| = |-V_{EE}|$$

$$V_{io} = \frac{R_c V}{R_b}$$

Let us now examine the effect of *Vio* in amplifiers with feedback. The non-inverting and inverting amplifiers with feedback are shown in Figure. To determine the effect of Vio, in each case, we have to reduce the input voltage vin to zero.

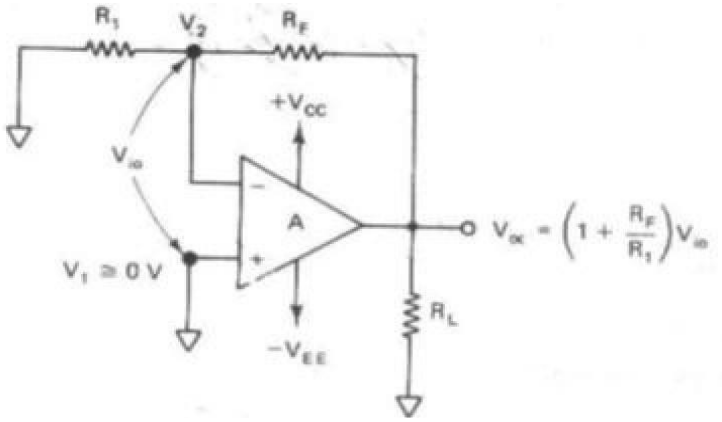


Fig Closed loop non inverting or inverting Amp

With vin reduced to zero, the circuits of both non-inverting and inverting amplifiers are the sameas the circuit in Figure. The internal resistance Rin of the input signal voltage is negligibly small.In the figure, the non-inverting input terminal is connected to ground; therefore, assume voltage*V1* at input terminal to be zero. The voltageV2 at the inverting input terminal can be determinedby applying the voltage-divider rule:

$$V_2 = \frac{R_1 V_{oo}}{R_1 + R_F}$$

Therefore,

$$V_{oo} = \frac{R_1 + R_F}{R_1} V_2$$

Since $V_{io} = |V_1 - V_2|$ and $V_1 = 0$ V,

$$V_{io} = |0 - V_2| = V_2$$

Therefore,

$$V_{oo} = \left(1 + \frac{R_F}{R_1}\right) V_{io} = (A_{oo})\, V_{io}$$

a) Input offset voltage

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage

b) Input bias current

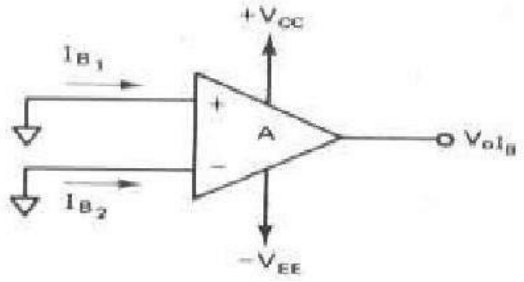
Input bias current IB as the average value of the base currents entering into terminal of an op- amp.

c) Input bias current

Input bias current IB as the average value of the base currents entering into terminal of an op- amp.

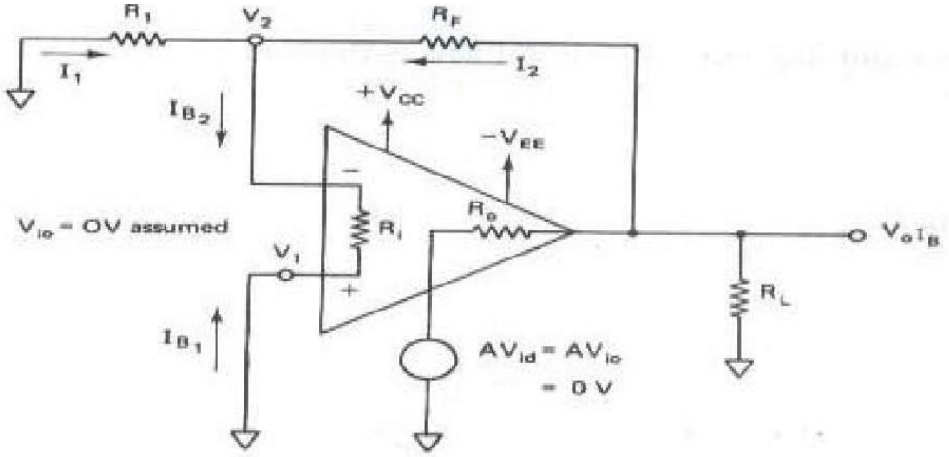
$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

where I_{B1} = dc bias current flowing into the noninverting input
I_{B2} = dc bias current flowing into the inverting input



$I_B = I_{B1} = I_{B2}$

Obtaining the expression for the output offset voltage caused by the input bias current IB in the inverting and non-inverting amplifiers and then devise some scheme to eliminate or minimize it.



In the figure, the input bias currents ‘81 and *1* are flowing into the non-inverting and inverting input leads, respectively. The non-inverting terminal is connected to ground; therefore, the voltage *V1* = 0 V. The controlled voltage source *A Vio* =0 V since Vio= 0 V is assumed. With output resistance Ro is negligibly small, the right end of *RF* is essentially at ground potential; that is, resistors *R1,* and *RF* are in parallel and the bias current *I,* flows through them. Therefore, the voltage at the inverting terminal is

d) Thermal Drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25oc may not remain so when the temperature rises to 35oc. This is called thermal drift.

AC CHARACTERISTICS:

a) Slew Rate

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage. An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage.

The symbolic diagram of an OPAMP is shown in fig

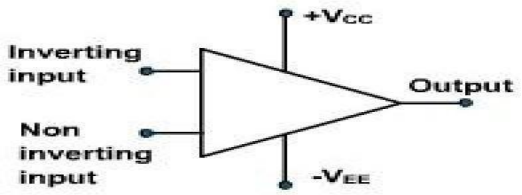


Fig. Op-Amp Symbol

b) Frequency Response

Need for frequency compensation in practical op-amps:

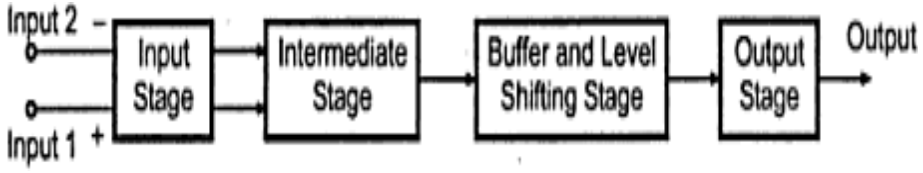
Frequency compensation is needed when large bandwidth and lower closed loop gain is desired. Compensating networks are used to control the phase shift and hence to improve the stability

Frequency compensation methods: a) Dominant- pole compensation b) Pole- zero compensation.

741c is most commonly used OPAMP available in IC package. It is an 8-pin DIP chip.

Block diagram of op-amp:

The block diagram of IC op-amp is as shown in figure



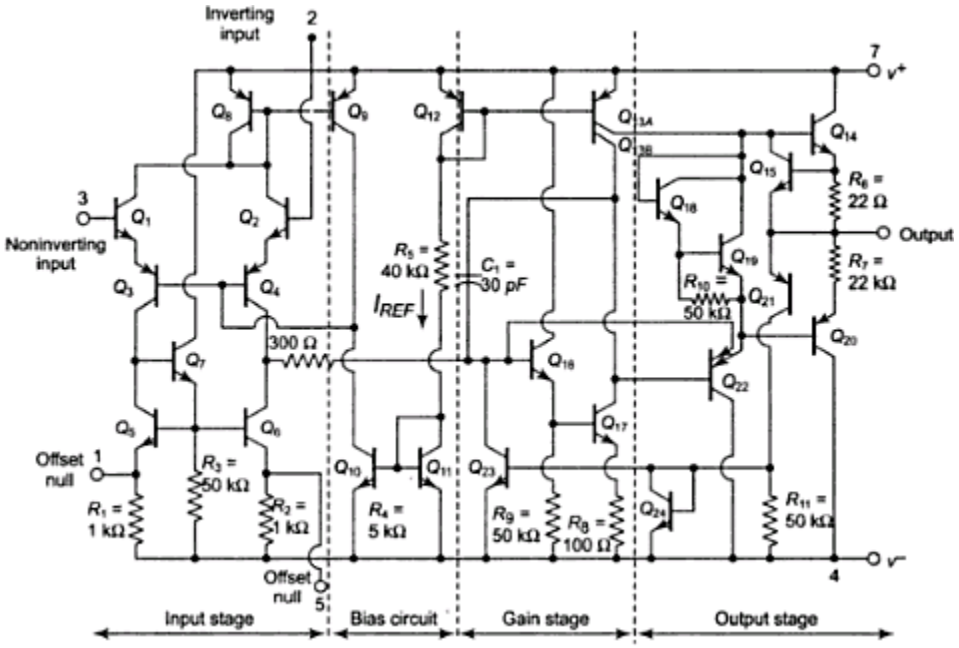
Ideal OP-AMP

An ideal OP-AMP would have the following characteristics:

1. The input resistance R_{IN} would be infinite
2. The output resistance R_{OUT} would be zero
3. The voltage gain, V_G would be infinite
4. The bandwidth (how quickly the output will follow the input) would be infinite
5. If the voltages on the two inputs are equal than the output voltage is zero (If the output is not zero it is said to have an offset)

Op-amp 741:

The IC 741 is high performance monolithic op-amp IC .It is available in 8 pin, 10 pin or 14 pin configuration. It can operate over a temperature of -55 to 125 centigrade.op-amp 741 equivalent circuit is as shown in figure.



Features of IC-741

- No frequency compensation required.
- Short circuit protection provided.
- Offset voltage null capability.
- Large common mode and Differential voltage range.
- No latch up.
- No External frequency compensation is required
- Short circuit Protection
- Low Power Dissipation

Parameters of OPAMP:

1. Input Offset Voltage:

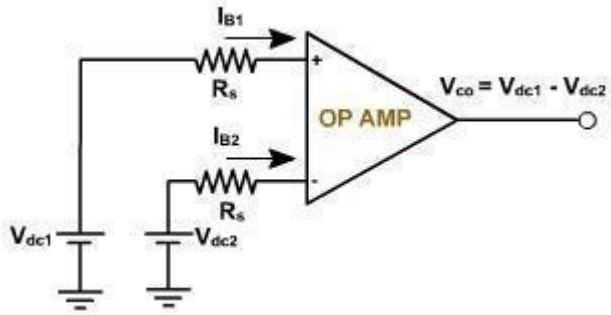


Fig. Input offset voltage

If no external input signal is applied to the op-amp at the inverting and non-inverting terminals the output must be zero. That is, if Vi=0, Vo=0. But as a result of the given biasing supply voltages, +Vcc and –Vcc, a finite bias current is drawn by the op-amps, and as a result of asymmetry on the differential amplifier configuration, the output will not be zero. This is known as offset. Since Vo must be zero when Vi=0 an input voltage must be applied such that the output offset is cancelled and Vo is made zero. This is known as input offset voltage. Input offset voltage (Vio) is defined as the voltage that must be applied between the two input terminals of an OPAMP to null or zero the output voltage. Fig 1.22 shows that two dc voltages are applied to input terminals to make the output zero.

$$Vio = Vdc1 - Vdc2$$

Vdc1 and Vdc2 are dc voltages and RS represents the source resistance. Vio is the difference of Vdc1 and Vdc2. It may be positive or negative. For a 741C OPAMP the maximum value of Vio is 6mV. It means a voltage ± 6 mV is required to one of the input to reduce the output offset voltage to zero. The smaller the input offset voltage the better the differential amplifier, because its transistors are more closely matched.

Input offset Current:

Though for an ideal op-amp the input impedance is infinite, it is not so practically. So the IC draws current from the source, however smaller it may be. This is called input offset current Iio. The input offset current Iio is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier as shown in fig

$$Iio = | IB1 - IB2 |$$

The Iio for the 741C is 200nA maximum. As the matching between two input terminals is improved, the difference between IB1 and IB2 becomes smaller, i.e. the Iio value decreases further. For a precision OPAMP 741C, Iio is 6 nA

Input Bias Current:

The input bias current IB is the average of the current entering the input terminals of a balanced amplifier i.e.

$IB = (IB1 + IB2) / 2$

For ideal op-amp IB=0. For 741C IB(max) = 700 nA and for precision 741C IB = ± 7 nA

Differential Input Resistance: (Ri)

Ri is the equivalent resistance that can be measured at either the inverting or non- inverting input terminal with the other terminal grounded. For the 741C the input resistance is relatively high 2 MΩ. For some OPAMP it may be up to 1000 G ohm.

Input Capacitance: (Ci)

Ci is the equivalent capacitance that can be measured at either the inverting and non inverting terminal with the other terminal connected to ground. A typical value of Ci is 1.4 pf for the 741C.

Offset Voltage Adjustment Range:

741 OPAMP have offset voltage null capability. Pins 1 and 5 are marked offset null for this purpose. It can be done by connecting 10 K ohm pot between 1 and 5.

By varying the potentiometer, output offset voltage (with inputs grounded) can be reduced to zero volts. Thus the offset voltage adjustment range is the range through which the input offset voltage can be adjusted by varying 10 K pot. For the 741C the offset voltage adjustment range is ± 15 mV.

Input Voltage Range :

Input voltage range is the range of a common mode input signal for which a differential amplifier remains linear. It is used to determine the degree of matching between the inverting and non-inverting input terminals. For the 741C, the range of the input common mode voltage is ± 13V maximum. This means that the common mode voltage applied at both input terminals can be as high as +13V or as low as -13V.

Large Signal Voltage Gain:

Since the OPAMP amplifies difference voltage between two input terminals, the voltage gain of the amplifier is defined as

$$\text{Voltage gain} = \frac{\text{Output voltage}}{\text{Differential input voltage}}$$

$$A = \frac{V_o}{V_{id}}$$

Because output signal amplitude is much large than the input signal the

voltage gain is commonly called large signal voltage gain. For 741C is voltage gain is 200,000 typically.

Output voltage Swing:

The ac output compliance PP is the maximum unclipped peak to peak output voltage that an OPAMP can produce. Since the quiescent output is ideally zero, the ac output voltage can swing positive or negative. This also indicates the values of positive and negative

saturation voltages of the OP-AMP. The output voltage never exceeds these limits for a given supply voltages +VCC and -VEE. For a 741C it is ± 13 V.

Output Resistance: (RO)

RO is the equivalent resistance that can be measured between the output terminal of the OPAMP and the ground. It is 75 ohm for the 741C OPAMP.

Output Short circuit Current :

In some applications, an OPAMP may drive a load resistance that is approximately zero. Even its output impedance is 75 ohm but cannot supply large currents. Since OPAMP is low power device and so its output current is limited. The 741C can supply a maximum short circuit output current of only 25mA.

Supply Current:

IS is the current drawn by the OP-AMP from the supply. For the 741C OPAMP the supply current is 2.8 m A.

Power Consumption:

Power consumption (PC) is the amount of quiescent power (Vin= 0V) that must be consumed by the OPAMP in order to operate properly. The amount of power consumed by the 741C is 85 mW.

Gain Bandwidth Product:

The gain bandwidth product is the bandwidth of the OPAMP when the open loop voltage gain is reduced to

1.32.1 From open loop gain vs frequency graph At 1 MHz shown in.fig.1.24,it can be found 1 MHz for the 741C OPAMP frequency the gain reduces to 1. The mid band voltage gain is 100, 000 and

cut off frequency is 10Hz.

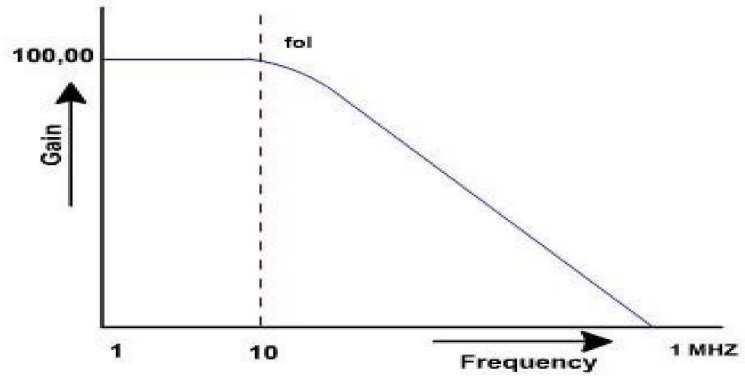


Fig.1.24 Band width of OP-AMP

Slew Rate:

The maximum rate of change of output voltage with respect to time is called Slew rate of the Op-amp.

It is expressed as, S = $_{max}$ and measured in

V/sec. The Slew rate equation is, S = $2\pi f V_m$

V/sec

Common Mode Rejection Ratio (CMRR).

CMRR is defined as the ratio of the differential voltage gain Ad to the common mode voltage gain

ACM CMRR = Ad / ACM.

For the 741C, CMRR is 90 dB typically. The higher the value of CMRR the better is the matching between two input terminals and the smaller is the output common mode voltage.

PSRR:

PSRR is Power Supply Rejection Ratio. It is defined as the change in the input offset voltage due to the change in one of the two supply voltages when other voltage is

maintained constant. It's ideal value should be Zero.

Slew Rate: Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions and is expressed in volts / μsecs.

To understand this, consider a charging current of a capacitor

$$i = C\frac{dV}{dt}$$

$$\frac{dV}{dt} = i/C$$

If 'i' is more, capacitor charges quickly. If 'i' is limited to Imax, then rate of change is also limited. Slew rate indicates how rapidly the output of an OP-AMP can change in response to changes in the input frequency with input amplitude constant. The slew rate changes with change in voltage gain and is normally specified at unity gain.

If the slope requirement is greater than the slew rate, then distortion occurs. For the 741C the slew rate is low 0.5 V / μS which limits its use in higher frequency applications.

Input Offset Voltage and Current Drift:

It is also called average temperature coefficient of input offset voltage or input offset current. The input offset voltage drift is the ratio of the change in input offset voltage to change in temperature and expressed in ΔV /° C. Input offset voltage drift = (ΔVio /ΔT). Similarly, input offset current drift is the ratio of the change in input offset current to the change in temperature. Input offset current drift = (ΔIio / ΔT).

For 741C,

$$\Delta Vio / \Delta T = 0.5 \text{ V / C. } \Delta \text{ Iio/ } \Delta T = 12 \text{ pA / C}$$

Unit 2
Op-amp Applications

SUMMING, SCALING, AND AVERAGING AMPLIFIERS

Inverting Configuration

Figure shows the inverting configuration with three inputs *Va, Vb,* and *Vc.* Depending on the relationship between the feedback resistor R_f and the input resistors *Ra, Rb,* and *Rc,* the circuit can be used as either a summing amplifier, scaling amplifier, or averaging amplifier. The circuit's function can be verified by examining the expression for the output voltage *V0,* which is obtained from Kirchhoff's current equation written at node *V2.* Referring to Figure

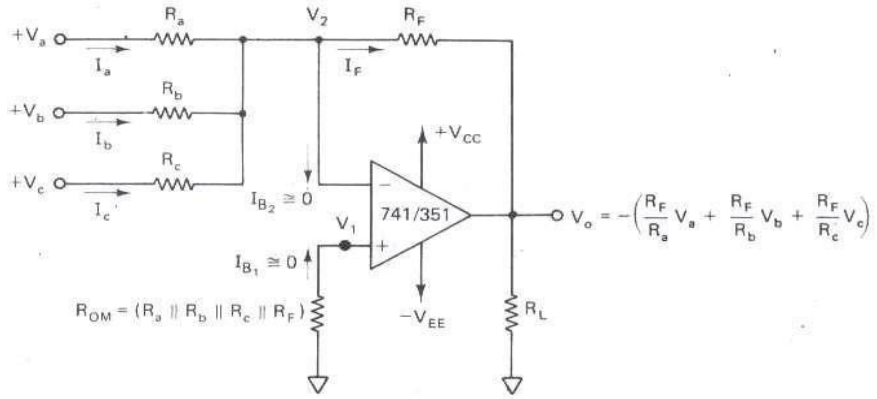


Figure Inverting configuration with three inputs can be used as a summing amplifier, scaling amplifier, or averaging amplifier.

$$I_a + I_b + I_c = I_B + I_F$$

Since R_i and A of the op-amp are ideally infinity, $I_B = 0$ A and $V_1 = V_2 \cong 0$ V. Therefore,

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_F}$$

or

$$V_o = -\left(\frac{R_F}{R_a} V_a + \frac{R_F}{R_b} V_b + \frac{R_F}{R_c} V_c\right)$$

Summing amplifier.

If Ra=Rb=Rc=R then

$$V_o = -\frac{R_F}{R}(V_a + V_b + V_c)$$

This means that the output voltage is equal to the *negative* sum of all the inputs times the gain of the circuit R_F/R; hence the circuit is called a *summing amplifier*. Obviously, when the gain of the circuit is 1, that is, $R_a = R_b = R_c = R_F$, the output voltage is equal to the *negative* sum of all input voltages. Thus

$$V_o = -(V_a + V_b + V_c)$$

Scaling or weighted amplifier. If each input voltage is amplified by a different factor, in other words, weighted differently at the output, the circuit in Figure is then called a *scaling* or *weighted amplifier*. This condition can be accomplished if R_a, R_b, and R_c are different in value. Thus the output voltage of the scaling amplifier is

$$V_o = -\left(\frac{R_F}{R_a}V_a + \frac{R_F}{R_b}V_b + \frac{R_F}{R_c}V_c\right)$$

where

$$\frac{R_F}{R_a} \neq \frac{R_F}{R_b} \neq \frac{R_F}{R_c}$$

Average circuit.

The circuit of Figure can be used as an *averaging circuit*, in which the output voltage is equal to the average of all the input voltages. This is accomplished by using all input resistors of equal value, $R_a = R_b = R_c = R$. In addition, the gain by which each input is amplified must be equal to 1 over the number of inputs; that is,

$$\frac{R_F}{R} = \frac{1}{n}$$

where n is the number of inputs.

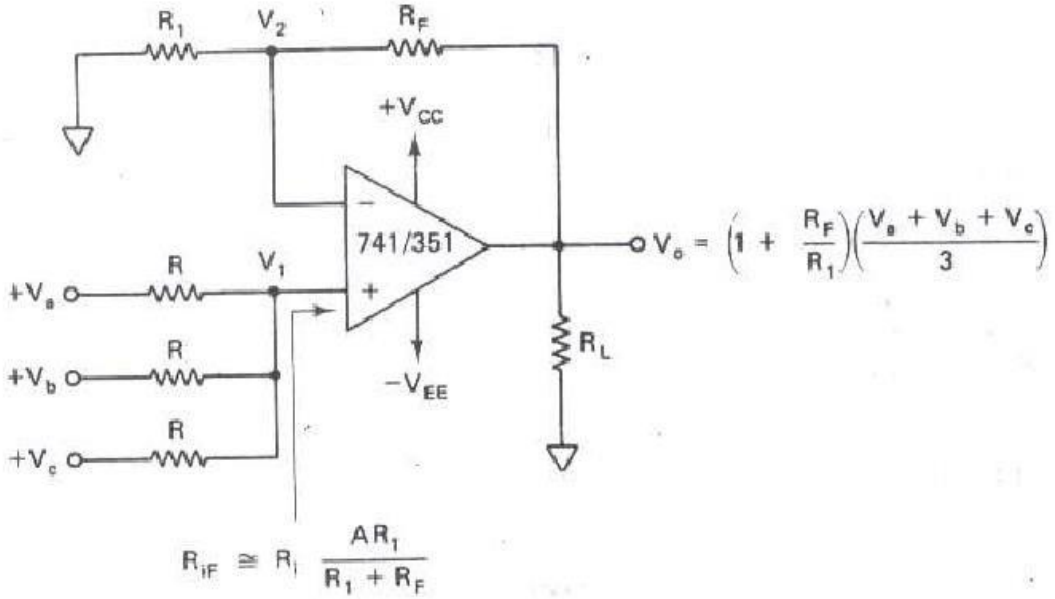
Noninverting Configuration

Again, to verify the functions of the circuit, the expression for the output voltage must be obtained. Recall that the input resistance R_{iF} of the noninverting amplifier is very large (see Figure . Therefore, using the superposition theorem, the voltage V_1 at the noninverting terminal is

$$V_1 = \frac{R/2}{R + R/2} V_a + \frac{R/2}{R + R/2} V_b + \frac{R/2}{R + R/2} V_c$$

or

$$V_1 = \frac{V_a}{3} + \frac{V_b}{3} + \frac{V_c}{3} = \frac{V_a + V_b + V_c}{3}$$



Hence the output voltage V_o is

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1$$

$$= \left(1 + \frac{R_F}{R_1}\right) \frac{V_a + V_b + V_c}{3}$$

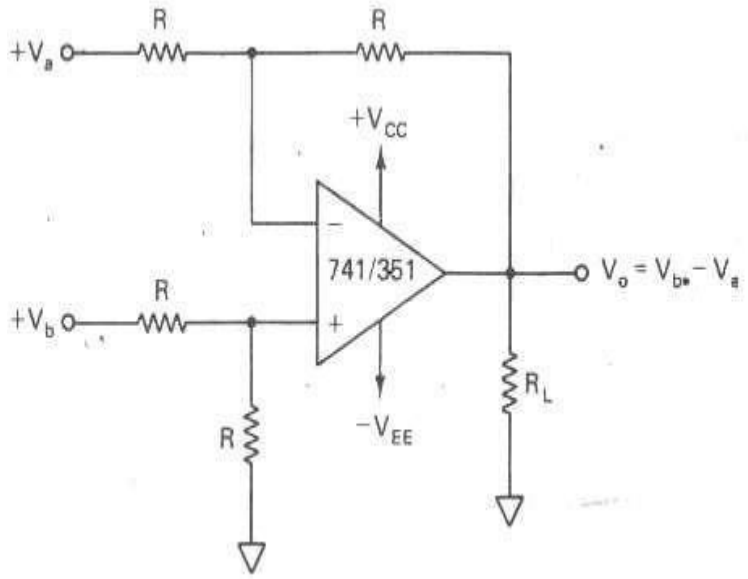
Averaging amplifier. If $(1+R_F/R_1)=1$; It will be averaging amplifier.

Summing amplifier. If $(1+R_F/R_1)=3$; It will be summing amplifier.

Scaling or weighted amplifier. It is basically scaling amplifier.

Differential Configuration

A subtractor.



From this figure, the output voltage of the differential amplifier with a gain of 1 is

$$V_o = -\frac{R}{R}(V_a - V_b)$$

That is,

$$V_o = V_b - V_a$$

INSTRUMENTATION AMPLIFIER

In many industrial and consumer applications the measurement and control of physical conditions are very important. For example, measurements of temperature and humidity inside a dairy or meat plant permit the operator to make necessary adjustments to maintain product quality. Similarly, precise temperature control of a plastic furnace is needed to produce a particular type of plastic.

Generally, a transducer is used at the measuring site to obtain the required information easily and safely. The *transducer* is a device that converts one form of energy into another.

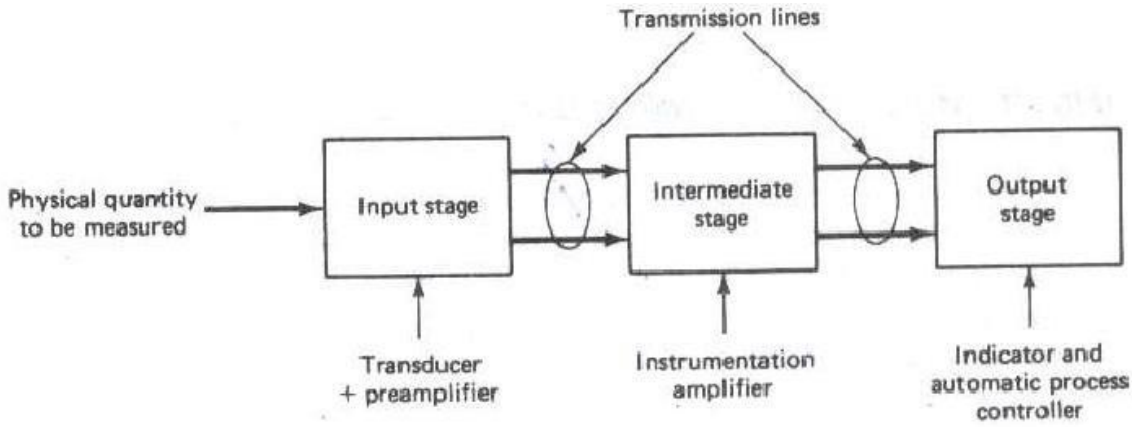
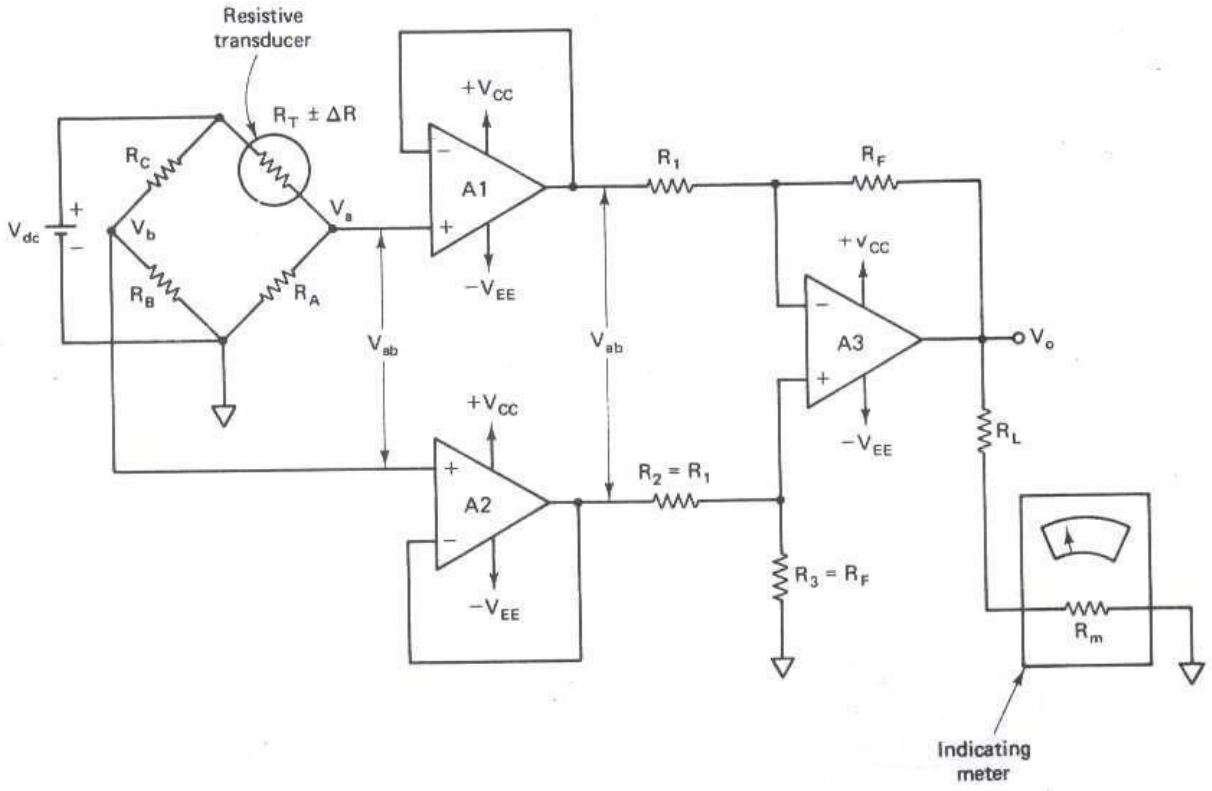


Figure 7–11 Block diagram of an instrumentation system.

An instrumentation system is used to measure the output signal produced by a transducer and often to control the physical signal producing it.

The input stage is composed of a preamplifier and some sort of transducer, depending on the physical quantity to be measured. The output stage may use devices such as meters, oscilloscopes, charts, or magnetic recoders.

Instrumentation Amplifier Using Transducer Bridge



A *resistive transducer* whose resistance changes as a function of some physical energy is connected in one arm of the bridge with a small circle around it and is denoted by $(R_T \pm \Delta R)$, where R_T is the resistance of the transducer and ΔR the change in resistance R_T.

The bridge in the circuit of Figure is dc excited but could be ac excited as well. For the balanced bridge at some reference condition,

$$V_b = V_a$$

or

$$\frac{R_B(V_{dc})}{R_B + R_C} = \frac{R_A(V_{dc})}{R_A + R_T}$$

That is,

$$\frac{R_C}{R_B} = \frac{R_T}{R_A}$$

The bridge is balanced initially at a desired reference condition. However, as the physical quantity to be measured changes, the resistance of the transducer also changes, which causes the bridge to unbalance ($V_a \neq V_b$). The output voltage of the bridge can be expressed as a function of the change in resistance of the transducer, as described next.

Let the change in resistance of the transducer be ΔR. Since R_B and R_C are fixed resistors, the voltage V_b is constant. However, voltage V_a varies as a function of the change in transducer resistance. Therefore, according to the voltage-divider rule,

$$V_a = \frac{R_A(V_{dc})}{R_A + (R_T + \Delta R)}$$

$$V_b = \frac{R_B(V_{dc})}{R_B + R_C}$$

Consequently, the voltage V_{ab} across the output terminals of the bridge is

$$V_{ab} = V_a - V_b$$

$$= \frac{R_A V_{dc}}{R_A + R_T + \Delta R} - \frac{R_B V_{dc}}{R_B + R_C}$$

However, if $R_A = R_B = R_C = R_T = R$, then

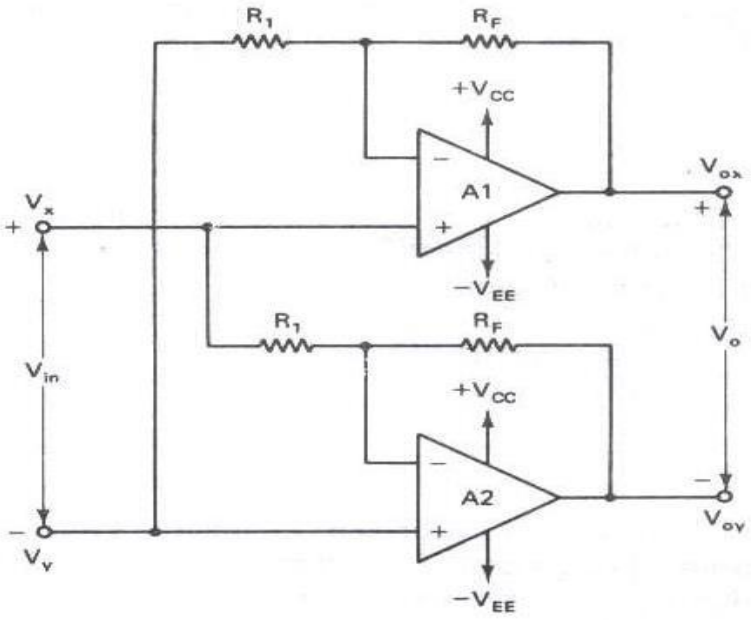
$$V_{ab} = -\frac{\Delta R(V_{dc})}{2(2R + \Delta R)}$$

The negative (−) sign in this equation indicates that $V_a < V_b$ because of the increase in the value of R_T.

The output voltage V_{ab} of the bridge is then applied to the differential instrumentation amplifier composed of three op-amps (see Figure). The voltage followers preceding the basic differential amplifier help to eliminate loading of the bridge circuit. The gain of the basic differential amplifier is $(-R_F/R_1)$; therefore, the output V_o of the circuit is

$$V_o = V_{ab}\left(-\frac{R_F}{R_1}\right) = \frac{(\Delta R)V_{dc}}{2(2R + \Delta R)}\frac{R_F}{R_1}$$

DIFFERENTIAL INPUT AND DIFFERENTIAL OUTPUT AMPLIFIER



superposition theorem, the output V_{ox} due to inputs V_x and V_y is

$$V_{ox} = \left(1 + \frac{R_F}{R_1}\right) V_x - \left(\frac{R_F}{R_1}\right) V_y$$

Similarly, the output V_{oy} is

$$V_{oy} = \left(1 + \frac{R_F}{R_1}\right) V_y - \left(\frac{R_F}{R_1}\right) V_x$$

However, the differential output V_o is

$$V_o = V_{ox} - V_{oy}$$

Therefore, from Equations (7-18a) and (7-18b),

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_x - \left(\frac{R_F}{R_1}\right) V_y - \left(1 + \frac{R_F}{R_1}\right) V_y + \left(\frac{R_F}{R_1}\right) V_x$$

$$= \left(1 + \frac{2R_F}{R_1}\right) (V_x - V_y)$$

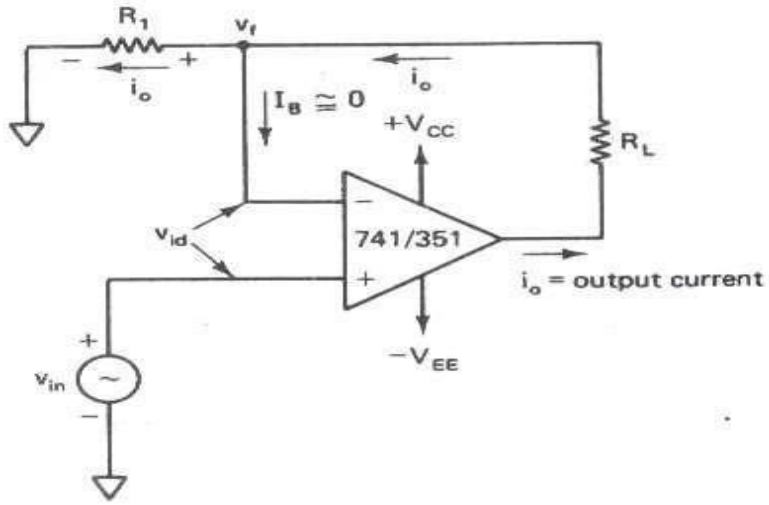
or

$$V_o = \left(1 + \frac{2R_F}{R_1}\right) V_{\text{in}}$$

This means that the differential input and output are in phase or of the same polarity provided that $V_{\text{in}} = V_x - V_y$ and $V_o = V_{ox} - V_{oy}$.

VOLTAGE-TO-CURRENT CONVERTER WITH FLOATING LOAD

Figure shows a voltage-to-current converter in which load resistor R_L is *floating* (not connected to ground). The input voltage is applied to the noninverting input terminal, and the feedback voltage across R_1 drives the inverting input terminal. This circuit is also called a *current-series negative feedback* amplifier because the feedback voltage across R_1 (applied to the inverting terminal) depends on the output current i_o and is in series with the input difference voltage v_{id}.



Writing Kirchhoff's voltage equation for the input loop,

$$v_{in} = v_{id} + v_f$$

But $v_{id} \cong 0$ V, since A is very large; therefore,

$$v_{in} = v_f$$

$$v_{in} = R_1 i_o$$

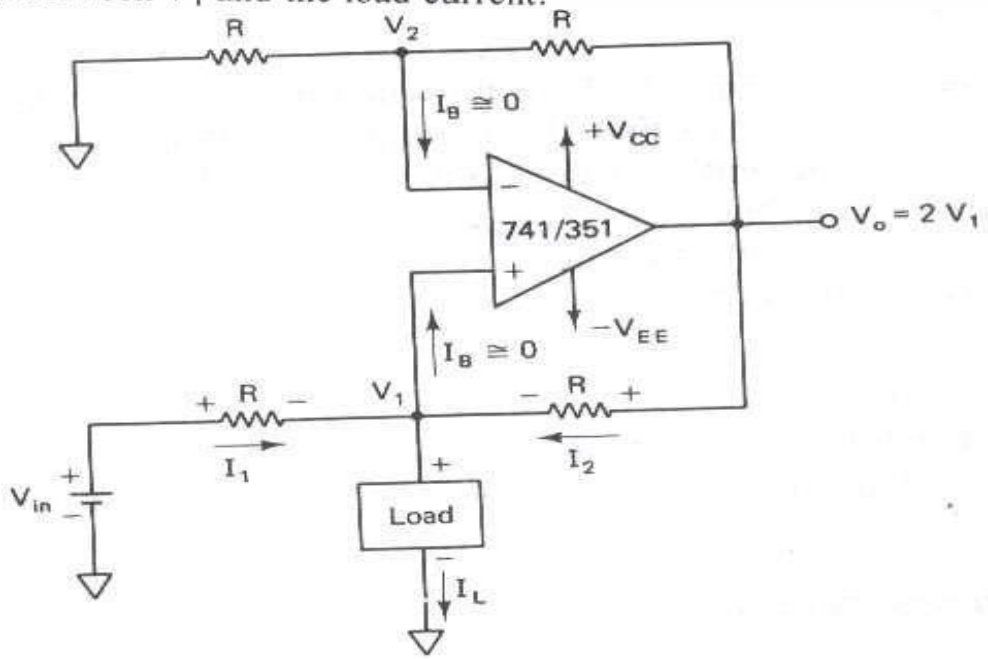
or

$$i_o = \frac{v_{in}}{R_1}$$

The voltage-to-current converter can be used in such applications as low-voltage dc and ac voltmeters, diode match finders, light-emitting diodes (LEDs), and zener diode testers.

VOLTAGE-TO-CURRENT CONVERTER WITH GROUNDED LOAD

The analysis of the circuit is accomplished by first determining the voltage V_1 at the noninverting input terminal and then establishing the relationship between V_1 and the load current.



Writing Kirchhoff's current equation at node V_1,

$$I_1 + I_2 = I_L$$

$$\frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R} = I_L$$

$$V_{in} + V_o - 2V_1 = I_L R$$

Therefore,

$$V_1 = \frac{V_{in} + V_o - I_L R}{2}$$

Since the op-amp is connected in the noninverting mode, the gain of the circuit in Figure is $1 + R/R = 2$. Then the output voltage is

$$V_o = 2V_1$$

$$= V_{in} + V_o - I_L R$$

That is,

$$V_{in} = I_L R$$

or

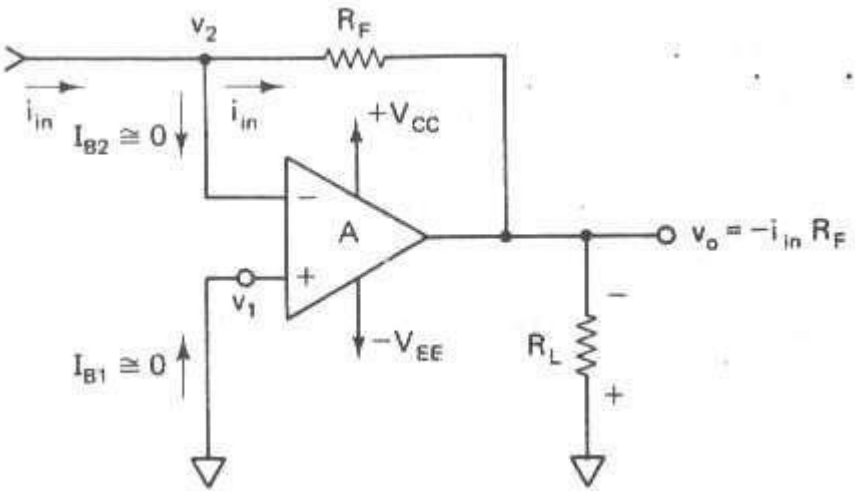
$$I_L = \frac{V_{in}}{R}$$

This means that the load current depends on the input voltage V_{in} and resistor R. Notice that all resistors must be equal in value.

The voltage-to-current converter of Figure 7-19 may also be used in testing such devices as zeners and LEDs forming a ground load. However, the circuit will perform satisfactorily provided that load size $\leq R$ value.

CURRENT-TO-VOLTAGE CONVERTER

the current-to-voltage (I-to-V) converter was presented as a special case of the inverting amplifier in which an input current is converted into a proportional output voltage. One of the most common uses of the current-to-voltage converter is in digital-to-analog circuits (DACs) and in sensing current through photodetectors such as photocells, photodiodes, and photovoltaic cells. Photosensitive devices produce a current that is proportional to an incident radiant energy or light and therefore can be used to detect the light.



Let us reconsider the ideal voltage-gain Equation of the inverting amplifier,

$$\frac{v_o}{v_{in}} = -\frac{R_F}{R_1}$$

Therefore,

$$v_o = -\left(\frac{v_{in}}{R_1}\right)R_F$$

However, since $v_1 = 0$ V and $v_1 = v_2$.

$$\frac{v_{in}}{R_1} = i_{in}$$

and

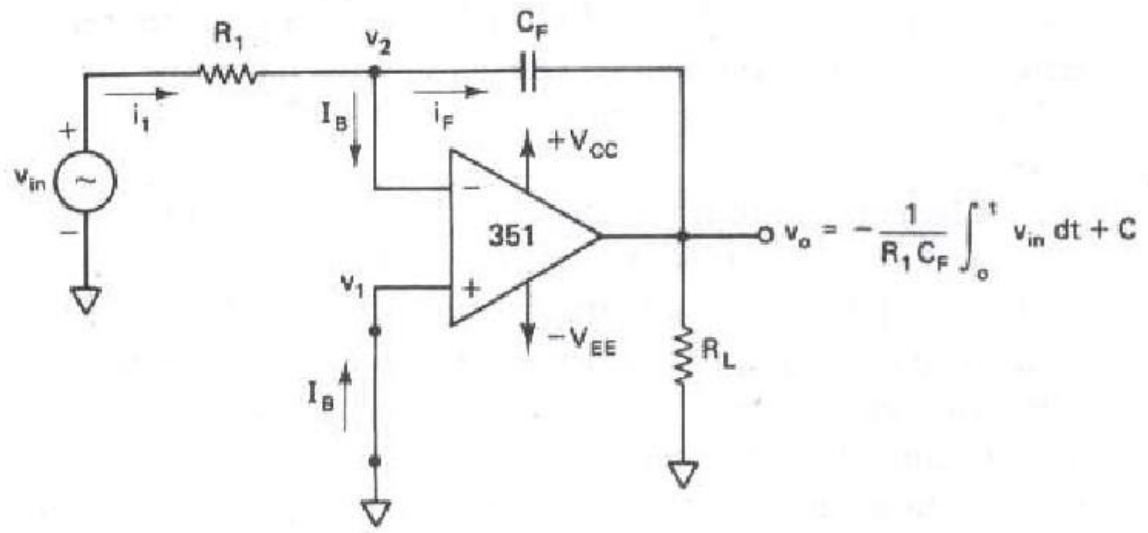
$$v_o = -i_{in}R_F$$

THE INTEGRATOR

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the *integrator* or the *integration amplifier*. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F

The expression for the output voltage v_o can be obtained by writing Kirchhoff's current equation at node v_2:

$$i_1 = I_B + i_F$$



Since I_B is negligibly small,

$$i_1 \cong i_F$$

Recall that the relationship between current through and voltage across the capacitor is

$$i_c = C \frac{dv_c}{dt}$$

Therefore,

$$\frac{v_{in} - v_2}{R_1} = C_F \left(\frac{d}{dt}\right)(v_2 - v_o)$$

However, $v_1 = v_2 \cong 0$ because A is very large. Therefore,

$$\frac{v_{in}}{R_1} = C_F \frac{d}{dt}(-v_o)$$

The output voltage can be obtained by integrating both sides with respect to time:

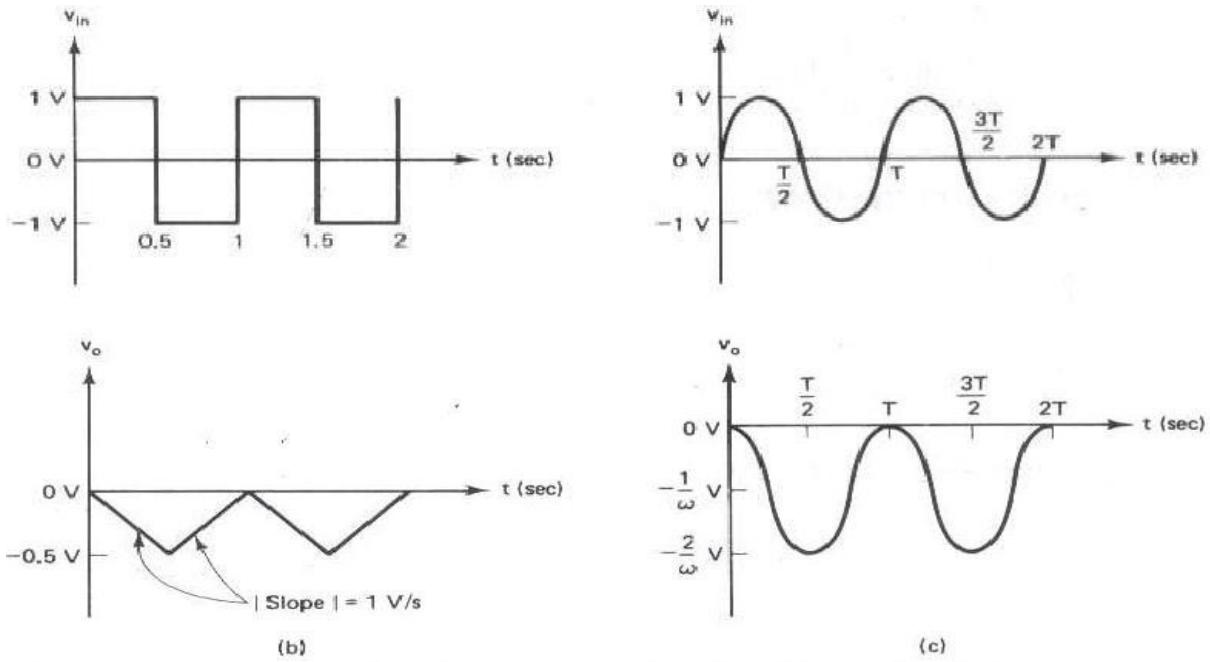
$$\int_0^t \frac{v_{in}}{R_1}\, dt = \int_0^t C_F \frac{d}{dt}(-v_o)\, dt$$

$$= C_F(-v_o) + v_o|_{t=0}$$

Therefore,

$$v_o = -\frac{1}{R_1 C_F} \int_0^t v_{in}\, dt + C$$

where C is the integration constant and is proportional to the value of the output voltage v_o at time $t = 0$ seconds.



(b) (c)

Figure (a) The integrator circuit. (b) and (c) Input and ideal output waveforms using a sine wave and square wave, respectively. $R_1C_F = 1$ second and $V_{ooT} = 0$ V assumed.

When $v_{in} = 0$, the integrator of Figure works as an open-loop amplifier. This is because the capacitor C_F acts as an open circuit ($X_{CF} = \infty$) to the input offset voltage V_{io}. In other words, the input offset voltage V_{io} and the part of the input current charging capacitor C_F produce the error voltage at the output of the integrator. Therefore, in the practical integrator shown in Figure , to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F. Thus, R_F limits the low-frequency gain and hence minimizes the variations in the output voltage.

The frequency response of the basic integrator is shown in Figure . In this figure, f_b is the frequency at which the gain is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

Both the stability and the low-frequency roll-off problems can be corrected by the addition of a resistor R_F as shown in the *practical integrator* of Figure The frequency response of the practical integrator is shown in Figure by a dashed line. In this figure, f is some relative operating frequency, and for frequencies f to f_a the gain R_F/R_1 is constant. However, after f_a the gain decreases at a rate of 20 dB/decade. In other words, between f_a and f_b the circuit of Figure acts as an integrator. The gain-limiting frequency f_a is given by

$$f_a = \frac{1}{2\pi R_F C_F}$$

Generally, the value of f_a and in turn R_1C_F and R_FC_F values should be selected such that $f_a < f_b$. For example, if $f_a = f_b/10$, then $R_F = 10R_1$.

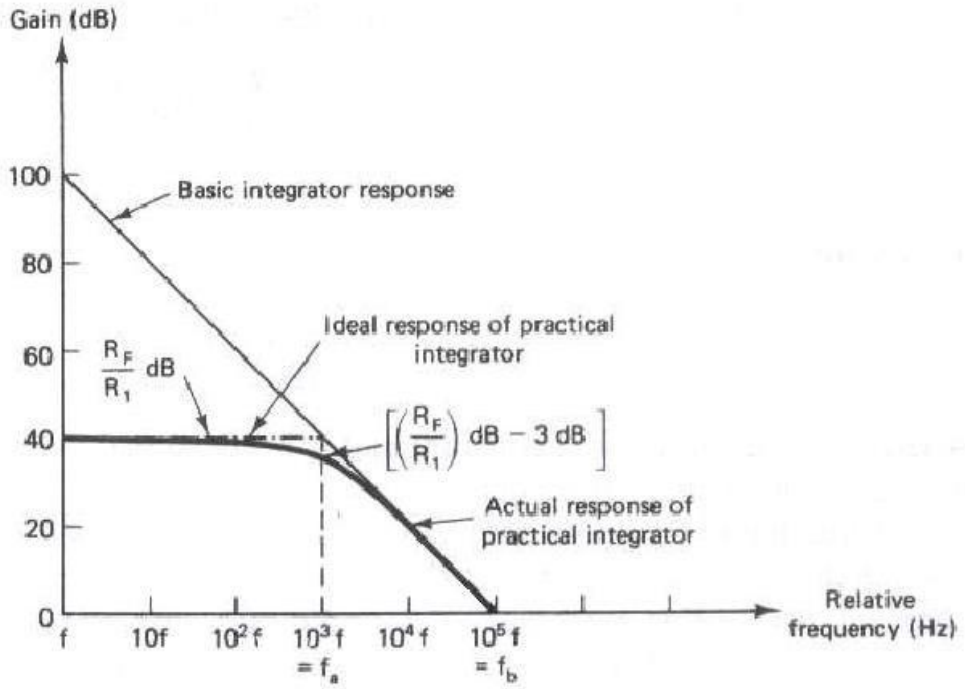


Figure Frequency response of basic and practical integrators. $f_a = 1/(2\pi R_FC_F)$ and $f_b = 1/(2\pi R_1C_F)$.

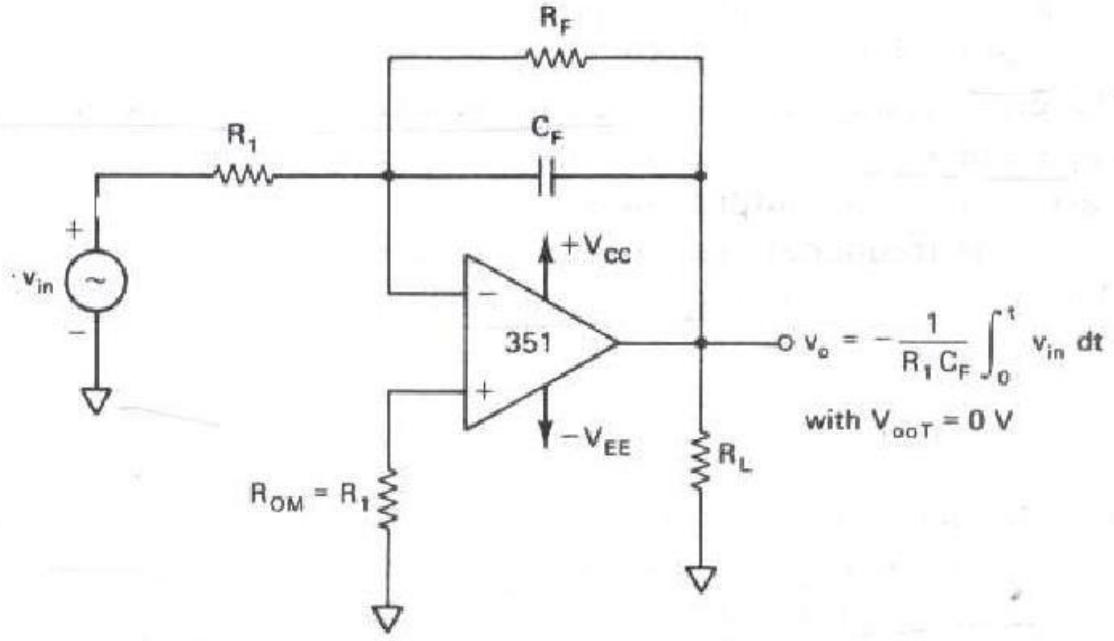


Figure Practical integrator.

input signal will be integrated properly if the time period T of the signal is larger than or equal to $R_F C_F$. That is,

$$T \geq R_F C_F$$

where

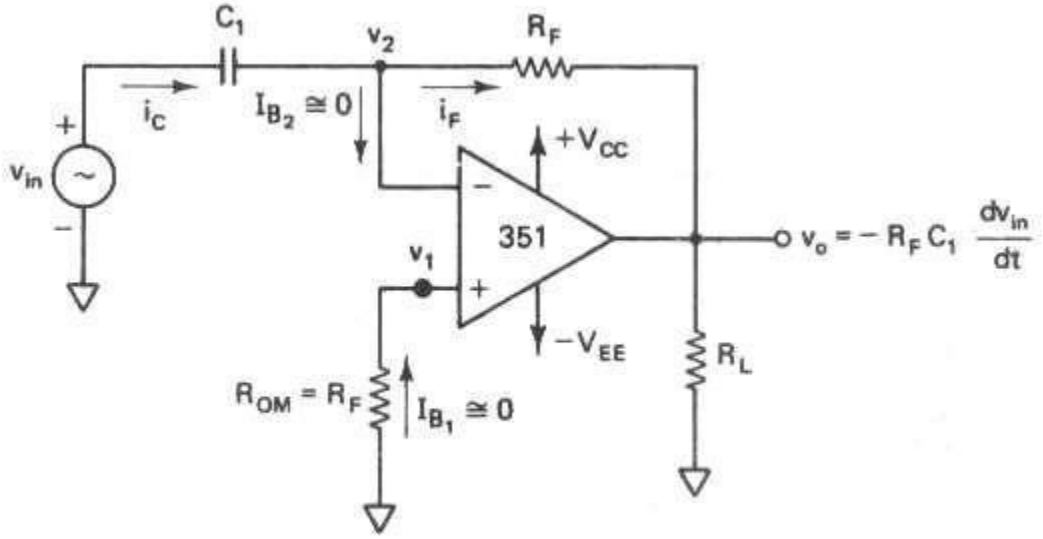
$$R_F C_F = \frac{1}{2\pi f_a}$$

THE DIFFERENTIATOR

Figure shows the *differentiator* or *differentiation amplifier*. As its name implies, the circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1.

The expression for the output voltage can be obtained from Kirchhoff's current equation written at node v_2 as follows:

$$i_C = i_B + i_F$$



(a)

Since $I_B \cong 0$,

$$i_C = i_F$$

$$C_1 \frac{d}{dt}(v_{in} - v_2) = \frac{v_2 - v_o}{R_F}$$

But $v_1 = v_2 \cong 0$ V, because A is very large. Therefore,

$$C_1 \frac{dv_{in}}{dt} = -\frac{v_o}{R_F}$$

or

$$v_o = -R_F C_1 \frac{dv_{in}}{dt}$$

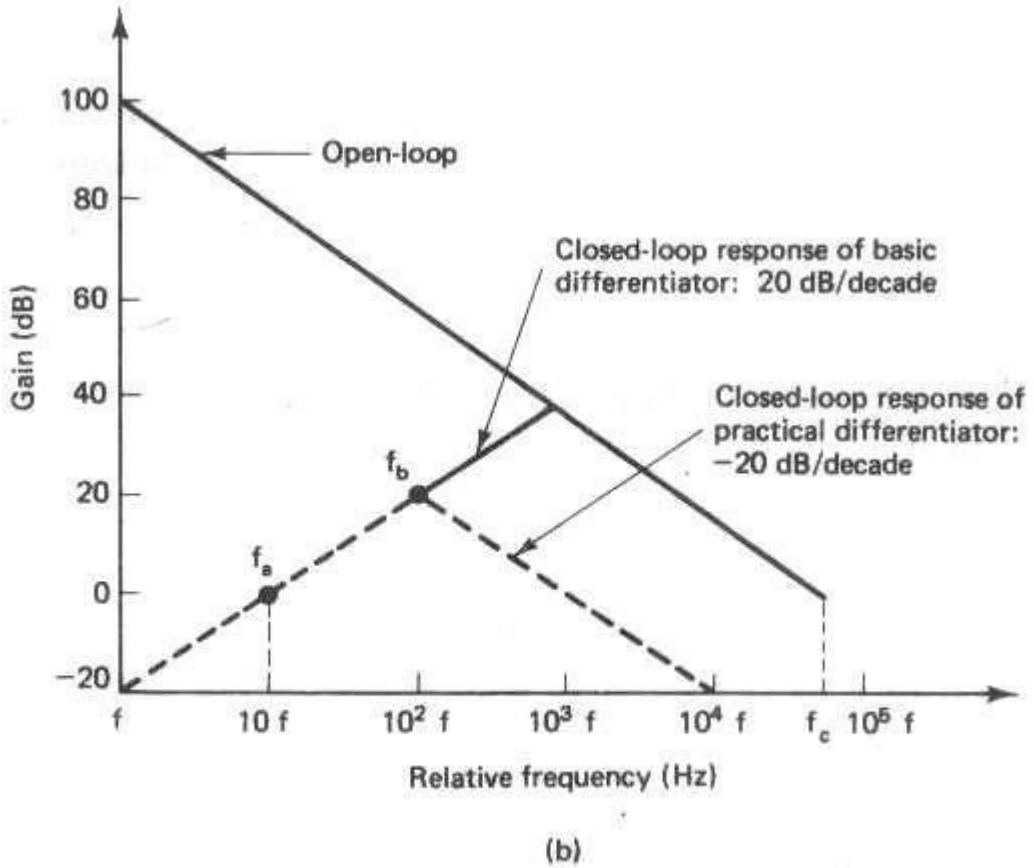
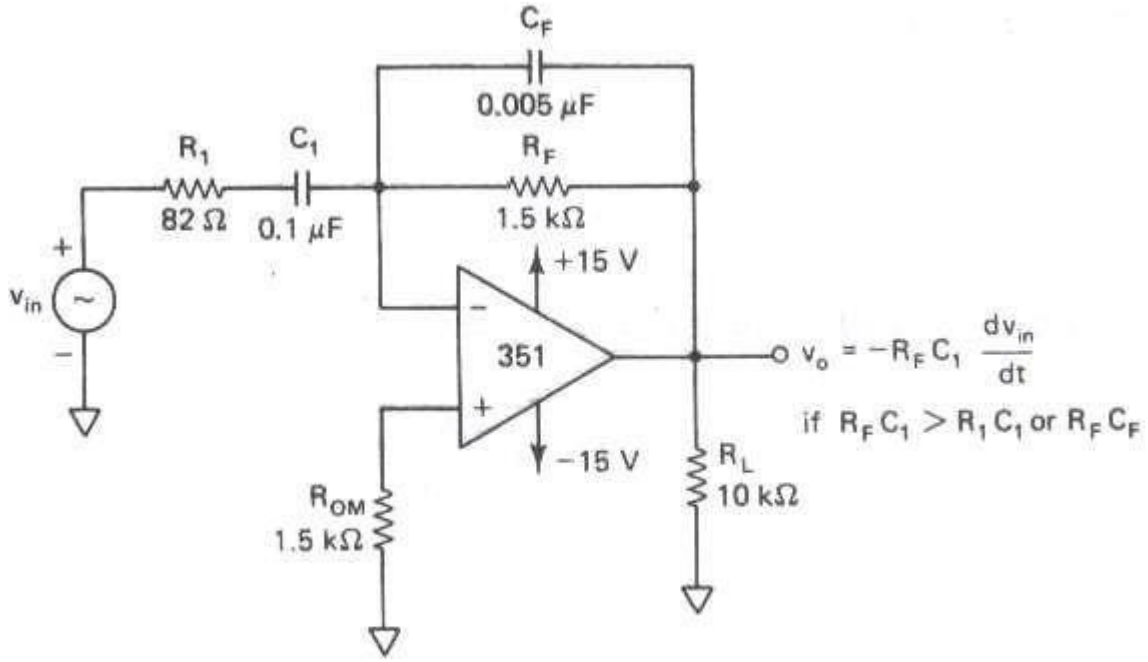


Figure Basic differentiator. (a) Circuit. (b) Frequency response.

The gain of the circuit (R_F/X_{C1}) increases with increase in frequency at a rate of 20 dB/decade. This makes the circuit unstable. Also, the input impedance X_{C1} decreases with increase in frequency, which makes the circuit very susceptible to high-frequency noise. When amplified, this noise can completely override the differentiated output signal. The frequency response of the basic differentiator is shown in Figure . In this figure, f_a is the frequency at which the gain is 0 dB and is given by

$$f_a = \frac{1}{2\pi R_F C_1}$$



(a)

Also, f_c is the unity gain–bandwidth of the op-amp, and f is some relative operating frequency.

Both the stability and the high-frequency noise problems can be corrected by the addition of two components: R_1 and C_F, as shown in Figure . This circuit is a *practical differentiator*, the frequency response of which is shown in Figure 7-27(b) by a dashed line. From frequency f to f_b, the gain increases at 20 dB/decade. However, after f_b the gain decreases at 20 dB/decade. This 40-dB/decade change in gain is caused by the R_1C_1 and R_FC_F combinations. The gain-limiting frequency f_b is given by

$$f_b = \frac{1}{2\pi R_1 C_1} \quad \text{where } R_1C_1 = R_FC_F.$$

turn R_1C_1 and R_FC_F values should be selected such that

$$f_a < f_b < f_c$$

$$f_a = \frac{1}{2\pi R_F C_1}$$

$$f_b = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_F C_F}$$

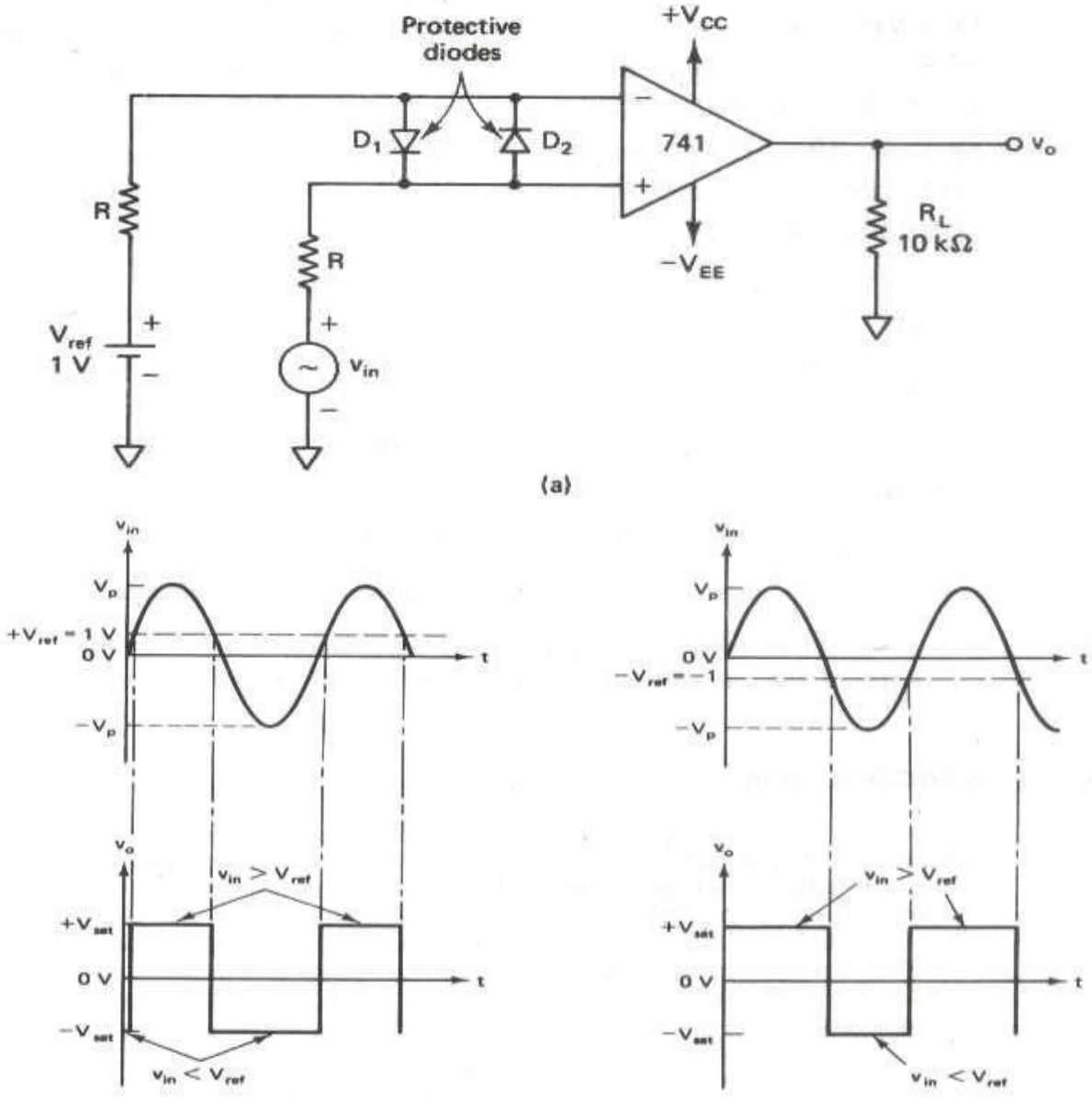
f_c = unity gain–bandwidth

The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_F C_1$. That is,

$$T \geq R_F C_1$$

BASIC COMPARATOR

Figure shows an op-amp used as a comparator. A fixed reference voltage V_{ref} of 1 V is applied to the (−) input, and the other time-varying signal voltage v_{in} is applied to the (+) input. Because of this arrangement, the circuit is called the *noninverting comparator.*



When v_{in} is less than V_{ref}, the output voltage v_o is at $-V_{sat}$ ($\cong -V_{EE}$) because the voltage at the (−) input is higher than that at the (+) input. On the other hand, when v_{in} is greater than V_{ref}, the (+) input becomes positive with respect to the (−) input, and v_o goes to $+V_{sat}$ ($\cong +V_{CC}$). Thus v_o changes from one saturation level to another whenever $v_{in} \cong V_{ref}$, as shown in Figure

ZERO-CROSSING DETECTOR

An immediate application of the comparator is the *zero-crossing detector* or *sine wave-to-square wave converter.*

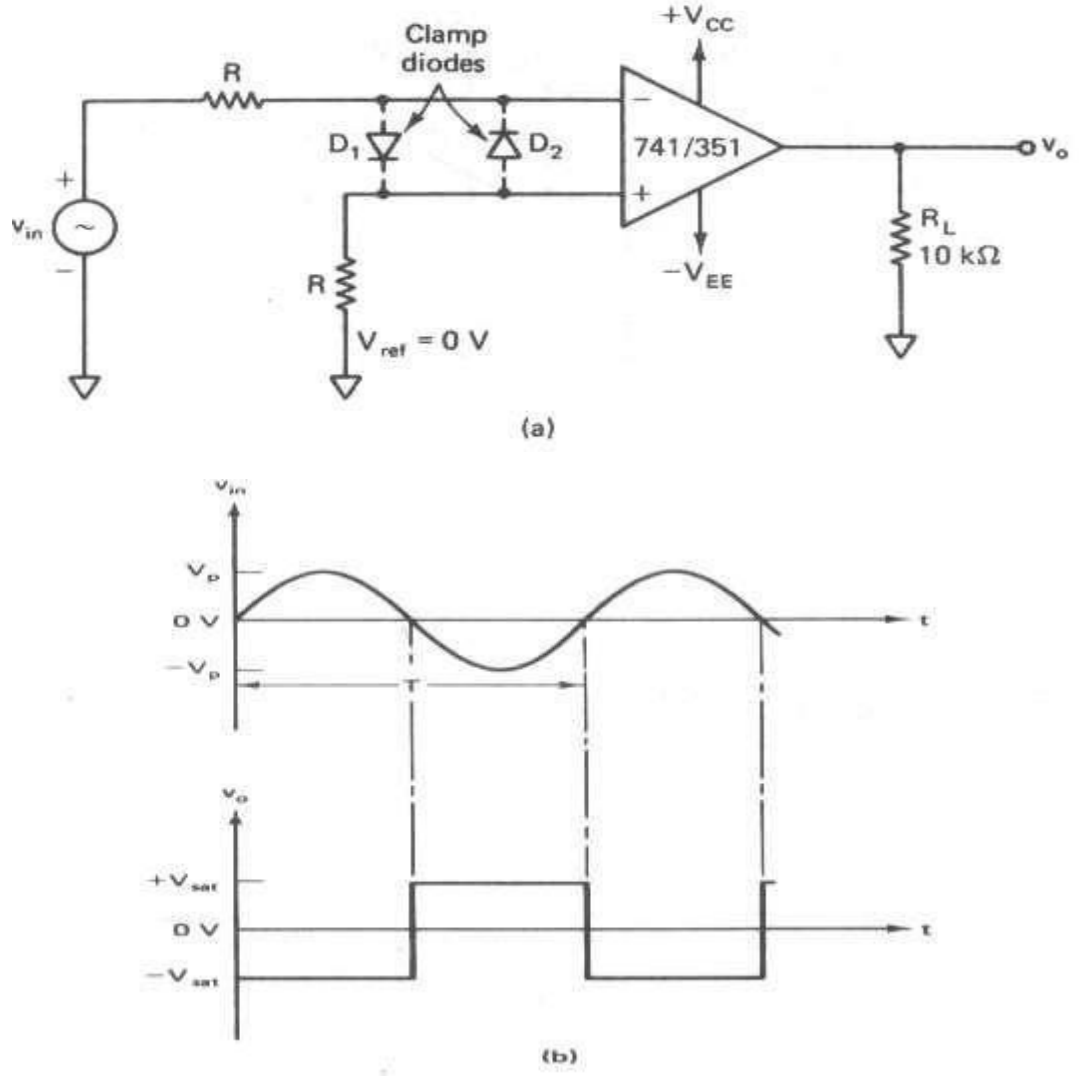
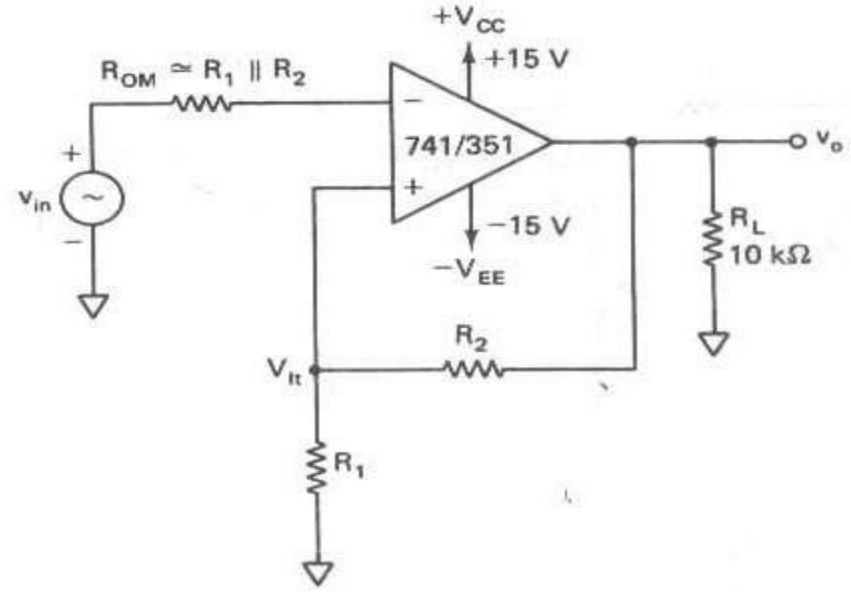


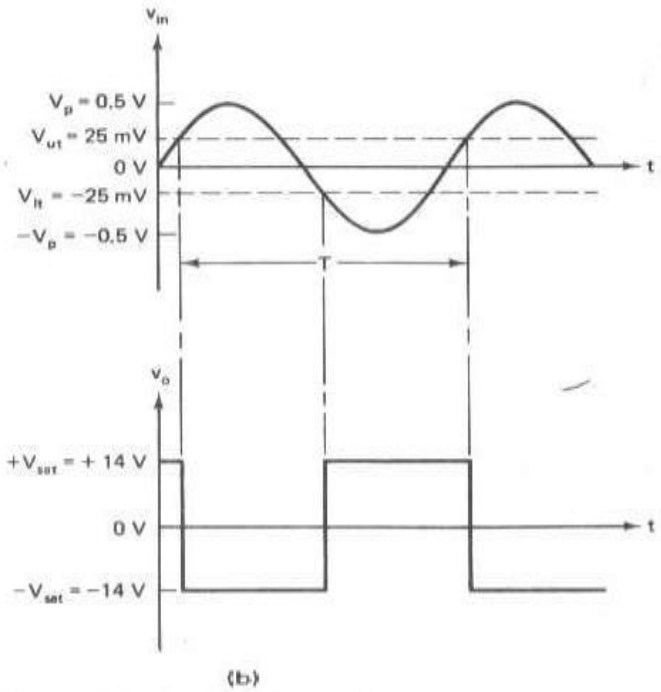
Figure 9–3 (a) Zero-crossing detector. (b) Its typical input and output waveforms.

SCHMITT TRIGGER

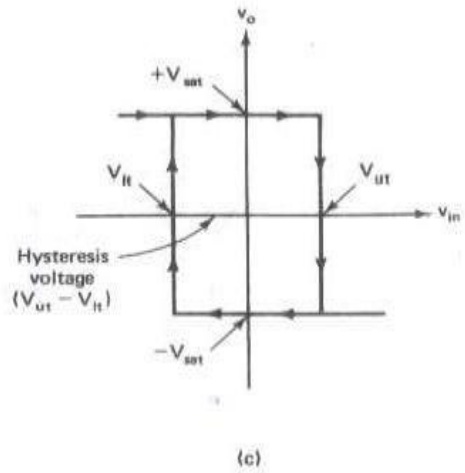
Figure shows an inverting comparator with *positive feedback*. This circuit converts an irregular-shaped waveform to a square wave or pulse. The circuit is known as the *Schmitt trigger* or squaring circuit. The input voltage v_{in} triggers



(a)



(b)



(c)

Figure 9–4 (a) Inverting comparator as Schmitt trigger. (b) Input and output waveforms of Schmitt trigger. (c) v_o versus v_{in} plot of the hysterisis voltage.

In Figure , these threshold voltages are obtained by using the voltage divider R_1–R_2, where the voltage across R_1 is fed back to the (+) input. The voltage across R_1 is a variable reference threshold voltage that depends on the value and polarity of the output voltage v_o. When $v_o = +V_{sat}$, the voltage across R_1 is called the *upper threshold voltage*, V_{ut}. The input voltage v_{in} must be slightly more positive than V_{ut} in order to cause the output v_o to switch from $+V_{sat}$ to $-V_{sat}$. As long as $v_{in} < V_{ut}$, v_o is at $+V_{sat}$. Using the voltage-divider rule,

$$V_{ut} = \frac{R_1}{R_1 + R_2}(+V_{sat})$$

On the other hand, when $v_o = -V_{sat}$, the voltage across R_1 is referred to as *lower threshold voltage*, V_{lt}. v_{in} must be slightly more negative than V_{lt} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$. In other words, for v_{in} values greater than V_{lt}, v_o is at $-V_{sat}$. V_{lt} is given by the following equation:

$$V_{lt} = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

Thus, if the threshold voltages V_{ut} and V_{lt} are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions. Also, the positive feedback, because of its regenerative action, will make v_o switch faster between $+V_{sat}$ and $-V_{sat}$. In Figure , resistance $R_{OM} \cong R_1 \| R_2$ is used to minimize the offset problems.

The comparator with positive feedback is said to exhibit *hysteresis*, a dead-band condition. That is, when the input of the comparator exceeds V_{ut}, its output switches from $+V_{sat}$ to $-V_{sat}$ and reverts back to its original state, $+V_{sat}$, when the input goes below V_{lt} . The hysteresis voltage is, of course, equal to the difference between V_{ut} and V_{lt}. Therefore,

$$V_{hy} = V_{ut} - V_{lt}$$

$$= \frac{R_1}{R_1 + R_2}[+V_{sat} - (-V_{at})]$$

SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

A simple op-amp square wave generator is shown in Fig. Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. In Fig. fraction $\beta = R_2/(R_1 + R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage V_{ref} is βv_o and may take values as

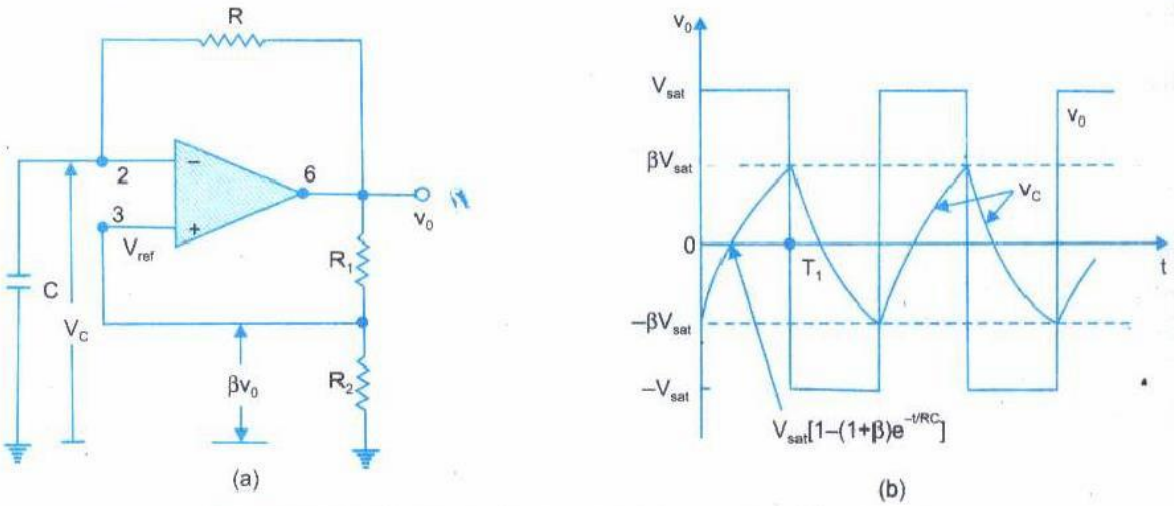


Fig. 5.10 (a) Simple op-amp square wave generator (b) waveforms

$+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also fed back to the (–) input terminal after integrating by means of a low-pass RC combination. Whenever input at the (–) input terminal just exceeds V_{ref}, switching takes place resulting in a square wave output. In astable multivibrator, both the states are quasi stable.

Consider an instant of time when the output is at $+V_{sat}$. The capacitor now starts charging towards $+V_{sat}$ through resistance R, as shown in Fig. The voltage at the (+) input terminal is held at $+\beta V_{sat}$ by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$, the reference voltage. When the voltage at the (–) input terminal becomes just greater than this reference voltage, the output is driven to $-V_{sat}$. At this instant, the voltage on the capacitor is $+\beta V_{sat}$. It begins to discharge through R, that is, charges toward $-V_{sat}$. When the output voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$. The output switches back to $+V_{sat}$. The cycle repeats itself as shown in Fig. 5.10 (b).

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa. The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC}$$

where, the final value, $V_f = +V_{sat}$

and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

or

$$v_c(t) = V_{sat} - V_{sat}\,(1 + \beta)\, e^{-t/RC}$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place, Therefore,

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/RC}$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1+\beta}{1-\beta}$$

This give only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta}$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$, it can be seen that $T = 2\ RC$

or

$$f_0 = \frac{1}{2RC}$$

The output swings from $+V_{sat}$ to $-V_{sat}$, so,

v_o peak-to-peak $= 2\ V_{sat}$

MONOSTABLE MULTIVIBRATOR

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The circuit shown in Fig. is a modified form of the astable multivibrator.

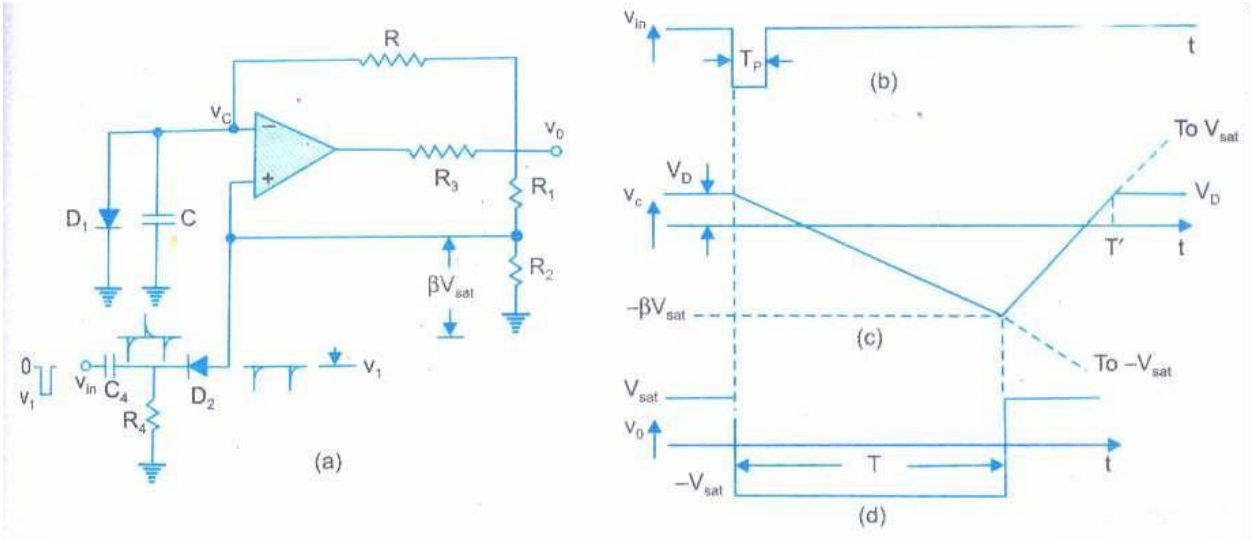


Fig. (a) Monostable multivibrator (b) negative going triggering signal (c) capacitor waveform (d) output voltage waveform

A diode D_1 clamps the capacitor voltage to 0.7V when the output is at $+V_{sat}$. A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative going triggering impulse and is applied to the (+) input terminal.

To analyse the circuit, let us assume that in the stable state, the output v_o is at $+V_{sat}$. The diode D_1 conducts and v_c the voltage across the capacitor C gets clamped to + 0.7V. The voltage at the (+) input terminal through R_1R_2 potentiometric divider is $+\beta V_{sat}$. Now, if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7V i.e. ($[\beta V_{sat} + (-V_1)] < 0.7$ V), the output of the op-amp will switch from $+V_{sat}$ to $-V_{sat}$. The diode will now get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$. When the capacitor voltage v_c becomes just slightly more negative than $-\beta V_{sat}$, the output of the op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until v_c is 0.7V as capacitor C gets clamped to the voltage. Various waveforms are shown in Fig. (b, c, d).

The pulse width T of monostable multivibrator is calculated as follows:

The general solution for a single time constant low pass RC circuit with V_i and V_f as initial and final values is,

$$v_o = V_f + (V_i - V_f)e^{-t/RC}$$

For the circuit, $V_f = -V_{sat}$ and $V_i = V_D$ (diode forward voltage).

The output v_c is,

$$v_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC}$$

at $t = T$,

$$v_c = -\beta V_{sat}$$

Therefore,

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

After simplification, pulse width T is obtained as

$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1 - \beta}$$

where $\beta = R_2/(R_1 + R_2)$

If, $V_{sat} >> V_D$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$T = 0.69\ RC$$

For monostable operation, the trigger pulse width T_p should be much less than T, the pulse width of the monostable multivibrator. The diode D_2 is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

Unit-3
ACTIVE FILTERS AND TIMERS

An electric filter is often a frequency-selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band. Filters may be classified in a number of ways:

1. **Analog or digital**
2. **Passive or active**
3. **Audio (AF) or radio frequency (RF)**

Analog filters are designed to process analog signals, while digital filters process analog signals using digital techniques. Depending on the type of elements used in their construction, filters may be classified as passive or active.

Elements used in passive filters are resistors, capacitors, and inductors. Active filters, on the other hand, employ transistors or op-amps in addition to the resistors and capacitors. The type of element used dictates the operating frequency range of the filter.

For example, RC filters are commonly used for audio or low- frequency operation, whereas LC or crystal filters are employed at RF or high –frequencies. Especially because of their high Q value (figure of merit), the crystal provide more stable operation at higher frequencies.

An active filter offers the following advantages over a passive filter:

1. Gain and frequency adjustment flexibility. Since the op-amp is capable of providing a gain, the input signal is not attenuated as it is in a passive filter. In addition, the active filter is easier to tune or adjust.
2. No loading prob1em. Because of the high input resistance and low output resistance of the op-amp, the active filter does not cause loading of the source or load.
3. Cost. Typically, active filters are more economical than passive filters. This is because of the variety of cheaper op-amps and the absence of inductors.

The most commonly used filters are these:

1. Low-pass filter
2. High-pass filter
3. Band-pass filter
4. Band-reject filter
5. All-pass filter

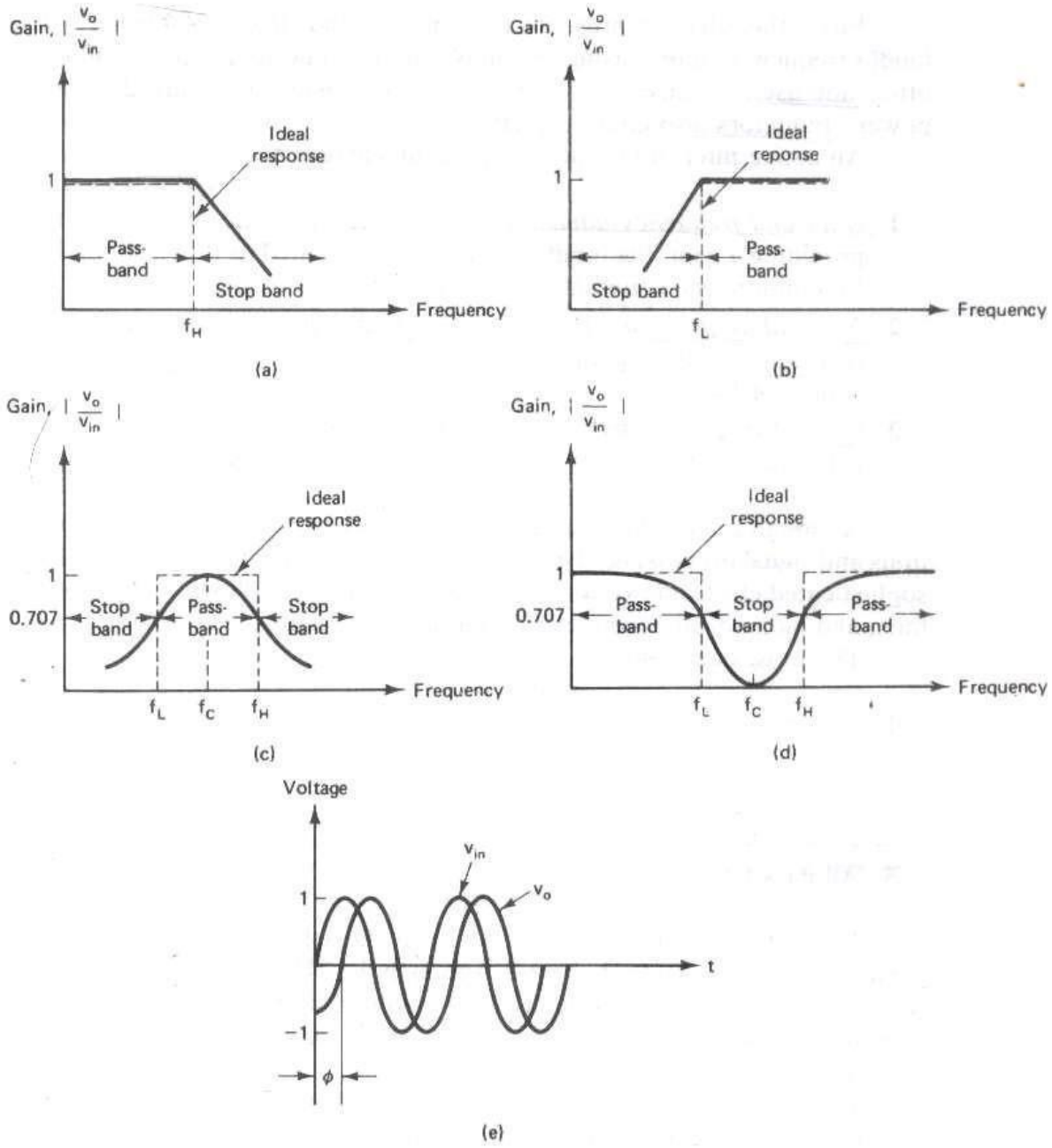


Figure 8–1 Frequency response of the major active filters. (a) Low pass. (b) High pass. (c) Band pass. (d) Band reject. (e) Phase shift between input and output voltages of an all-pass filter.

Fig. 8-1 shows the frequency response characteristics of the five types of filters. The ideal response is shown by dashed curves, while the solid lines indicate the practical filter response. A low-pass filter has a constant gain from 0 Hz to a high cutoff frequency f_H. Therefore, the bandwidth is also f_H.

At f_H the gain is down by 3 dB; after that ($f > f_H$) it decreases with the increase in input frequency. The frequencies between 0 Hz and f_H are known as the passband frequencies, whereas the range of frequencies, those beyond f_H that are attenuated includes the stopband frequencies.

Fig. 8-1(a) shows the frequency response of the low-pass filter. As indicated by the dashed line, an ideal filter has a zero loss in its passband and infinite loss in its stopband. Unfortunately, ideal filter response is not practical because linear networks cannot produce the discontinuities. However, it is possible to obtain a practical response that approximates the ideal response by using special design techniques, as well as precision component values and high-speed op-amps.

Butterworth, Chebyshev, and Cauer filters are some of the most commonly used practical filters that approximate the ideal response. The key characteristic of the Butterworth filter is that it has a flat passband as well as stopband. For this reason, it is sometimes called a flat-flat filter.

The Chebyshev filter has a ripple passband and flat stopband, i.e. the Cauer filter has a ripple passband and a ripple stopband. Generally, the Cauer filter gives the best stopband response among the three. Because of their simplicity of design, the low-pass and high-pass Butterworth filters are discussed here.

Figure 8-1(b) shows a high-pass filter with a stopband $0 < f < f_L$ and a passband $f > f_L$. f_L is the low cutoff frequency, and f is the operating frequency. A band-pass filter has a passband between two cutoff frequencies f_H and f_L, where $f_H > f_L$ and two stop-bands: $0 < f < f_L$ and $f > f_H$. The bandwidth of the band- pass filter, therefore, is equal to $f_H - f_L$. The band-reject filter performs exactly opposite to the band-pass; that is, it has a band-stop between two cutoff frequencies f_H and f_L and two passbands: $0 < f < f_L$ and $f > f_H$. The band-reject is also called a band-stop or band-elimination filter. The frequency responses of band- pass and band-reject filters are shown in Figure 8-1(c) and (d), respectively. In these figures, f_C is called the center frequency since it is approximately at the center of the passband or stopband.

Fig. 8.1(e) sows the phase shift between input and output voltages of an all-pass filter. This filter passes all frequencies equally well; that is, output and input voltages equal in amplitude for all frequencies, with the phase shift between the two a function of frequency. The highest frequency up to which the input and output amplitudes remain equal is dependent on the unity gain bandwidth of the op-amp. (At this frequency, however, the phase shift between the input and output is maximum.

The rate at which the gain of the filter changes in the stopband is determined by the order of the filter. For example, for the first order low-pass filter the gain-rolls-off at the rate of 20 dB/decade in the stopband, that is, for $f>f_{H;}$ on the other hand, for the second-order low-pass filter the roll-off rate is 40 dB/decade and so on. By contrast, for the first-order high-pass filter the gain increases at the rate of 20 dB/decade in the stopband, that is, until $f=f_L$; the increase is 40dB/decade for the second-order high-pass filter;

FIRST-ORDER LOW-PASS BUTTER WORTH FILTER

Fig. 8-2 shows a first-order low-pass Butterworth filter that uses an RC network for filtering. Note that the op-amp is used in the non-inverting configuration; hence it does not load down the RC network. Resistors R1 and RF determine the gain of the filter.

According to the voltage-divider rule, the voltage at the non-inverting terminal (across capacitor C) is

$$v_1 = \frac{-jX_C}{R - jX_C} v_{in}$$

$$j = \sqrt{-1} \quad \text{and} \quad -jX_C = \frac{1}{j2\pi fC}$$

$$v_1 = \frac{v_{in}}{1 + j2\pi fRC}$$

$$v_o = \left(1 + \frac{R_F}{R_1}\right) v_1$$

$$v_o = \left(1 + \frac{R_F}{R_1}\right) \frac{v_{in}}{1 + j2\pi fRC}$$

$$\frac{v_o}{v_{in}} = \frac{A_F}{1 + j(f/f_H)}$$

where $\frac{v_o}{v_{in}}$ = gain of the filter as a function of frequency

$A_F = 1 + \frac{R_F}{R_1}$ = passband gain of the filter

f = frequency of the input signal

$f_H = \frac{1}{2\pi RC}$ = high cutoff frequency of the filter

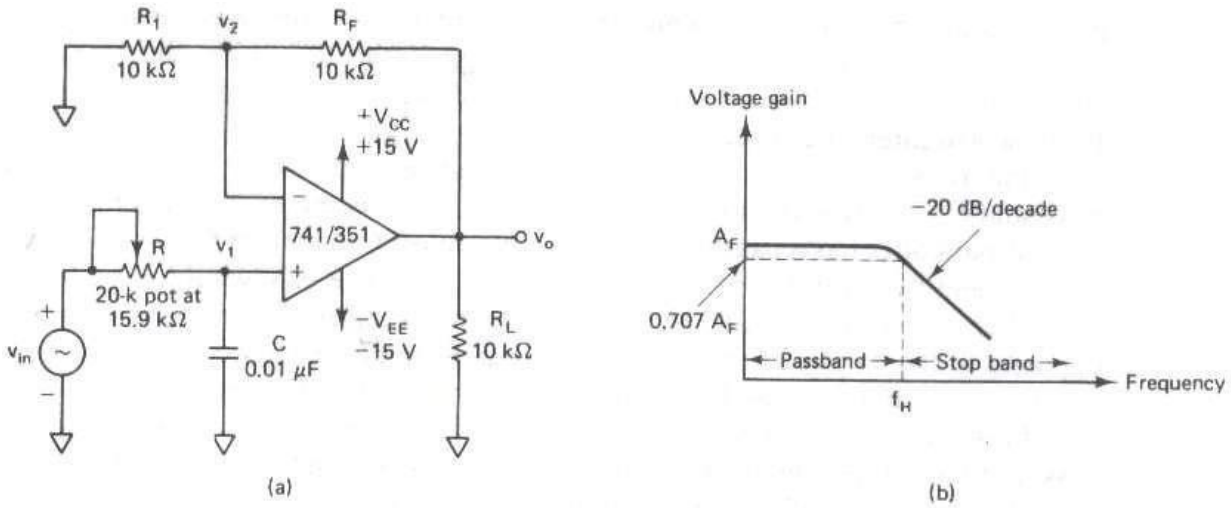


Figure 8–2 First-order low-pass Butterworth filter. (a) Circuit. (b) Frequency response.

The gain magnitude and phase angle equations of the low-pass filter can be obtained by converting Equation (1) into its equivalent polar form, as follows:

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}$$

$$\phi = -\tan^{-1}\left(\frac{f}{f_H}\right)$$

Where φ is the phase angle in degrees.

The operation of the low-pass filter can be verified from the gain magnitude equation, (2):

1. At very low frequencies, that is, $f < f_H$, $\left|\frac{v_o}{v_{in}}\right| \cong A_F$
2. At $f = f_H$, $\left|\frac{v_o}{v_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707A_F$
3. At $f > f_H$, $\left|\frac{v_o}{v_{in}}\right| < A_F$

Filter Design

A low-pass filter can be designed by implementing the foI1owng steps:

1. Choose a value of high cutoff frequency f_H.
2. Select a value of C less than or equal to 1 µF. Mylar or tantalum capacitors are recommended for better performance.
3. Calculate the value of R using

$$R = \frac{1}{2\pi f_H C}$$

4. Finally, select values of R1 and R_F dependent on the desired passband gain A_F using

$$A_F = 1 + \frac{R_F}{R_1}$$

Frequency Scaling

Once a filter designed; there may sometimes be a need to change its cutoff frequency. The procedure used to convert an original cutoff frequency f_H to a new cutoff frequency f'_H is called frequency scaling. Frequency scaling is accomplished as follows. To change a high cutoff frequency, multiple R or C. but not both, by the ratio of the original cutoff frequency to the new cutoff frequency.

SECOND-ORDER LOW-PASS BUTTER WORTH FILTER

A stop-band response having a 40-dB/decade roll-off is obtained with the second order low-pass filter. A first-order low-pass filter can be converted into a second order type simply by using an additional RC network, as shown in Fig. 8-4.

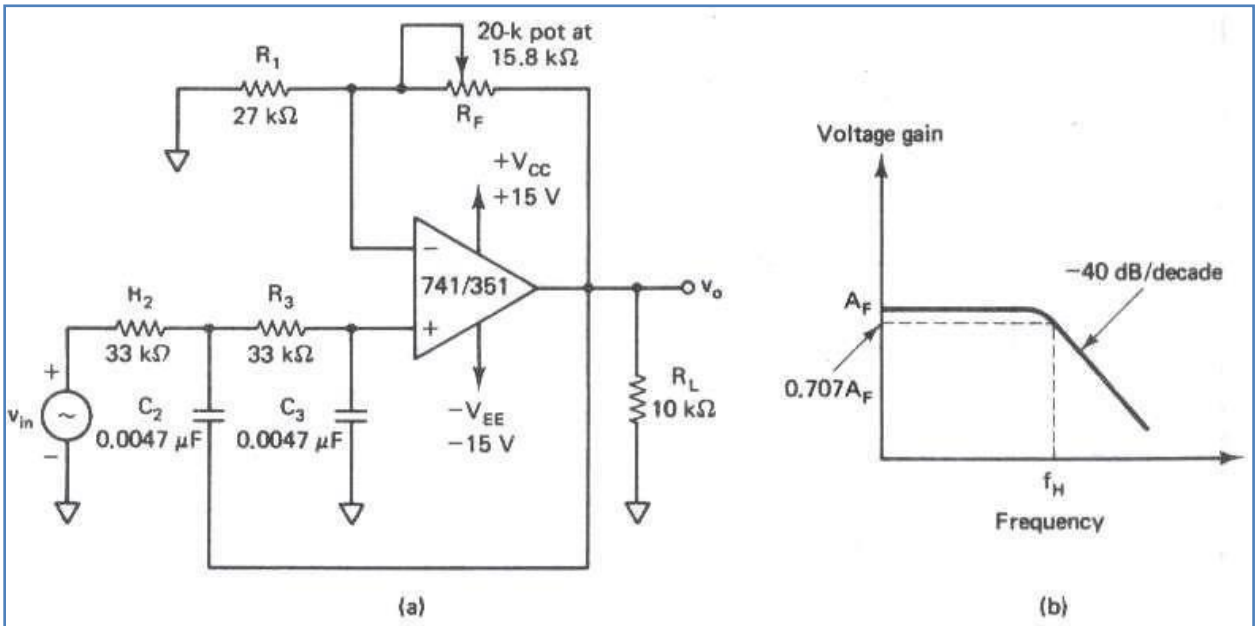


Figure 8–4 Second-order low-pass Butterworth filter. (a) Circuit. (b) Frequency response.

Second-order filters are important because higher-order filters can be designed using them. The gain of the second-order filter is set by R1 and R_F, while the high cutoff frequency f_H is determined by R2, C2, R3, and C3, as follows:

$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

Furthermore, for a second-order low-pass Butterworth response, the voltage gain magnitude equation is

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^4}}$$

where $A_F = 1 + \dfrac{R_F}{R_1}$ = passband gain of the filter

f = frequency of the input signal (Hz)

$f_H = \dfrac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$ = high cutoff frequency (Hz)

FIRST-ORDER HIGH-PASS BUITERWORTH FILTER

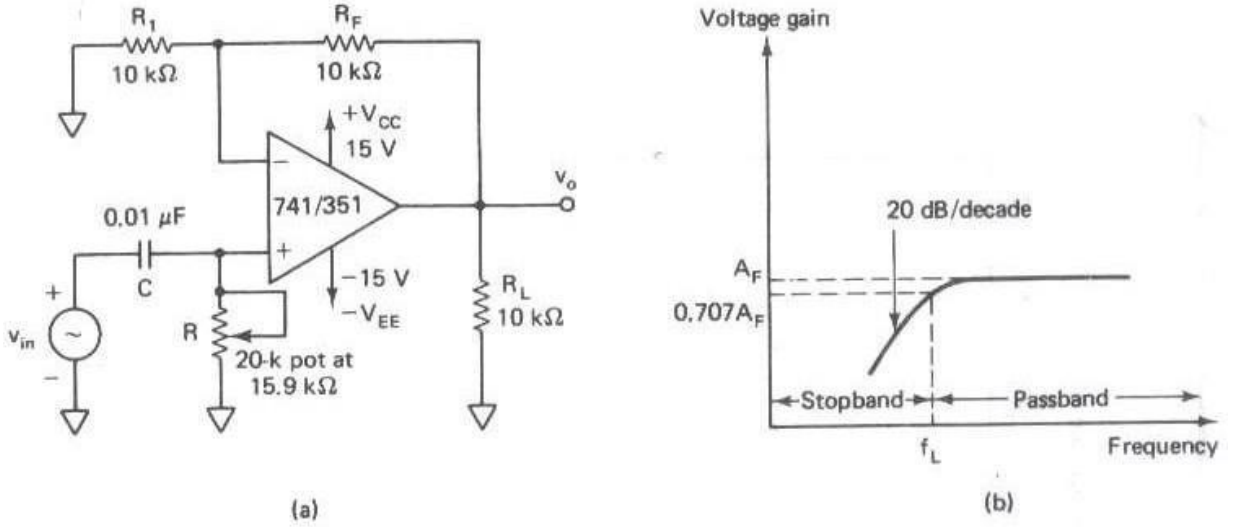


Figure 8–6 (a) First-order high-pass Butterworth filter. (b) Its frequency response.

High-pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters. That is, a first-order high-pass filter is formed from a first-order low-pass type by interchanging components R and C.

Similarly, a second-order high-pass filter is obtained from a second-order low-pass filter if R and C are interchanged, and so on. Figure 8-6 shows a first-order high- pass Butterworth filter with a low cutoff frequency of f_L.

This is the frequency at which the magnitude of the gain is 0.707 times its passband value. Obviously, all frequencies higher than f_L are passband frequencies, with the highest frequency determined by the closed-loop bandwidth of the op-amp.

Note that the high-pass filter of Figure 8-6(a) and the low-pass filter of Figure 8-2(a) are the same circuits, except that the frequency-determining components (R and C) are interchanged.

For the first-order high-pass filter of Figure 8-6(a), the output voltage is

$$v_o = \left(1 + \frac{R_F}{R_1}\right) \frac{j2\pi fRC}{1 + j2\pi fRC} v_{in}$$

$$\frac{v_o}{v_{in}} = A_F \left[\frac{j(f/f_L)}{1 + j(f/f_L)} \right]$$

where $A_F = 1 + \frac{R_F}{R_1}$ = passband gain of the filter

f = frequency of the input signal (Hz)

$f_L = \frac{1}{2\pi RC}$ = low cutoff frequency (Hz)

Hence the magnitude of the voltage gain is

$$\left| \frac{v_o}{v_{in}} \right| = \frac{A_F(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

Since high-pass filters are formed from low-pass filters simply by interchanging R's and *C's,* the design and frequency scaling procedures of the low-pass filters are also applicable to the high- pass filters.

SECOND-ORDER HIGH-PASS BUTTERWORTH FILTER

As in the case of the first-order filter, a second-order high-pass filter can be formed from a second-order low-pass filter simply by interchanging the frequency-determining resistors and capacitors. Figure 8-8(a) shows the second-order high-pass filter.

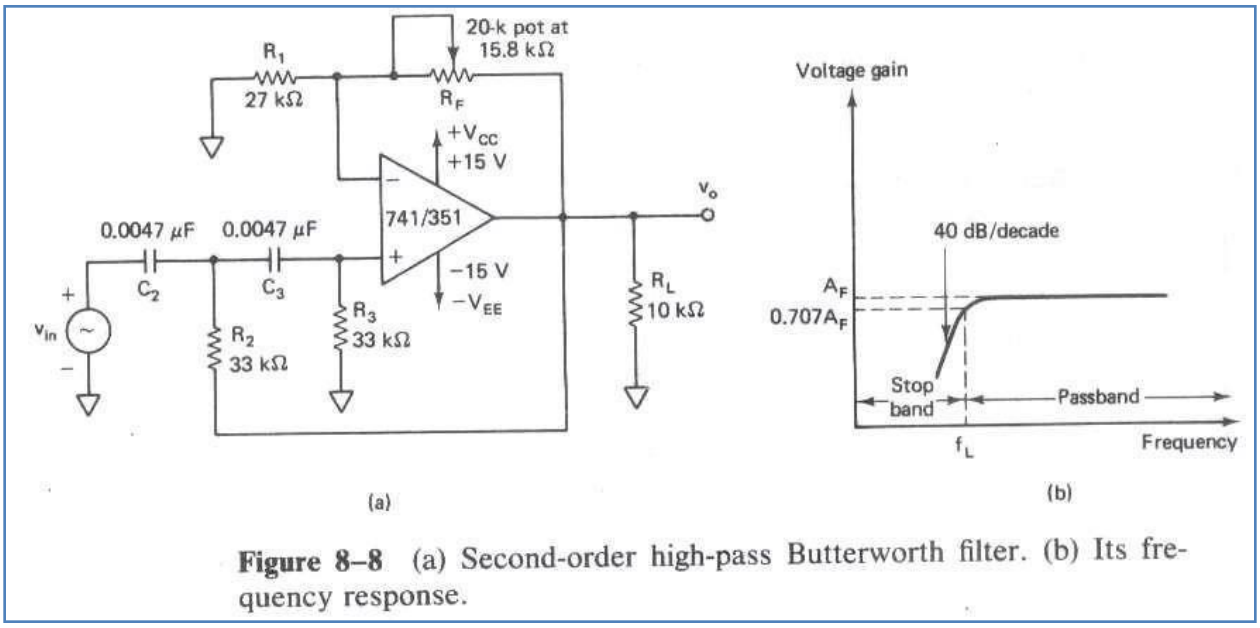


Figure 8–8 (a) Second-order high-pass Butterworth filter. (b) Its frequency response.

The voltage gain magnitude equation of the second-order high-pass filter is as follows:

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_F}{\sqrt{1 + (f_L/f)^4}}$$

Where $A_F = 1.586$ = passband gain for the second-order Butterworth response
f = frequency of the input signal (Hz)
f_L = low cutoff frequency (Hz)

Since second-order low-pass and high-pass filters are the same circuits except that the positions of resistors and capacitors are interchanged, the design and frequency scaling procedures for the high-pass filter are the same as those for the low-pass filter.

BAND-PASS FILTERS

A band-pass filter has a passband between two cutoff frequencies f_H and f_L such that $f_H > f_L$.
Any input frequency outside this passband is attenuated.
Basically, there are two types of band-pass filters:
(1) Wide band pass, and
(2) Narrow band pass.
Unfortunately, there is no set dividing line between the two. However, we will define a filter as wide band pass if its figure of merit or quality factor Q<10.On the other hand, if we will call the filter a narrow band-pass filter. Thus Q is a measure of selectivity, meaning the higher the value Q, the more selective is the filter or the narrower its bandwidth (BW). The relationship between Q, the 3-dB bandwidth, and the center frequency fc is given by

$$Q = \frac{f_C}{\text{BW}} = \frac{f_C}{f_H - f_L}$$

For the wide band-pass filter the center frequency fc can be defined as

$$f_C = \sqrt{f_H f_L}$$

where f_H = high cutoff frequency (Hz)
f_L = low cutoff frequency of the wide band-pass filter (Hz)
In a narrow band-pass filter, the output voltage peaks at the center frequency.

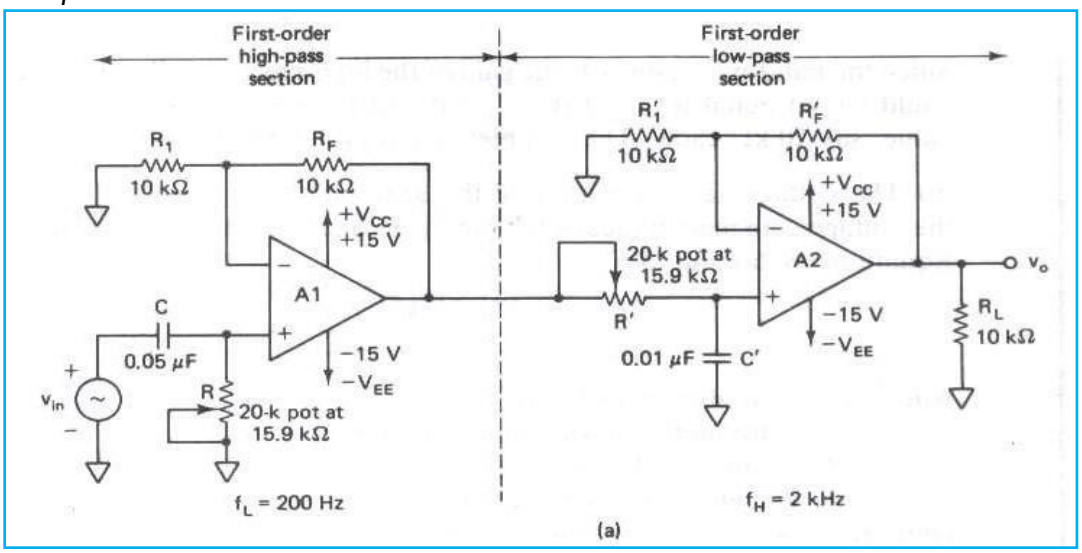
Wide band-pass filter

A wide band-pass filter can be formed by simply cascading high-pass and low-pass sections and is generally the choice for simplicity of design and performance.

To obtain ±20dB/decade band-pass, first-order high pass and first order low-pass sections are cascaded; for a ±40-dB/decade band-pass filter, second-order high- pass and second-order low-pass sections are connected in series.

The order of the band-pass filter depends on the order of the high- pass and low-pass filter sections.

Figure 8-11 shows the ±20-dB/decade wide band-pass filter, which is composed of first-order high-pass and first-order low-pass filters. To realize a band- pass response, however, f_H must be larger than f_L.



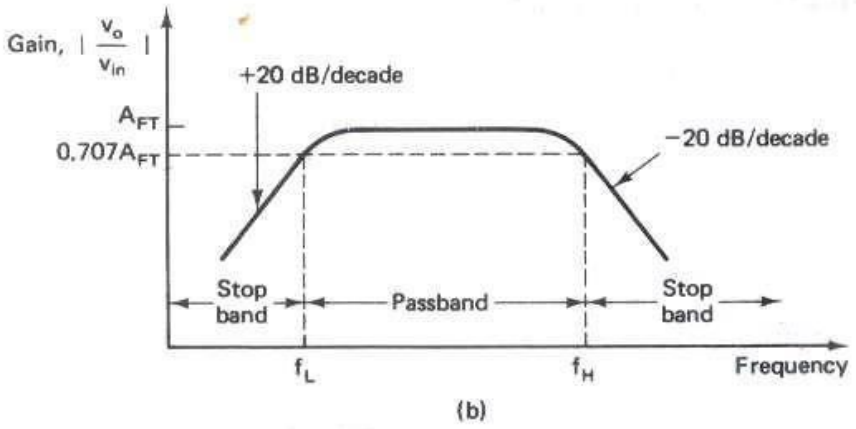


Figure 8–11 (a) ±20 dB/decade-wide band-pass filter. (b) Its frequency response. A_1 and A_2 dual op-amp: 1458/353.

Since the band-pass gain is 4, the gain of the high-pass as well as low-pass sections could be set equal to 2. That is, input and feedback resistors must be equal in value, say 10 kΩ each. The complete band-pass filter is shown in Figure 8-11(a).

(b) The voltage gain magnitude of the band-pass filter is equal to the product of the voltage gain magnitudes of the high-pass and low-pass filters. Therefore, from Equations (8-2a) and (8-6),

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}} \qquad \left|\frac{v_o}{v_{in}}\right| = \frac{A_F(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_{FT}(f/f_L)}{\sqrt{[1 + (f/f_L)^2][1 + (f/f_H)^2]}}$$

where A_{FT} = total passband gain
f = frequency of the input signal (Hz)
f_L = low cutoff frequency (Hz)
f_H = high cutoff frequency (Hz)

Narrow Band-Pass Filter

The narrow band-pass filter using multiple feedback is shown in Figure 8-13. As shown in this figure, the filter uses only one op-amp. Compared to all the filters discussed so far, this filter is unique in the following respects:

1. It has two feedback paths, hence the name multiple-feedback filter.
2. The op-amp is used in the inverting mode. :

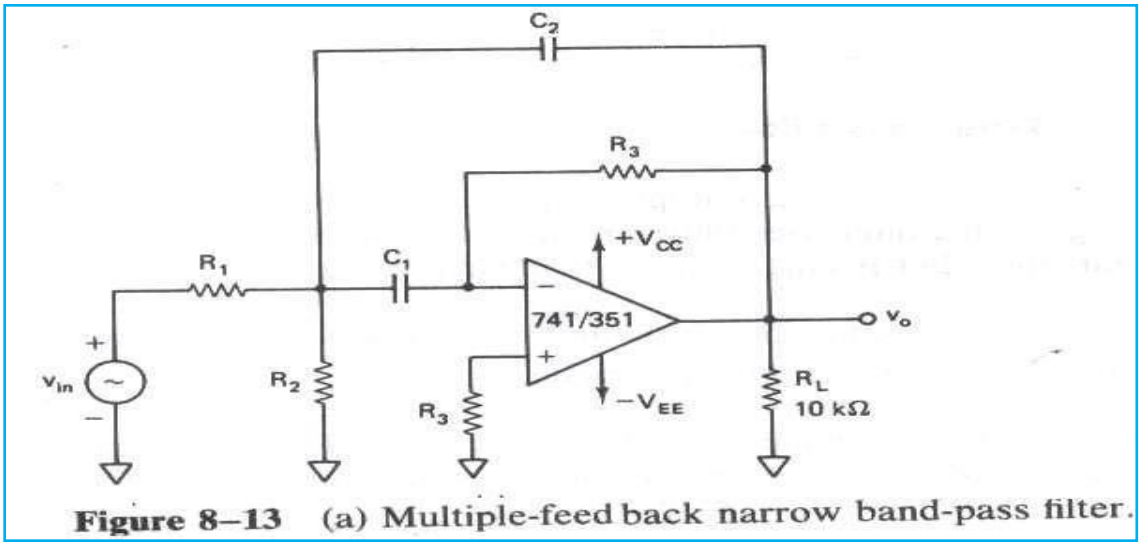


Figure 8–13 (a) Multiple-feed back narrow band-pass filter.

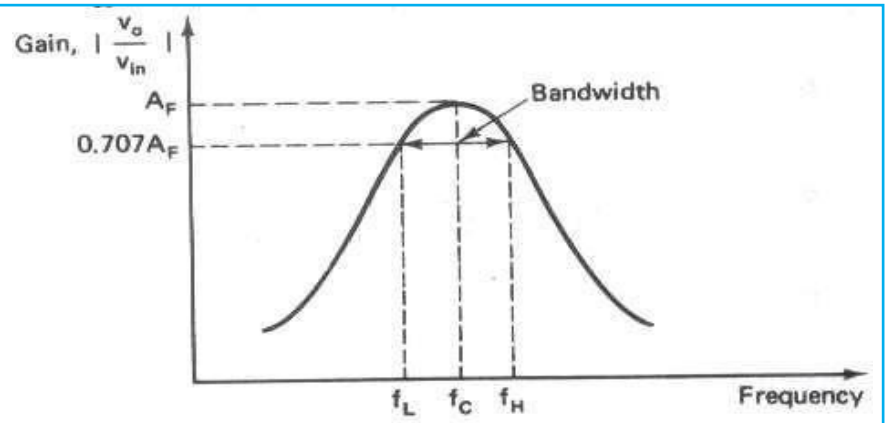


Figure 8–13 (b) Its frequency response.

Generally, the narrow band-pass filter is designed for specific values of center frequency *fc* and Q or *fc* and bandwidth. The circuit components are determined from the following relationships. To simplify the design calculations, choose C1 = C2 = C.

$$R_1 = \frac{Q}{2\pi f_C C A_F} \qquad R_2 = \frac{Q}{2\pi f_C C(2Q^2 - A_F)} \qquad R_3 = \frac{Q}{\pi f_C C}$$

Where A_F is the gain at *fc* , given by

$$A_F = \frac{R_3}{2R_1}$$

The gain A_F, however, must satisfy the condition

$$A_F < 2Q^2$$

Another advantage of the multiple feedback filter of Figure 8-13 is that its center frequency *fc* can be changed to a new frequency *f'c* without changing the gain or bandwidth. This is accomplished simply by changing R_2 to R'_2 so that

$$R'_2 = R_2 \left(\frac{f_C}{f'_C}\right)^2$$

BA ND-REJECT FILTERS

The band-reject filter is also called a band-stop or band-elimination filter. In this filter, frequencies are attenuated in the stopband while they are passed outside this band, as shown in Figure 8-1(d).

As with band-pass filters, the band-reject filters can also be classified as (1) wide band-reject or (2) narrow band-reject. The narrow band-reject filter is commonly called the notch filter. Because of its higher Q (>10), the bandwidth of the narrow band-reject filter is much smaller than that of the wide band-reject filter.

Wide Band-Reject Filter

Figure 8-14(a) shows a wide band-reject filter using a low-pass filter, a high-pass filter, and a summing amplifier. To realize a band-reject response, the low cutoff frequency f_L of the high-pass filter must be larger than the high cutoff frequency f_H of the low-pass filter. In addition, the passband gain of both the high-pass and low-pass sections must be equal. The frequency response of the wide band-reject filter is shown in Figure 8-14(b).

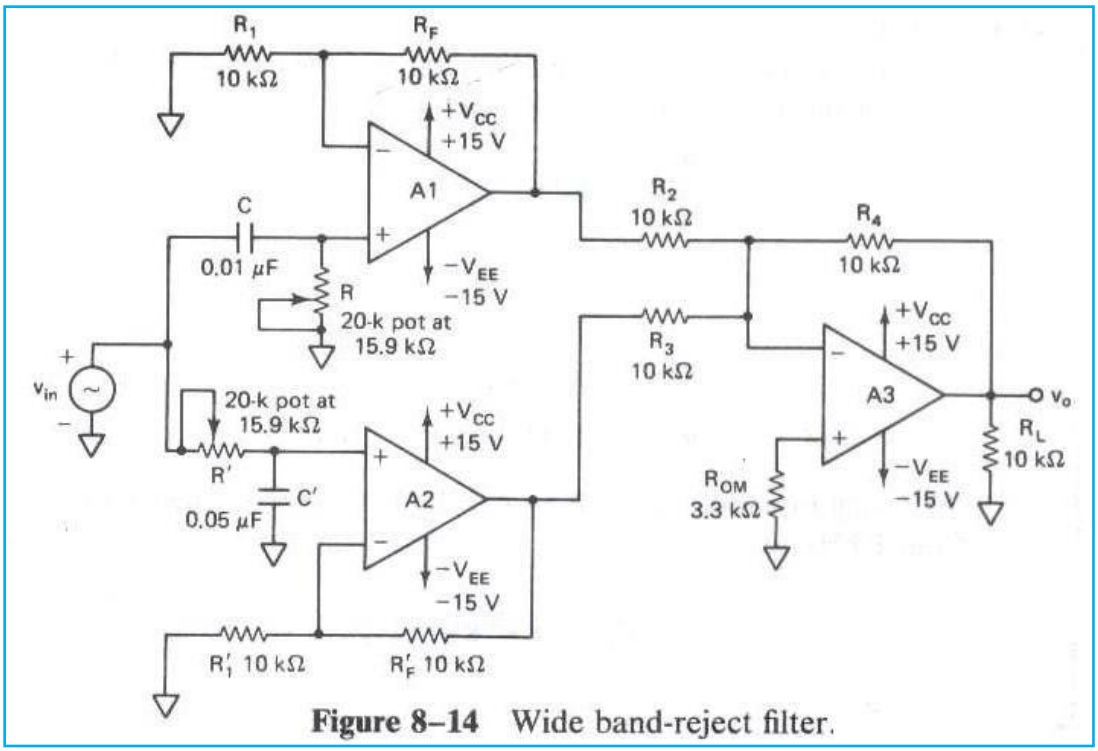


Figure 8–14 Wide band-reject filter.

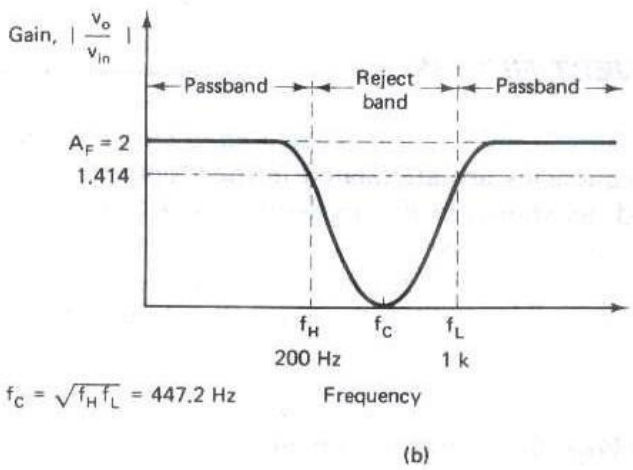


Figure 8–14 Wide band-reject filter. (a) Circuit. (b) Frequency response. For A_1, A_2, and A_3 use quad op-amp μAF774/MC34004.

Narrow Band-Reject Filter

The narrow band-reject filter, often called the notch filter, is commonly used for the rejection of a single frequency such as the 60-Hz power line frequency hum. The most commonly used notch filter is the twin-T network shown in Figure 8-15(a). This is a passive filter composed of two T-shaped networks. One T network is made up of two resistors and a capacitor, while the other uses two capacitors and a resistor. The notch-out frequency is the frequency at which maximum attenuation occurs; it is given by

$$f_N = \frac{1}{2\pi RC}$$

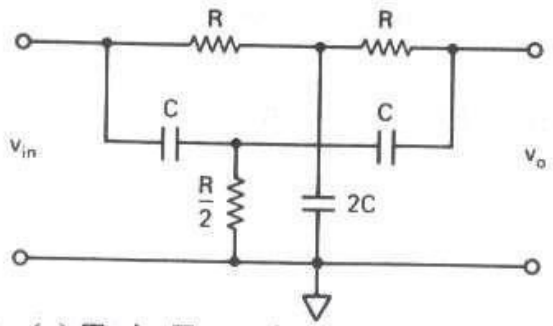
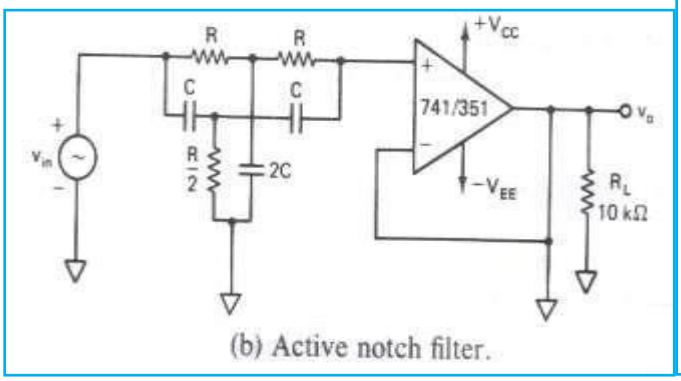
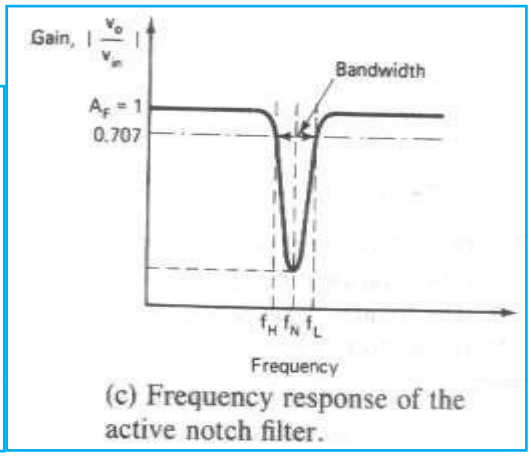


Figure 8–15 (a) Twin-T notch filter.



(b) Active notch filter.



(c) Frequency response of the active notch filter.

ALL-PASS FILTER

As the name suggests, an all-pass filter passes all frequency components of the input signal without attenuation, while providing predictable phase shifts for different frequencies of the input signal. When signals are transmitted over transmission lines, such as telephone wires, they undergo change in phase. To compensate for these phase changes, all-pass filters are required. The all-pass filters are also called delay equalizers or phase correctors. Figure 8-16(a) shows an all- pass filter wherein $R_F = R_1$. The output voltage Vo of the filter can be obtained by using the superposition theorem:

$$v_o = -v_{in} + \frac{-jX_C}{R - jX_C} v_{in} \quad (2)$$

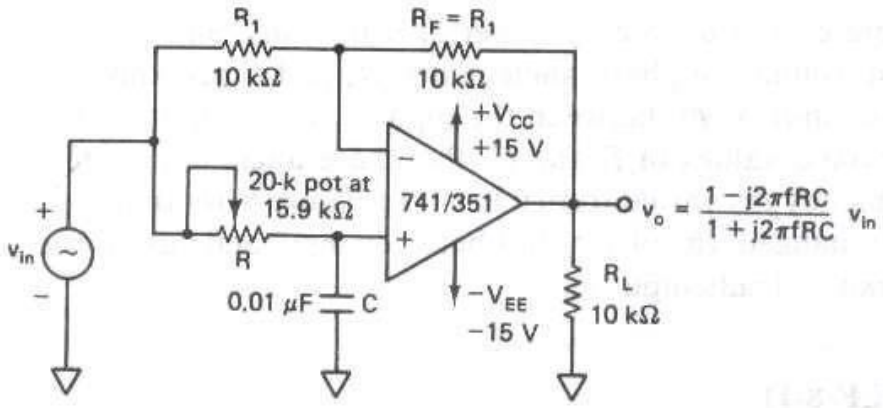


Figure 8–16 All-pass filter. (a) Circuit.

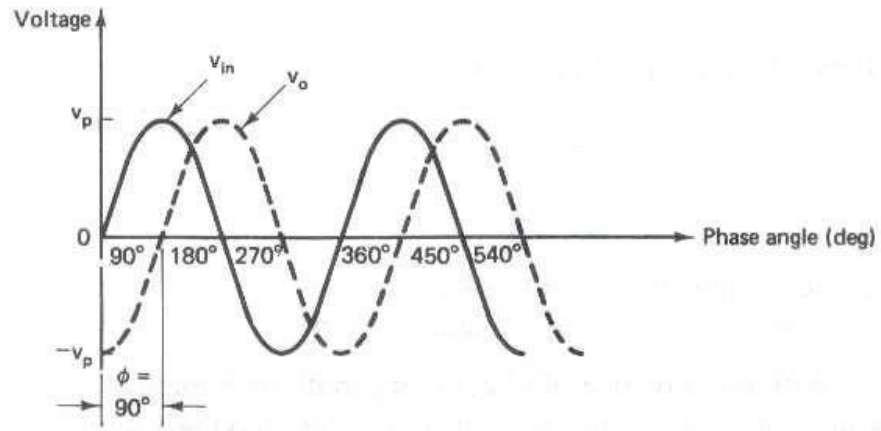


Figure 8–16 (b) Phase shift between input and output voltages.

But -j = 1/j and $X_C = 1/2\prod fC$. Therefore, substituting for X_C and simplifying, we get

$$v_o = v_{in}\left(-1 + \frac{2}{j2\pi fRC + 1}\right)$$

$$\frac{v_o}{v_{in}} = \frac{1 - j2\pi fRC}{1 + j2\pi fRC}$$

Where f is the frequency of the input signal in hertz.

Equation indicates that the amplitude of Vo/Vin is unity; that is, |Vo|=|Vin| throughout the useful frequency range, and the phase shift between Vo and Vin is a function of input frequency f. The phase angle φ is given by

$$\phi = -2\tan^{-1}\left(\frac{2\pi fRC}{1}\right).$$

Where φ is in degrees, in hertz, R in ohms, and C in farads. Equation is used to find the phase angle φ if f, R, and C are known. Figure 8-16(b) shows a phase shift of 90° between the input Vin and output Vo. That is, Vo lags Vin by 90°. For fixed values of R and C, the phase angle φ changes from 0 to 180°as the frequency f is varied from 0 to ∞. In Figure 8-16(a), if the positions of R and C are interchanged, the phase shift between input and output becomes positive. That is, output Vo leads input Vin.

INTRODUCTION TO 555 TIMER:

One of the most versatile linear integrated circuits is the *555* timer. A sample of these applications includes mono-stable and astable multivibrators, dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control, infrared transmitters, burglar and toxic gas alarms, voltage regulators, electric eyes, and many others.

The 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillation. The timer basically operates in one of the two modes: either as monostable (one-shot) multivibrator or as an astable (free running) multivibrator. The device is available as an 8-pin metal can, an 8-pin mini DIP, or a 14-pin DIP.

The SE555 is designed for the operating temperature range from -55°Cto + 125°C, while the NE555 operates over a temperature range of 0° to +70°C. The important features of the 555 timer are these: it operates on +5 to + 18 V supply voltage in both free-running (astable) and one- shot (monostable) modes; it has an adjustable duty cycle; timing is from microseconds through hours; it has a high current output; it can source or sink 200 mA; the output can drive TTL and has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005%/°C.

Like general-purpose op-amps, the 555 timer is reliable, easy to us, and low cost.

Pin 1: Ground.

All voltages are measured with respect to this terminal.

Pin 2: Trigger.

The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. The output is low if the voltage at this pin is greater than 2/3 VCC. However,when a negative-going pulse of amplitude larger than 1/3 VCC is applied to this pin, the comparator 2 output goes low, which in turn switches the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage.

Pin 3: Output.

There are two ways a load can be connected to the output terminal: either between pin 3 and ground (pin 1) or between pin 3 and supply voltage + VCC (pin 8). When the output is low, the load current flows through the load connected between pin 3 and + VCC into the output terminal and is called the sink current.

However, the current through the grounded load is zero when the output is low. For this reason, the load connected between pin 3 and + VCC is called the normally on load and that connected between pin 3 and ground is called the normally off load.

On the other hand, when the output is high, the current through the load connected between pin 3and + VCC (normally on load) is zero. However, the output terminal supplies current to the normally off load. This current is called the source current. The maximum value of sink or source current is 200 mA.

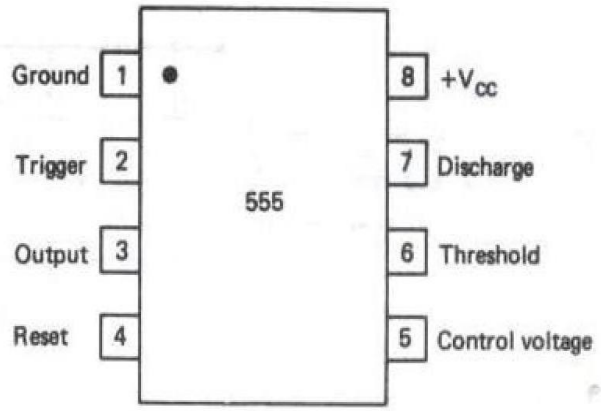


Fig 2.1 Pin diagram of 555Timer

Pin 4: Reset.

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to + VCC to avoid any possibility of false triggering.

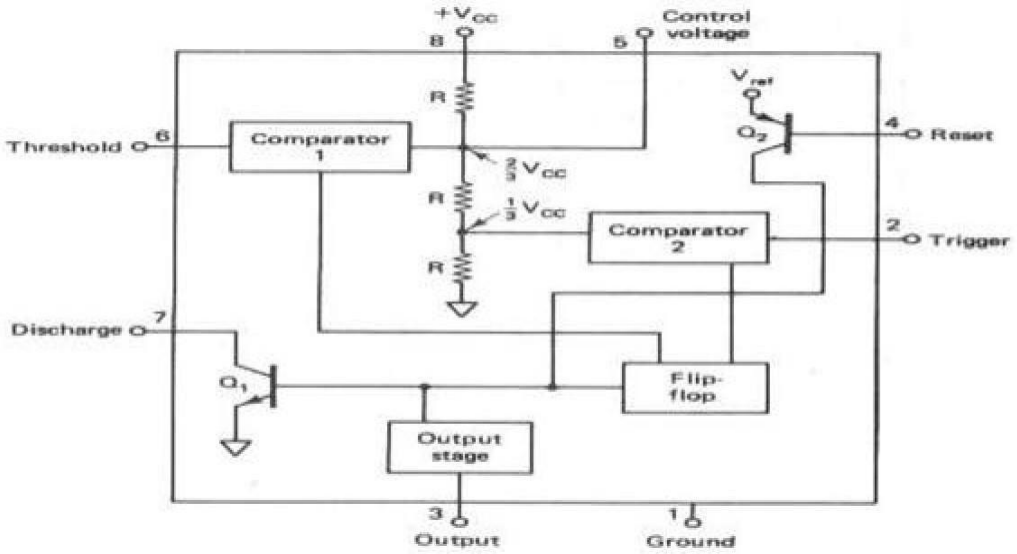


Fig 2.1(a) Block Diagram

Pin 5: Control voltage.

An external voltage applied to this terminal changes the threshold as well as the trigger voltage . In other words, by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not

used, the control pin should be bypassed to ground with a 0.01-μF capacitor to prevent any noise problems.

Pin 6: Threshold. This is the non-inverting input terminal of comparator 1, which monitors the voltage across the external capacitor. When the voltage at this pin is threshold voltage 2/3 V, the output of comparator 1 goes high, which in turn switches the output of the timer low.

Pin 7: Discharge. This pin is connected internally to the collector of transistor Q1, as shown in Figure 2.1(b). When the output is high, Q1 is off and acts as an open circuit to the external capacitor C connected across it. On the other hand, when the output is low, Q1 is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin 8: + VCC.

The supply voltage of +5 V to +18 is applied to this pin with respect to ground (pin 1).

FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER:

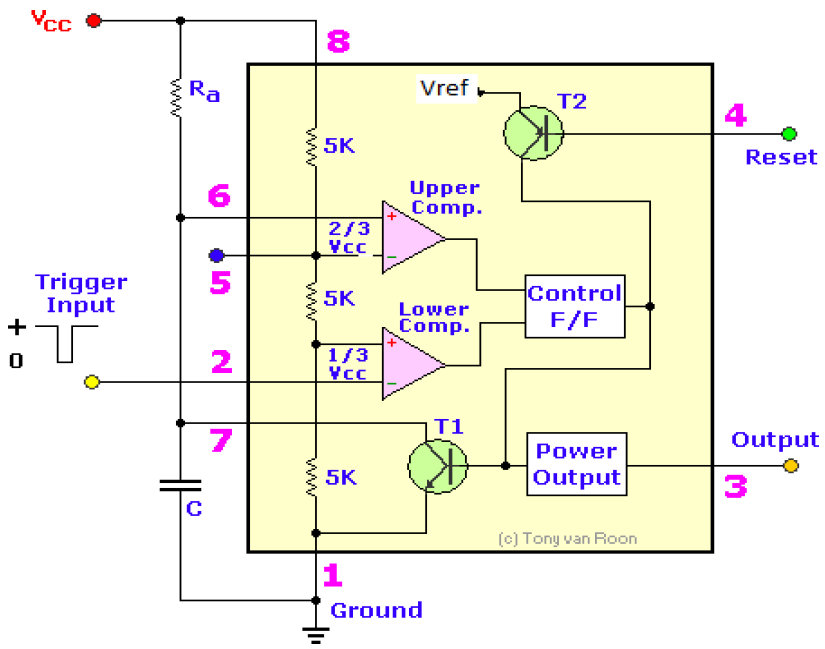


Fig 2.1(b) Block diagram of timer

THE 555 AS A MONOSTABLE MULTIVIBRATOR

A monostable multivibrator, often called a one-shot multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer.

In a stable or standby state the output of the circuit is approximately zero or at logic- low level. When an external trigger pulse is applied, the output is forced to go high (≈VCC). The time the output remains high is determined by the external RC network connected to the

timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats.

The monostable circuit has only one stable state (output low), hence the name mono- stable. Normally, the output of the mono- stable multivibrator is low. Fig 2.2 (a) shows the

555 configured for monostable operation. To better explain the circuit's operation, the internal block diagram is included in Fig 2.2(b).

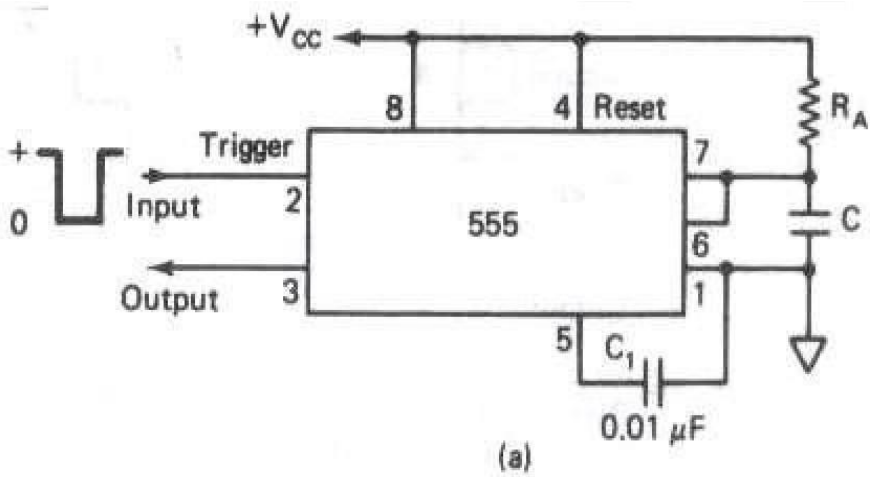


Figure 2.2(a) IC555 as monostable multivibrator

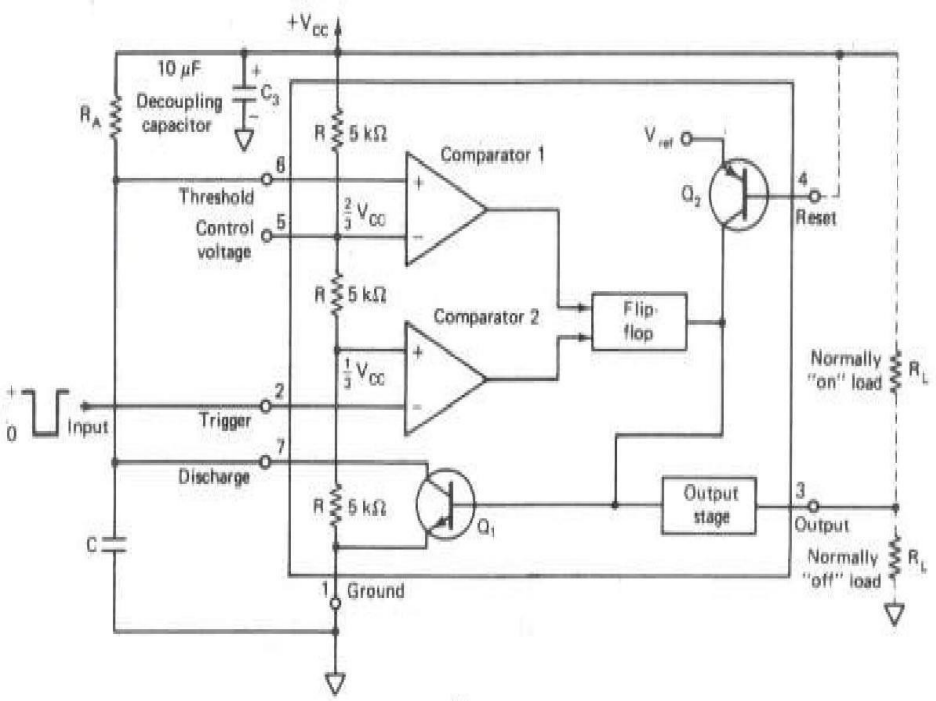
Mono-stable operation:

According to Fig 2.2(b), initially when the output is low, that is, the circuit is in a stable state, transistor Q is on and capacitor C is shorted out to ground. However, upon application of a negative trigger pulse to pin 2, transistor Q is turned off, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up toward Vcc through RA.

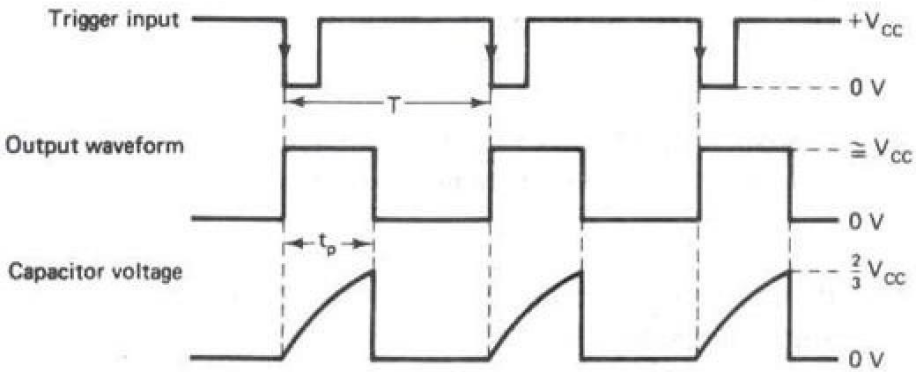
However, when the voltage across the capacitor equals 2/3 Va., comparator I

‘s output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-flop turns transistor Q on, and hence capacitor C rapidly discharges through the transistor.

The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. Figure 4-2(c) shows the trigger input, output voltage, and capacitor voltage waveforms. As shown here, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also, the trigger pulse must be a negative- going input signal with amplitude larger than 1/3 the time during which the output remains high is given by where



(b)



(c)

Fig.2.2 (b) 555 connected as a Monostable Multivibrator (c) input and output waveforms Where RA is in ohms and C is in farads. Figure 2.2(c) shows a graph of the various

combinations of RA and C necessary to produce desired time delays. Note that this graph can only be used as a guideline and gives only the approximate value of RA and C for a given time delay. Once triggered, the circuit's output will remain in the high state until the set time 1, elapses. The output will not change its state even if an input trigger is applied again during this time interval T. However, the circuit can be reset during the timing cycle by applying a negative pulse to the reset terminal. The output will then remain in the low state until a trigger is again applied.

Often in practice a decoupling capacitor (10 F) is used between + (pin 8) and ground (pin 1) to eliminate unwanted voltage spikes in the output waveform. Sometimes, to prevent

any possibility of mistriggering the monostable multivibrator on positive pulse edges, a wave shapingcircuit consisting of R, C2, and diode D is connected between the trigger input pin 2 and pin 8, as shown in Figure 4-3. The values of R and C2 should be selected so that the time constant RC2 is smaller than the output pulse width.

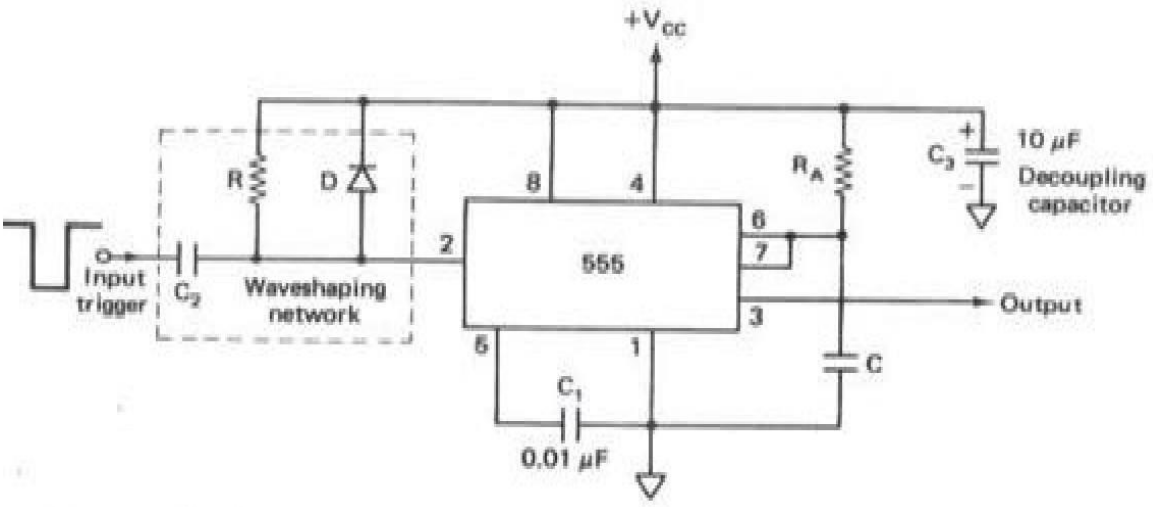


Fig.2.3 Monostable Multivibrator with wave shaping network to prevent +ve pulse edge triggering

Monostable Multivibrator Applications

(a) Frequency divider: The monostable multivibrator of Figure 2.2(a) can be used as a frequency divider by adjusting the length of the timing cycle tp, with respect to the tine period T of the trigger input signal applied to pin 2. To use monostable multivibrator as a divide-by-2 circuit, the timing interval tp must be slightly larger than the time period T of the trigger input signal, as shown in Figure 2.4. By the same concept, to use the monostable multivibrator as a divide-by-3 circuit, tp must be slightly larger than twice the period of the input trigger signal, and so on. The frequency-divider application is possible because the monostable multivibrator cannot be triggered during the timing cycle.

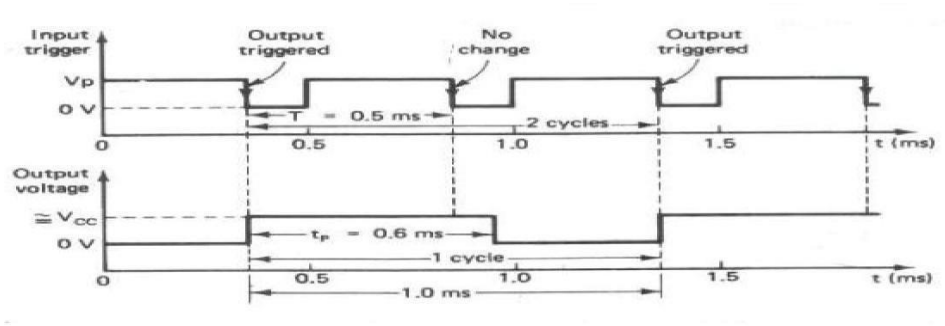


Fig 2.4 input and output waveforms of a monostable multi vibrator as a divide-by-2 network

(b) Pulse stretcher: This application makes use of the fact that the output pulse width (timing interval) of the rnonostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name pulse stretcher. Often, narrow-pulse- width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but is not visible to the eye because its on time is infinitesimally small compared to its off time. The 555 pulse stretcher can be used to remedy this problem

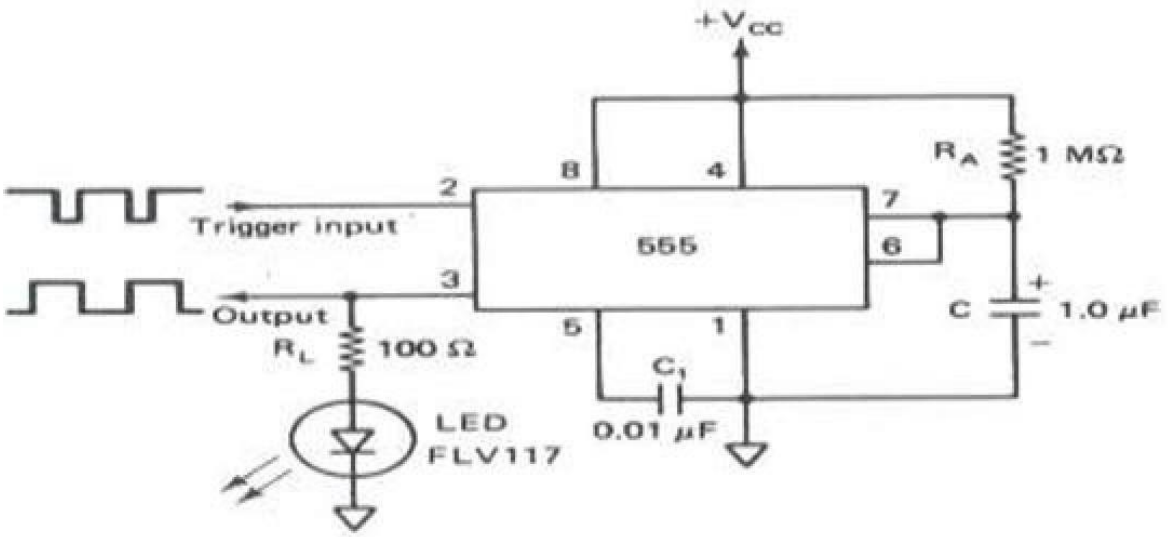


Fig 2.5 Monostable multi vibrator as a Pulse stretcher

Figure 2.5 shows a basic monostable used as a pulse stretcher with an LED indicator at the output. The LED will be on during the timing interval tp = 1.1RAC, which can be varied by changing the value of RA and/or C.

THE 555 AS AN ASTABLE MULTIVIBRATOR:

The 555 as an Astable Multivibrator, often called a free-running multivibrator, is a rectangular- wave-generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the 555 timer. Fig 4-6(a) shows the 555 timer connected as an astable multivibrator. Initially, when the output is high, capacitor C starts charging toward V through RA and R8. However as soon as voltage across the capacitor equals 2/3 Vcc, comparator I triggers the flip flop, and the output switches low. Now capacitor C starts discharging through R8 and transistor Q. When the voltage across C

equals 1/3 comparator 2's output triggers the flip-flop, and the output goes high. Then the cycle repeats.

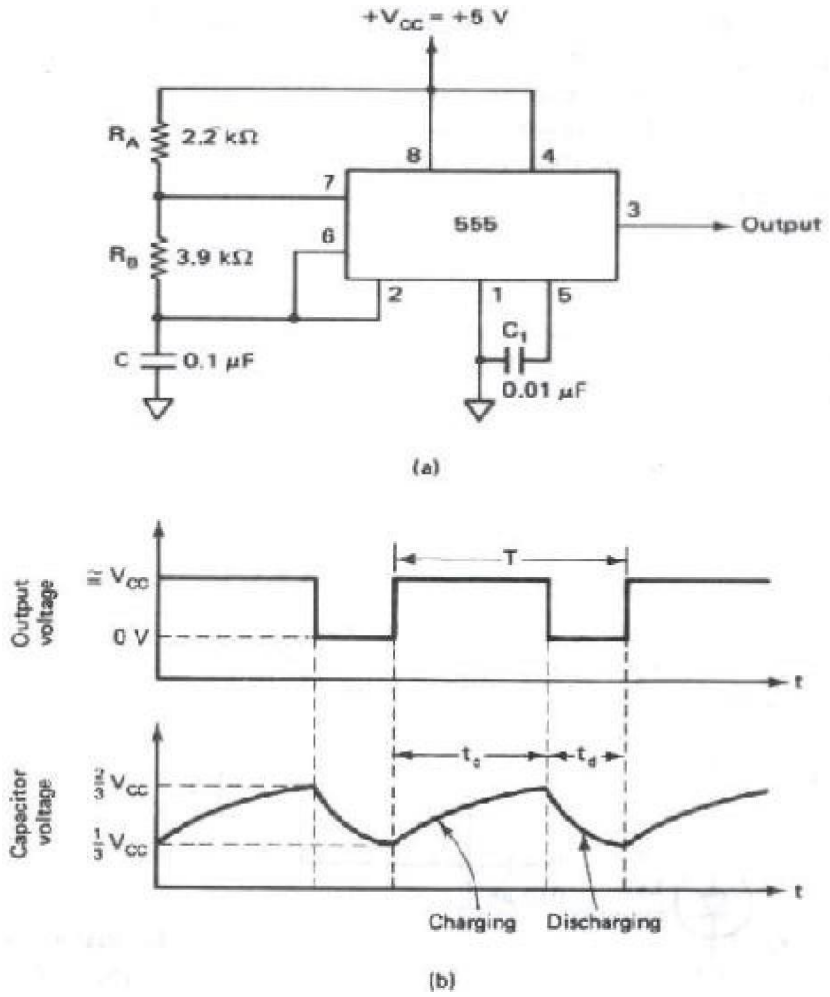


Fig 4-6 The 555 as a Astable Multivibrator (a)Circuit(b)Voltage across Capacitor and O/P waveforms.

The output voltage and capacitor voltage waveforms are shown in Figure 2.6(b). As shown in this figure, the capacitor is periodically charged and discharged between 2/3 Vcc and 1/3 V, respectively. The time during which the capacitor charges from 1/3 V to 2/3 V. is equal to the time the output is high and is given by

$$t_C = 0.69(R_A + R_B)C$$

where RA and R3 are in ohms and C is in farads. Similarly, the time during which the capacitor discharges from 2/3 V to 1/3 V is equal to the time the output is low and is given by

$$t_d = 0.69(R_B)C$$

where RB is in ohms and C is in farads. Thus the total period of the output waveform is

$$T = t_C + t_d = 0.69(R_A + 2R_B)C$$

This, in turn, gives the frequency of oscillation as

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

Above equation indicates that the frequency fo is independent of the supply voltage V. Often the term duty cycle is used in conjunction with the astable multivibrator . The duty cycle is the ratio of the time t during which the output is high to the total time period T. It is generally expressed as a percentage. In equation form,

$$\%\, duty\ cycle = \frac{t_C}{T} \times 100$$

$$= \frac{R_A + 2R_B}{R_A + 2R_B} \times 100$$

Astable Multivibrator Applications:

Square-wave oscillator: Without reducing RA = 0 , the astable multivibrator can be used to produce a square wave output simply by connecting diode D across resistor RB, as shown in Figure 4-7. The capacitor C charges through RA and diode D to approximately 2/3 Vcc and discharges through RB and terminal 7 until the capacitor voltage equals approximately 1/3 Vcc; then the cycle repeats. To obtain a square wave output (50% duty cycle), RA must be a combination of a fixed resistor and potentiometer so that the potentiorneter can be adjusted for the exact square wave.

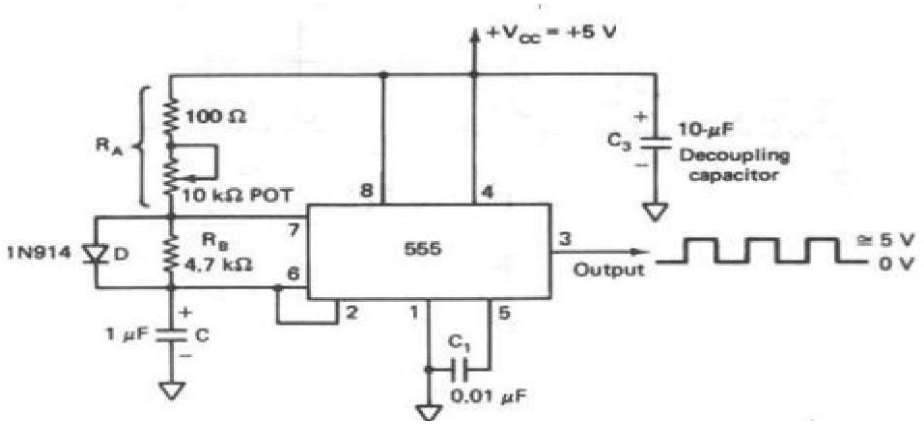


Fig 2.7 Astable Multivibrator as a Square wave generator

Free-running ramp generator: The astable multivibrator can be used as a free-running ramp generator when resistors RA and R3 are replaced by a current mirror. Figure 2.8(a) shows an astable multivibrator configured to perform this function. The current mirror starts charging capacitor C toward Vcc at a constant rate.

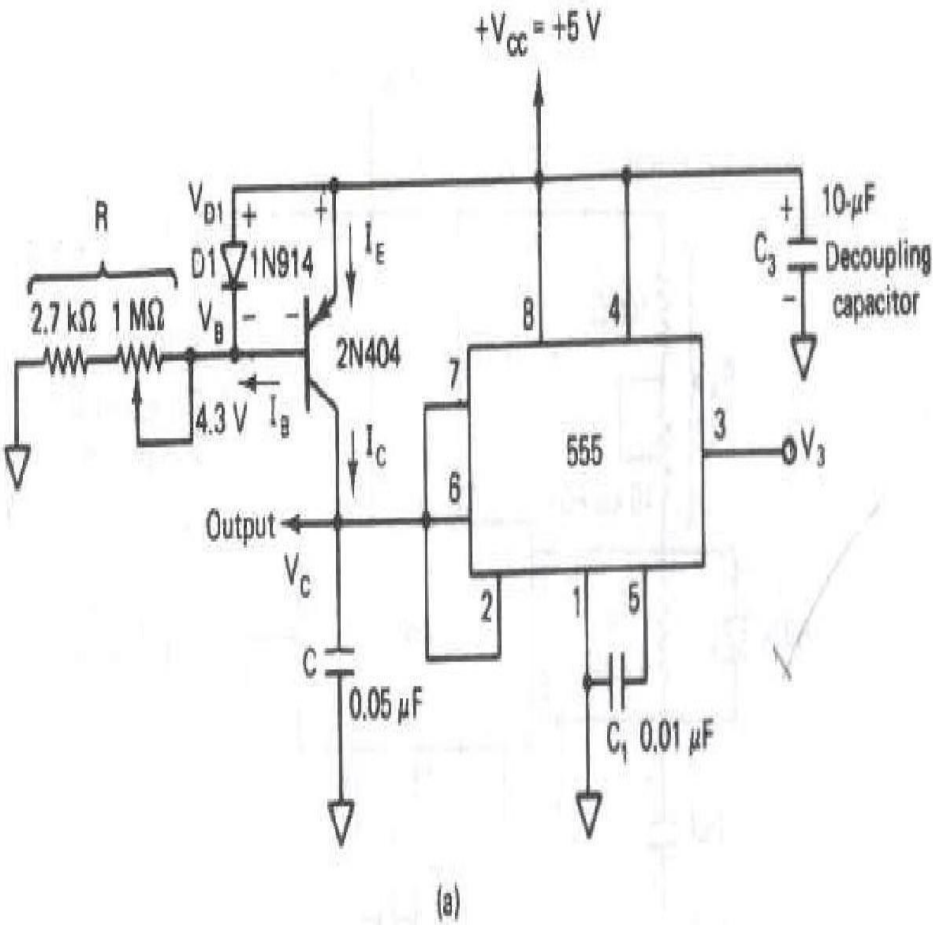
When voltage across C equals 2/3 Vcc, comparator 1 turns transistor Q on, and C rapidly discharges through transistor Q. However, when the discharge voltage across C is approximately equal to 1/3 Vcc, comparator 2 switches transistor Q off, and then capacitor C starts charging up again. Thus the charge— discharge cycle keeps repeating. The discharging time of the capacitor is relatively negligible compared to its charging time; hence, for all practical purposes, the time period of the ramp waveform is equal to the charging time and is approximately given by

$$T = \frac{V_{cc}C}{3I_C}$$

Where I = (Vcc — VBE)/R = constant current in amperes and C is in farads.

Therefore, the free running frequency of the ramp generator is

$$f_o = \frac{3I_C}{V_{cc}C}$$



(a)

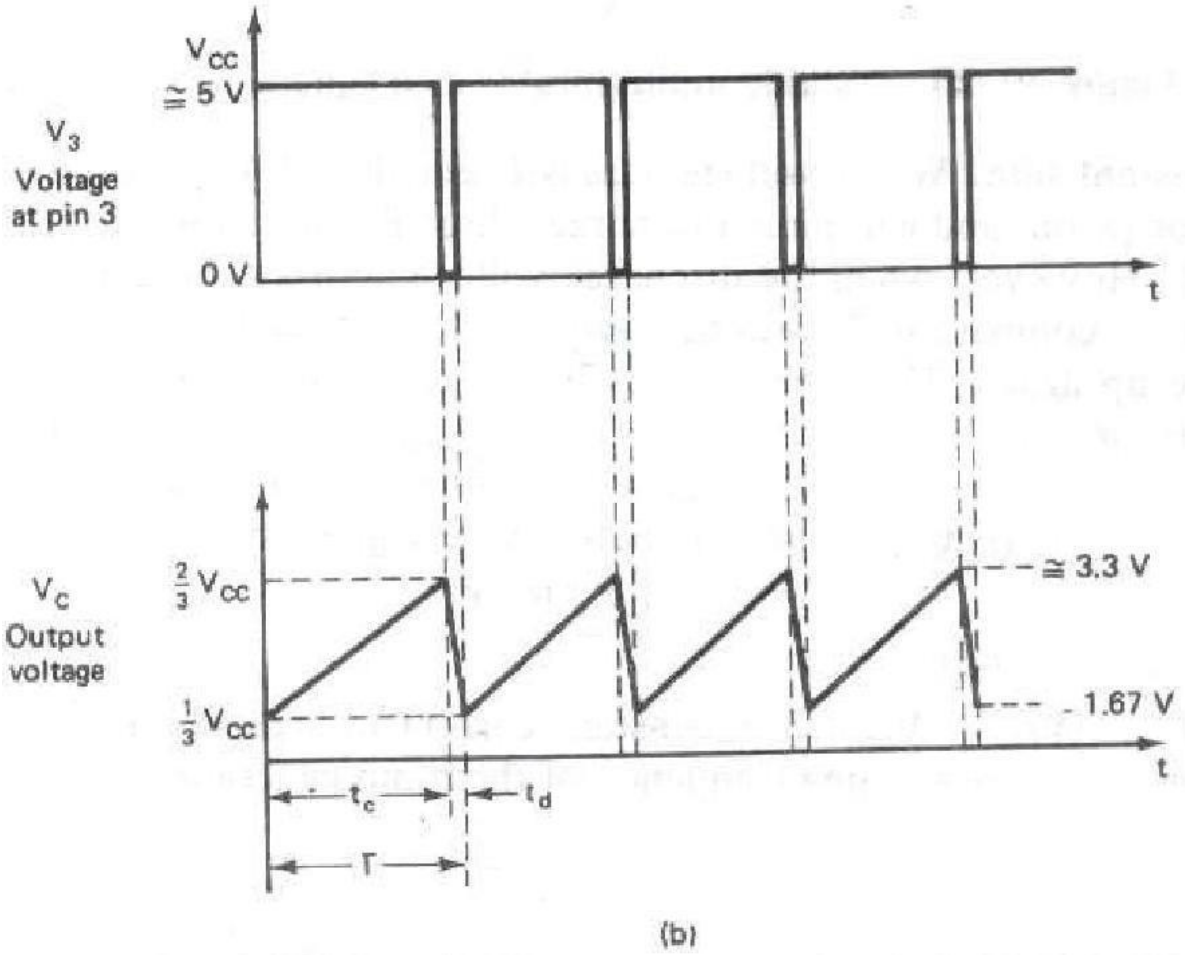


Fig 2.8(a) Free Running ramp generator (b) Output waveform.

SCHMITT TRIGGER:

The below fig 2.9 shows the use of 555 timer as a Schmitt trigger:

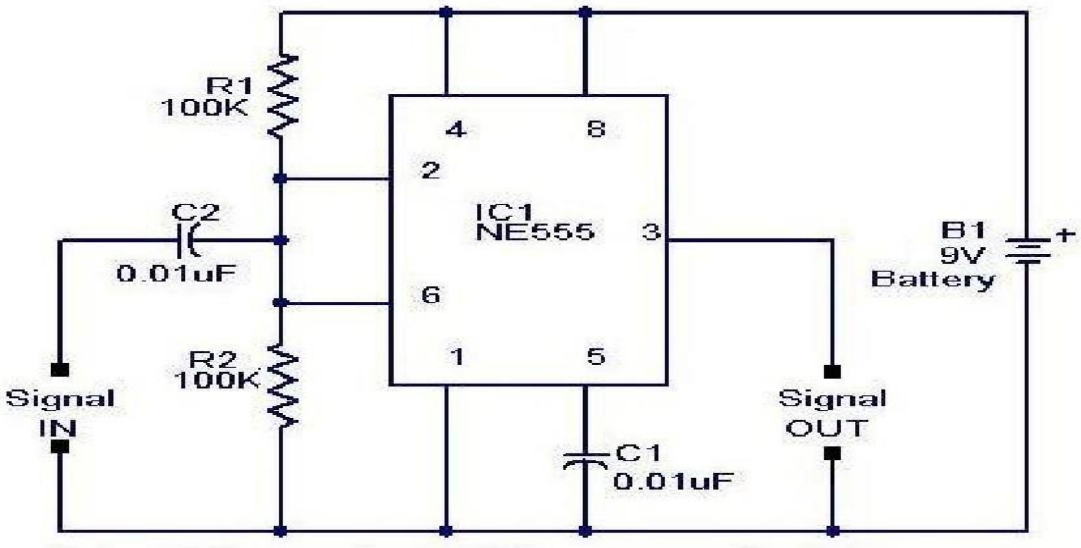


Fig 2.9 Timer as Schmitt trigger

The input is given to the pin 2 and pin 6 which are tied together. Pins 4 and 8 are connected to supply voltage +Vcc. The common point of two pins 2 and 6 are externally biased at Vcc/2 through the resistance network R1 and R2.Generally R1=R2 to the gate biasing of Vcc/2.The upper comparator will trip at 2/3Vccwhile lower comparator at 1/3Vcc.The bias provided by R1 and R2 is centered within these two thresholds. Thus when sine wave of sufficient amplitude, greater than Vcc/6 is applied to the circuit as input, it causes the internal flip flop to alternately set and reset. Due to this, the circuit produces the square wave at the output.

PHASE-LOCKED LOOPS

The phase-locked loop principle has been used in applications such as FM (frequency modulation) stereo decoders, motor speed controls, tracking filters, frequency synthesized transmitters and receivers, FM demodulators, frequency shift keying (FSK) decoders, and a generation of local oscillator frequencies in TV and in FM tuners.

Today the phase-locked loop is even available as a single package, typical examples of which include the Signetics SE/NE 560 series (the 560, 561, 562, 564, 565, and 567). However, for more economical operation, discrete ICs can be used to construct a phase- locked loop.

Bloch Schematic and Operating Principle

Figure 2.10 shows the phase-locked loop (PLL) in its basic form. As illustrated in this figure, the phase-locked loop consists of (1) a phase detector, (2) a low-pass filter, and, (3) a voltage controlled oscillator

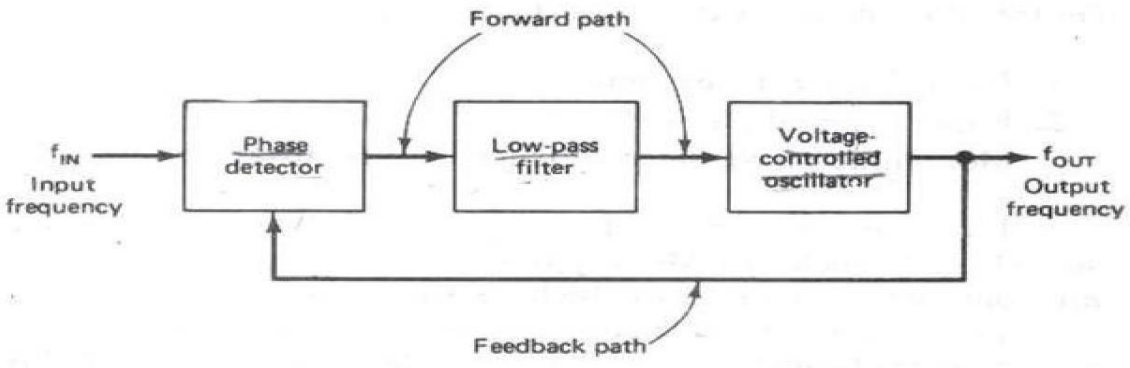


Fig 2.10 Block Diagram of Phase Locked Loop

The phase detectors or comparator compares the input frequency *f*IN with the feedback frequency *f*OUT.. The output voltage of the phase detector is a dc voltage and therefore is often referred to as the error voltage. The output of the phase is then applied to the low-pass filter, which removes the high-frequency noise and produces a dc level.

This dc level, in turn, is the input to the voltage-controlled oscillator (VCO). The filter also helps in establishing the dynamic characteristics of the PLL circuit. The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies. In short, the phase-locked loop goes through three states: free- running, capture, and phase lock. Before the input is applied, the phase-locked loop is in the free-running state. Once the input frequency is applied, the VCO frequency starts to change and the phase-locked loop is said to be in the capture mode. The VCO frequency continues to change until it equals the input frequency, and the phase- locked loop is then in the phase-locked state. When phase locked, the loop tracks any change in the input frequency through its repetitive action. Before studying the specialized phase-locked-loop IC, we shall consider the discrete phase-locked loop, which may be assembled by combining a phase detector, a low-pass filter, and a voltage-controlled oscillator.

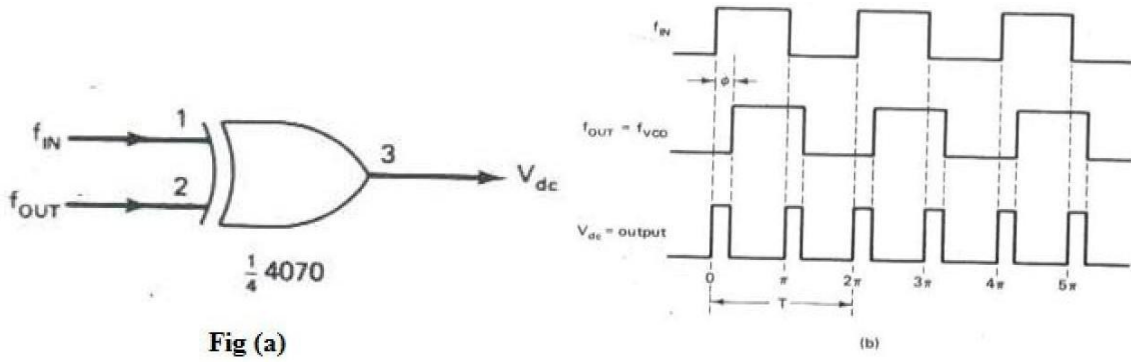
(a) Phase detector:

The phase detector compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase difference between the two frequencies. Depending on the analog or digital phase detector used, the PLL is either called an analog or digital type, respectively. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors in use are of the digital type mainly because of its simplicity.

A double-balanced mixer is a classic example of an analog phase detector. On the other hand,examples of digital phase detectors are these:

1. Exclusive-OR phase detector
2. Edge-triggered phase detector
3. Monolithic phase detector (such as type 4044)

The following fig 2.11 shows Exclusive-OR phase detector:



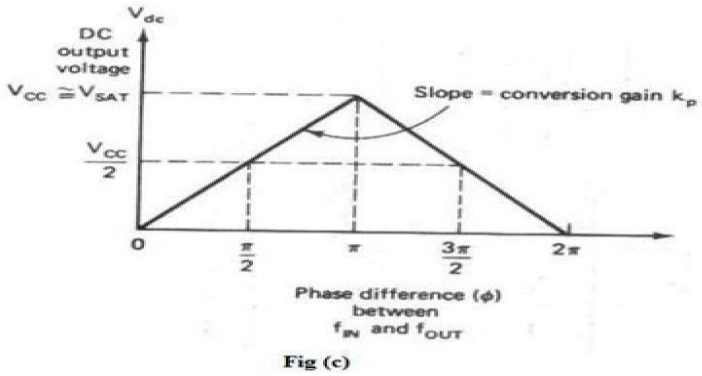


Fig 2.11 (a) Exclusive-OR phase detector: connection and logic diagram. (b) Input and output waveforms. (c) Average output voltage versus phase difference between *f*IN and *f*OUT curve.

(b) Low-pass filter.

The function of the low-pass filter is to remove the high-frequency components in the output of the phase detector and to remove high-frequency noise.

More important, the 1ow-pass filter controls the dynamic characteristics of the phase- locked loop. These characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency *f*IN. An equivalent term for lock range is tracking range. On the other hand, the capture range is the frequency range in which the PLL acquires phase lock. Obviously, the capture range is always smaller than the lock range.

(c) *Voltage-controlled oscillator:*

A third section of the PLL is the voltage-controlled oscillator. The VCO generates an output frequency that is directly proportional to its input voltage. Typical example of VCO is Signetics NE/SE 566 VCO, which provides simultaneous square wave and triangular wave outputs as a function of input voltage. The block diagram of the VCO is shown in Fig 2.12. The frequency of oscillations is determined by three external R1 and capacitor C1 and the voltage VC applied to the control terminal 5.

The triangular wave is generated by alternatively charging the external capacitor C1 by one current source and then linearly discharging it by another. The charging and discharging levels are determined by Schmitt trigger action. The schmitt trigger also provides square wave output. Both the wave forms are buffered so that the output impedance of each is 50 ohms.

In this arrangement the R1C1 combination determines the free running frequency and the control voltage VC at pin 5 is set by voltage divider formed with R2 and R3. The initial voltage VC at pin 5 must be in the range

$$\frac{3}{4}(+V) \leq V_C \leq +V$$

Where +V is the total supply voltage.The modulating signal is ac coupled with the capacitor C and must be <3 VPP. The frequency of the output wave forms is approximated by

$$f_o \cong \frac{2(+V - V_C)}{R_1 C_1 (+V)}$$

where R1should be in the range 2KΩ < R1< 20KΩ. For affixed VC and constant C1, the frequency fO can be varied over a 10:1 frequency range by the choice of R1 between 2KΩ < R1< 20KΩ.

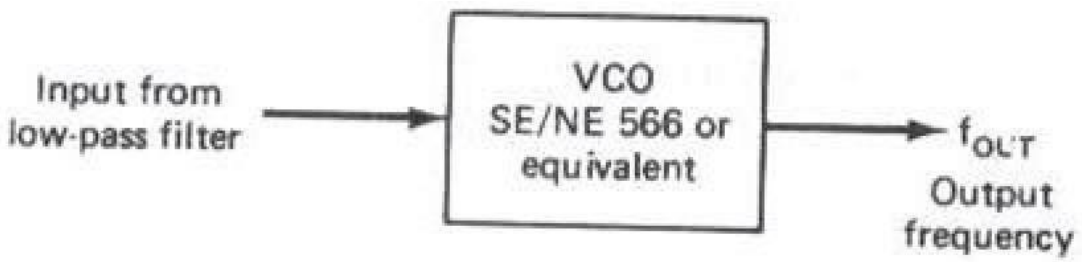


Fig 2.12: VCO Block Diagram

MONOLITHIC PHASE LOCK LOOPS IC 565:

Monolithic PLLs are introduced by signetics as SE/NE 560 series and by national semiconductors LM 560 series.

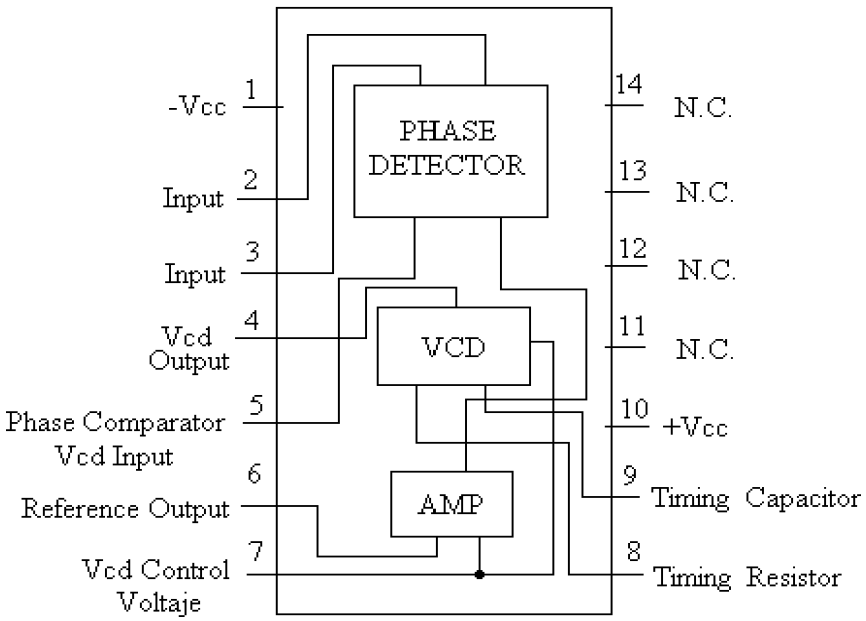


Fig 2.13 Pin configuration of IC 565

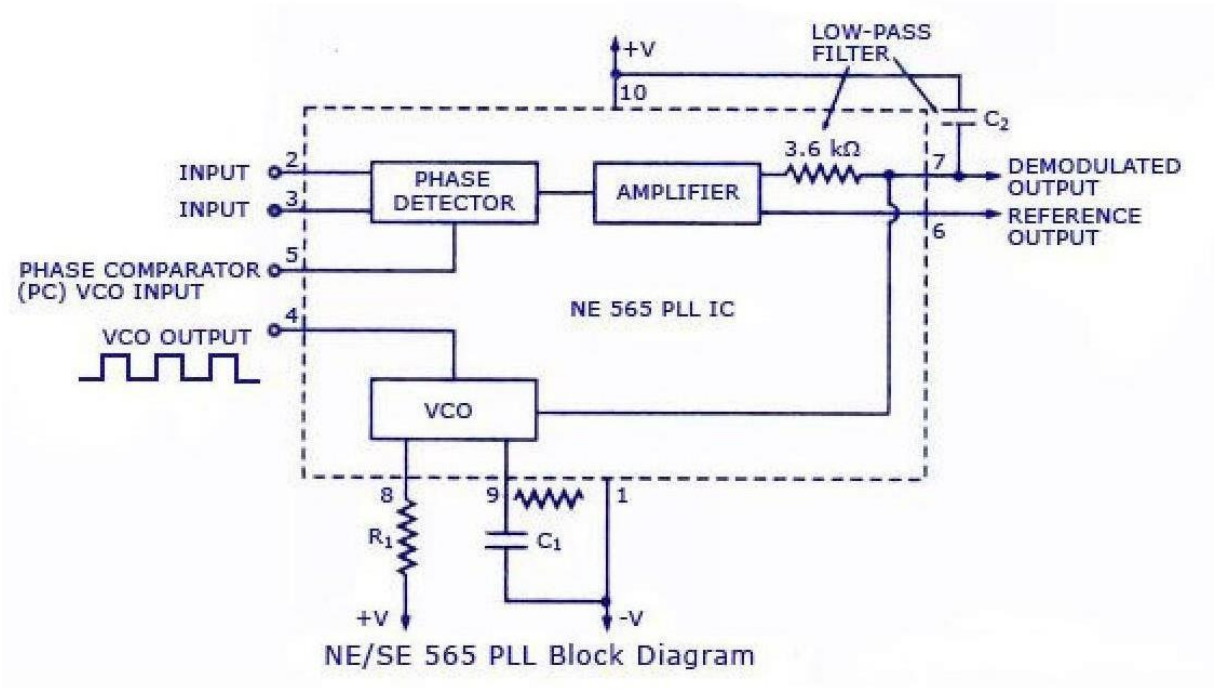


Fig 2.14 Block Diagram of IC 565

Fig 2.13 and 2.14 shows the pin diagram and block diagram of IC 565 PLL. It consists of phase detector, amplifier, low pass filter and VCO.As shown in the block diagram the phase locked feedback loop is not internally connected. Therefore, it is necessary to connect output of VCO to the phase comparator input, externally. In

$$f_o = \frac{1.2}{4R_1C_1}$$

frequency multiplication applications a digital frequency divider is inserted into the loop i.e., between pin 4 and pin 5. The centre frequency of the PLL is determined by the free-running frequency of the VCO and it is given by

Where R1 and C1 are an external resistor and capacitor connected to pins 8 and 9, respectively. The values of R1 and C1 are adjusted such that the free running frequency will be at the centre of the input frequency range. The values of R1 are restricted from 2 kΩ to 20 kΩ,but a capacitor can have any value. A capacitor C2 connected between pin 7 and the positive supply forms a first order low pass filter with an internal resistance of 3.6 kΩ. The value of filter capacitor C2 should be larger enough to eliminate possible demodulated output voltage at pin 7 in order to stabilize the VCO frequency

The PLL can lock to and track an input signal over typically ±60% bandwidth w.r.t fo as the center frequency. The lock range fL and the capture range fC of the PLL are given by the following equations.

$$f_L = \pm\frac{8f_0}{V}$$

Where fo=free running frequency And V=(+V)-(-V)Volts
And

$$f_C = \pm\sqrt{\frac{f_L}{2\pi(3.6)10^3C_2}}$$

From above equation the lock range increases with an increase in input voltage but decrease with increase in supply voltage. The two inputs to the phase detector allows direct coupling of an input signal, provided that there is no dc voltage difference between the pins and the dc resistances seen from pins 2 and 3 are equal.

Unit 4
DATA CONVERTER

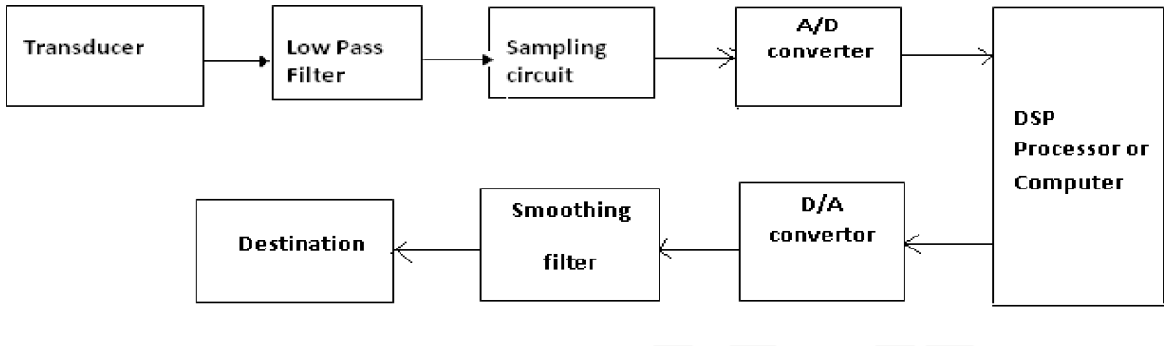


Fig 2.15: Application of A/D and D/A converters

Fig 2.15 shows the application of A/D and D/A converters. The transducer circuit will gives an analog signal. This signal is transmitted through the LPF circuit to avoid higher components, and then the signal is sampled at twice the frequency of the signal to avoid the overlapping. The output of the sampling circuit is applied to A/D converter where the samples are converted into binary data i.e. 0's and 1's. Like this the analog data converted into digital data.

The digital data is again reconverted back into analog by doing exact opposite operation of first half of the diagram. Then the output of the D/A convertor is transmitted through the smoothing filter to avoid the ripples.

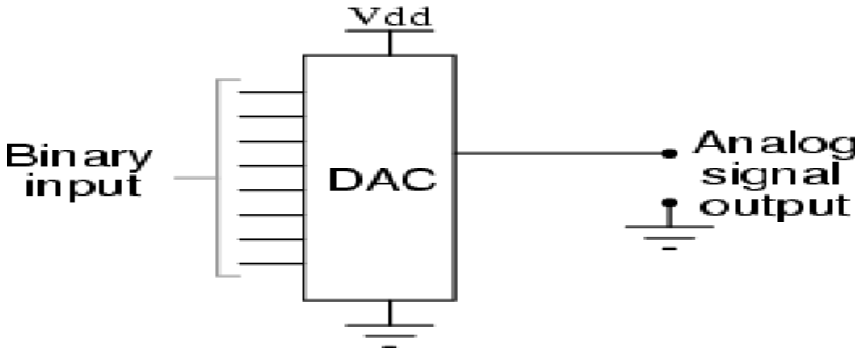
BASIC DAC TECHNIQUES

The input of the block diagram is binary data i.e, 0 and 1,it contain 'n' number of input bits designated as d1,d2,d3,…..dn .this input is combined with the reference voltage called Vdd to give an analog output.

Where d1 is the MSB bit and dn is the LSB bit

$$Vo=Vdd(d1*2-1+d2*2-2+d3*2-3+ \ldots\ldots\ldots\ldots\ldots +dn*2-n)$$

Fig .2.16: Basic DAC diagram



Weighted Resistor:

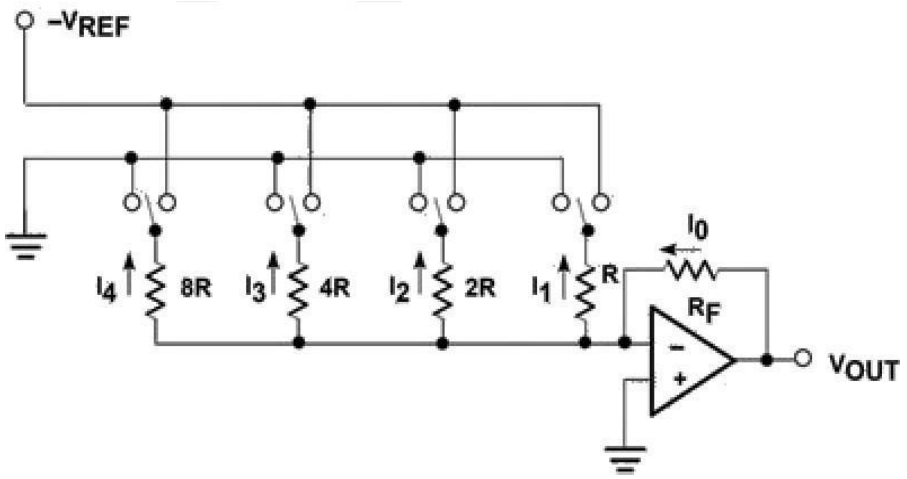


Fig: 2.17 simple 4-bit weighted resistor

Fig. 2.17 shows a simplest circuit of weighted resistor. It uses a summing inverting amplifier. It contains n- electronic switches (i.e. 4 switches) and these switches are controlled by binary input bits d1, d2, d3, d4. If the binary input bit is 1 then the switch is connected to reference voltage –VREF , if the binary input bit is 0 then the switch is connected to ground. The output current equation is Io=I1+I2+ I3+I 4

Io= VREF (d1*2-1+d2*2-2+d3*2-3+d4*2-4)

The transfer characteristics are shown below (fig 2.13) for a 3-bit weighted resistor

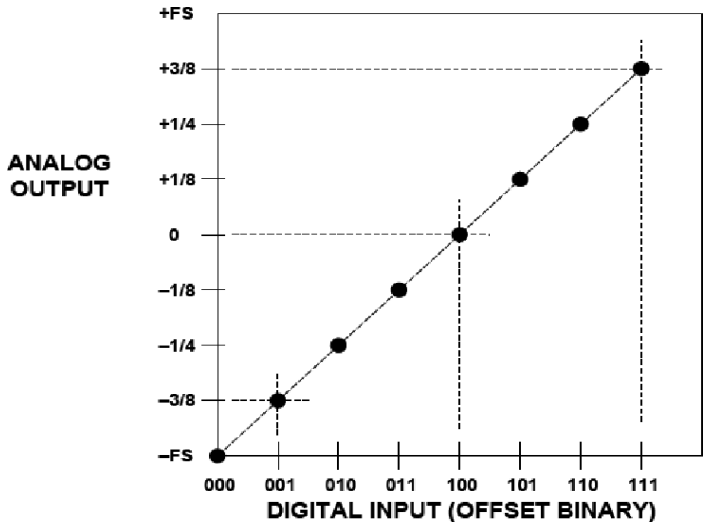


Fig 2.18 Transfer characteristics of 3-bit weighted resistor

Disadvantages of Weighted resistor D/A converter:

Wide range of resistor's are required in this circuit and it is very difficult to fabricate such a wide range of resistance values in monolithic IC. This difficulty can be eliminated using R-2R ladder network.

R-2R LADDER DAC

Wide range of resistors required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC. The circuit of R-2R ladder network is shown in fig

2.19. The basic theory of the R-2R ladder network is that current flowing through any input resistor (2R) encounters two possible paths at the far end. The effective resistances of both paths are the same (also 2R), so the incoming current splits equally along both paths. The half-current that flows back towards lower orders of magnitude does not reach the op amp, and therefore has no effect on the output voltage. The half that takes the path towards the op amp along the ladder can affect the output. The inverting input of the op-amp is at virtual earth. Current flowing in the elements of the ladder network is therefore unaffected by switch positions.

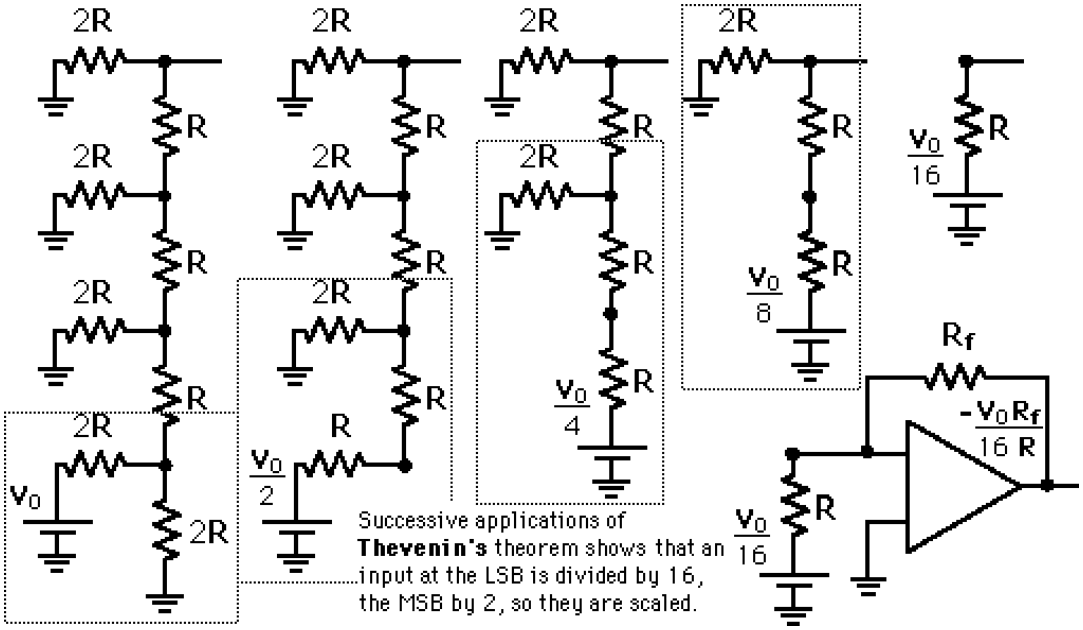


Fig 2.19: A 4-bit R-2R Ladder DAC

If we label the bits (or inputs) bit 1 to bit N the output voltage caused by connecting a particular bit to Vr with all other bits grounded is:

$$Vout = Vr/2N$$

where N is the bit number. For bit 1, Vout =Vr/2, for bit 2, Vout = Vr/4 etc.

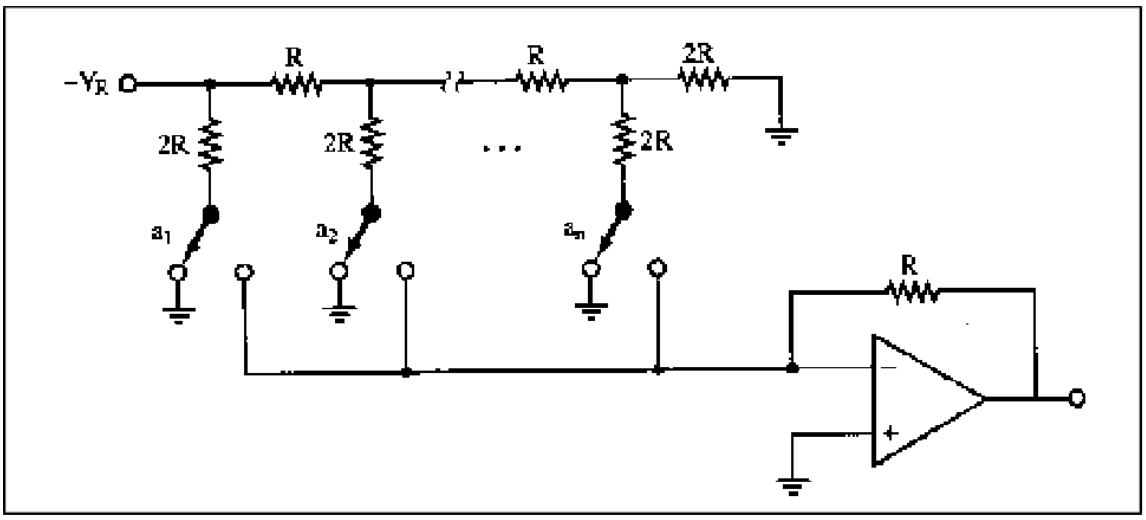
Since an R/2R ladder is a linear circuit, we can apply the principle of superposition to calculate Vout. The expected output voltage is calculated by summing the effect of all bits connected to Vr. For example, if bits 1 and 3 are connected to Vr with all other inputs grounded, the output voltage is calculated by: Vout = (Vr/2)+(Vr/8) which reduces to Vout = 5Vr/8.

An R/2R ladder of 4 bits would have a full-scale output voltage of 1/2 +1/4 + 1/8 + 1/16 = 15Vr/16 or 0.9375 volts (if Vr=1 volt) while a 10bit R/2R ladder would have a full- scale output voltage of 0.99902 (if Vr=1 volt).

INVERTED R-2R LADDER DAC

In weighted resistor and R-2R ladder DAC the current flowing through the resistor is always changed because of the changing input binary bits 0 and 1. More power dissipation causes heating, which in turn cerates non-linearity in DAC. This problem can be avoided by using INVERTED R-2R LADDER DAC (fig 2.20)

In this MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of op-amp which is also at virtual ground. When the input binary in logic 1 then it is connected to the virtual ground, when input binary is logic 0 then it is connected to the ground i.e. the current flowing through the resistor is constant.



DIFFERENT TYPES OF ADC'S

It provides the function just opposite to that of a DAC. It accepts an analog input voltage Va and produces an output binary word d1, d2, d3….dn. Where d1 is the most significant bit and dn is the least significant bit.

ADCs are broadly classified into two groups according to their conversion techniques

1) Direct type

2) Integrating type

Direct type ADCs compares a given analog signal with the internally generated equivalent signal. This group includes

i) Flash (Comparator) type converter

ii) Successive approximation type convertor

iii) Counter type

iv) Servo or Tracking type

Integrated type ADCs perform conversion in an indirect manner by first changing the analog input signal to linear function of time or frequency and then to a digital code.

FLASH (COMPARATOR) TYPE CONVERTER:

A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, 2N - 1, doubles with each additional bit, requiring a large, expensive circuit. ADCs of this type have a large die size, a high input capacitance, high power dissipation, and are prone to produce

glitches at the output (by outputting an out-of- sequence code). Scaling to newer sub-micrometre technologies does not help as the device mismatch is the dominant design limitation. They are often used for video, wideband communications or other fast signals in optical storage.

A Flash ADC (also known as a direct conversion ADC) is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors; however modern implementations show that capacitive voltage division is also possible. The output of these comparators is generally fed into a digital encoder which converts the inputs into a binary value (the collected outputs from the comparators can be thought of as a unary value).

Also called the *parallel* A/D converter, this circuit is the simplest to understand. It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.

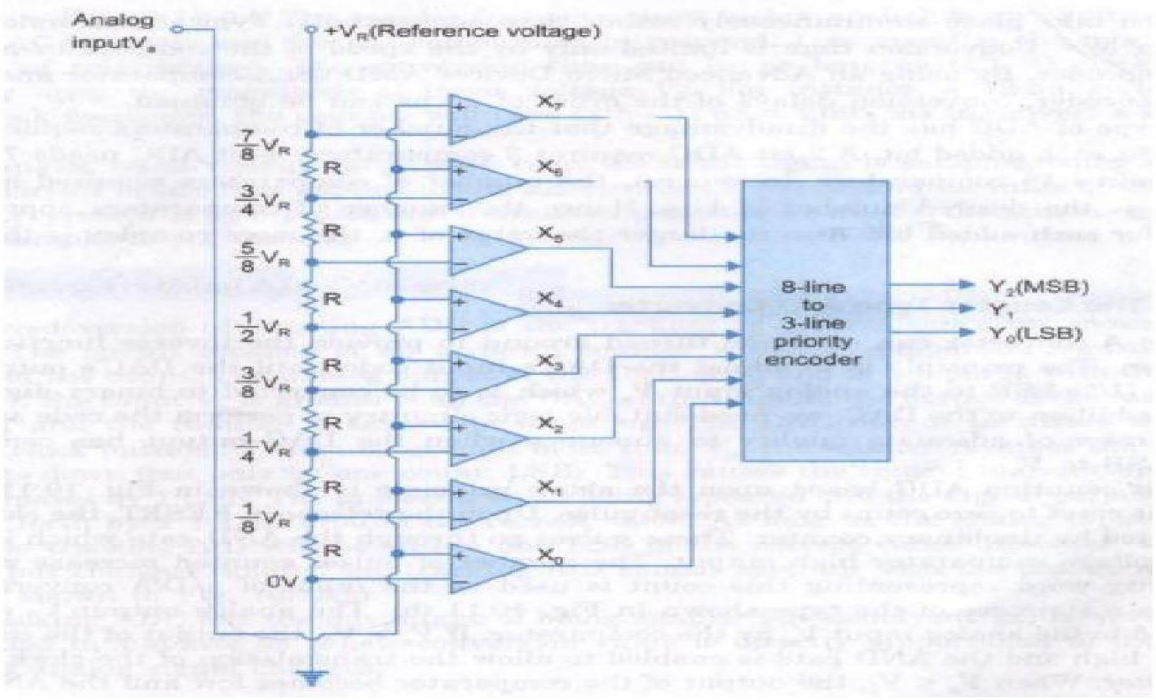


Fig 2.21: flash (parallel comparator) type ADC

VR is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic. As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

COUNTER TYPE A/D CONVERTER

In the fig 2.22 the counter is reset to zero count by reset pulse. After releasing the reset pulse the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time.

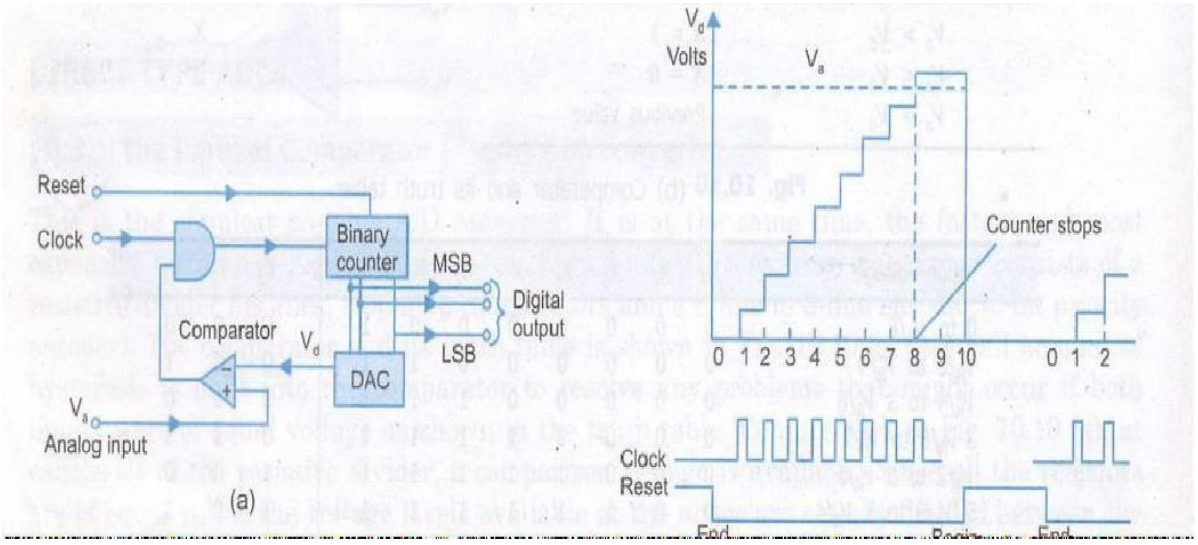


Fig 2.22: Countertype A/D converter

The binary word representing this count is used as the input of a D/A converter whose output is a stair case. The analog output Vd of DAC is compared to the analog input input Va by the comparator. If Va>Vd the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When Va<Vd the output of the comparator becomes low and the AND gate is disabled. This stops the counting we can get the digital data.

SERVO TRACKING A/D CONVERTER :

An improved version of counting ADC is the tracking or servo converter shown in fig 2.23. The circuit consists of an up/down counter with the comparator controlling the direction of the count.

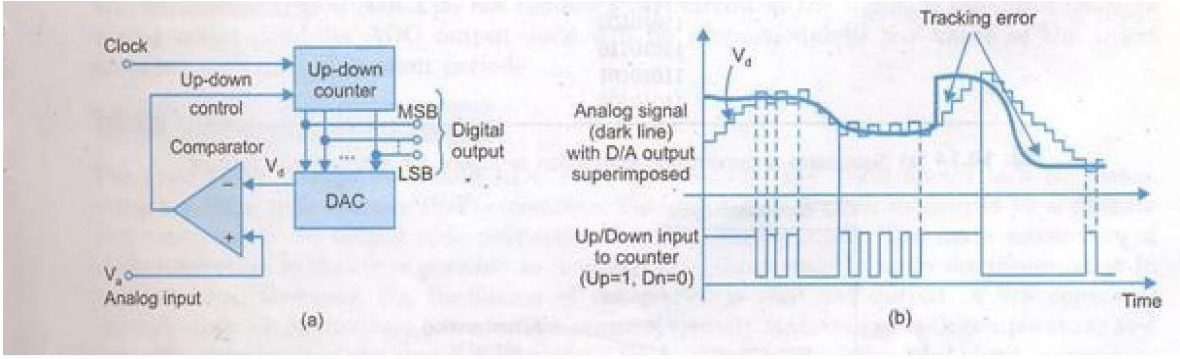


Fig: 2.23 (a) A tracking A/D converter (b) waveforms associated with a tracking A/D converter

The analog output of the DAC is Vd and is compared with the analog input Va. If the input Va is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up. The DAC output increases with each incoming clock pulse when it becomes more than Va the counter reverses the direction and counts down.

SUCCESSIVE-APPROXIMATION ADC:

One method of addressing the digital ramp ADC's shortcomings is the so-called successive- approximation ADC. The only change in this design as shown in the fig 2.19 is a very special counter circuit known as a successive-approximation register.

Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit. Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly. The way the register counts is identical to the "trial-and-fit" method of decimal-to-binary conversion, whereby different values of bits are tried from MSB to LSB to get a binary number that equals the original decimal number. The advantage to this counting strategy is much faster results: the DAC output converges on the analog signal input in much larger steps than with the 0-to-full count sequence of a regular counter.

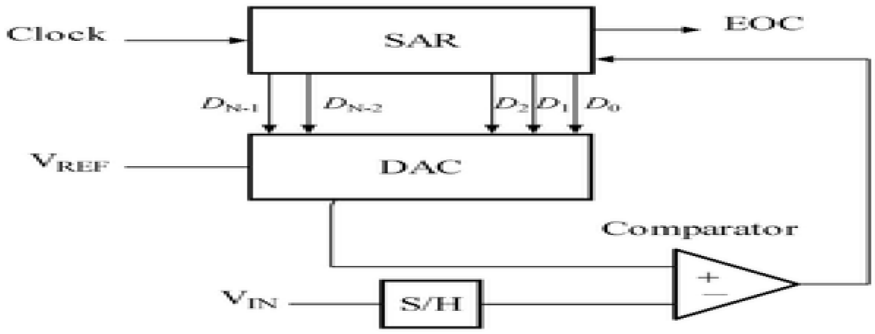


Fig: 2.24: Successive approximation ADC circuits

The successive approximation analog to digital converter circuit typically consists of four chief sub

1. A sample and hold circuit to acquire the input voltage (Vin).

2. An analog voltage comparator that compares Vin to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).

3. A successive approximation register sub circuit designed to supply an approximate digital code of Vin to the internal DAC.

4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with Vin.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds Vin the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

Mathematically, let Vin = xVref, so x in [-1, 1] is the normalized input voltage. The objective is to approximately digitize x to an accuracy of 1/2n. The algorithm proceeds as follows:

1. Initial approximation x0 = 0.

2. ith approximation xi = xi-1 - s(xi-1 - x)/2i.

where, s(x) is the signum-function(sgn(x)) (+1 for $x \geq 0$, -1 for $x < 0$). It follows using mathematical induction that $|xn - x| \leq 1/2n$.

As shown in the above algorithm, a SAR ADC requires:

1. An input voltage source Vin.

2. A reference voltage source Vref to normalize the input.

3. A DAC to convert the ith approximation xi to a voltage.

4. A Comparator to perform the function s(xi - x) by comparing the DAC's voltage with the input voltage.

5. A Register to store the output of the comparator and apply xi-1 - s(xi-1 - x)/2i.

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons.

For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary search.

The analogue value is rounded to the nearest binary value below, meaning

this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required. ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.

DUAL-SLOPE ADC

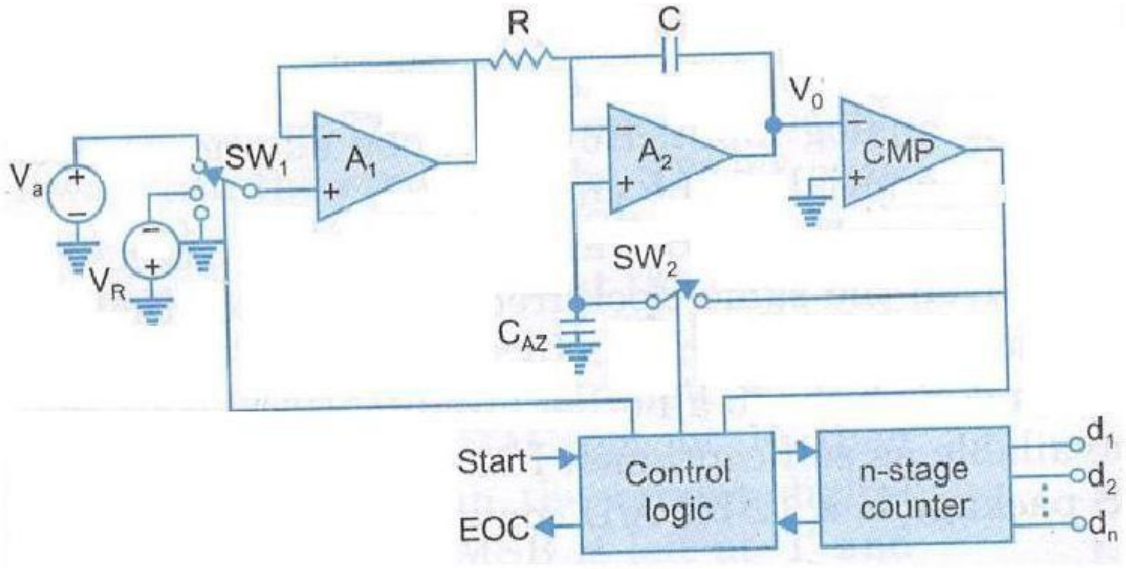


Fig 2.25 (a): Functional diagram of dual slope ADC

An integrating ADC (also **dual-slope** ADC) shown in fig 2.25 (a) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.

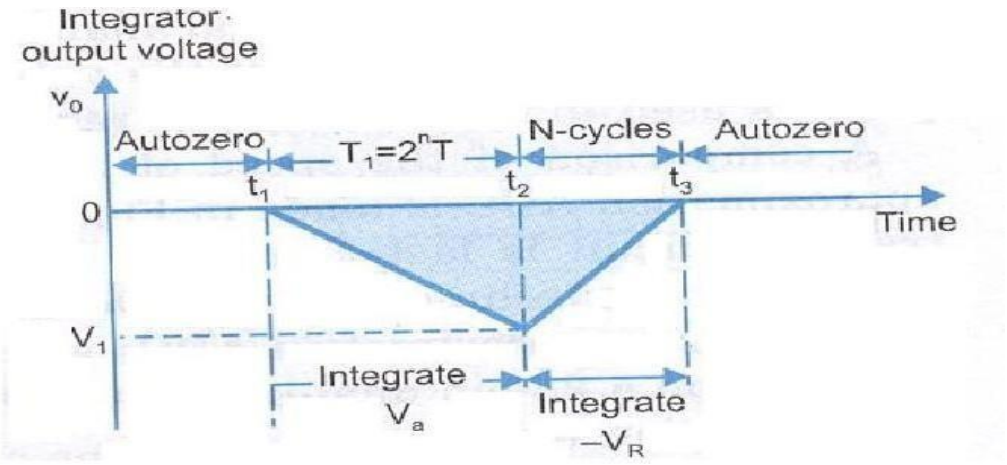


Fig 2.25 (b) o/p waveform of dual slope ADC

In operation the integrator is first zeroed (close SW2), then attached to the input (SW1 up) for a fixed time *M* counts of the clock (frequency 1/*t*). At the end of that time it is attached to the reference voltage (SW1 down) and the number of counts *N* which accumulate before the integrator reaches zero volts output and the comparator output changes are determined. The waveform of dual slope ADC is shown in fig 2.25 (b).

The equations of operation are therefore:

$$T_1 = t_2 - t_1 = \frac{2^n\ counts}{clock\ rate}$$

And

$$t_3 - t_2 = \frac{digitalcountN}{clockrate}$$

For an integrator,

The voltage Vo will be equal to V1 at the instant t2 and can be written as

$$V_1 = \frac{-1}{RC} V_a (t_2 - t_1) \qquad \Delta V_O = \frac{-1}{RC} V(\Delta t)$$

The voltage V1 is also given by

$$V_1 = \frac{-1}{RC}(-V_R)(t_2 - t_3)$$

So,

$$V_a(t_2 - t_1) = (V_R)(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and

$(t_3 - t_2) = N$ we get

$$V_a(2^n) = (V_R)N$$

Or,

$$V_a = (V_R)\left(\frac{N}{2^n}\right)$$

SPECIFICATIONS FOR DAC/ADC

1. RESOLUTION: The Resolution of a converter is the smallest change in voltage which may be produced at the output of the converter.

Resolution (in volts)=(VFS)/(2n-1)= 1 LSB increment

Ex: An 8-bit D/A converter have 28-1=255 equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range.

An 8-bit DAC is said to have: 8 bit resolution

: a resolution of 0.392 of full scale

: a resolution of 1 part in 255

Similarly the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output.

Ex: the input range of 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10V input range is 39.22 mV = (10V/255)

2. LINEARITY: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal characteristics.

3. GLITCHES (PARTICULARLY DAC): In transition from one digital input to the next, like 0111 to 1000, it may effectively go through 1111 or 0000, which produces ―unexpected‖ voltage briefly. If can cause problems elsewhere.

4. ACCURACY: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.

5. MONOTONIC: A monotonic DAC is the one whose analog output increases for an increase in digital input. It is essential in control applications. If a DAC has to be monotonic, the error should de lessthan ±(1/2) LSB at each output level.

6. SETTLING TIME: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input. It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Its

ranges from 100ns to 10μs.

7. STABILITY: The performance of converter changes with temperature, age and power supply variations. So the stability is required.

Successive Approximation Converter

The successive approximation technique uses a very e1ient code search strategy to complete n-bit conversion in just n-clock periods. An eight bit converter would require eight clock pulses to obtain a digital output. Figure 10.13 shows an eight bit converter. The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows. With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now compared with analog input V_a. If V is greater than the DAC output V_d then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

However, if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses V_a, the comparator changes state and this can be taken as the end of conversion (EOC) command. Figure 10.14 (a) shows a typical conversion sequence and Fig. 10.14 (b)

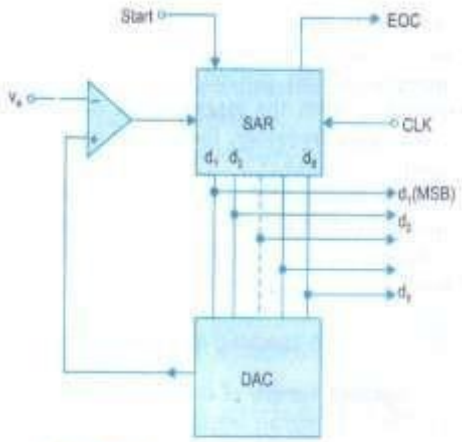


Fig. 10.13 Functional diagram of the successive approximation ADC

Correct digital representation	Successive approximation register output V_d at different stages in the conversion	Comparator output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 10.14 (a) Successive approximation conversion sequence for a typical analog input

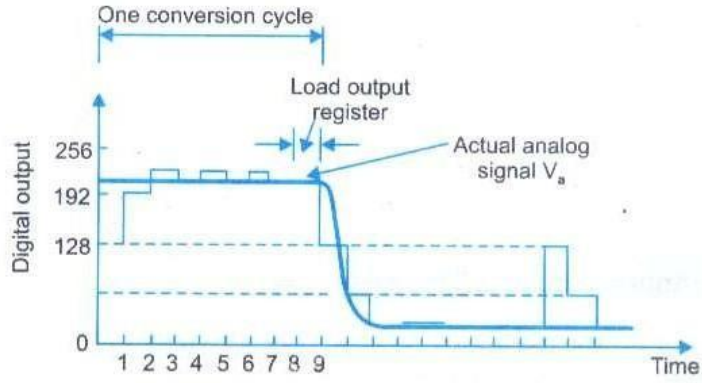


Fig. 10.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

shows the associated wave forms. It can be seen that the D/A output voltage becomes' successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in Fig. 10.15. Given the same clock frequency, we see that the tracking circuit is faster only for small changes in the input. In general, the successive approximation technique is more versatile and superior to all other circuits discussed so far. Successive approximation ADCs are available as self contained ICs. The AD7592 (Analog Devices Co.) a 28-pin dual-in-line CMOS package is a 12-bit AID converter using successive approximation technique.

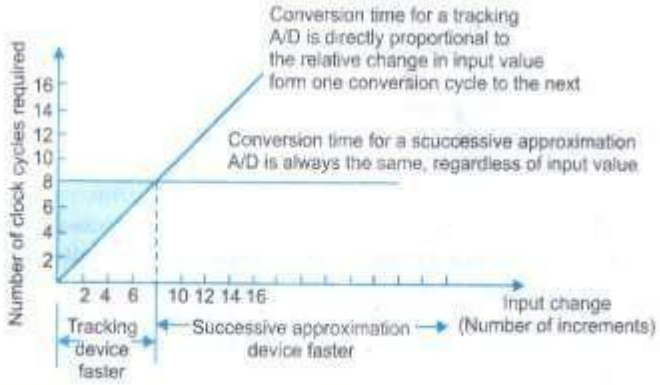


Fig. 10.15 Comparison of conversion times for tracking and successive approximation A/D devices

DAC/ADC SPECIFICATIONS

Both D/A and A/D converters are available with wide range of specifications. The various important specifications of converters generally specified by the manufacturers are analyzed. Resolution: The resolution of a converter is the smallest change in voltage which may he produced at the output (or input) of the converter. For example, an 8-bit D/A converter has 2^8-1 = 255 equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range. In short, the resolution is the value of the LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment} \qquad (10.8)$$

However, resolution is stated in a number of different ways. An 8-bit DAC is said to have

:8 bit resolution
: a resolution of 0.392 of full-scale
: a resolution of 1 part in 255

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. As an example, the input range of an 8-bit AID converter is divided into 255 intervals. So the resolution for a 10 V input range is 39.22 mV (= 10 V/255). Table 10.1 gives the resolution for 6-16 bit DACs.

Table 10.1 Resolution for 6–16 bit DACs

Bits	Intervals	LSB size (% of Full Scale)	LSB size (10 V Full Scale)
6	63	1.588%	158.8 mV
8	256	0.392%	39.2 mV
10	1023	0.0978%	9.78 mV
12	4095	0.0244%	2.44 mV
14	16383	0.0061%	0.61 mV
16	65535	0.0015%	0.15 mV

Linearity: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. However, in an actual DAC, output voltages do not fall on a straight line because of gain and offset errors as shown by the solid line curve in Fig. 10.17. The static performance of a DAC is determined by fitting a straight line through the measured output points. The linearity error measures the deviation of the actual output from the fitted line and is given by €/Δ as shown in Fig. 10.17. The error is uua1ly expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ± (1/2) LSB.

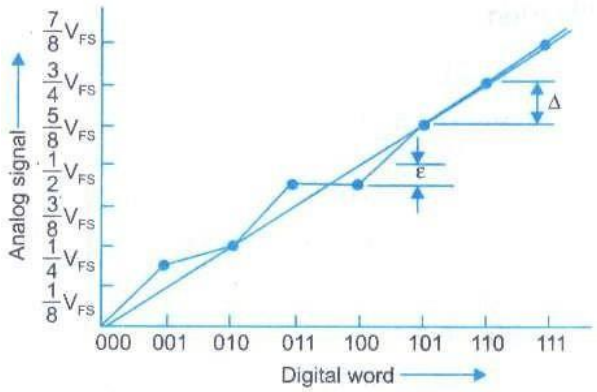


Fig. 10.17 Linearity error for 3-bit DAC

Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. Data sheets normally specie relative accuracy rather than absolute accuracy. The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

Monotonicity: A monotonic DAC is the one whose analog output increases for an increase in digital input. Figure 10.18 represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications, otherwise oscillations can result. In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes.

If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. All the commercially available DACs are monotonic because the linearity error never exceeds ± (1/2) LSB at each output level.

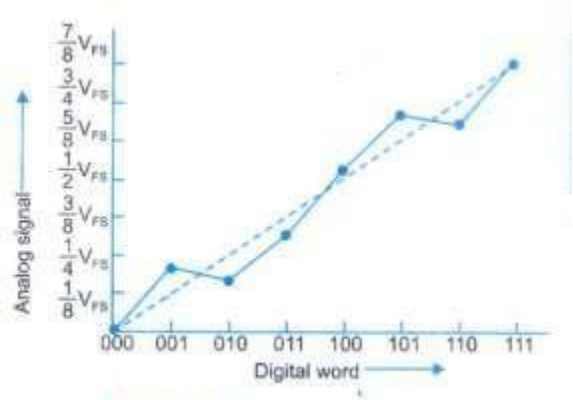


Fig. 10.18 A non-monotonic 3-bit DAC

Settling time: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (usually a full ca1e change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10 is depending on word length and type of circuit used.

Stability: The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

A brief overview of ADC and DAC selection guide is given below:

A/D converters:	
AD 7520/AD 7530	10-bit binary multiplying type
AD 7521/AD 7531	12-bit binary multiplying type
ADC 0800/0801/0802	8-bit ADC
D/A converters:	
DAC 0800/0801/0802	8-bit DAC
DAC 0830/0831/0832	microprocessor compatible 8-bit DAC
DAC 1200/1201	12-bit DAC
DAC 1208/1209/1210	12-bit microprocessor compatible DAC

UNIT-V

Digital IC Applications

CLASSIFICATION OF IC 'S:

Integrated Circuit is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.

Based on mode of operation

a. Digital IC's

b. Linear IC's

Digital IC's: Digital IC's are complete functioning logic networks that are equivalents of basic transistor logic circuits.

Ex:- gates ,counters, multiplexers, de-multiplexers, shift registers.

Linear IC's: Linear IC's are equivalents of discrete transistor networks, such as amplifiers, filters, frequency multipliers, and modulators that often require additional external components for satisfactory operation.

Based on fabrication

a. Monolithic IC's

b. Hybrid IC's

a. Monolithic IC's : In monolithic ICs all components (active and passive) are formed simultaneously by a diffusion process. Then a metallization process is used in interconnecting these components to form the desired circuit.

b. Hybrid IC's: .In hybrid ICs, passive components (such as resistors and capacitors) and the interconnections between them are formed on an insulating substrate. The substrate is used as a chassis for the integrated components. Active components such as transistors and diodes as well as monolithic integrated circuits, are then connected to form a complete circuit.

4.1.3. Based on number of components integrated on IC's

a. SSI <10 components

b. MSI <100 components

c. LSI >100 components

d. VLSI >1000 components

CHIP SIZE AND CIRCUIT COMPLEXITY:

Invention of transistor	1948
Development of silicon transistor	1955-1959
Silicon planar technology	1959
First IC, Small Scale Integration (SSI),3 to 30 gates/chip	1960
Medium Scale Integration (MSI), 30 to 300 gates/chip	1965-1970
Large Scale Integration (LSI), 300 to 3000 gates/chip	1970-1975
Very Large Scale Integration (VLSI) more than 3000 gates/chip	1975

An integrated circuit or monolithic integrated circuit (also referred to as IC, chip, or microchip) is an electronic circuit. Integrated circuits are used in virtually all electronic equipment today and have revolutionized the world of electronics. Computers, cell phones, and other digital appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of production of integrated circuits. There are two main advantages of ICs over discrete circuits: cost and performance. Cost is low because the chips, with all their components, are printed as a unit by photolithography rather than being constructed one transistor at a time. Furthermore, much less material is used to construct a packaged IC die than to construct a discrete circuit. Performance is high because the components switch quickly and consume little power (compared to their discrete counterparts) as a result of the small size and close proximity of the components.

CLASSIFICATION OF INTEGRATED CIRCUITS

Classification of ICs based on complexity:

- Small Scale Integration or (SSI) - Contain up to 10 transistors or a few gates within a single package such as AND, OR, NOT gates.
- Medium Scale Integration or (MSI) - between 10 and 100 transistors or tens of gates within a single package and perform digital operations such as adders, decoders, counters, flip-flops and multiplexers.
- Large Scale Integration or (LSI) - between 100 and 1,000 transistors or hundreds of gates and perform specific digital operations such as I/O chips, memory, arithmetic and logic units.
- Very-Large Scale Integration or (VLSI) - between 1,000 and 10,000 transistors or thousands of gates and perform computational operations such as processors, large memory arrays and programmable logic devices.

- Super-Large Scale Integration or (SLSI) - between 10,000 and 100,000 transistors within a single package and perform computational operations such as microprocessor chips, micro-controllers, basic PICs and calculators.
- Ultra-Large Scale Integration or (ULSI) - more than 1 million transistors - the big boys that are used in computers CPUs, GPUs, video processors, micro-controllers, FPGAs and complex PICs.

While the "ultra large scale" ULSI classification is less well used, another level of integration which represents the complexity of the Integrated Circuit is known as the **System-on-Chip** or (**SOC**) for short. Here the individual components such as the microprocessor, memory, peripherals, I/O logic etc, are all produced on a single piece of silicon and which represents a whole electronic system within one single chip, literally putting the word "integrated" into integrated circuit. These chips are generally used in mobile phones, digital cameras, micro-controllers, PICs and robotic applications, and which can contain up to 100 million individual silicon-CMOS transistor gates within one single package.

Classification of integrated circuits based on the signal processed:

- DIGITAL INTEGRATED CIRCUITS

Digital integrated circuits, primarily used to build computer systems, also occur in cellular phones, stereos and televisions. Digital integrated circuits include microprocessors, microcontrollers and logic circuits. They perform mathematical calculations, direct the flow of data and make decisions based on Boolean logic principles. The Boolean system used centers on on two numbers: 0 and 1.

- ANALOG INTEGRATED CIRCUITS

Analog integrated circuits most commonly make up a part of power supplies, instruments and communications. In these applications, analog integrated circuits amplify, filter and modify electrical signals. In cellular phones, they amplify and filter the incoming signal from the phone's antenna. The sound encoded into that signal has a low amplitude level; after the circuit filters the sound signal from the incoming signal, the circuit amplifies the sound signal and sends it to the speaker in your cell phone, allowing you to hear the voice on the other end.

- MIXED-SIGNAL INTEGRATED CIRCUITS

Mixed-signal circuits occur in cellular phones, instrumentation, motor and industrial control applications. These circuits convert digital signals to analog signals, which in turn set the

speed of motors, the brightness of lights and the temperature of heaters, for example. They also convert digital signals to sound waveforms, allowing for the design of digital musical instruments such as electronic organs and computer keyboards capable of playing music.

Mixed-signal integrated circuits also convert analog signals to digital signals. They will convert analog voltage levels to digital number representations of the voltage level of the signals. Digital integrated circuits then perform mathematical calculations on these numbers.

- MEMORY-INTEGRATED CIRCUITS

Though primarily used in computer systems, memory-integrated circuits also occur in cellular phones, stereos and televisions. A computer system may include 20 to 40 memory chips, while other types of electronic systems may contain just a few. Memory circuits store information, or data, as two numbers: 0 and 1. Digital integrated circuits will often retrieve these numbers from memory and perform calculations with them, then save the calculation result a memory chip's data storage locations. The more data it accesses---pictures, sound and text---the more memory an electronic system will require.

INTRODUCTION TO DIGITAL LOGIC GATES

A **Digital Logic Gate** is an electronic device that makes logical decisions based on the different combinations of digital signals present on its inputs. A digital logic gate may have more than one input but only has one digital output. Standard commercially available digital logic gates are available in two basic families or forms:

- *Transistor-Transistor Logic*(TTL) such as the 7400 series, and
- *Complementary Metal-Oxide-Silicon (CMOS)* which is the 4000 series of chips.

This notation of TTL or CMOS refers to the logic technology used to manufacture the integrated circuit, (IC).**TTL** IC's use NPN (or PNP) type *Bipolar Junction Transistors* while **CMOS** IC's use *Field Effect Transistors* or FET's for both their input and output circuitry.

Digital Logic States

In digital logic design only two voltage levels or states are allowed and these states are generally referred to as Logic "1" and Logic "0", High and Low. Most *digital logic gates* and logic systems use "Positive logic", in which a logic level "0" or "LOW" is represented by a zero voltage, 0v or ground and a logic level "1" or "HIGH" is represented by a higher voltage such as +5 volts, There also exists a complementary "Negative Logic" system in which the values and the rules of a logic "0" and a logic "1" are reversed but in this tutorial section about digital logic gates we shall only refer to the positive logic convention as it is the most commonly used.

STANDARD TTL-NAND GATE ANALYSIS AND CHARACTERISTICS

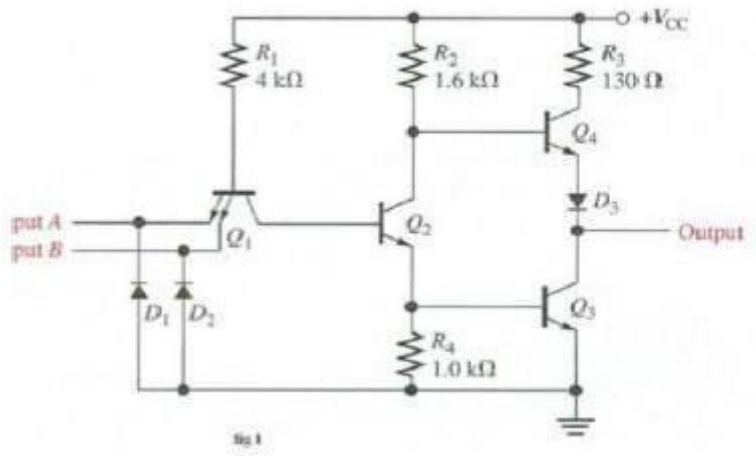


Fig 4.1: Two input TTL NAND gate

A two input TTL NAND gate is shown in fig 6.1. In standard TTL (transistor-transistor logic) IC's there is a pre-defined voltage range for the input and output voltage levels which define exactly what is a logic "1" level and what is a logic "0" level and these are shown below. **Transistor–transistor logic** (**TTL**) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called *transistor–transistor logic* because both the logic gating function (e.g., AND) and the amplifying function are performed by transistors (contrast with RTL and DTL). TTL inputs are the emitters of a multiple-emitter transistor. This IC structure is functionally equivalent to multiple transistors where the bases and collectors are tied together. The output is buffered by a common emitter amplifier.

Input logical ones:

When all the inputs are held at high voltage, the base–emitter junctions of the multiple-emitter transistor are backward-biased. In contrast with DTL, small (about 10 μA) "collector" currents are drawn by the inputs since the transistor is in a reverse-active mode (with swapped collector and emitter). The base resistor in combination with the supply voltage acts as a substantially constant current source.It passes current through the base–collector junction of the multiple-emitter transistor and the base–emitter junction of the output transistor thus turning it on; the output voltage becomes low (logical zero).

Input logical zero:

If one input voltage becomes zero, the corresponding base–emitter junction of the multiple-emitter transistor connects in parallel to the two connected in series junctions (the base–collector junction of the multiple-emitter transistor and the base–emitter junction of the second transistor). The input base–emitter junction steers all the base current of the output

transistor to the input source (the ground). The base of the output transistor is deprived of current causing it to go into cut-off and the output voltage becomes high (logical one). During the transition the input transistor is briefly in its active region; so it draws a large current away from the base of the output transistor and thus quickly discharges its base. This is a critical advantage of TTL over DTL that speeds up the transition over a diode input structure.

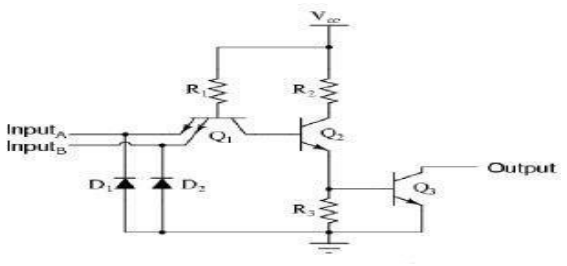
Disadvantage of TTL:

The main disadvantage of TTL with a simple output stage is the relatively high output resistance at output logical "1" that is completely determined by the output collector resistor. It limits the number of inputs that can be connected (the fanout). Some advantage of the simple output stage is the high voltage level (up to VCC) of the output logical "1" when the output is not loaded.

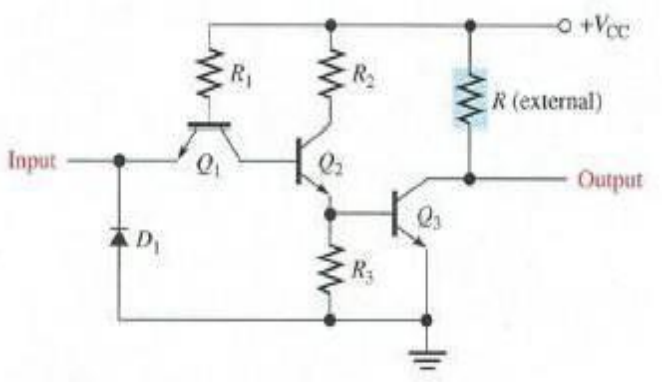
TTL OPEN COLLECTOR OUTPUTS

An **open collector** is a common type of output found on many integrated circuits (IC). Instead of outputting a signal of a specific voltage or current, the output signal is applied to the base of an internal NPN transistor whose collector is externalized (open) on a pin of the IC. The emitter of the transistor is connected internally to the ground pin. If the output device is a MOSFET the output is called **open drain** and it functions in a similar way.

An open collector inverter circuit is shown in the fig 6.2. In the single-input (inverter) circuit, shown in fig 4.2 grounding the input resulted in an output that assumed the "high" (1) state. In the case of the open-collector output configuration, this "high" state was simply "floating." Allowing the input to float (or be connected to Vcc) resulted in the output becoming grounded, which is the "low" or 0 state. Thus, a 1 in resulted in a 0 out, and vice versa. Since this circuit bears so much resemblance to the simple inverter circuit, the only difference being a second input terminal connected in the same way to the base of transistor Q2, we can say that each of the inputs will have the same effect on the output. Namely, if either of the inputs is grounded, transistor Q2 will be forced into a condition of cutoff, thus turning Q3 off and floating the output (output goes "high"). The following series of illustrations shows this for three input states (00, 01, and 10):



When Q3 is OFF, the output is pulled up to Vcc through the external resistor. When Q3 is ON, the output is connected to near-ground through the saturated transistor



TRISTATE TTL GATES:

In digital electronics three-**state**, **tri-state**, or **3-state**logic allows an output port to assume a high impedance state in addition to the 0 and 1 logic levels, effectively removing the output from the circuit. This allows multiple circuits to share the same output line or lines (such as a bus).

Three-state outputs are implemented in many registers, bus drivers, and flip-flops in the 7400 and 4000 series as well as in other types, but also internally in many integrated circuits. Other typical uses are internal and external buses in microprocessors, memories, and peripherals. Many devices are controlled by an active-low input called OE (Output Enable) which dictates whether the outputs should be held in a high-impedance state or drive their respective loads (to either 0- or 1- level).

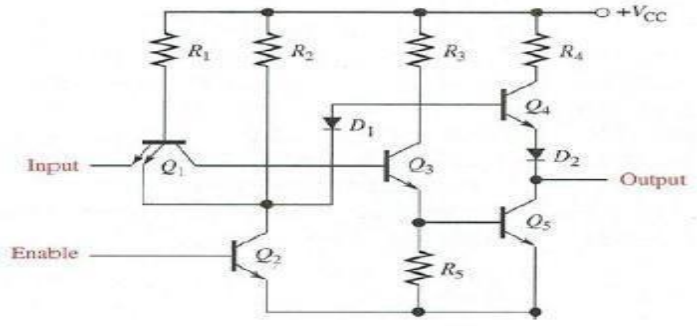


Fig 4.2: Tristate TTL Gate

Fig shows the basic circuit for a TTL tri-state inverter. When the enable input is LOW, Q2 is OFF, and the output circuit operates as a normal totem-pole configuration, in which the

output state depends on the input state. When the enable input is HIGH, Q2 is ON. There is thus a LOW on the second emitter of Q1, causing Q3 and Q5 to turn OFF, and diode D1 is forward biased, causing Q4 also to turn OFF. When both totem-pole transistors are OFF, they are effectively open, and the output is completely disconnected from the internal circuitry.

BASIC CMOS DIGITAL LOGIC GATE

One of the main disadvantages of the TTL logic series is that the gates are based on bipolar transistor logic technology and as transistors are current operated devices, they consume large amounts of power from a fixed +5 volt power supply. Also, TTL bipolar transistor gates have a limited operating speed when switching from an "OFF" state to an "ON" state and vice-versa called the "gate" or "propagation delay". To overcome these limitations complementary MOS called "CMOS" logic gates using "Field Effect Transistors" or FET's were developed.

As these gates use both P-channel and N-channel MOSFET's as their input device, at quiescent conditions with no switching, the power consumption of CMOS gates is almost zero, (1 to 2uA) making them ideal for use in low-power battery circuits and with switching speeds upwards of 100MHz for use in high frequency timing and computer circuits.

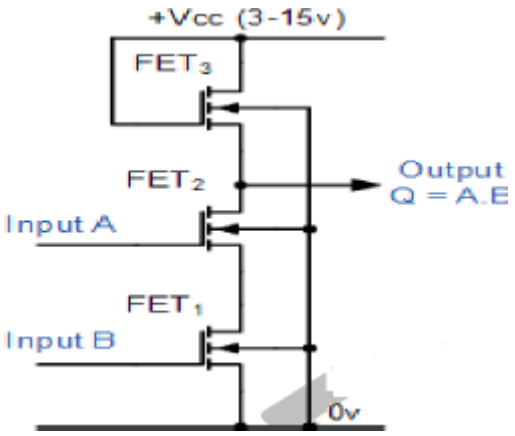


Fig 4.4: 2-input NAND gate

This CMOS gate example contains 3 N-channel MOSFET's, one for each input FET1 and FET2 and one for the output FET3. When both the inputs A and B are at logic level "0", FET1 and FET2 are both switched "OFF" giving output logic "1" from the source of FET3. When one or both of the inputs are at logic level "1" current flows through the corresponding FET giving an output state at Q equivalent to logic "0", thus producing a NAND gate function.

For example, CMOS NAND gate:

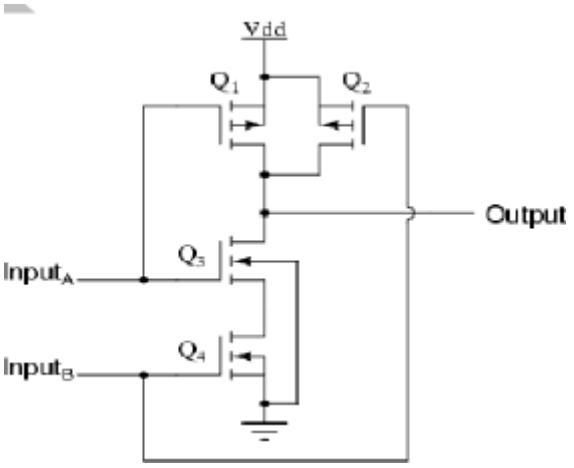


Fig 4.5: CMOS NAND gate

In fig the transistors Q1 and Q3 are series-connected complementary pair from the inverter circuit. Both are controlled by the same input signal (input A), the upper transistor turning off and the lower transistor turning on when the input is "high" (1), and vice versa. The transistors Q2 and Q4 are similarly controlled by the same input signal (input B), and how they will also exhibit the same on/off behaviour for the same input logic levels. The upper transistors of both pairs (Q1 and Q2) have their source and drain terminals paralleled, while the lower transistors (Q3 and Q4) are series-connected. What this means is that the output will go "high" (1) if *either* top transistor saturates, and will go "low" (0) only if *both* lower transistors saturate. The following sequence of illustrations shows the behaviour of this NAND gate for all four possibilities of input logic levels (00, 01, 10, and 11):

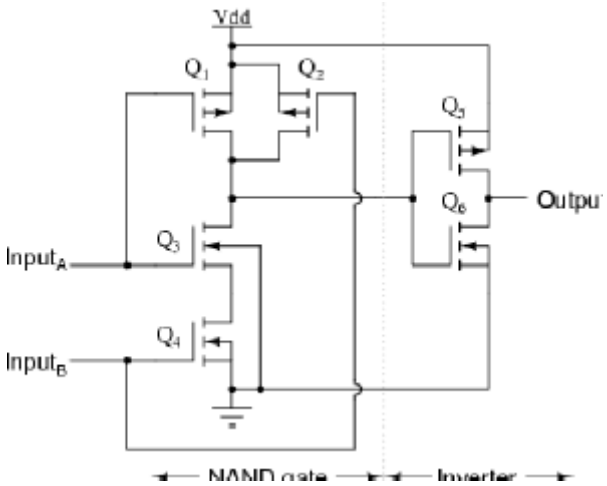


Fig 4.6: CMOS AND gate

A CMOS NOR gate circuit (fig 6.8) uses four MOSFETs just like the NAND gate, except that its transistors are differently arranged. Instead of two paralleled *sourcing* (upper) transistors

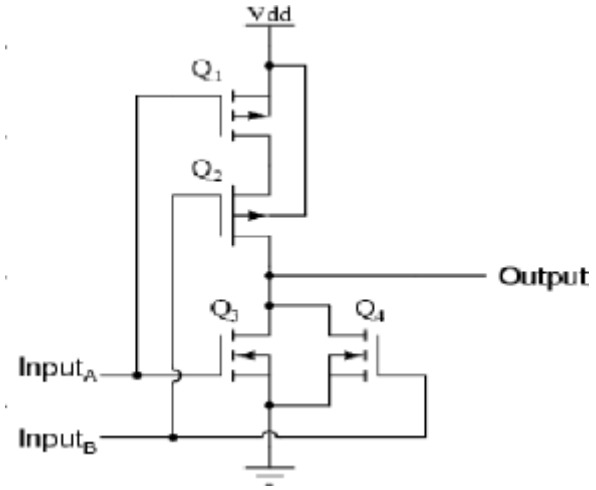


Fig 4.7: CMOS NOR Gate

connected to Vdd and two series-connected *sinking* (lower) transistors connected to ground, the NOR gate uses two series-connected sourcing transistors and two parallel-connected sinking transistors like this: As with the NAND gate, transistors Q1 and Q3 work as a complementary pair, as do transistors Q2 and Q4. Each pair is controlled by a single input signal. If *either* input A *or* input B are "high" (1), at least one of the lower transistors (Q3 or Q4) will be saturated, thus making the output "low" (0). Only in the event of *both* inputs being "low" (0) will both lower transistors be in cutoff mode and both upper transistors be saturated, the conditions necessary for the output to go "high" (1). This behavior, of course, defines the NOR logic function.

The OR function may be built up from the basic NOR gate with the addition of an inverter stage on the output (fig 4.8):

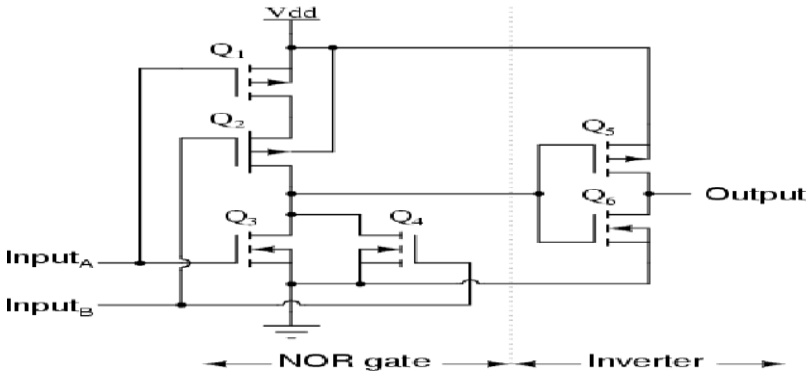
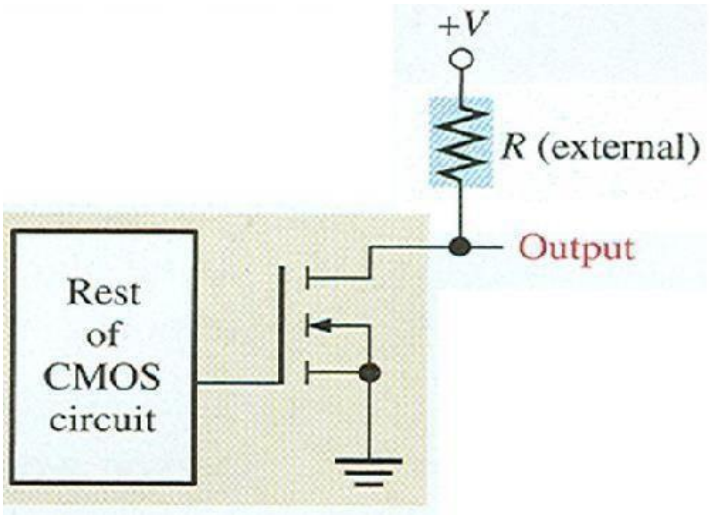


Fig 4.8: CMOS OR Gate

OPEN DRAIN CMOS



The term open drain means that the drain terminal of the output transistor is unconnected and must be connected externally to VDD through a load.

An open-drain output circuit is a single n-channel MOSFET as shown in fig 6.10. It is used to produce a HIGH output state.

CMOS TRISTATE OUTPUTS

The tri-state output combines the advantages of the totem-pole and open-collector circuits.

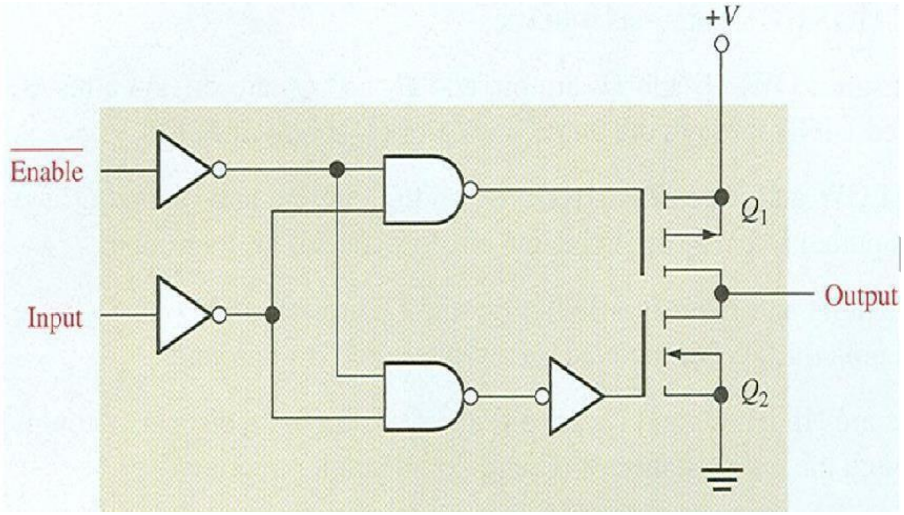


Fig 4.9:CMOS Tristate outputs

From the fig 6.11 when the enable input is LOW, the device is enabled for normal logic operation. When the enable is HIGH both Q1 and Q2 are OFF and the circuit is in the high Z-state.

COMPARISION OF VARIOUS LOGIC FAMILIES

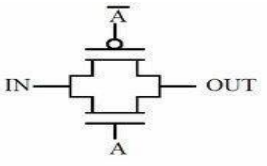
	Bipolar(TTL)			CMOS					
					5V			3.3V	
	F	LS	ALS	HC	AC	AHC	LV	LVC	ALVC
speed									
t_p(ns)	3.3	10	7	7	5	3.7	9	4.3	3
Max.clock Freq(MHz)	145	33	45	50	160	170	90	100	150
power dissipation per gate TTL(mW) CMOS(µW)	6	2.2	1.4	2.75	0.55	2.75	1.6	0.8	0.8
Output drive(mA)	20	8	8	4	24	8	12	24	24

	BIPOLAR(TTL)	CMOS	BIPOLAR(ECL)	
	F	AHC	10H	E-LITE
speed				
t_p(ns)	3.3	3.7	1	0.22
Max.clock Freq(MHz)	145	170	330	2800
s power dissipation per gate	8.9mW	2.5µW	25mW	73mW

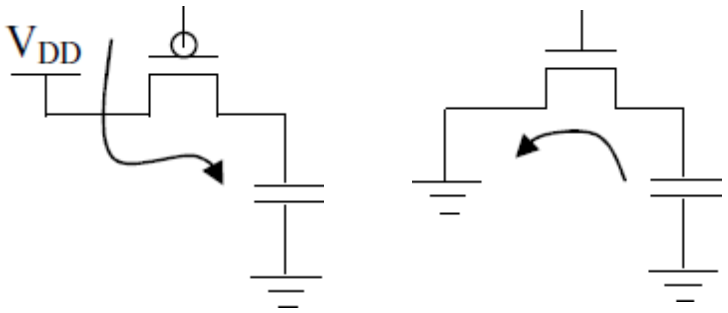
Where tp is the propagation delay in ns.

CMOS Transmission Gates:

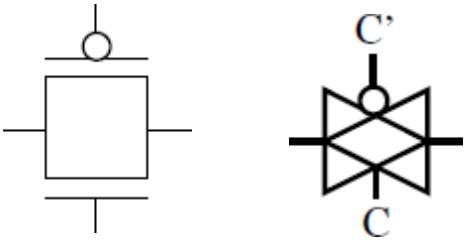
A Transmission Gate (TG) is a complementary CMOS switch.



PMOS and NMOS are in parallel and are controlled by complementary signals. Both transistors are ON or OFF simultaneously. The NMOS switch passes a good zero but a poor The PMOS switch passes a good one but a poor 0. Combining them we get a good 0 and a good 1 passed in both directions.



Circuit Symbols for TGs:

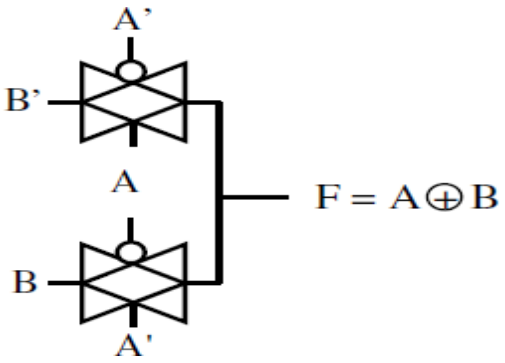


TGs are efficient in implementing some functions such as multiplexers, XORs, XNORs, latches, and Flip-Flops.

2 I./P XOR using TGs:

F = A.B' + A'.B , we need this: if A=1 _ F = B' (pass B' to F)

if A=0 _ F = B (pass B to F) using TGs:

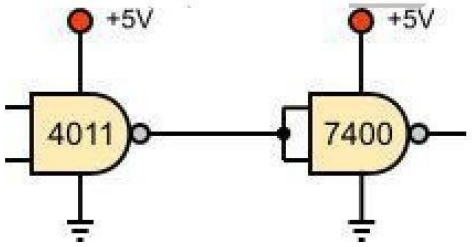


8 Ts (2 inverters for A and B and two TGs) Versus 12 Ts for regular CMOS.

IC INTERFACING-CMOS DRIVING TTL AND CMOS DRIVING TTL

Interfacing ICs under 5Volts power supply

1) Interfacing a CMOS to a TTL under 5Volts power supply



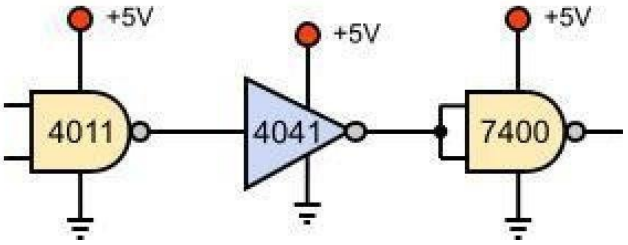


Fig 4.11(a) Fig 4.11(b)

Fig 4.11 showing interfacing CMOS to TTL

The high state of the CMOS output is enough to drive directly a TTL input into high state without problems. The low state, could cause malfunctions in some cases. Is it possible to sink a TTL input current into low state without exceeding the maximum value of the TTL low state input voltage? Typical CMOS gates are specified to sink about 0.4 mA in the low state while maintaining an output voltage of 0.4 volts or less, sufficient to drive two LS TTL inputs or one Schottky input (Fig. 6.12.a), but insufficient to drive standard TTL. In this case, a 4041 buffer (or another buffer) should be used to eliminate this problem (Fig. 6.12.b).

2) Interfacing a TTL to a CMOS under 5Volts power supply

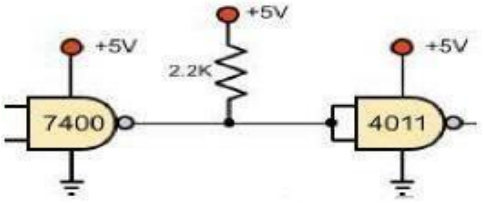


Fig. 4.12: interfacing TTL to CMOS

Interfacing ICs with different power supply voltages:

1) Interfacing a CMOS to a TTL with different power supply voltages

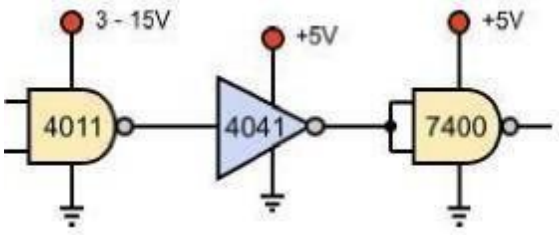


Fig. 4.13: Interfacing a CMOS to a TTL with different power supply voltages

TTL with different voltages (fig 6.14) is as easy as with same voltages. The reason is because the CMOS can be supplied also with 5V like the TTL. So, a 4041 buffer can be powered with 5V to do the interface. In the following drawing, the 4041 could be omitted if the 4011 was supplied with 5V.

2) Interfacing a TTL to a CMOS with different power supply voltages

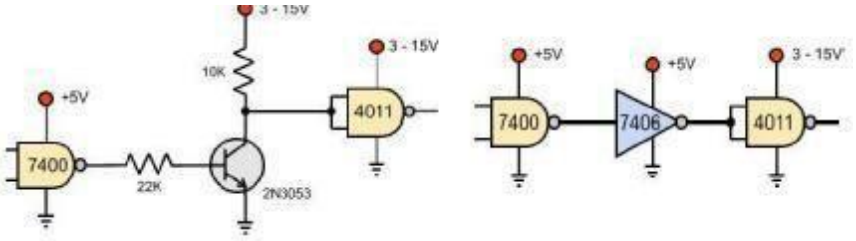


Fig 4.15 (a and b): Interfacing a TTL to a CMOS with different power supply voltages

In this case, a use of NPN transistor a essential to implement the interface (Fig. 6.15.a). The base of the transistor is controlled by the output of the TTL chip. When it is in low state, the collector voltage is nearly the CMOS voltage. When the TTL output is driven into high state, the transistor is driven into saturation causing the CMOS input to become nearly 0. This interface is also causing an inversion of the signal so be sure that you have this in mind during designing.

Another technique is the use of an open collector TTL buffer like 7406 (Fig.6.5.b). This technique is useful if you have multiple outputs to interface. The 7406 VDD pins are connected to the TTL's power line (5V)

Decoders

A *decoder* is a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. The input code generally has fewer bits than the output code, and there is a one-to one mapping from input code words into output code words. In a *one-to-one mapping*, each input code word produces a different output code word.

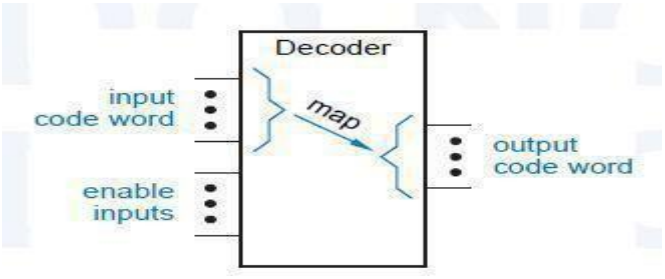


Fig 5.1: Decoder

The general structure of a decoder circuit is shown. The enable inputs, if present, must be asserted for the decoder to perform its normal mapping function. Otherwise, the decoder maps all input code words into a single, ―disabled,‖ output code word.

The most commonly used output code is a 1-out-of-*m* code, which contains *m* bits, where one bit is asserted at any time. Thus, in a 1-out-of-4 code with active-high outputs, the code words are 0001, 0010, 0100, and 1000. With active-low outputs, the code words are 1110, 1101, 1011, and 0111.

Binary Decoders

The most common decoder circuit is an *n*-to-2*n* decoder or *binary decoder*. Such a decoder has an *n*-bit binary input code and a 1-out-of-2*n* output code. A binary decoder is used when you need to activate exactly one of 2*n* outputs based on an *n*-bit input value.

Inputs			*Outputs*			
EN	I1	I0	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Table 1: 2 to 4 decoder

Table 1 is the truth table of a 2-to-4 decoder. The input code word 1,I0 represents an integer in the range 0–3. The output code word Y3,Y2,Y1,Y0 has Y*i* equal to 1 if and only if the input code word is the binary representation of *i* and the *enable input* EN is 1. If EN is 0, then all of the outputs are 0. A gate-level circuit for the 2-to-4 decoder is shown in Figure 2 Each AND gate *decodes* one combination of the input code word I1, I0.

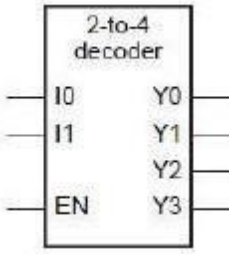


Fig 5.2: 2 to 4 decoder logic symbol

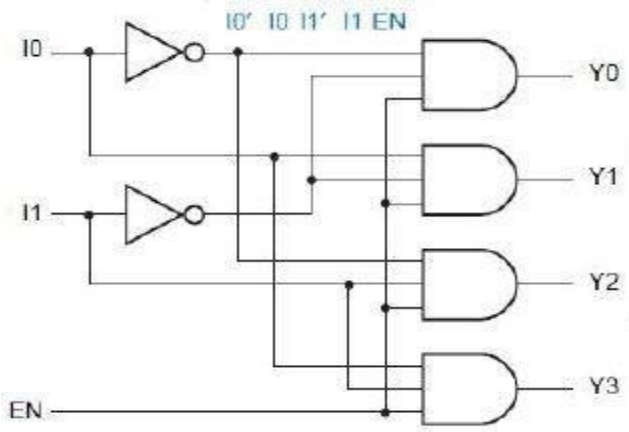


Fig 5.3: logic diagram of 2 to 4 decoder

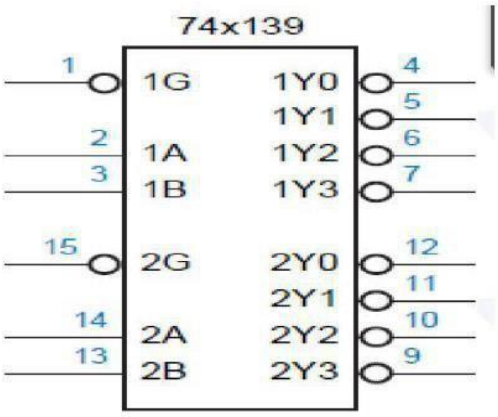
The 74x139 Dual 2-to-4 Decoder

Two independent and identical 2-to-4 decoders are contained in a single MSI part, the *74x139*. The gate-level circuit diagram for this IC is shown in Figure 5.

1. The outputs and the enable input of the ’139 are active-low.

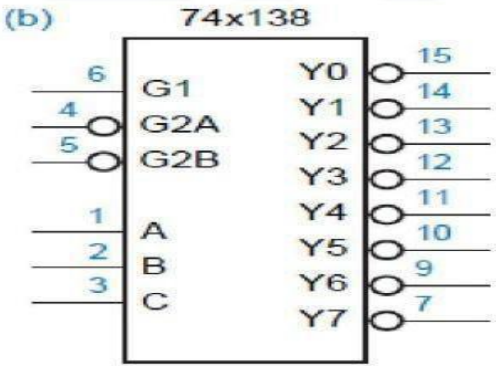
2. Most MSI decoders were originally designed with active-low outputs, since TTL inverting gates are generally faster than non inverting ones.

3. ’139 has extra inverters on its select inputs. Without these inverters, each select input would present three AC or DC loads instead of one, consuming much more of the fan-out budget of the device that drives it. In this case, the assignment of the generic function to one half or the other of a particular ’139 package can be deferred until the schematic is completed Table 5-6 is the truth table for a 74x139-type decoder.



The 74x138 3-to-8 Decoder

The *74x138* is a commercially available MSI 3-to-8 decoder whose gate-level circuit diagram and symbol are shown in Figure 7; its truth table is given in Table 5-7. Like the 74x139, the 74x138 has active-low outputs, and it has three enable inputs (G1, /G2A, /G2B), all of which must be asserted for the selected output to be asserted.



. Fig 5.4: logic symbol of 74X138

Inputs						*Outputs*							
G1	G2A_L	G2B_L	C	B	A	Y7_L	Y6_L	Y5_L	Y4_L	Y3_L	Y2_L	Y1_L	Y0_L
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

Fig 5.5: Truth Table of 74X138 3 to 8 decoder

The logic function of the ’138 is straightforward—an output is asserted if and only if the decoder is enabled and the output is selected. Thus, we can easily write logic equations for an internal output signal such as Y5 in terms of the internal input signals:

$$Y5 = \underbrace{G1 \cdot G2A \cdot G2B}_{\text{enable}} \cdot \underbrace{C \cdot B' \cdot A}_{\text{select}}$$

However, because of the inversion bubbles, we have the following relations between internal and external signals:

$$\begin{aligned} G2A &= G2A\_L' \\ G2B &= G2B\_L' \\ Y5 &= Y5\_L' \end{aligned}$$

Therefore, if we’re interested, we can write the following equation for the external output signal Y5_L in terms of external input signals:

$$\begin{aligned} Y5\_L = Y5' &= (G1 \cdot G2A\_L' \cdot G2B\_L' \cdot C \cdot B' \cdot A)' \\ &= G1' + G2A\_L + G2B\_L + C' + B + A' \end{aligned}$$

On the surface, this equation doesn’t resemble what you might expect for a decoder, since it is a logical sum rather than a product. However, if you practice bubble-to-bubble logic design, you don’t have to worry about this; you just give the output signal an active-low name and remember that it’s active low when you connect it to other inputs.

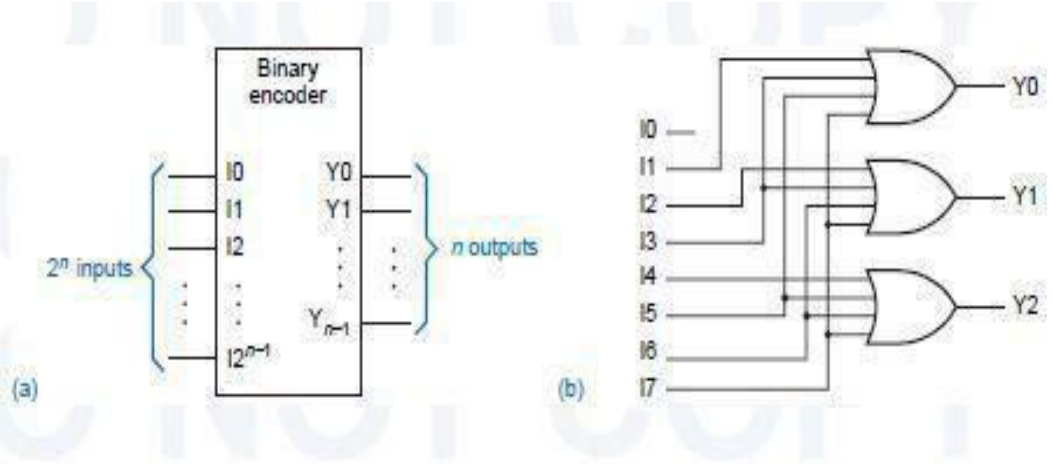
Encoders

A decoder’s output code normally has more bits than its input code. If the device’s output code has *fewer* bits than the input code, the device is usually called an *encoder*.

Probably the simplest encoder to build is a 2*n*-to-*n* or *binary encoder*. As shown in Figure 5-45(a), it has just the opposite function as a binary *de*coder— its input code is the 1-out-of-2*n* code and its output code is *n*-bit binary. The equations for an 8-to-3 encoder with inputs I0–I7 and outputs Y0–Y2 are given below:

$$\begin{aligned} Y0 &= I1 + I3 + I5 + I7 \\ Y1 &= I2 + I3 + I6 + I7 \\ Y2 &= I4 + I5 + I6 + I7 \end{aligned}$$

The corresponding logic circuit is shown in (b). In general, a 2*n*-to-*n* encoder can be built from *n* 2*n* 1-input OR gates. Bit *i* of the input code is connected to OR gate *j* if bit *j* in the binary representation of *i* is 1.



Priority Encoders

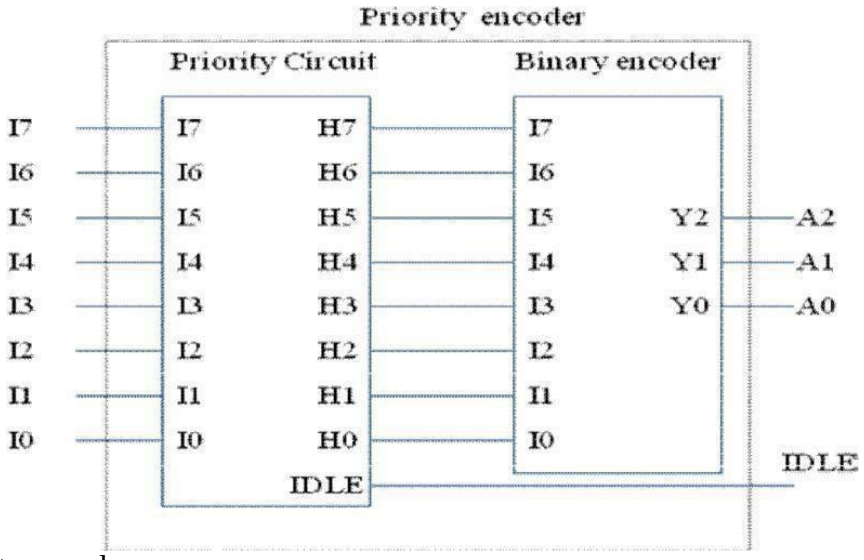
The 1-out-of-2*n* coded outputs of an *n*-bit binary decoder are generally used to control a set of 2*n* devices, where at most one device is supposed to be active at any time. Conversely, consider a system with 2*n inputs*, each of which indicates a request for service. This structure is often found in microprocessor input/output subsystems, where the inputs might be interrupt requests.

In this situation, it may seem natural to use a binary encoder. to observe the inputs and indicate which one is requesting service at any time. However, this encoder works properly only if the inputs are guaranteed to be asserted at most one at a time. If multiple requests can be made simultaneously, the encoder gives undesirable results. For example, suppose that inputs I2 and I4 of the 8-to-3 encoder are both 1; then the output is 110, the binary encoding of 6.

Y0 = I1 + I3 + I5 + I7
Y1 = I2 + I3 + I6 + I7
Y2 = I4 + I5 + I6 + I7

Either 2 or 4, not 6, would be a useful output in the preceding example, but how can the encoding device decide which? The solution is to assign *priority* to the input lines, so that when multiple requests are asserted, the encoding device produces the number of the highest-priority requestor. Such a device is called a *priority encoder*. Input I7 has the highest priority. Outputs A2–A0 contains the number of the highest-priority asserted input, if any. The IDLE output is asserted if no inputs are asserted.

In order to write logic equations for the priority encoder's outputs, we first define eight intermediate variables H0–H7, such that Hi is 1 if and only if Ii is the highest priority 1 input: Using these signals, the equations for the A2–A0 outputs are similar to the ones for a simple binary encoder:



8-input priority encoder

- I7 has the highest priority, I0 least

- A2-A0 contain the number of the highest-priority asserted input if any.

- IDLE is asserted if no inputs are asserted.

The 74x148 Priority Encoder

The *74x148* is a commercially available, MSI 8-input priority encoder it has an enable input, EI_L that must be asserted for any of its outputs to be asserted. The complete truth table is given in Table 5-22. Instead of an IDLE output, the ’148 has a GS_L output that is asserted when the device is enabled and one or more of the request inputs is asserted. The manufacturer calls this ―Group Select,‖ but it’s easier to remember as ―Got Something.‖ The EO_L signal is an enable *output* designed to be connected to the EI_L input of another ’148 that handles lower-priority requests. /EO is asserted if EI_L is asserted but no request input is asserted; thus, a lower-priority ’148 may be enabled.

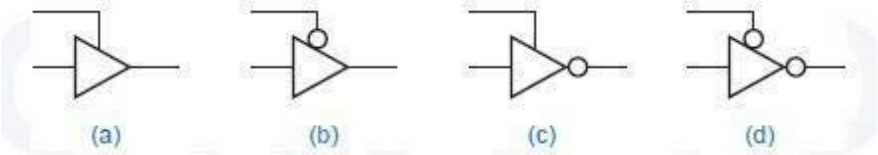
Figure 5-50 shows how four 74x148s can be connected in this way to accept 32 request inputs and produce a 5-bit output, RA4–RA0, indicating the highest-priority requestor. Since the A2–A0 outputs of at most one ’148 will be enabled at any time, the outputs of the individual ’148s can be O Red to produce RA2–RA0. Likewise, the individual GS_L outputs can be combined in a 4-to-2 encoder to produce RA4 and RA3. The RGS output is asserted if any GS output is asserted.

Inputs									Outputs				
/EI	/I0	/I1	/I2	/I3	/I4	/I5	/I6	/I7	/A2	/A1	/A0	/GS	/EO
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	x	x	x	x	x	x	x	0	0	0	0	0	1
0	x	x	x	x	x	x	0	1	0	0	1	0	1
0	x	x	x	x	x	0	1	1	0	1	0	0	1
0	x	x	x	x	0	1	1	1	0	1	1	0	1
0	x	x	x	0	1	1	1	1	1	0	0	0	1
0	x	x	0	1	1	1	1	1	1	0	1	0	1
0	x	0	1	1	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

Three-State Devices

Three-State Buffers

The most basic three-state device is a *three-state buffer*, often called a *three-state driver*. The logic symbols for four physically different three-state buffers are shown in Figure 5-52.



The basic symbol is that of a non inverting buffer (a, b) or an inverter (c, d). The extra signal at the top of the symbol is a *three-state enable* input, which may be active high (a, c) or active low (b, d). When the enable input is asserted, the device behaves like an ordinary buffer or inverter. When the enable input is negated, the device output ―floats‖; that is, it goes to high impedance (Hi-Z), disconnected state and functionally behaves as if it weren't even there.

Both enable inputs, G1_L and G2_L, must be asserted to enable the device's three-state outputs. The little rectangular symbols inside the buffer symbols indicate *hysteresis*, an Electrical characteristic of the inputs that improves noise immunity. The 74x541 inputs typically have 0.4 volts of hysteresis.

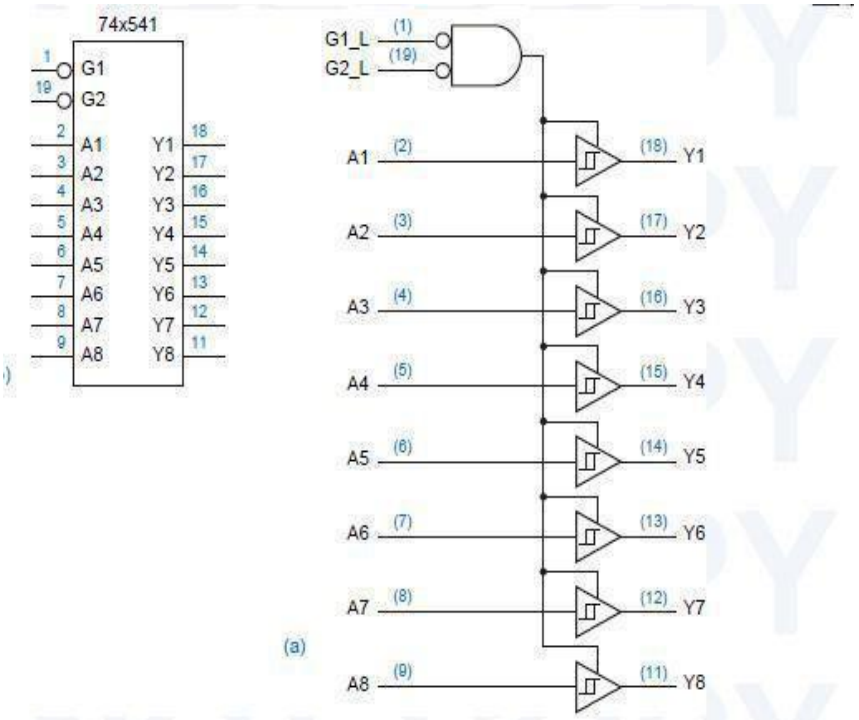


Figure 5-57 shows part of a microprocessor system with an 8-bit data bus, DB[0–7], and a 74x541 used as an input port. The microprocessor selects Input Port 1 by asserting INSEL1 and requests a read operation by asserting READ. The selected 74x541 responds by driving the microprocessor data bus with user supplied input data. Other input ports may be selected when a different INSEL line is asserted along with READ.

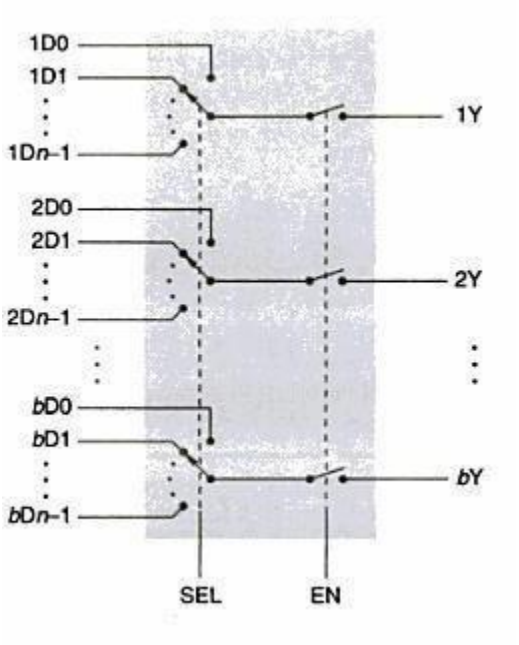
Multiplexers

A *multiplexer* is a digital switch—it connects data from one of *n* sources to its output. Figure 5-61(a) shows the inputs and outputs of an *n*-input, *b*-bit multiplexer. There are *n* sources of data, each of which is *b* bits wide. A multiplexer is often called a *mux* for short.

A multiplexer can use addressing bits to select one of several input bits to be the output. A selector chooses a single data input and passes it to the MUX output. It has one output selected at a time.

Figure shows a switch circuit that is roughly equivalent to the multiplexer. However, unlike a mechanical switch, a multiplexer is a unidirectional device: information flows only from inputs (on the left) to outputs (on the right. Multiplexers are obviously useful devices in any application in which data must be switched from multiple sources to a destination. A common application in computers is the multiplexer between the processor's registers and its arithmetic logic unit (ALU). For example, consider a 16-bit processor in which each instruction has a 3-bit field that specifies one of eight registers to use. This 3-bit field is connected to the select inputs of an 8-input, 16-bit multiplexer. The multiplexer's data inputs

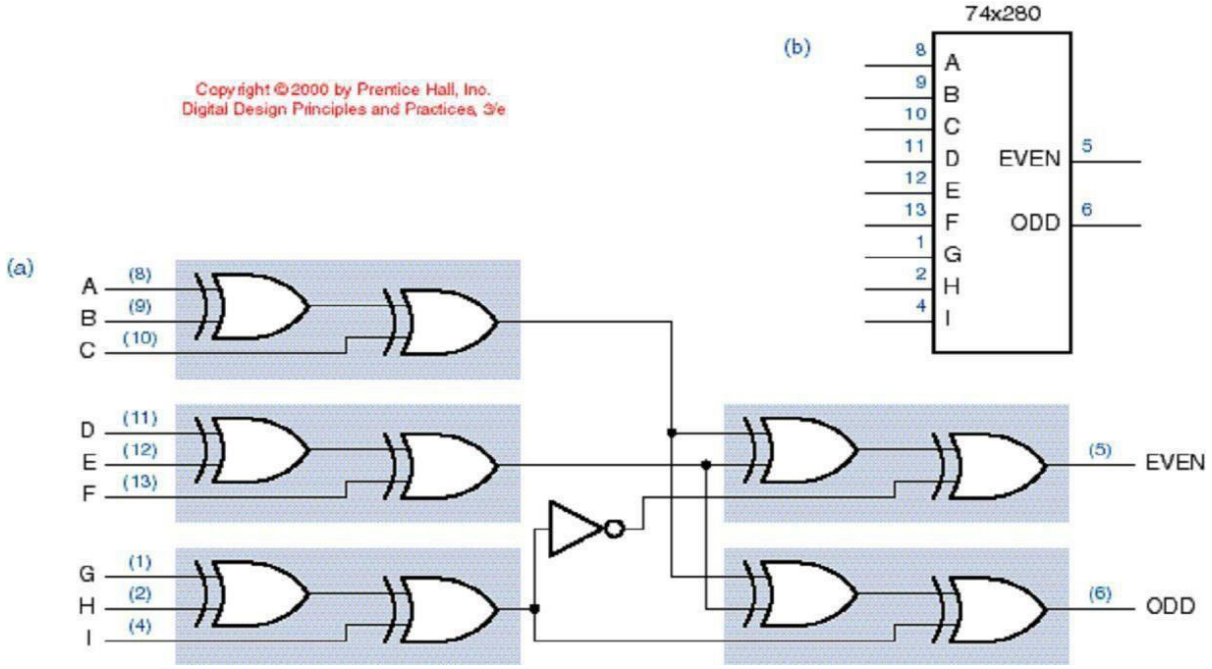
are connected to the eight registers, and its data outputs are connected to the ALU to execute the instruction using the selected register.



Parity Circuits

N XOR gates may be cascaded to form a circuit with *n* 1 inputs and a single output. This is called an *odd-parity circuit*, because its output is 1 if an odd number of its inputs are 1. If the output of either circuit is inverted, we get an *even-parity circuit*, whose output is 1 if an even number of its inputs is 1.

5.5.1 The 74x280 9-Bit Parity Generator



Rather than build a multi bit parity circuit with discrete XOR gates, it is more economical to put all of the XORs in a single MSI package with just the primary inputs and outputs available at the external pins. The *74x280* 9-bit parity generator, shown in Figure is such a device. It has nine inputs and two outputs that indicate whether an even or odd number of inputs are 1.

Comparators

Inputs				Outputs		
A_1	A_0	B_1	B_0	A > B	A = B	A< B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

A > B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

$$A>B = A_0\overline{B}_1\overline{B}_0 + A_1\overline{B}_1 + A_1A_0\overline{B}_0$$

A = B

A_1A_0 \ B_1B_0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

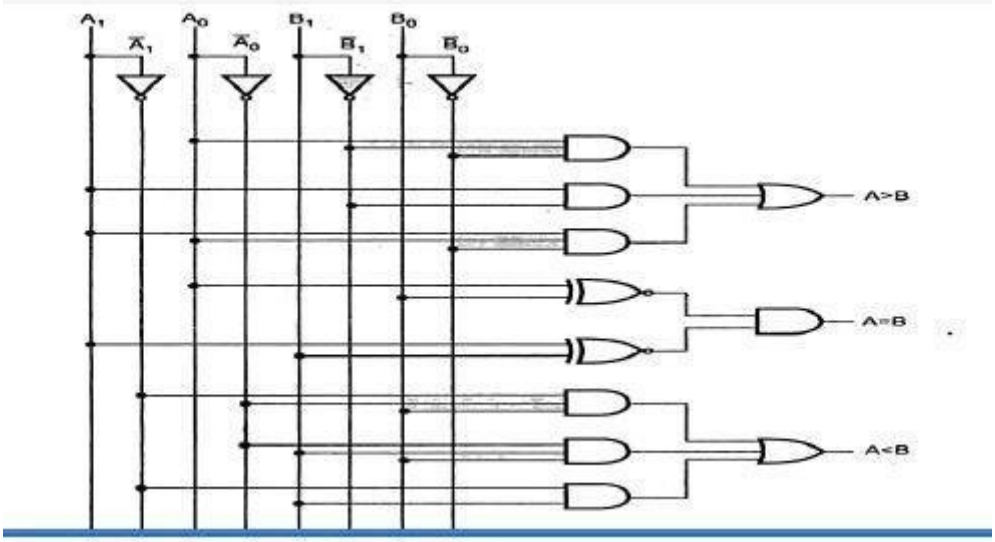
A < B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

Fig. 4.93

$$(A = B) = \overline{A}_1\overline{A}_0\overline{B}_1\overline{B}_0 + \overline{A}_1A_0\overline{B}_1B_0 + A_1A_0B_1B_0 + A_1\overline{A}_0B_1\overline{B}_0$$
$$= \overline{A}_1\overline{B}_1(\overline{A}_0\overline{B}_0 + A_0B_0) + A_1B_1(A_0B_0 + \overline{A}_0\overline{B}_0)$$
$$= (A_0 \odot B_0)(A_1 \odot B_1)$$
$$(A < B) = \overline{A}_1\overline{A}_0B_0 + \overline{A}_0B_1B_0 + \overline{A}_1B_1$$

Comparing two binary words for equality is a commonly used operation in computer systems and device interfaces. we showed a system structure in which devices are enabled by comparing a ―device select‖ word with a predetermined ―device ID.‖ A circuit that compares two binary words and indicates whether they are equal is called a *comparator*. Some comparators interpret their input words as signed or unsigned numbers and also indicate an arithmetic relationship (greater or less than) between the words. These devices are often called *magnitude comparators*.



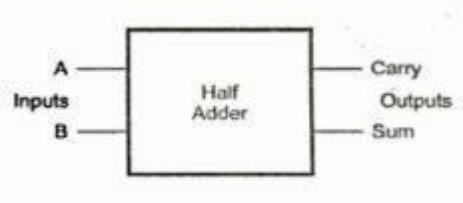
Adders, Subtractors, and ALUs

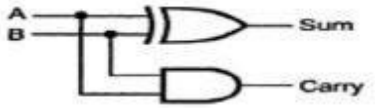
Addition is the most commonly performed arithmetic operation in digital systems. An *adder* combines two arithmetic operands using the addition rules. the same addition rules and therefore the same adders are used for both unsigned and two's-complement numbers. An adder can perform subtraction as the addition of the minuend and the complemented (negated) subtrahend, but you can also build *subtractor Half Adder: adds two 1-bit operands*

5.7.1 Half Adders and Full Adders

The simplest adder, called a *half adder*, adds two 1-bit operands X and Y, producing a 2-bit sum. The sum can range from 0 to 2, which requires two bits to express. The low-order bit of the sum may be named HS (half sum), and the high-order bit may be named CO (carry out). We can write the following equations for HS and CO:

Inputs		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0





To add operands with more than one bit, we must provide for carries between bit positions. The building block for this operation is called a *full adder*. Besides the addend-bit inputs X and Y, a full adder has a carry-bit input, CIN. The sum of the three inputs can range from 0 to 3, which can still be expressed with just two output bits, S and COUT, having the following equations: Here, S is 1 if an odd number of the inputs are 1, and COUT is 1 if two or more of the inputs are 1.

Basic Bi stable Element

A combinational system is a system whose outputs depend only upon its current inputs. A sequential system is a system whose output depends on current input *and* past history of inputs.

All systems we have looked at to date have been combinational systems. Outputs depend on the current inputs and the system's current state. State embodies all the information about the past needed to predict current output based on current input.

- *State variables*, one or more bits of information.

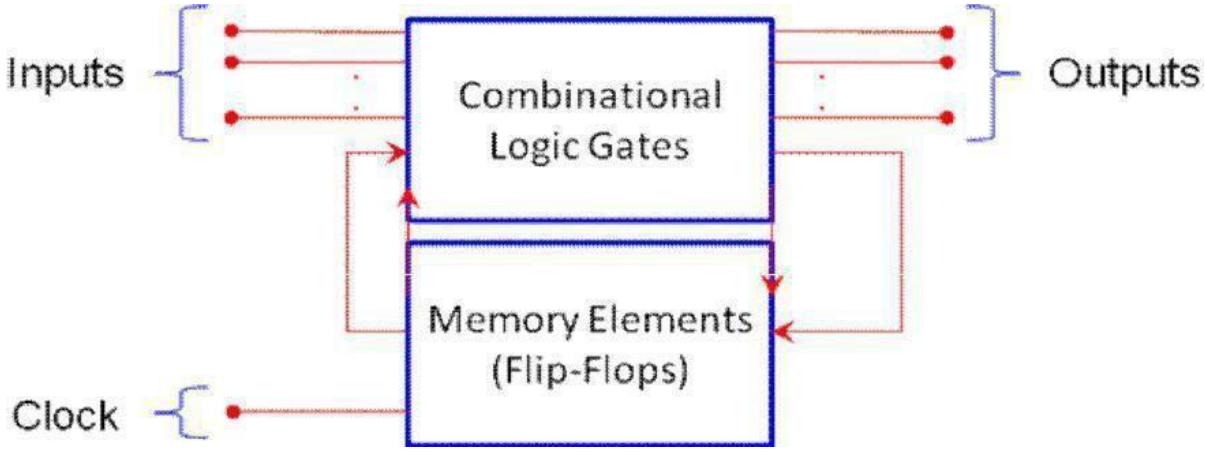
The state is a collection of state variables whose values at any one time contain all the information about the past necessary to account for the circuit's future behavior.

- The simplest sequential circuit, no way to control its state.
- Two states
- One state variable, say, Q, two possible states

A *bistable memory device* is the generic term for the elements we are studying. Latches and Flip flops Latches *and flip-flops* (FFs) are the basic building blocks of sequential circuits.

 latch: bistable memory device with level sensitive triggering (no clock), watches all of its inputs continuously and changes its outputs at any time, independent of a clocking signal.

 flip-flop: bistable memory device with edge-triggering (with clock), samples its inputs, and changes its output only at times determined by a clocking signal.



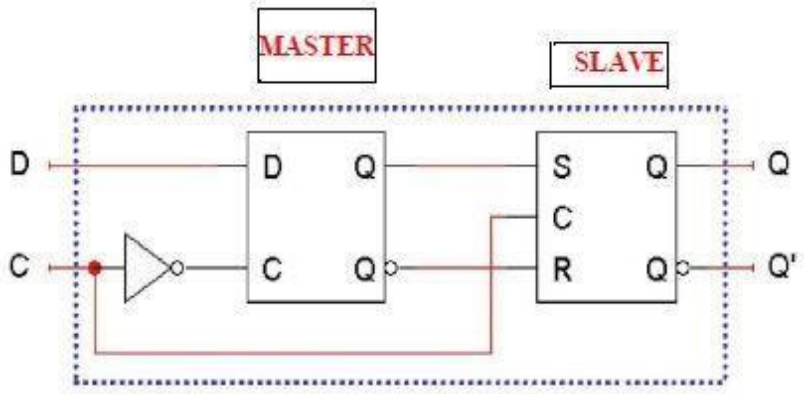
Here is an SR latch with a control input C.

• Notice the hierarchical design!

– The dotted blue box is the S'R' latch.

– The additional NAND gates are simply used to generate the correct inputs for the S'R' latch.

• The control input acts just like an enable.



D flip-flops when C=0

• The D flip-flop's control input C enables *either* the D latch or the SR latch, but not both.

• When C = 0:

– The master latch is enabled, and it monitors the flip-flop input D. Whenever D changes, the master's output changes too.

– The slave is disabled, so the D latch output has no effect on it. Thus, the slave just maintains the flip-flop's current state.

D flip-flops when C=1

• *As soon as C becomes 1,*

–The master is disabled. Its output will be the *last* D input value seen just before C became 1.

– Any subsequent changes to the D input while C = 1 have no effect on the master latch, which is now disabled.

– The slave latch is enabled. Its state changes to reflect the master's output, which again the D input value from right is when C became 1.

Positive edge triggering

• This is called a positive edge-triggered flip-flop.

– The flip-flop output Q changes *only* after the positive edge of C.

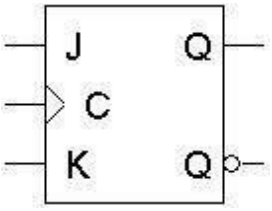
– The change is based on the flip-flop input values that were present right at the positive edge of the clock signal.

The D flip-flop's behavior is similar to that of a D latch except for the positive edge-triggered nature, which is not explicit in this table

Flip-flop variations

• We can make different versions of flip-flops based on the D flip-flop, just like we made different latches based on the S'R' latch.

• A JK flip-flop has inputs that act like S and R, but the inputs JK=11 are used to *complement* the flip-flop's current state.



Characteristic equations

• We can also write characteristic equations, where the next state Q(t+1) is defined in terms of the current state Q(t) and inputs.

D	Q(t+1)	Operation
0	0	Reset
1	1	Set

$Q(t+1) = D$

J	K	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

$Q(t+1) = K'Q(t) + JQ'(t)$

T	Q(t+1)	Operation
0	Q(t)	No change
1	Q'(t)	Complement

$t+1) = T'Q(t) + TQ'(t)$

$= T \ Q(t)$

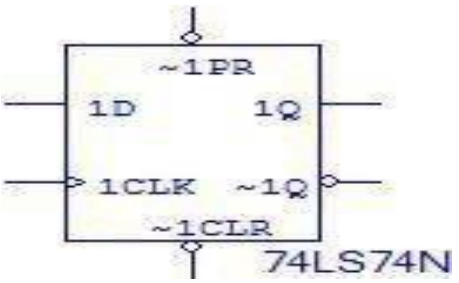
Flip-Flop vs. Latch

• The primary difference between a D flip-flop and D latch is the EN/CLOCK input.

• The flip-flop's CLOCK input is edge sensitive, meaning the flip-flop's output changes on the edge (rising or falling) of the CLOCK input.

• The latch's EN input is level sensitive, meaning the latch's output changes on the level (high or low) of the EN input.

Flip-Flops & Latches



Counters

• Counters are a specific type of sequential circuit.

• Like registers, the state, or the flip-flop values themselves, serves as the ―output.‖

• The output value increases by one on each clock cycle.

• After the largest value, the output ―wraps around‖ back to 0.

• Using two bits, we'd get something like this:

resent State A	B	xt State A	B
0	0	)	1
0	1	1	0
1	0	1	1
1	1	)	0

Counters can act as simple clocks to keep track of ―time.‖

• You may need to record how many times something has happened.

– How many bits have been sent or received?

– How many steps have been performed in some computation?

• All processors contain a program counter, or PC.

– Programs consist of a list of instructions that are to be executed one after another (for the most part).

– The PC keeps track of the instruction currently being executed.

– The PC increments once on each clock cycle, and the next program instruction is then executed. **Asynchronous Counters**

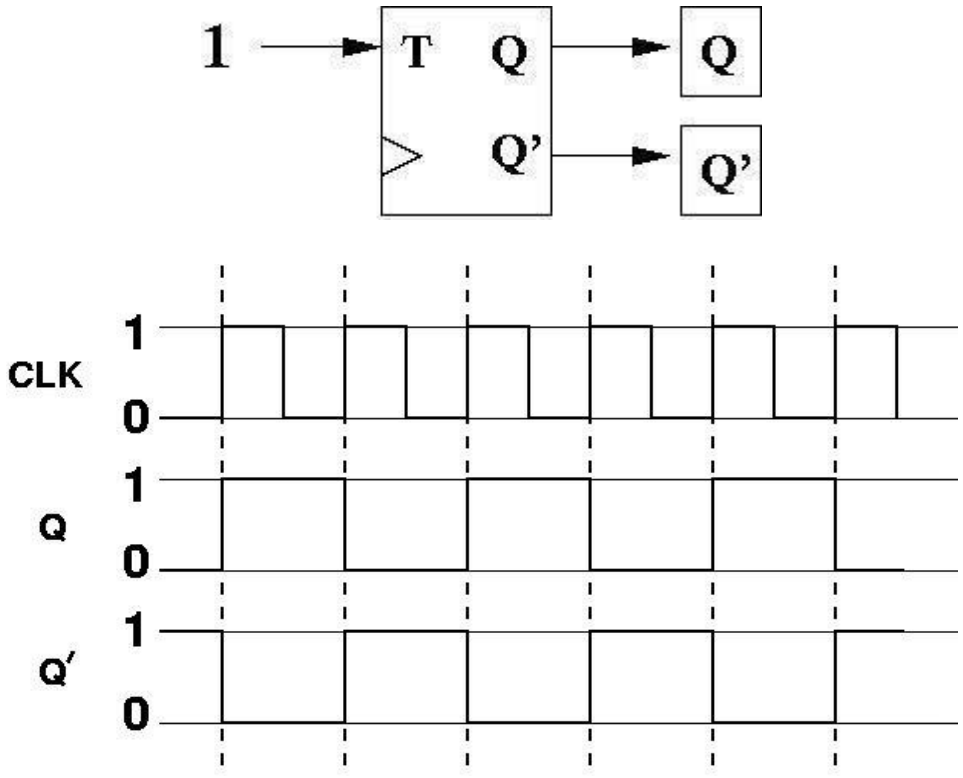
• This counter is called *asynchronous* because not all flip flops are hooked to the same clock.

• Look at the waveform of the output, **Q**, in the timing diagram. It resembles a clock as well. If the period of the clock is T, then what is the period of **Q**, the output of the flip flop? It's 2T!

• We have a way to create a clock that runs twice as slow. We feed the clock into a T flip flop, where T is hardwired to 1. The output will be a clock who's period is twice as long.

• If the clock has period T. **Q0** has period 2T. **Q1** period is 4T

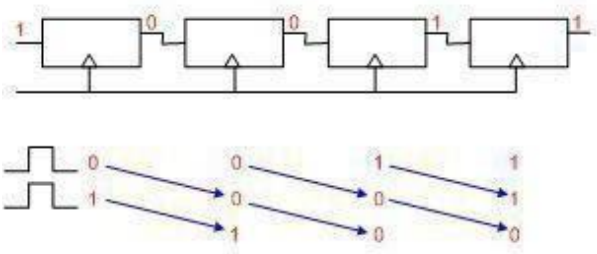
• With n flip flops the period is 2n



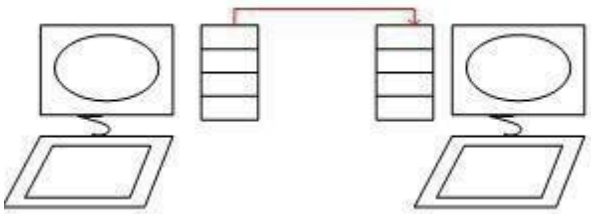
Shift Register

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All the flip-flops are driven by a common clock, and all are set or reset simultaneously. In this chapter, the basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In - Serial Out, Parallel In - Parallel Out, and bidirectional shift registers. A special form of counter - the shift register counter, is also introduced.

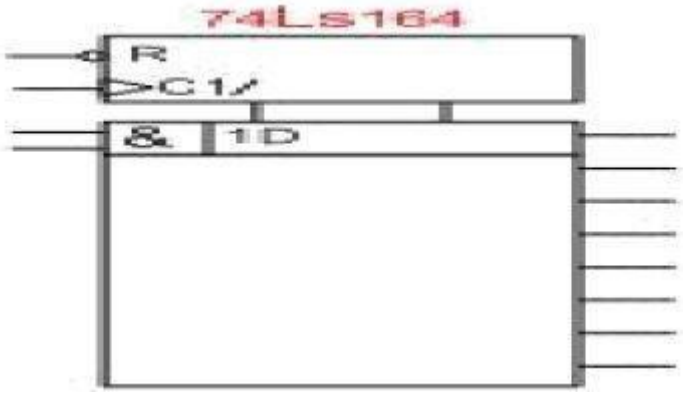
Let's observe the values of the flip flops in this shift register for the next couple of clock pulse:



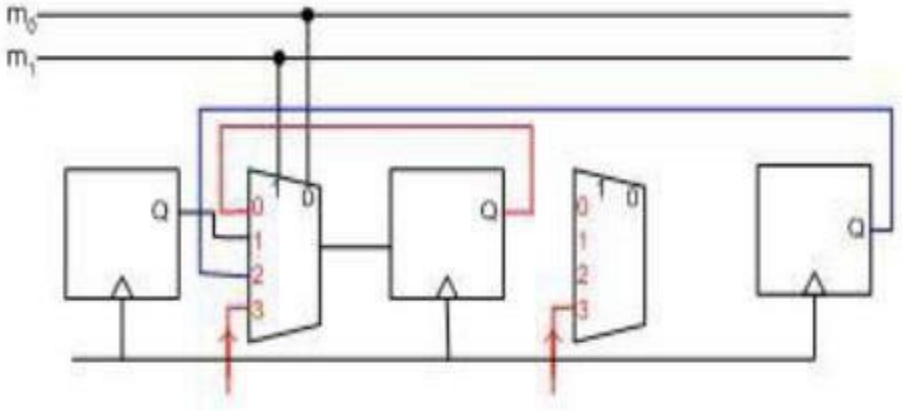
We are actually shifting our data to the right on every clock pulse. Shift registers are widely used in parallel to serial converters which find applications in computer communications.



74ls164: This package has two inputs and eight outputs. It can be useful in serial to parallel conversion of data but not parallel to serial because there is no parallel loading.



We now want to see how universal shift registers are made. Consider the following circuit:

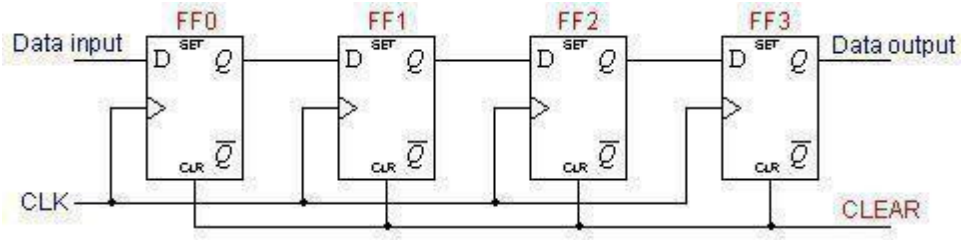


In the last diagram, you can see that 4 modes of operation exist. When m1m0 is 00, nothing happens, that is the contents of the flip flops don't change due to feed backing. m1m0=01

puts us in right shift mode and 10 in left shift, whereas m1m0=11 gives us parallel load. This structure can be used in a shift register to give us parallel to serial conversion abilities.
74ls194: This package give us right and left shifting as well as parallel load in mode 11.

Serial In - Serial Out Shift Registers

A basic four-bit shift register can be constructed using four D flip-flops, as shown below. The operation of the circuit is as follows. The register is first cleared, forcing all four outputs to zero. The input data is then applied sequentially to the D input of the first flip-flop on the left (FF0). During each clock pulse, one bit is transmitted from left to right. Assume a data word to be 1001. The least significant bit of the data has to be shifted through the register from FF0 to FF3.

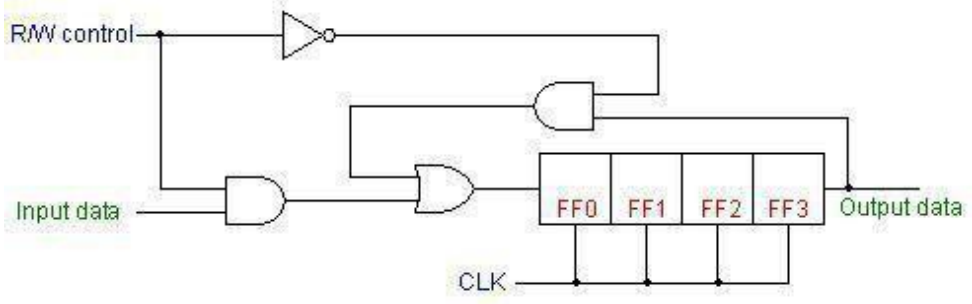


	FF0	FF1	FF2	FF3
CLEAR	0	0	0	0

In order to get the data out of the register, they must be shifted out serially. This can be done destructively or non-destructively. For destructive readout, the original data is lost and at the end of the read cycle, all flip-flops are reset to zero.

	FF0	FF1	FF2	FF3
CLEAR	0	0	0	0

To avoid the loss of data, an arrangement for a non-destructive reading can be done by adding two AND gates, an OR gate and an inverter to the system. The construction of this circuit is shown below

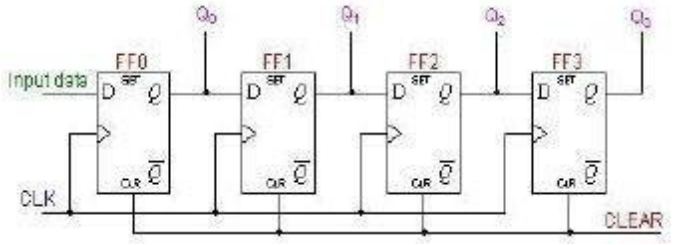


The data is loaded to the register when the control line is HIGH (ie WRITE). The data can be shifted out of the register when the control line is LOW (ie READ). This is shown in the animation below

WRITE 1001	FF0	FF1	FF2	FF3
	0	0	0	0

Serial In - Parallel Out Shift Registers

For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown below.

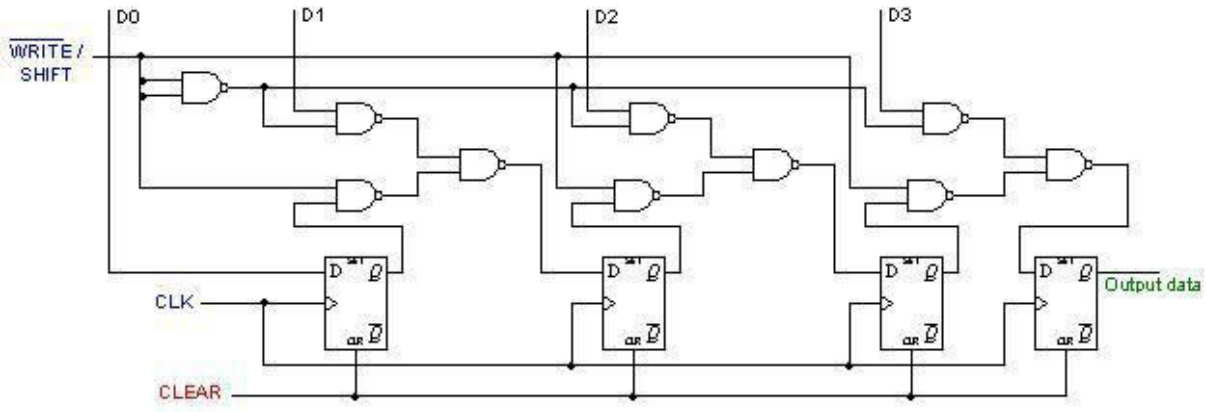


In the animation below, we can see how the four-bit binary number 1001 is shifted to the Q outputs of the register**.**

CLEAR 1001	Q0	Q1	Q2	Q3
	0	0	0	0

Parallel In - Serial Out Shift Registers

A four-bit parallel in - serial out shift register is shown below. The circuit uses D flip-flops and NAND gates for entering data (ie writing) to the register.

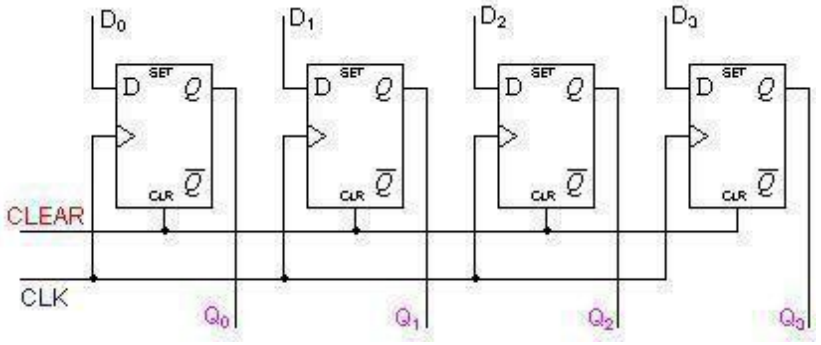


D0, D1, D2 and D3 are the parallel inputs, where D0 is the most significant bit and D3 is the least significant bit. To write data in, the mode control line is taken to LOW and the data is clocked in. The data can be shifted when the mode control line is HIGH as SHIFT is active high. The register performs right shift operation on the application of a clock pulse, as shown in the animation below.

	Q0	Q1	Q2	Q3
CLEAR	0	0	0	0

Parallel In - Parallel Out Shift Register

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flops.



The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.