# LECTURE NOTES

# ON

# ELECTRONIC DEVICES AND CIRCUITS

## B.Tech IIIsemester
## (EEE)

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**INSTITUTE OF AERONAUTICAL ENGINEERING**
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# ELECTRONIC DEVICES AND CIRCUITS

**III Semester: ECE/EEE**

| Course Code | Category | Hours / Week | | | Credits | Maximum Marks | | |
|---|---|---|---|---|---|---|---|---|
| | | L | T | P | C | CIA | SEE | Total |
| AEC001 | Foundation | 3 | 1 | - | 4 | 30 | 70 | 100 |
| Contact Classes: 45 | Tutorial Classes: 15 | Practical Classes: Nil | | | | Total Classes: 60 | | |

**OBJECTIVES:**

**The course should enable the students to:**

1. Be acquainted with electrical characteristics of ideal and practical diodes under forward and reverse bias to analyze and design diode application circuits such as rectifiers and voltage regulators.
2. Utilize operational principles of bipolar junction transistors and field effect transistors to derive appropriate small-signal models and use them for the analysis of basic amplifier circuits.
3. Perform DC analysis (algebraically and graphically using current voltage curves with super imposed load line) and design of CB,CE and CC transistor circuits.
4. Compare and contrast different biasing and compensation techniques

| UNIT-I | SEMICONDUCTOR DIODES | Classes: 08 |
|---|---|---|

PN Junction Diode : Theory of PN diode, energy band diagram of PN diode, PN junction as a diode, operation and V-I characteristics , static and dynamic resistances, diode equivalent circuits, diffusion and transition capacitance, diode current equation, temperature dependence of V-I characteristics, Zener diode characteristics ,break down mechanisms in semiconductor diodes, Zener diode as a voltageregulator.

| UNIT-II | SPECIAL PURPOSE ELECTRONIC DEVICES AND RECTIFIERS | Classes: 10 |
|---|---|---|

Special purpose electronic devices: principles of operation and characteristics of silicon controlled rectifier, tunnel diode, varactor diode, photodiode; Half wave rectifier, full wave rectifier, general filter consideration, harmonic components in a rectifier circuit , Inductor Filter, capacitor filter, L-Section filter, multiple L-C section, RC filter, comparison of filters.

| UNIT-III | TRANSISTORS | Classes: 08 |
|---|---|---|

Bipolar Junction Transistors: Construction of BJT, operation of BJT, minority carrier distributions and current components, configurations, characteristics, BJT specifications; Applications: Amplifier,switch.

Field Effect Transistors: Types of FET, FET construction, symbol, principle of operation, V-I characteristics, FET parameters, FET as voltage variable resistor, comparison of BJT and FET; MOSFET construction and operation; Uni-Junction Transistor: Symbol, principle of operation, characteristics, applications (UJT as relaxation oscillator).

| UNIT-IV | BIASING AND COMPENSATION TECHNIQUES | Classes: 10 |
|---|---|---|

Need for biasing, BJT operating point, The DC and AC load lines, types of biasing circuits, bias stability, stabilization factors, stabilization against variations in $V_{BE}$ and $\beta$; Bias compensation techniques, thermal runaway, thermal stability, biasing the FET and MOSFET.

| UNIT-V | BJT AND FET AMPLIFIERS | Classes: 09 |
|---|---|---|

BJT small signal analysis, BJT hybrid model, determination of h-parameters from transistor characteristics, transistor amplifiers analysis using h- parameters; FET small signal model, FET as common source amplifier, FET as common drain amplifier, FET as common gate amplifier, generalized FET amplifier .

**Text Books:**

1. J. Millman, C.C.Halkias, "Millman's Integrated Electronics", Tata McGraw-Hill, 2nd Edition, 2001.
2. J. Millman, C.C.Halkias, Satyabrata Jit, ―Millman's Electronic Devices and Circuits‖, Tata McGrawHill, 2nd Edition, 1998.
3. David A. Bell, ―Electronic Devices and Circuits‖, Oxford University Press ,5th Edition,2008.

**Reference Books:**

1. Sedha.R.S, "A Text Book of Applied Electronics‖, Sultan Chand Publishers",1st Edition, 2008
2. R L. Boylestad, Louis Nashelsky, "Electronic Devices and Circuits‖, PEI/PHI", 9th edition, 2006.Gupta.J.B,
3. "Electron Devices and Circuits‖, S.K.Kataria & Sons", 2nd Edition,2012. Salivahanan, N. Suresh Kumar,A. Vallavaraj.

**Web References:**

Hhttp://wwwmdp.eng.cam.ac.uk/web/library/enginfo/electrical/hong1.pd
https://archive.org/details/ElectronicDevicesCircuits http://nptel.ac.in/courses/Webcourse-contents/
http://www.satishkashyap.com/2013/03/video-lectures-on-electron-devices-by.html

**E-Text Books:**

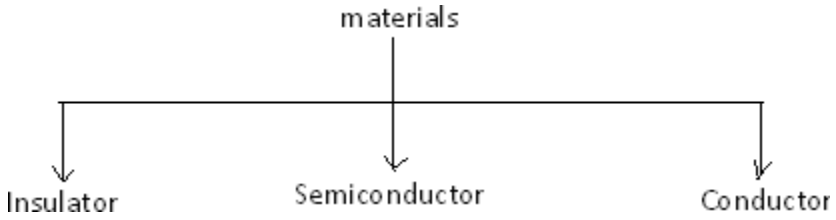
http://services.eng.uts.edu.au/pmcl/ec/Downloads/LectureNotes.pdf
http://nptel.ac.in/courses/122106025/
http://www.freebookcentre.net/electronics-ebooks-download/Electronic-Devices-and-Circuits-(PDF-313p).html
https://www.jntubook.com/electronic-device-circuits-textbook-free-download/http://www.faadooengineers.com/threads/32735-Electronic-Devices-And-Circuits-(EDC)-by- J-B-Gupta-full-book-pdf

# UNIT 1

# PN JUNCTION DIODE

## INTRODUCTON

Based on the electrical conductivity all the materials in nature are classified as insulators, semiconductors, and conductors.




**Insulator**: An insulator is a material that offers a very low level (or negligible) of conductivity when voltage is applied. Eg: Paper, Mica, glass, quartz. Typical resistivity level of an insulator is of the order of $10^{10}$ to $10^{12}$ Ω-cm. The energy band structure of an insulator is shown in the fig.1.1. Band structure of a material defines the band of energy levels that an electron can occupy. Valance band is the range of electron energy where the electron remain bended too the atom and do not contribute to the electric current. Conduction bend is the range of electron energies higher than valance band where electrons are free to accelerate under the influence of external voltage source resulting in the flow of charge.

The energy band between the valance band and conduction band is called as forbidden band gap. It is the energy required by an electron to move from balance band to conduction band i.e. the energy required for a valance electron to become a free electron.

$$1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}$$

For an insulator, as shown in the fig.1.1 there is a large forbidden band gap of greater than 5Ev. Because of this large gap there a very few electrons in the CB and hence the conductivity of insulator is poor. Even an increase in temperature or applied electric field is insufficient to transfer electrons from VB to CB.

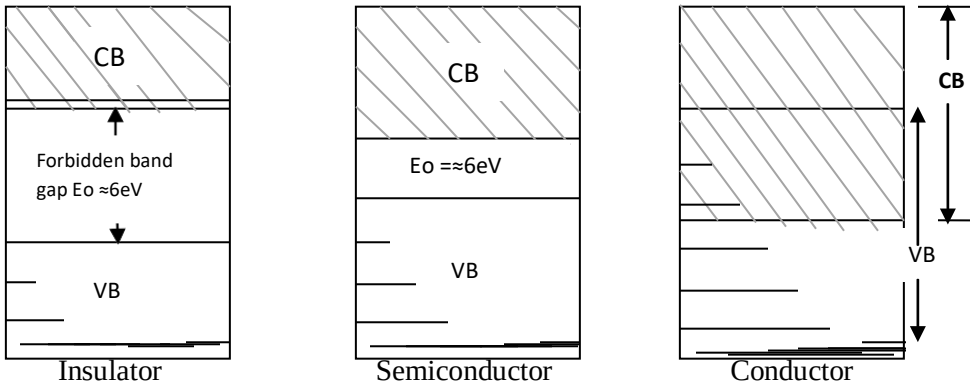



FiG:1.1 Energy band diagrams insulator, semiconductor and conductor

**Conductors:** A conductor is a material which supports a generous flow of charge when a voltage is applied across its terminals. i.e. it has very high conductivity. Eg: Copper, Aluminum, Silver, Gold. The resistivity of a conductor is in the order of $10^{-4}$and $10^{-6}$ Ω-cm. The Valance and conduction bands overlap (fig1.1) and there is no energy gap for the electrons to move from valance band to conduction band. This implies that there are free electrons in CB even at absolute zero temperature (0K). Therefore at room temperature when electric field is applied large current flows through the conductor.

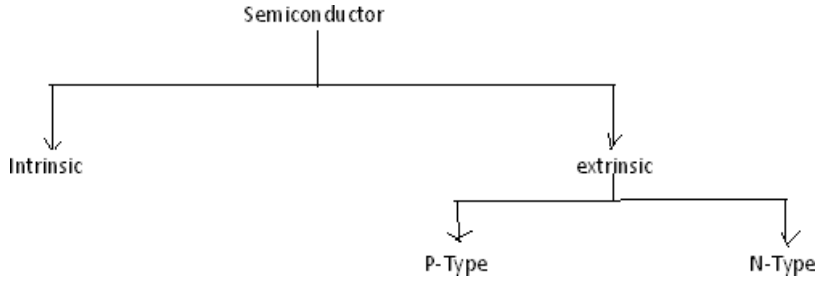
**Semiconductor**: A semiconductor is a material that has its conductivity somewhere between the insulator and conductor. The resistivity level is in the range of 10 and $10^4$ Ω-cm. Two of the most commonly used are Silicon (Si=14 atomic no.) and germanium (Ge=32 atomic no.). Both have 4 valance electrons. The forbidden band gap is in the order of 1eV. For eg., the band gap energy for Si, Ge and GaAs is 1.21, 0.785 and 1.42 eV, respectively at absolute zero temperature (0K). At 0K and at low temperatures, the valance band electrons do not have sufficient energy to move from V to CB. Thus semiconductors act a insulators at 0K. as the temperature increases, a large number of valance electrons acquire sufficient energy to leave the VB, cross the forbidden bandgap and reach CB. These are now free electrons as they can move freely under the influence of electric field. At room temperature there are sufficient electrons in the CB and hence the semiconductor is capable of conducting some current at roomtemperature.

Inversely related to the conductivity of a material is its resistance to the flow of charge or current. Typical resistivity values for various materials' are given as follows.

| Insulator | Semiconductor | Conductor |
|---|---|---|
| $10^{-6}$ Ω-cm (Cu) | 50Ω-cm (Ge) | $10^{12}$ Ω-cm (mica) |
| | $50x10^{3}$ Ω-cm (Si) | |

Typical resistivity values

**SemiconductorTypes**




A pure form of semiconductors is called as intrinsic semiconductor. Conduction in intrinsic sc is either due to thermal excitation or crystal defects. Si and Ge are the two most important semiconductors used. Other examples include Gallium arsenide GaAs, Indium Antimonide (InSb) etc.

Let us consider the structure of Si.A Si atomic no. is 14 and it has 4 valance electrons. These 4 electrons are shared by four neighboring atoms in the crystal structure by means of covalent bond. Fig. 1.2a shows the crystal structure of Si at absolute zero temperature (0K). Hence a pure SC acts has poor conductivity (due to lack of free electrons) at low or absolute zero temperature.

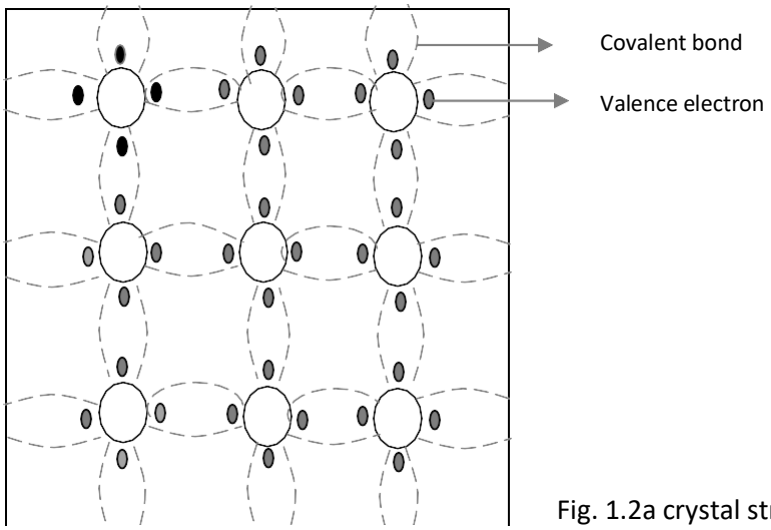



Fig. 1.2a crystal structure of Si at 0K

At room temperature some of the covalent bonds break up to thermal energy as shown in fig 1.2b. The valance electrons that jump into conduction band are called as free electrons that are available forconduction.

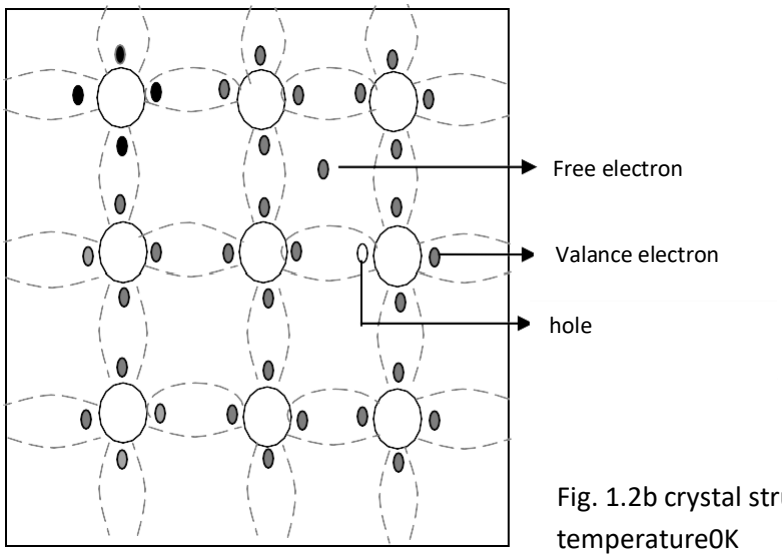
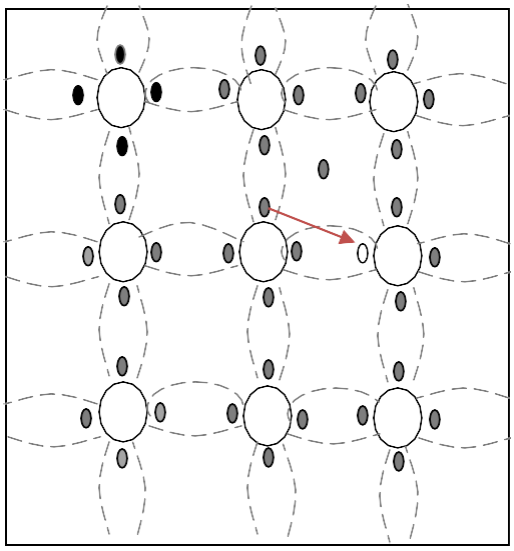



Fig. 1.2b crystal structure of Si at room temperature0K

The absence of electrons in covalent bond is represented by a small circle usually referred to as hole which is of positive charge. Even a hole serves as carrier of electricity in a manner similar to that of freeelectron.

The mechanism by which a hole contributes to conductivity is explained as follows:

When a bond is in complete so that a hole exists, it is relatively easy for a valance electron in the neighboring atom to leave its covalent bond to fill this hole. An electron moving from a bond to fill a hole moves in a direction opposite to that of the electron. This hole, in its new position may now be filled by an electron from another covalent bond and the hole will correspondingly move one more step in the direction opposite to the motion of electron. Here we have a mechanism for conduction of electricity which does not involve free electrons. This phenomenon is illustrated infig1.3



Electron movement

Hole movement

Fig. 1.3a

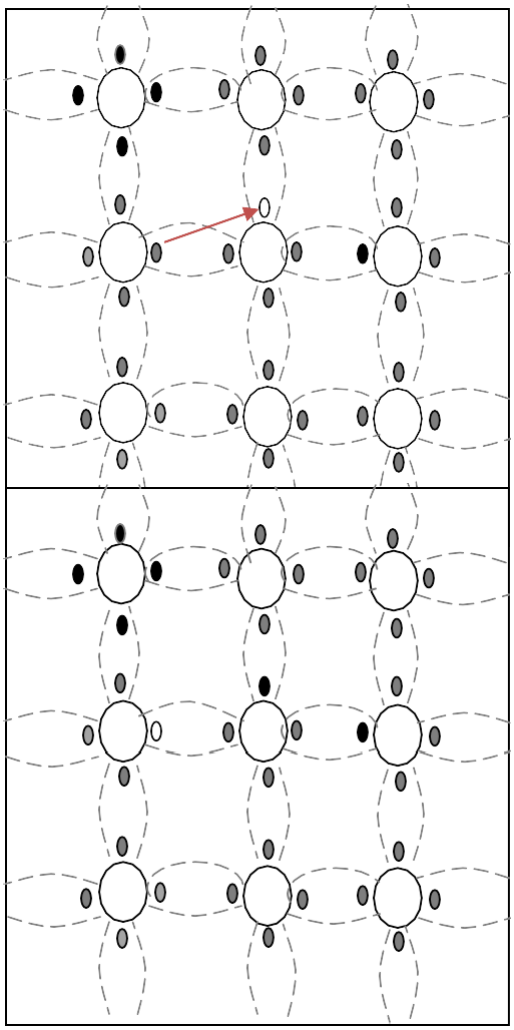


Fig. 1.3b

Fig. 1.3c

Fig 1.3a show that there is a hole at ion 6.Imagine that an electron from ion 5 moves into the hole at ion 6 so that the configuration of 1.3b results. If we compare both fig1.3a &fig 1.3b, it appears as if the hole has moved towards the left from ion6 to ion 5. Further if we compare fig 1.3b and fig 1.3c, the hole moves from ion5 to ion 4. This discussion indicates the motion of hole is in a direction opposite to that of motion of electron. Hence we consider holes as physical entities whose movement constitutes flow ofcurrent.

In a pure semiconductor, the number of holes is equal to the number of free electrons.

## EXTRINSICSEMICONDUCTOR:

Intrinsic semiconductor has very limited applications as they conduct very small amounts of current at room temperature. The current conduction capability of intrinsic semiconductor can be increased significantly by adding a small amounts impurity to the intrinsic semiconductor. By adding impurities it becomes impure or extrinsic semiconductor. This process of adding impurities is called as doping. The amount of impurity added is 1 part in $10^6$ atoms.

**N type semiconductor:** If the added impurity is a pentavalent atom then the resultant semiconductor is called N-type semiconductor. Examples of pentavalent impurities are Phosphorus, Arsenic, Bismuth, Antimony etc.

A pentavalent impurity has five valance electrons. Fig 1.3a shows the crystal structure of N-type semiconductor material where four out of five valance electrons of the impurity atom(antimony) forms covalent bond with the four intrinsic semiconductor atoms. The fifth electron is loosely bound to the impurity atom. This loosely bound electron can be easily

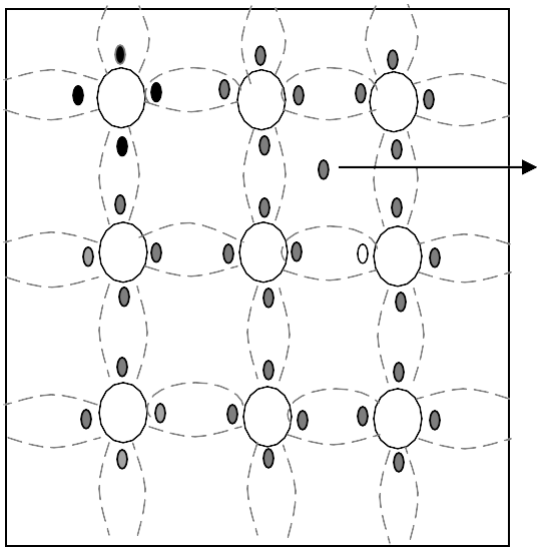



Fig. 1.3a crystal structure of NtypeSC

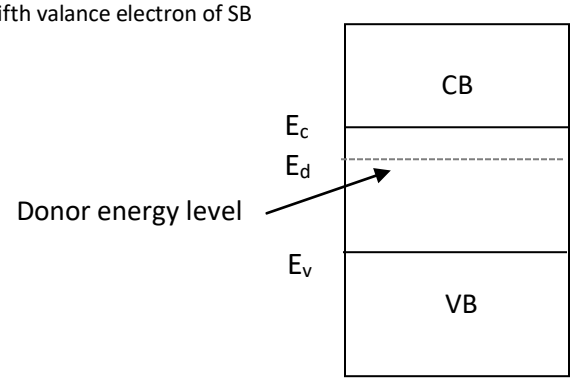



Fig. 1.3bEnergy band diagram of Ntype

excited from the valance band to the conduction band by the application of electric field or increasing the thermal energy. The energy required to detach the fifth electron form the impurity atom is very small of the order of 0.01ev for Ge and 0.05 eV for Si.

The effect of doping creates a discrete energy level called donor energy level in the forbidden band gap with energy level $E_d$ slightly less than the conduction band (fig 1.3b). The difference between the energy levels of the conducting band and the donor energy level is the energy required to free the fifth valance electron (0.01 eV for Ge and 0.05 eV for Si). At room temperature almost all the fifth electrons from the donor impurity atom are raised to conduction band and hence the number of electrons in the conduction band increases significantly. Thus every antimony atom contributes to one conduction electron without creating a hole.

In the N-type sc the no. of electrons increases and the no. of holes decreases compared to those available in an intrinsic sc. The reason for decrease in the no. of holes is that the larger no. of electrons present increases the recombination of electrons with holes. Thus current in N type sc is dominated by electrons which are referred to as majority carriers. Holes are the minority carriers in N typesc

**P type semiconductor:** If the added impurity is a trivalent atom then the resultant semiconductor is called P-type semiconductor. Examples of trivalent impurities are Boron, Gallium , indium etc.

The crystal structure of p type sc is shown in the fig1.3c. The three valance electrons of the impurity (boon) forms three covalent bonds with the neighboring atoms and a vacancy exists in the fourth bond giving rise to the holes. The hole is ready to accept an electron from the neighboring atoms. Each trivalent atom contributes to one hole generation and thus introduces a large no. of holes in the valance band. At the same time the no. electrons are decreased compared to those available in intrinsic sc because of increased recombination due to creation of additional holes.

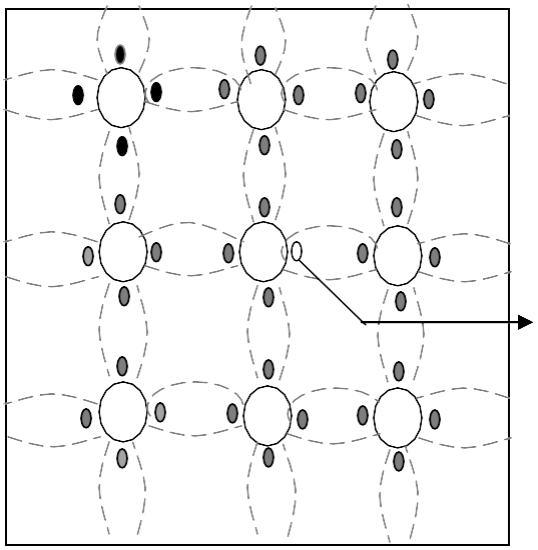



Fig. 1.3c crystal structure of P type sc

Thus in P type sc , holes are majority carriers and electrons are minority carriers. Since each trivalent impurity atoms are capable accepting an electron, these are called as acceptor atoms. The following fig 1.3d shows the pictorial representation of P type sc

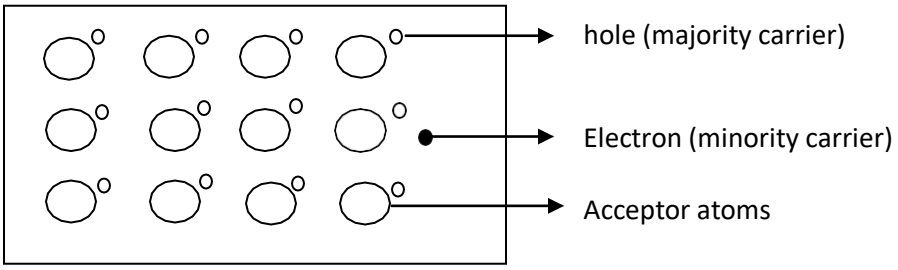



Fig. 1.3d crystal structure of P type sc

- The conductivity of N type sc is greater than that of P type sc as the mobility of electron is greater than that ofhole.
- For the same level of doping in N type sc and P type sc, the conductivity of anNtype sc is around twice that of a P typesc

## CONDUCTIVITY OFSEMICONDUCTOR:

In a pure sc, the no. of holes is equal to the no. of electrons. Thermal agitation continue to produce new electron- hole pairs and the electron hole pairs disappear because of recombination. with each electron hole pair created , two charge carrying particles are formed . One is negative which is a free electron with mobility $\mu_n$ . The other is a positive i.e., hole with mobility $\mu_p$ . The electrons and hole move in opppsitte direction in a an electric field E, but since they are of opposite sign, the current due to each is in the same direction. Hence the total current density J within the intrinsic sc is given by

$J = J_n + J_p$

$=q\ n\ \mu_n\ E + q\ p\ \mu_p\ E$

$= (n\ \mu_n + p\ \mu_p)qE$

$=\sigma\ E$

Where n=no. of electrons / unit volume i.e., concentration of free electrons

P= no. of holes / unit volume i.e., concentration of holes

E=applied electric field strength, V/m

q= charge of electron or hole I n Coulombs

Hence, σ is the conductivity of sc which is equal to $(n \mu_n + p \mu_p)q$. he resistivity of sc is reciprocal of conductivity.

$P = 1/ \sigma$

It is evident from the above equation that current density with in a sc is directly proportional to applied electric field E.

For pure sc, $n=p= n_i$ where $n_i$ = intrinsic concentration. The value of $n_i$ is given by

$n_i^2=AT^3 \exp (-E_{GO}/KT)$

therefore, $J= n_i ( \mu_n + \mu_p) qE$

Hence conductivity in intrinsic sc is $\sigma i= n_i ( \mu_n + \mu_p) q$

Intrinsic conductivity increases at the rate of 5% per $^o$ C for Ge and 7% per $^o$ C for Si.

**Conductivity in extrinsic sc (N Type and P Type):**

The conductivity of intrinsic sc is given by $\sigma i= n_i ( \mu_n + \mu_p) q = (n \mu_n + p \mu_p)q$

For N type , n>>p

Therefore $\sigma= q n \mu_n$

For P type ,p>>n

**The energy band diagram of p-n junction under open circuitconditions**

( Expression for pn junction diode barrier potential. )

- It is known that the Fermi level in n-type material lies just below the conduction band while in p-type material, it lies just above the valenceband.
- When p-n junction is formed, the diffusion starts. The changes get adjusted so as toequalize the Fermi level in the two parts of p-njunction.
- This is similar to adjustment of water levels in two tanks of unequal level, when connected eachother.
- The changes flow from p to n and n to p side till, the Fermi level on two sides get linedup.
- In n-type semi conductor , EF is close to conduction band Ecn and it is close to valence band edge EVP onp-side.
- So the conduction band edge of n-type semiconductor can‟t be at the same level as that of p-type semiconductor.

- Hence, as shown, the energy band diagram for p-n junction is where a shift in energy levels E0 isindicated.

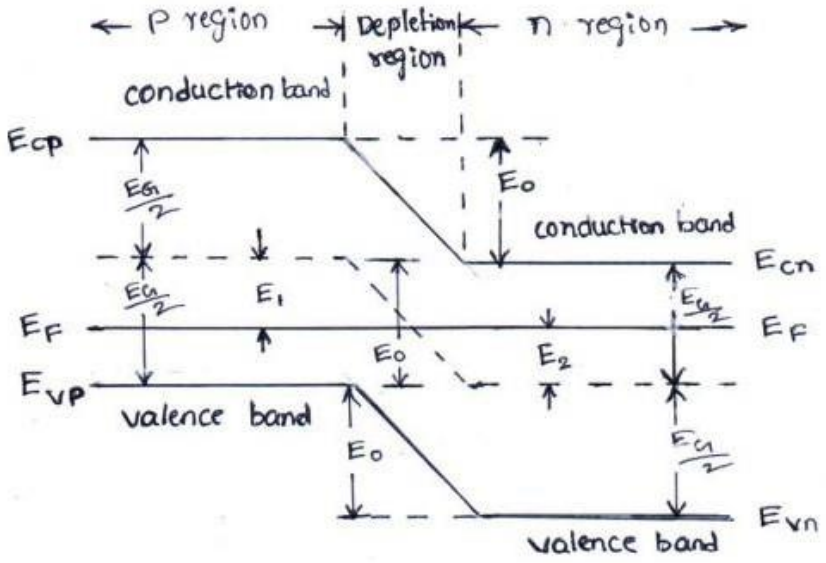



Fig:Energy Band Diagram for p-n Junction under open-circuit Conditions

we know that, for n-type, $E_F = E_{Cn} - kT \ln\left[\frac{N_C}{N_D}\right]$

$$E_{Cn} - E_F = kT \ln\left[\frac{N_C}{N_D}\right] \cdots\cdots\cdots\cdots\cdots\cdots (1)$$

for p-type, $E_F = E_{Vp} + kT \ln\left[\frac{N_V}{N_A}\right]$

$$E_F - E_{Vp} = kT \ln\left[\frac{N_V}{N_A}\right] \cdots\cdots\cdots\cdots\cdots\cdots (2)$$

Since, $n = p = n_i$ *and* $np = n_i^2$

In N-type, $n_n \cong N_D$

$$n_n p_n \cong n_i^2$$

$$p_n = \frac{n_i^2}{N_D} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (3)$$

In P-type $p_p \cong N_A$

$$n_p p_p \cong n_i^2$$

$$n_p = \frac{n_i^2}{N_A} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (4)$$

From the energy band diagram

$$E_{Cn} - E_F = \frac{E_G}{2} - E_2 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (5)$$

$$E_F - E_{Vp} = \frac{E_G}{2} - E_1 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (6)$$

From equation (5)and equation (6), we get,

$$E_1 + E_2 = E_G - \left[E_{Cn} - E_{Vp}\right] \cdots\cdots\cdots\cdots\cdots\cdots (7)$$

Also from band structure, $E_0 = E_1 + E_2$ $\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (8)$

From equation (7) and equation (8), we get,

$$E_0 = E_G - \left[E_{Cn} - E_{Vp}\right] \cdots\cdots\cdots\cdots (9)$$

By adding equation (1) and (2), we get,

$$E_{Cn} - E_F + E_F - E_{Vp} = kT \ln\left[\frac{N_C}{N_D}\right] + kT \ln\left[\frac{N_V}{N_A}\right]$$

$$E_{Cn} - E_{Vp} = kT \ln\left[\frac{N_C}{N_D}\right] + kT \ln\left[\frac{N_V}{N_A}\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (10)$$

Since, $np = e^{-(E_C - E_F)/kT} . N_C e^{-(E_F - E_V)/kT} . N_V$

$$n_i^2 = N_C N_V e^{-(E_C - E_V + E_F - E_F)/kT}$$

$$\frac{n_i^2}{(N_C N_V)} = e^{-(E_C - E_V)/kT}$$

$$\gg \quad \frac{n_i^2}{(N_C N_V)} = e^{-\left(\frac{E_G}{kT}\right)} \qquad [\because E_C - E_V = E_G]$$

Taking ln on both sides we get,

$$\ln\left[\frac{n_i^2}{N_C N_V}\right] = -\left[\frac{E_G}{kT}\right]$$

$$kT \ln\left[\frac{N_C N_V}{n_i^2}\right] = E_G \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (11)$$

substituting the values of equation (10) and equation (11) in equation (9), we get,

$$E_0 = kT \ln\left[\frac{N_C N_V}{n_i^2}\right] - kT \ln\left[\frac{N_C}{N_D}\right] - kT \ln\left[\frac{N_V}{N_A}\right]$$

$$E_0 = kT \ln\left[\frac{N_C N_V}{n_i^2} \times \frac{N_D}{N_C} \times \frac{N_A}{N_V}\right]$$

$$E_0 = kT \ln\left[\frac{N_A N_D}{n_i^2}\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (12)$$

Further for p-type, $p_{p_0} = N_A$, $n_{p0} = \frac{n_i^2}{N_A}$, $N_A = \frac{n_i^2}{n_{p0}}$

Further for N-type, $n_{n_0} = N_D$, $p_{n0} = \frac{n_i^2}{N_D}$, $N_D = \frac{n_i^2}{p_{n0}}$

Therefore $E_0 = kT \ln\left[\frac{n_{n0}}{n_{p0}}\right]$ and $E_0 = kT \ln\left[\frac{p_{p0}}{p_{n0}}\right]$

Where the subscript '0' indicate that the above relations are obtained under thermal conditions of equilibrium.

## 1.0..5 Doide current equation

- When a forward bias ($V_A$>0) is applied, the potential barrier to diffusion across the junction isreduced
  - Minority carriers are "injected" into the quasi-neutral regions =>D$n_p$> 0, D$p_n$>0
- Minority carriers diffuse in the quasi-neutral regions, recombining with majoritycarriers
- Solve minority-carrier diffusion equations in quasi-neutral regions to obtain excess carrier distributionsD$n_p$($x$,$V_A$),D$p_n$($x$,$V_A$)

- boundaryconditions:
  - p side: D$n_p$(-$x_p$),D$n_p$(-∞)
  - n side: D$p_n$($x_n$),D$p_n$(∞)

- Find minority-carrier current densities in quasi-neutral regionsEvaluate $J_n$ at $x$=-$x_p$&$J_p$ at $x$=$x_n$ to obtain total current density $J$

$$J(V_A) = J_n(-x_p, V_A) + J_p(x_n, V_A)$$

Consider the equilibrium ($V_A$ = 0) carrier concentrations:

Consider the **equilibrium** ($V_A$ = 0) carrier concentrations:

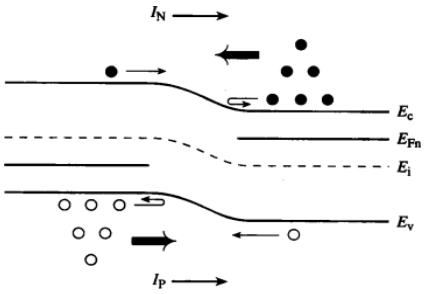
| **p side** | **n side** |
|---|---|
| $p_{p0}(-x_p) = N_A$ | $n_{n0}(x_n) = N_D$ |
| $n_{p0}(-x_p) = \frac{n_i^2}{N_A}$ | $p_{n0}(x_n) = \frac{n_i^2}{N_D}$ |

If low-level injection conditions hold in the quasi-neutral regions when $V_A \neq 0$, then

$$p_p(-x_p) = N_A \qquad n_n(x_n) = N_D$$

The voltage applied to a pn junction falls mostly across the depletion region (assuming low-level injection in the quasi-neutral regions).

We can draw 2 quasi-Fermi levels in the depletion region:




$$p = n_i e^{(E_i - F_P)/kT}$$

$$n = n_i e^{(F_N - E_i)/kT}$$

$$pn = n_i^2 e^{(F_N - F_P)/kT}$$

$$\boxed{pn = n_i^2 e^{qV_A/kT}}$$

# Excess Carrier Concentrations at $-x_p$, $x_n$

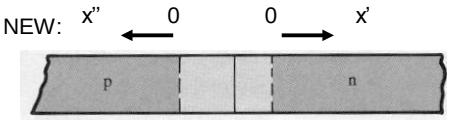
| **p side** | **n side** |
|---|---|
| $p_p(-x_p) = N_A$ | $n_n(x_n) = N_D$ |
| $n_p(-x_p) = \dfrac{n_i^2 e^{qV_A/kT}}{N_A} = n_{p0} e^{qV_A/kT}$ | $p_n(x_n) = \dfrac{n_i^2 e^{qV_A/kT}}{N_D} = p_{n0} e^{qV_A/kT}$ |
| $\Delta n_p(-x_p) = \dfrac{n_i^2}{N_A}\left(e^{qV/kT} - 1\right)$ | $\Delta p_n(x_n) = \dfrac{n_i^2}{N_D}\left(e^{qV_A/kT} - 1\right)$ |

Excess Carrier Distribution (n side)

- From the minority carrier diffusionequation: $\frac{d^2\Delta p}{dx^2}_{n} = \frac{\Delta p_n}{D_p \tau_p} = \frac{\Delta p_n}{L_p^2}$
- We have the following boundary conditions:

$$\Delta p_n(x_n) = p_{no}(e^{qV_A/kT} - 1) \qquad \Delta p_n(\infty) \to 0$$

- For simplicity, use a new coordinatesystem:




- Then, the solution is of theform: $\Delta p_n(x') = Ae_1^{x'/L_p} + A\, e_2^{-x'/L_p}$

$$\Delta p_n(x') = Ae_1^{x'/L_p} + A\, e_2^{-x'/L_p}$$

Fromthe$x=\infty$boundarycondition:

Fromthe$x=x_n$boundarycondition:

Therefore $\Delta p_n(x') = p_{no}\ (e^{qV_A/kT} - 1)e^{-x'/L_p}, \quad x' > 0$

Similarly, we can derive

$$\Delta n_p(x'') = n_{po}(e^{qV_A/kT} - 1)e^{-x''/L_n}, \quad x'' > 0$$

# Total Current Density

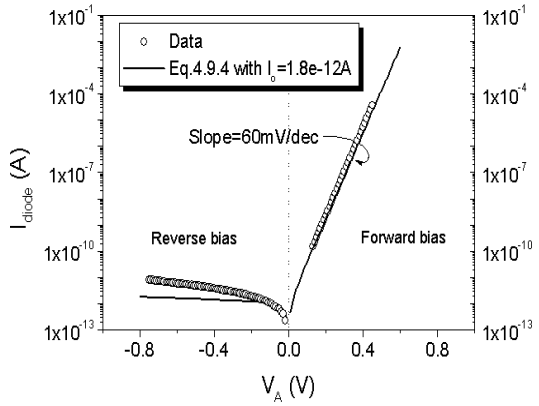
**p side:** $J_n = -qD_n \frac{d\Delta n_p(x'')}{dx''} = q\frac{D_n}{L_n} n_{p0}(e^{qV_A/kT}-1)e^{-x''/L_n}$

**n side:** $J_p = -qD_p \frac{d\Delta p_n(x')}{dx'} = q\frac{D_p}{L_p} p_{n0}(e^{qV_A/kT}-1)e^{-x'/L_p}$

$$J = J_n|_{x=-x_p} + J_p|_{x=x_n} = J_n|_{x'=0} + J_p|_{x'=0}$$

$$J = qn_i^2\left[\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right](e^{qV_A/kT}-1)$$

# Ideal Diode Equation




$$I = I_0(e^{qV_A/kT}-1)$$

$$I_0 = Aqn_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)$$

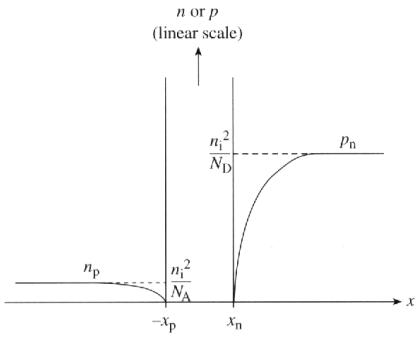
# Diode Saturation Current $I_0$

- $I_0$ can vary by orders of magnitude,depending on the semiconductor material and dopant concentrations:

$$I_0 = Aqn_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)$$

- In an asymmetrically doped (one-sided) pn junction, theterm associated with the more heavily doped side is negligible:
  - If the p side is much more heavily doped, $I_0 \cong Aqn_i^2\left(\frac{D_p}{L_p N_D}\right)$
  - If the n side is much more heavily doped, $I_0 \cong Aqn_i^2\left(\frac{D_n}{L_n N_A}\right)$

# Carrier Concentration Profiles under ReverseBias

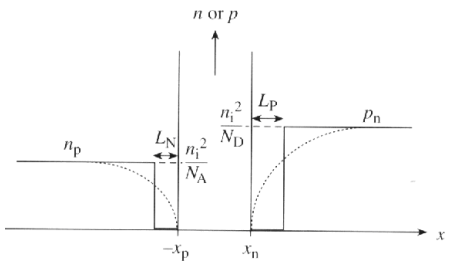



- Depletion of minority carriers at edges of depletionregion
- The only current which flows is due to **drift** of minority carriers across the junction. This current is fed by diffusion of minority carriers toward junction (supplied by thermalgeneration).

# Alternative Derivation of Formula for $I_0$

**"Depletion approximation":**

- **$I_0$ is the rate at which carriers are thermally generated within one diffusion length of the depletionregion:**




$$\frac{\partial n}{\partial t} = -\frac{\Delta n_p}{\tau_n} = \frac{n_i^2 / N_A}{\tau_n} \qquad -L_N \le x \le -x_p$$

$$\frac{\partial p}{\partial t} = -\frac{\Delta p}{\tau_p} = \frac{n_i^2 / N_D}{\tau_p} \qquad x_n \le x \le x_n + L_P$$

$$I_0 = qAL_N \left| \frac{\left( n_i^2 / N_A \right)}{\tau_n} \right| + qAL_P \left| \frac{\left( n_i^2 / N_D \right)}{\tau_p} \right|$$

- Under forward bias ($V_A > 0$), the potential barrier to carrier diffusionisreduced→minoritycarriersare"injected"intothe quasi-neutralregions.
  - The minority-carrier concentrations at the edges of the depletionregion change with the applied bias $V_A$, by the factor $e^{qV_A/kT}$
  - The excess carrier concentrations in the quasi-neutral regions decay to zero away from the depletion region, due torecombination.

pn junction diodecurrent $$I = qAn_i^2 \left[ \frac{D_n}{L_N N_A} + \frac{D_p}{L_p N_D} \right] \left( e^{qV_A/kT} - 1 \right)$$

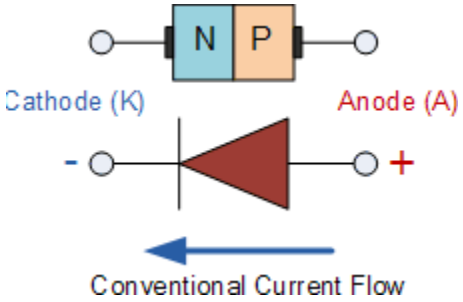
- $I_0$canbeviewedasthedriftcurrentduetominoritycarriers generatedwithinadiffusionlengthofthedepletionregion

# QUANTITATIVE THEORY OF PN JUNCTIONDIODE:

## PN JUNCTION WITH NO APPLIED VOLTAGE OR OPENCIRCUIT CONDITION:

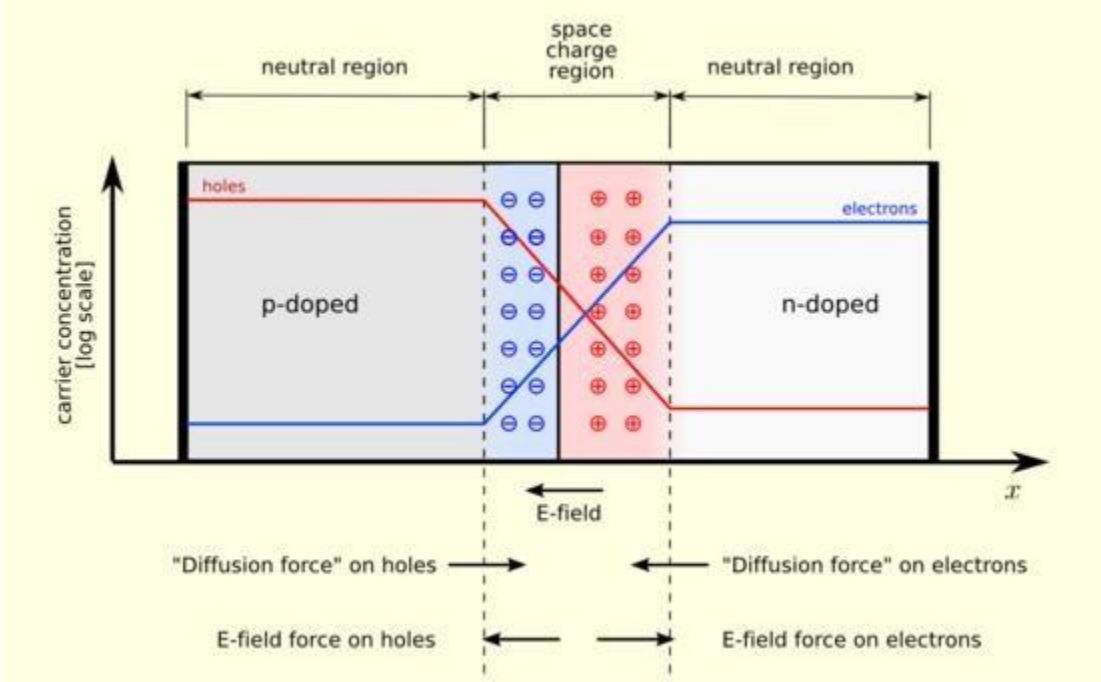
In a piece of sc, if one half is doped by p type impurity and the other half is doped by n type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. As shown in the fig the n type material has high concentration of free electrons, while p type material has high concentration of holes. Therefore at the junction there is a tendency of

free electrons to diffuse over to the P side and the holes to the N side. This process is called

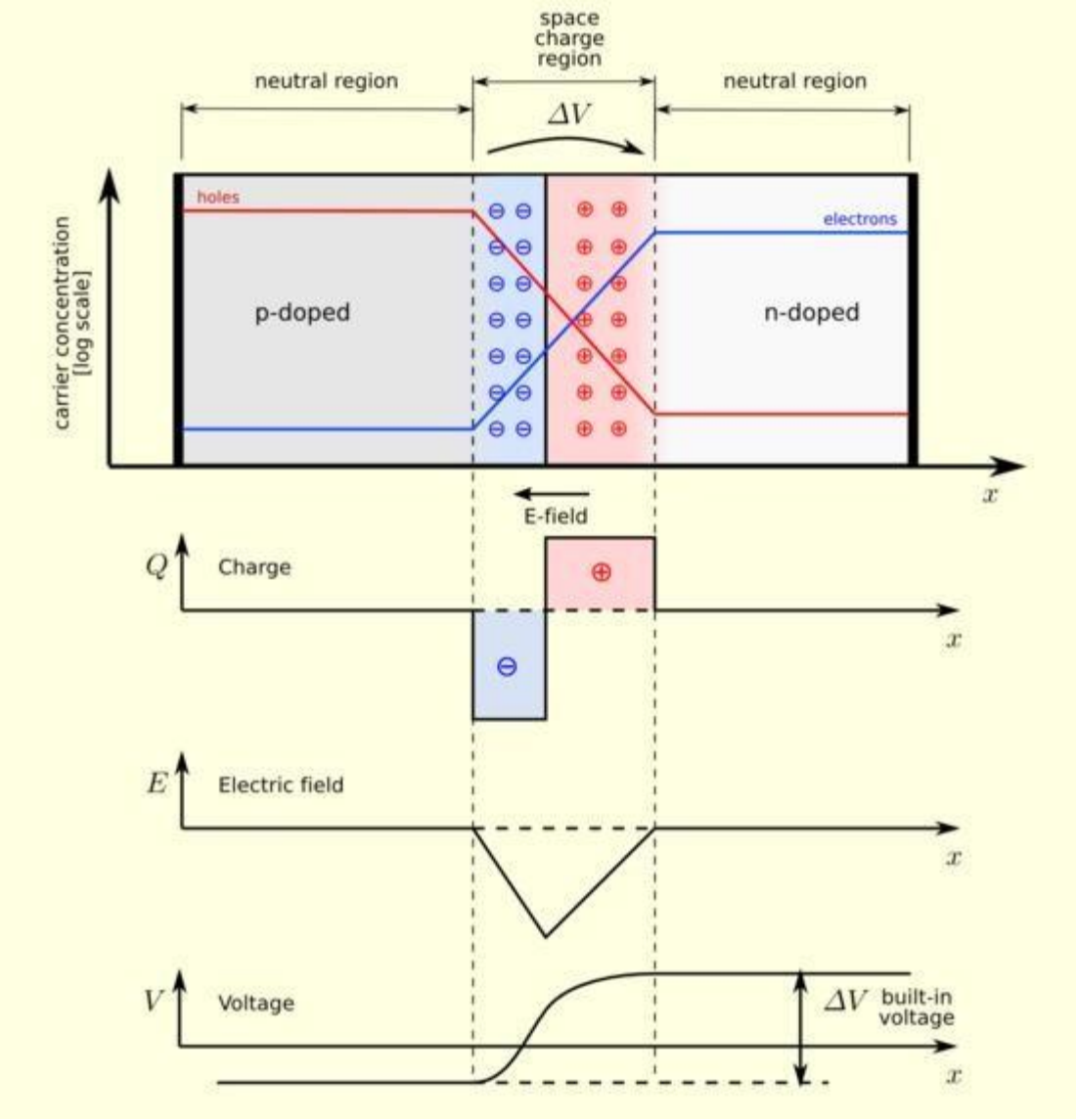



diffusion. As the free electrons move across the junction from N type to P type, the donor atoms become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filing the holes. Therefore a negative charge is developed on the p –side of the junction..This net negative charge on the p side prevents further diffusion of electrons into the p side. Similarly the net positive charge on the N side repels the hole crossing from p side to N side. Thus a barrier sis set up near the junction which prevents the further movement of charge carriers i.e. electrons and holes. As a consequence of induced electric field across the depletion layer, an electrostatic potential difference is established between P and N regions, which are called the potential barrier, junction barrier, diffusion potential or contact potential, Vo. The magnitude of the contact potential Vo varies with doping levels and temperature. Vo is 0.3V for Ge and 0.72 V for Si.

The electrostatic field across the junction caused by the positively charged N-Type region tends to drive the holes away from the junction and negatively charged p type regions tend to drive the electrons away from the junction. The majority holes diffusing out of the P region leave behind negatively charged acceptor atoms bound to the lattice, thus exposing a negatives pace charge in a previously neutral region. Similarly electrons diffusing from the N region expose positively ionized donor atoms and a double space charge builds up at the junction as shown in the fig. 1.7




It is noticed that the space charge layers are of opposite sign to the majority carriers diffusing into them, which tends to reduce the diffusion rate. Thus the double space of the layer causes an electric field to be set up across the junction directed from N to P regions, which is in such a direction to inhibit the diffusion of majority electrons and holes as illustrated in fig 1.7. The shape of the charge density, ρ, depends upon how diode id doped. Thus the junction region is depleted of mobile charge carriers. Hence it is called depletion layer, space region, and transition region. The depletion region is of the order of 0.5μm thick. There are no mobile carriers in this narrow depletion region. Hence no current flows across the junction and the system is in equilibrium. To the left of this depletion layer, the carrier concentration is $p= N_A$and to its right it is $n=N_D$.

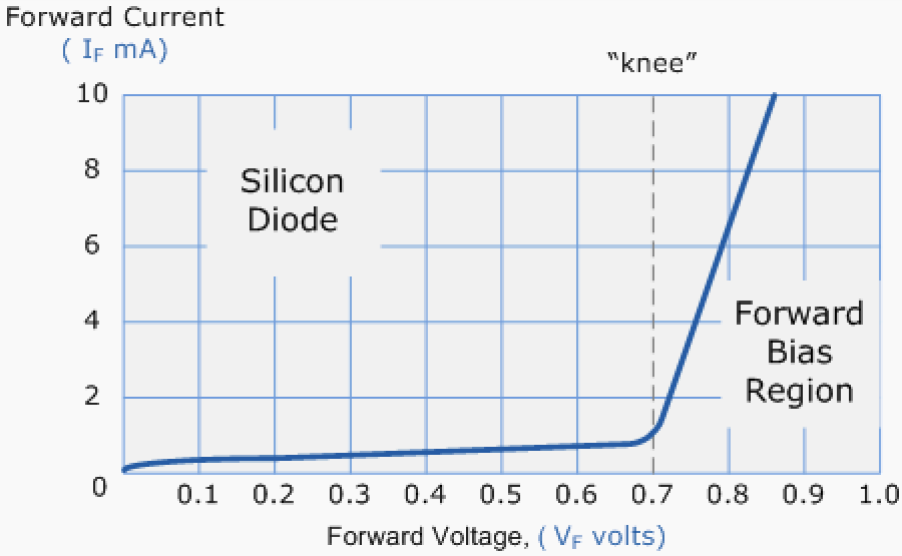



## FORWARD BIASED JUNCTIONDIODE

When a diode is connected in a **Forward Bias** condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current

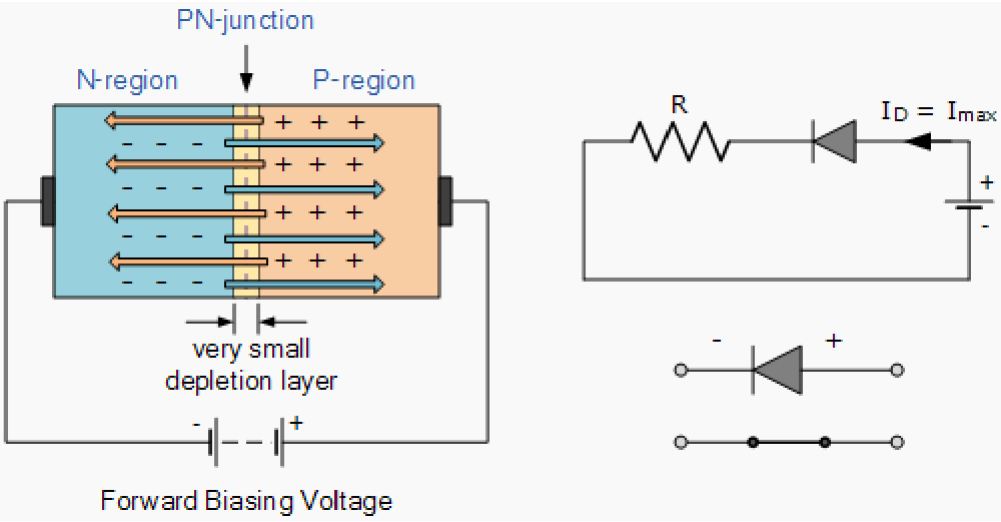
flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.

**Forward Characteristics Curve for a Junction Diode**



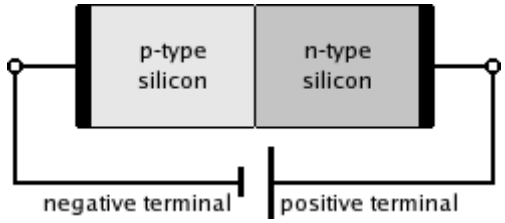

The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the "knee" point.

**Forward Biased Junction Diode showing a Reduction in the Depletion Layer**



This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes. Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow. Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

### 1.1.2 PN JUNCTION UNDER REVERSE BIAS CONDITION:

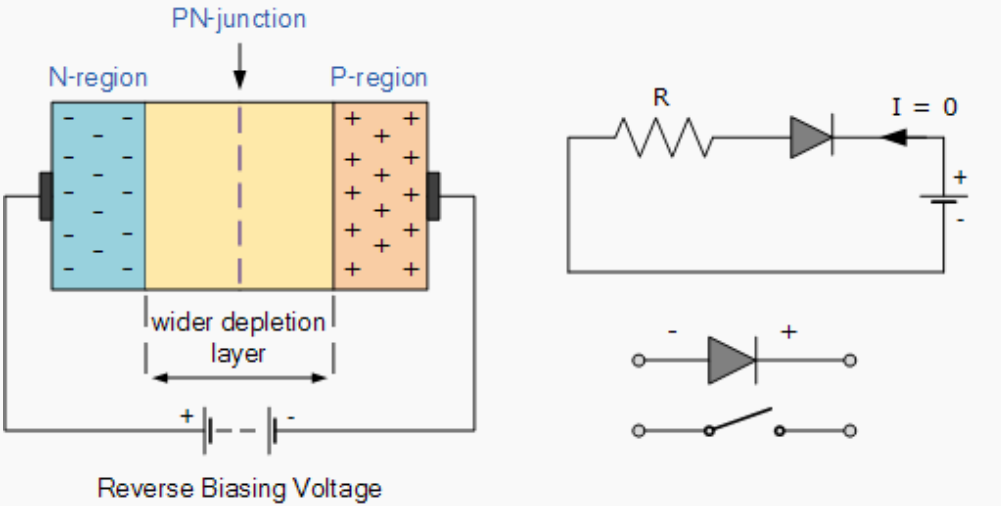



A silicon p–n junction in reverse bias.

**Reverse Biased Junction Diode**

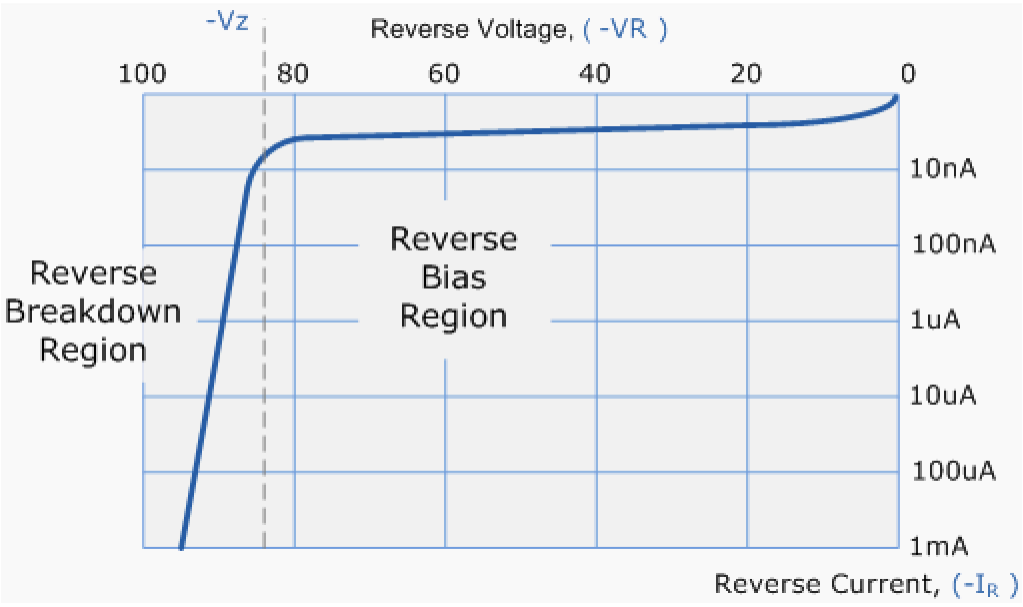
When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away fromthe junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

**Reverse Biased Junction Diode showing an Increase in the Depletion Layer**




This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current** does flow through the junction which can be measured in microamperes, (μA). One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will cause the PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve below.

**Reverse Characteristics Curve for a Junction Diode**



Sometimes this avalanche effect has practical applications in voltage stabilising circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset maximum value thereby producing a fixed voltage output across the diode. These types of diodes are commonly known as **Zener Diodes** and are discussed in a later tutorial.

## V-I CHARACTERISTICS AND THEIRTEMPERATURE DEPENDENCE:

Diode terminal characteristics equation for diode junction current:

$$I_D = J(e^{\frac{v}{\eta v_T}} - 1)$$

Where VT = kT/q;

VD_ diode terminal voltage, Volts

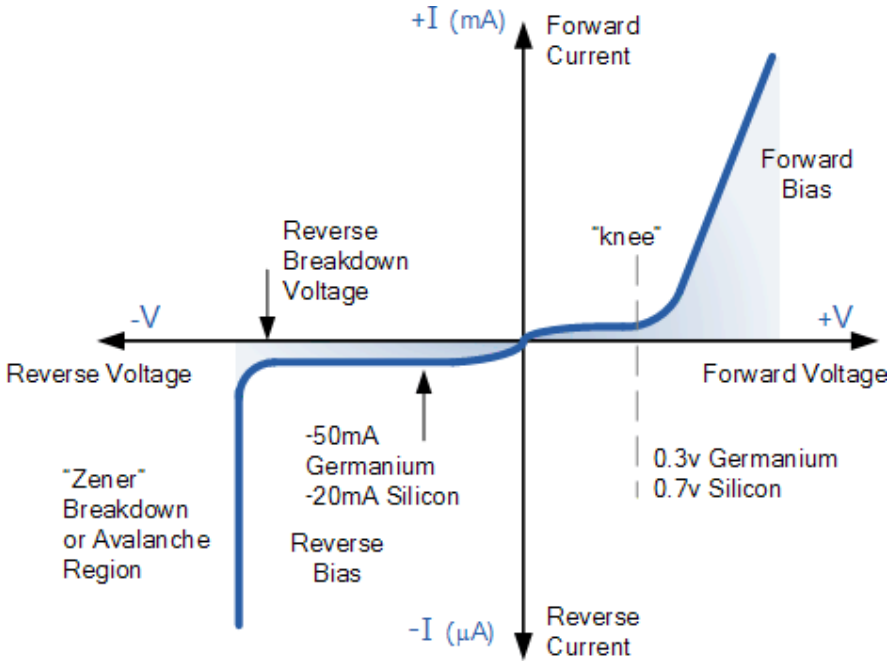
Io _ temperature-dependent saturation current, µA

T _ absolute temperature of p-n junction, K

k _ Boltzmann's constant 1.38x 10 -23J/K)

q _ electron charge 1.6x10-19 C

$\eta$= empirical constant, 1 for Ge and 2 for Si




**Temperature Effects on Diode**

Temperature can have a marked effect on the characteristics of a silicon semiconductor diode as shown in Fig. 1.24. It has been found experimentally that the reverse saturation current Io will just about double in magnitude for every 10°C increase in temperature.

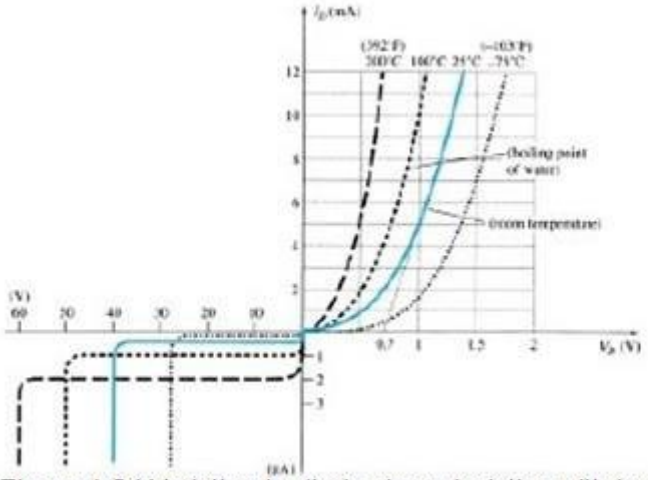


Figure 1.24 Variation in diode characteristics with temperature change.

It is not uncommon for a germanium diode with an Io in the order of 1 or 2 A at 25°C to have a leakage current of 100 A _ 0.1 mA at a temperature of 100°C. Typical values of Io for silicon are much lower than that of germanium for similar power and current levels. The result is that even at high temperatures the levels of Io for silicon diodes do not reach the same high levels obtained.for germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium. The increasing levels of Io with temperature account for the lower levels of threshold voltage, as shown in Fig. 1.24. Simply increase the level of Io in and not rise in diode current. Of course, the level of TK also will be increase, but the increasing level of Io will overpower the smaller percent change in TK. As the temperature increases the forward characteristics are actually becoming more“ideal,”

# IDEAL VERSUS PRACTICAL RESISTANCELEVELS

**DC or Static Resistance**

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of VD and ID as shown in Fig. 1.25 and applying the followingEquation:

$$R_D = \frac{V_D}{I_D}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

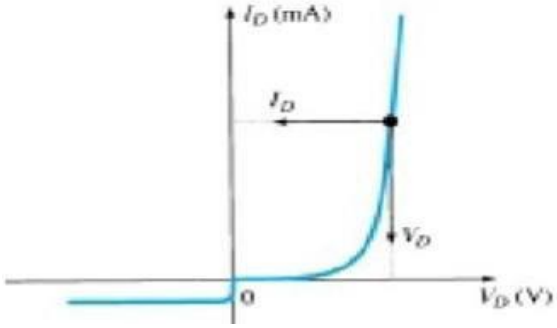



Figure 1.25 determining the dc resistance of a diode at a particular operating point.

**AC or Dynamic Resistance**

It is obvious from Eq. 1.5 that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.27. With no applied varying signal, the point of operation would be the Q-point appearing on Fig. 1.27 determined by the applied dc levels. The designation Q-point is derived from the word quiescent, which means "still or unvarying." A straight-line drawn tangent to the curve through the Q-point as shown in Fig. 1.28 will define a particular change in voltage and current that can be used to determine the ac or dynamic resistance for this region of the diode characteristics. In equationform,

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

where Δ signifies a finite change in the quantity.

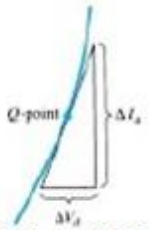



Figure 1.28 determining the ac resistance at a Q-point.

# DIODE EQUIVALENTCIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region. In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behaviour of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

**Piecewise-Linear Equivalent Circuit**

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.31. The resulting equivalent circuit is naturally called the piecewise-linear equivalent circuit. It should be obvious from Fig. 1.31 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behaviour of the device. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open- circuit state for the device. Since a silicon semiconductor, diode does not reach the conduction state until VD reaches 0.7 V with a forward bias (as shown in Fig. 1.31), a battery VT opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.32. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established, the resistance of the diode will be the specified value of rav.

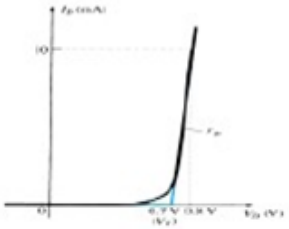


Figure 1.31 Defining the piecewise-linear equivalent circuit using straight-line segments to

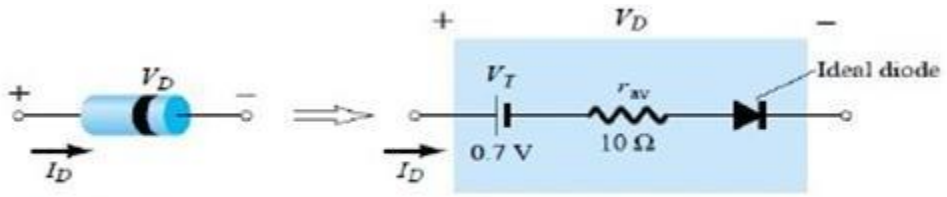



Figure 1.32 Components of the piecewise-linear equivalent circuit.

The approximate level of rav can usually be determined from a specified operating point on the specification sheet. For instance, for a silicon semiconductor diode, if IF _ 10 mA (a forward conduction current for the diode) at VD _ 0.8 V, we know for silicon that a shift of 0.7 V is required before the characteristics rise.

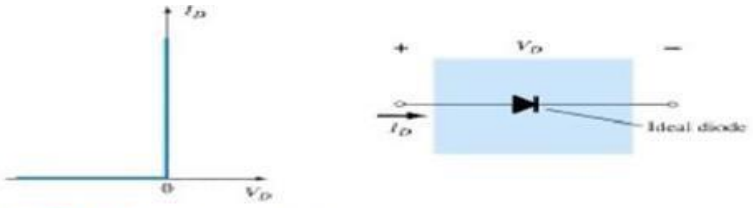
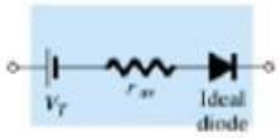
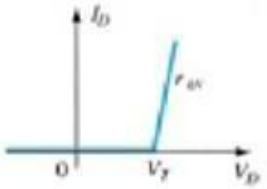
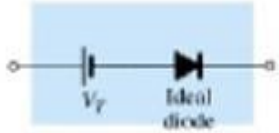
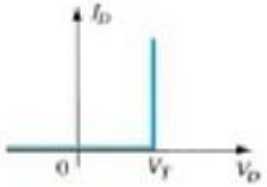
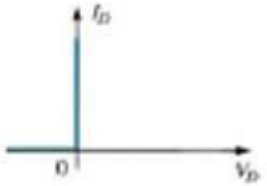



Figure 1.34 Ideal diode and its characteristics.

**TABLE 1.3 Diode Equivalent Circuits (Models)**

| Type | Conditions | Model | Characteristics |
|---|---|---|---|
| Piecewise-linear model | |   |   |
| Simplified model | $R_{network} \gg r_{av}$ |   |   |
| Ideal device | $R_{network} \gg r_{av}$<br>$E_{network} \gg V_T$ |   |   |

# TRANSITION AND DIFFUSIONCAPACITANCE

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance XC=1/2πfC is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. XC will become sufficiently small due to the high value of f to introduce a low-reactance “shorting” path. In the p-n semiconductor diode, there are two capacitive effects to be considered. In the reverse-bias region we have the transition- or depletion region capacitance (CT), while in the forward-bias region we have the diffusion (CD) or storage capacitance. Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by C=€A/d, where € is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In the reverse-, bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. Although the effect described above will also be present in the forward-bias region, it is over shadowed by a capacitance effect directly dependent on the rate at which charge is injectedinto

the regions just outside the depletion region. The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

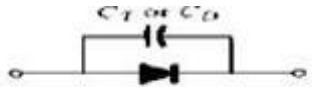



Figure 1.38 Including the effect of the transition or diffusion capacitance on the semiconductor diode.

**Diode capacitances:** The diode exhibits two types of capacitances transition capacitance and diffusion capacitance.

. Transition capacitance: The capacitance which appears between positive ion layer in n-region and negative ion layer inp-region.

· Diffusion capacitance: This capacitance originates due to diffusion of charge carriers in the oppositeregions.

The transition capacitance is very small as compared to the diffusion capacitance.

In reverse bias transition, the capacitance is the dominant and is given by:

$$C_T = \epsilon A/W$$

where $C_T$ - transition capacitance

A - diode cross sectional area

W - depletion region width

In forward bias, the diffusion capacitance is the dominant and is given by:

$$C_D = dQ/dV = \tau * dI/dV = \tau * g = \tau/r \text{ (general)}$$

where $C_D$ - diffusion capacitance

dQ - change in charge stored in depletion region

V - change in applied voltage

$\tau$- time interval for change in voltage

g - diode conductance

r - diode resistance

The diffusion capacitance at low frequencies is given by the formula:

$C_D = \tau^* g/2$ (low frequency) The diffusion capacitance at high frequencies is inversely proportional to the frequency and is given by the formula:

$C_D = g(\tau/2\omega)^{1/2}$ *Note: The variation of diffusion capacitance with applied voltage is used in the design ofvaractor.*

# BREAK DOWNMECHANISMS

When an ordinary **P-N junction diode**is reverse biased, normally only very small reverse saturation current flows. This current is due to movement of minority carriers. It is almost independent of the voltage applied. However, if the reverse bias is increased, a point is reached when the junction breaks down and the reverse current increases abruptly. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its breakdown region to its normal (reverse saturation) level. It is found that for a suitably designed diode, the breakdown voltage is very stable over a wide range of reverse currents. This quality gives the *breakdown**diode***many useful applications as a *voltage referencesource.*

The critical value of the voltage, at which the breakdown of a P-N junction diode occurs is called the *breakdown voltage.* The breakdown voltage depends on the width of the depletion region, which, in turn, depends on the doping level. The junction offers almost zero resistance at the breakdown point.

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction :

1. ***avalanche breakdown*and**
2. ***Zenerbreakdown.***

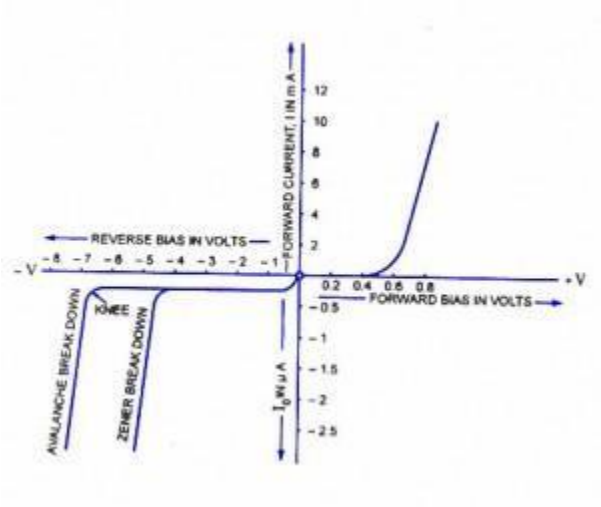
***Avalanche breakdown* and**

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of

collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. *The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.*

**Zener breakdown**

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3 x 10^7 V/m.




Either of the two (Zener breakdown or avalanche breakdown) may occur independently, or both of these may occur simultaneously. Diode junctions that breakdown below 5 V are caused by Zener effect. Junctions that experience breakdown above 5 V are caused by avalanche effect. Junctions that breakdown around 5 V are usually caused by combination of two effects. The Zener breakdown occurs in heavily doped junctions (P-type semiconductor moderately doped and N-type heavily doped), which produce narrow depletion layers. The avalanche breakdown occurs in lightly doped junctions, which produce wide depletion layers. With the increase in junction temperature Zener breakdown voltage is reduced while the avalanche breakdown voltage increases. The Zener diodes have a negative temperature coefficient while avalanche diodes have a positive temperature coefficient. Diodes that have breakdown voltages around 5 V have zero temperature coefficient. The breakdown phenomenon is reversible and harmless so long as the safe operating temperature ismaintained.

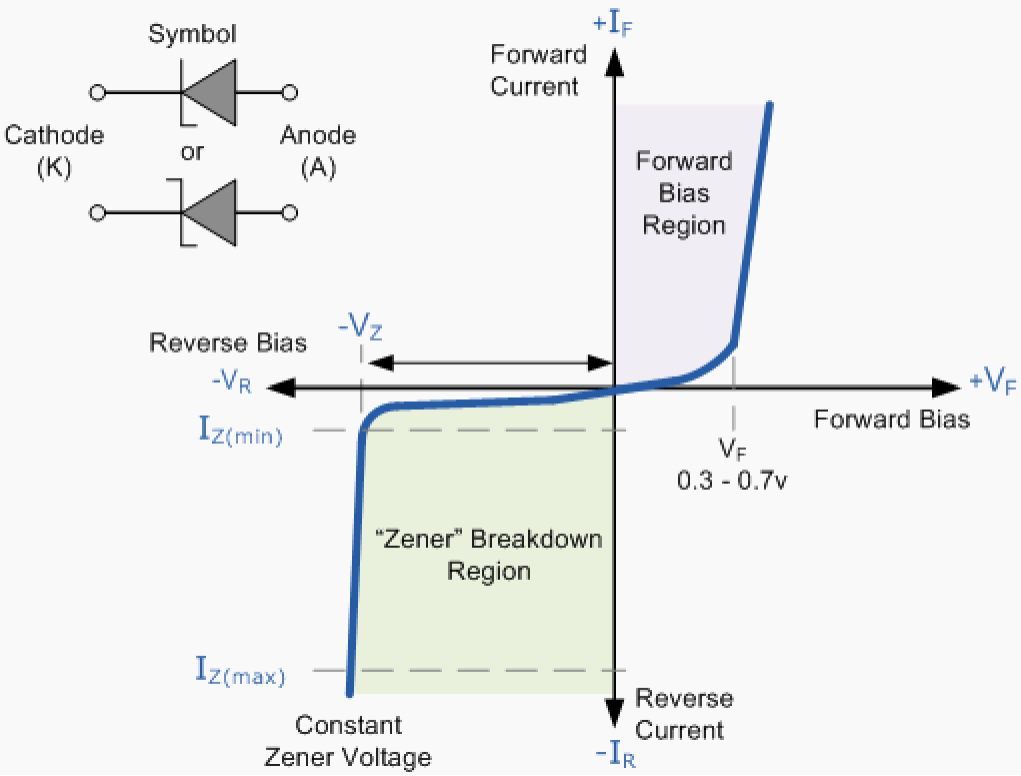
# ZENERDIODES

The **Zener diode** is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but as soon as a reverse voltage applied across the zener diode exceeds the rated voltage of the device, the diodes breakdown voltage $V_B$is reached at which point a process called *Avalanche Breakdown* occurs in the semiconductor depletion layer and a current starts to flow through the diode to limit this increase in voltage.

The current now flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor) and once achived this reverse saturation current remains fairly constant over a wide range of applied voltages. This breakdown voltage point, $V_B$is called the "zener voltage" for zener diodes and can range from less than one volt to hundreds of volts.

The point at which the zener voltage triggers the current to flow through the diode can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes semiconductor construction giving the diode a specific *zener breakdown voltage*, (Vz) for example, 4.3V or 7.5V. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

**Zener Diode I-V Characteristics**




The **Zener Diode** is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects

to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current $I_{Z(min)}$and the maximum current rating$I_{Z(max)}$.

This ability to control itself can be used to great effect to regulate or stabilise a voltage source against supply or load variations. The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important application of the zener diode as a voltage regulator. The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum $I_{Z(min)}$value in the reverse breakdown region.

# UNIT-II

# SPECIAL PURPOSE ELECTRONIC DEVICES AND RECTIFIERS

## PRINCIPLE OF OPERATION AND CHARACTERISTICS OF TUNNELDIODE:

A **tunnel diode** or **Esaki diode** is a type of semiconductor diode which is capable of very fast operation, well into the microwave frequency region, by using quantum mechanical effects.

It was invented in August 1957 by Leo Esaki when he was with Tokyo Tsushin Kogyo, now known as Sony. In 1973 he received the Nobel Prize in Physics, jointly with Brian Josephson, for discovering the electron tunneling effect used in these diodes. Robert Noyce independently came up with the idea of a tunnel diode while working for William Shockley, but was discouraged from pursuing it.


Fig:Tunnel diode schematic symbol

These diodes have a heavily dopedp–n junction only some 10 nm (100 Å) wide. The heavy doping results in a broken bandgap, where conduction band electron states on the n-side are more or less aligned with valence band hole states on the p-side.

Tunnel diodes were manufactured by Sony for the first time in 1957 followed by GeneralElectric and other companies from about 1960, and are still made in low volume today. Tunnel diodes are usually made from germanium, but can also be made in gallium arsenide and silicon materials. They can be used as oscillators, amplifiers, frequency converters anddetectors.

**Tunnelling Phenomenon:**

In a conventional semiconductor diode, conduction takes place while the p–n junction is forward biased and blocks current flow when the junction is reverse biased. This occurs up to a point known as the “reverse breakdown voltage” when conduction begins (often accompanied by destruction of the device). In the tunnel diode, the dopant concentration in the p and n layers are increased to the point where the **reverse breakdown voltage** becomes **zero** and the diode conducts in the reverse direction. However, when forward-biased, an odd effect occurs called

"quantum mechanical tunnelling" which gives rise to a region where an *increase* in forward voltage is accompanied by a *decrease* in forward current. This negative resistance region can be exploited in a solid state version of the dynatron oscillator which normally uses a tetrodethermionic valve (or tube).

**Forward bias operation**

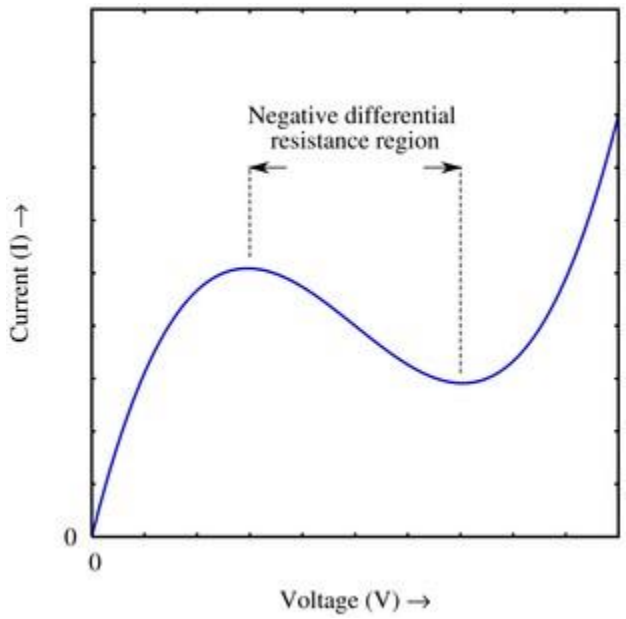
Under normal forward bias operation, as voltage begins to increase, electrons at first tunnel through the very narrow p–n junction barrier because filled electron states in the conduction band on the n-side become aligned with empty valence band hole states on the p-side of the p-n junction. As voltage increases further these states become more misaligned and the current drops – this is called *negative resistance* because current decreases with increasing voltage. As voltage increases yet further, the diode begins to operate as a normal diode, where electrons travel by conduction across the p–n junction, and no longer by tunneling through the p–n junction barrier. Thus the most important operating region for a tunnel diode is the negative resistance region.

**Reverse bias operation**

When used in the reverse direction they are called **back diodes** and can act as fast rectifiers with zero offset voltage and extreme linearity for power signals (they have an accurate square law characteristic in the reverse direction).

Under reverse bias filled states on the p-side become increasingly aligned with empty states on the n-side and electrons now tunnel through the pn junction barrier in reverse direction – this is the Zener effect that also occurs in zener diodes.

**Technical comparisons**




A rough approximation of the VI curve for a tunnel diode, showing the negative differential resistance region.The Japanese physicist Leo Esaki invented the tunnel diode in 1958.It consists of a p-n junction with highly doped regions. Because of the thinness of the junction, the electrons can pass through the potential barrier of the dam layer at a suitable polarization, reaching the energy states on the other sides of the junction. The current-voltage characteristic of the diode is represented in Figure 1. In this sketch *i p* and *Up* are the peak, and *iv* and *Uv* are the valley values for the current and voltage respectively. The form of this dependence can be qualitatively explained by considering the tunneling processes that take place in a thin p-njunction.

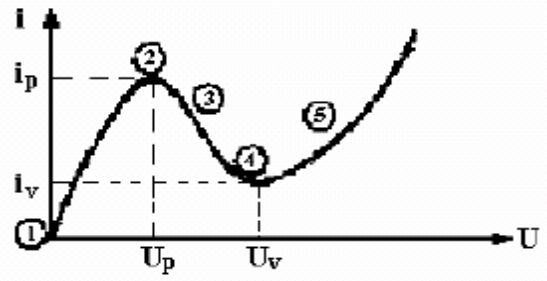



Figure 1.

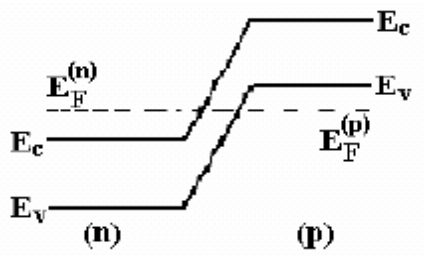



Figure 2.

**Energy band structure of tunnel diode:**

For the degenerated semiconductors, the energy band diagram at thermal equilibrium is presented in Figure2.

In Figure 3 the tunneling processes in different points of the current voltage characteristic for the tunnel diode are presented.

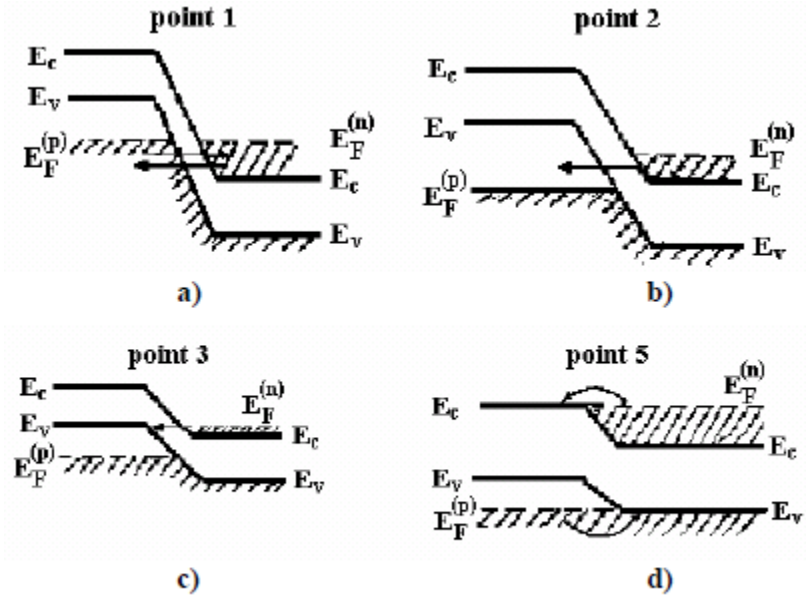



Figure 3.

In Fig. 3a, the thermal equilibrium situation corresponding to point 1

from the Fig. 1 diagram presented; in this case the electrons will uniformly tunnel in both directions, so the current will be null. At a direct polarization, a non-zero electron flow will tunnel from the occupied states of the conduction band of the n region to the emptystates
of the valence band from the p region. The current attains a maximum when the overlap of the empty and occupied states reaches the maximum value; a minimum value is reached when there are no states for tunneling on the sides of the barrier. In this case, the tunnel current should drop to zero.

## Advantages of tunnel diodes:

- Environmental immunity i.e peak point is not a function oftemperature.
- lowcost.
- low noise.
- low powerconsumption.
- High speed i.e tunneling takes place very fast at the speed of light in the order of nanoseconds
- simplicity i.e a tunnel diode can be used along with a d.c supply and a few passive elements to obtain various applicationcircuits.

## Applications for tunnel diodes:

- local oscillators for UHF televisiontuners
- Trigger circuits inoscilloscopes
- High speed counter circuits and very fast-rise time pulse generatorcircuits
- The tunnel diode can also be used as low-noise microwaveamplifier.

# VARACTORDIODE:

Varactor diode is a special type of diode which uses transition capacitance property i.e voltage variable capacitance .These are also called as varicap,VVC(voltage variable capacitance) or tuning diodes.

The varactor diode symbol is shown below with a diagram representation.

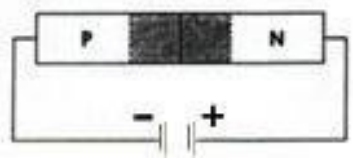



Fig:symbol of varactor diode

When a reverse voltage is applied to a PN junction , the holes in the p-region are attracted to the anode terminal and electrons in the n-region are attracted to the cathode terminal creating a region where there is little current.This region ,the depletion region, is essentially devoid of carriers and behaves as the dielectric of a capacitor.

The depletion region increases as reverse voltage across it increases; and since capacitance varies inversely as dielectric thickness, the junction capacitance will decrease as the voltage across the PN junction increases. So by varying the reverse voltage across a PN junction the junction capacitance can be varied .This is shown in the typical varactor voltage-capacitance curve below.

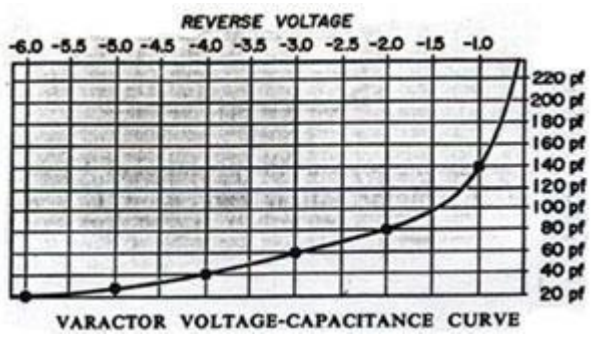



Fig:voltage- capacitance curve

Notice the nonlinear increase in capacitance as the reverse voltage is decreased. This nonlinearity allows the varactor to be used also as a harmonic generator.

Major varactor considerations are:
**(a)** Capacitancevalue
**(b)** Voltage
**(c)** Variation in capacitance withvoltage.
**(d)** Maximum workingvoltage
**(e)** Leakage current

## Applications:

- Tunedcircuits.
- FMmodulators
- Automatic frequency controldevices
- Adjustable bandpassfilters
- Parametric amplifiers
- Televisionreceivers.

## SCHOTTKYDIODE:

A Schottky diode is a majority carrier device, where electron-hole recombination is usually not important. Hence, Schottky diodes have a much faster response under forward bias conditions than *p-n* junction diodes. Therefore, Schottky diodes are used in applications where the speed of a response is important, for example, in microwave detectors, mixers, and varactors. schottky diodes are specially manufactured to solve the problem of fast switching which consists of a metal to semiconductor junction**.**The symbol of schottky diode is as follows:


Fig:symbol of schottky diode

**Structure and principle of operation**

**1. Structure**

The structure of a metal-semiconductor junction is shown in Figure 1. It consists of a metal contacting a piece of semiconductor. An ideal Ohmic contact, a contact such that no potential exists between the metal and the semiconductor, is made to the other side of the semiconductor. The sign convention of the applied voltage and current is also shown on Figure 1.

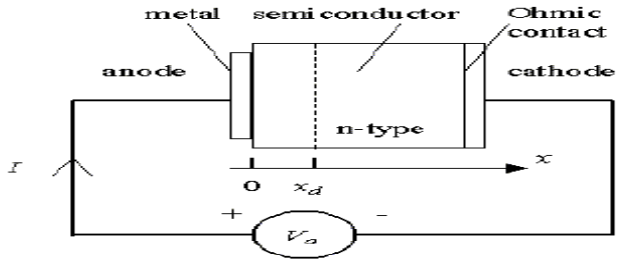



**Figure 1 :** Structure and sign convention of a metal-semiconductor junction

**Flatband diagram and built-inpotential**

The barrier between the metal and the semiconductor can be identified on an energy band diagram. To constructsuchdiagramwefirstconsidertheenergybanddiagramofthemetalandthesemiconductor,and align them using the same vacuum level as shown in Figure 2 (a). As the metal and semiconductor are brought together, the Fermi energies of the metal and the semiconductor do not change right away. This yields the flatband diagram of Figure 2(b).

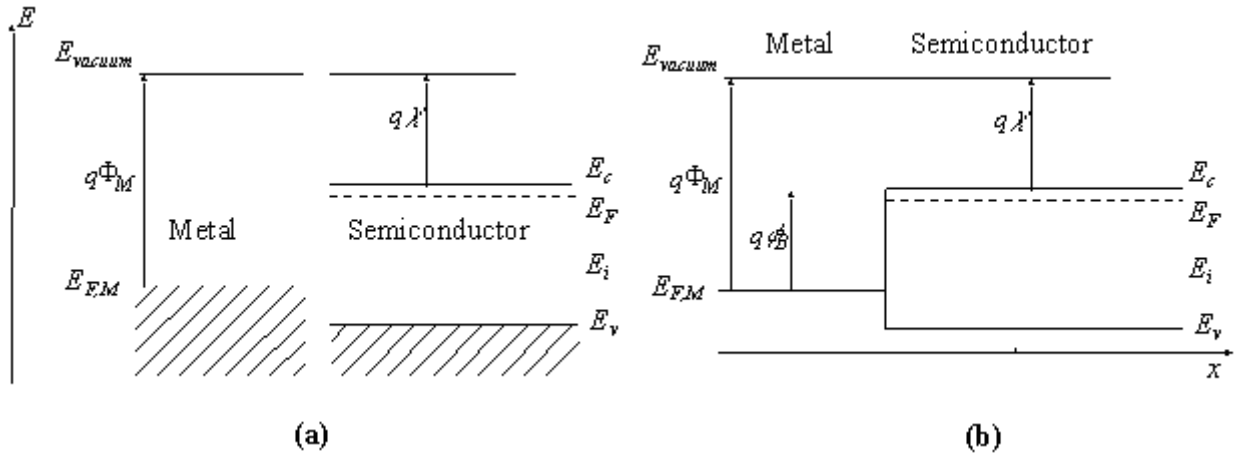



**Figure 2 :** Energy band diagram of the metal and the semiconductor before (a) and after (b) contact is made.

The barrier height, $\phi_B$, is defined as the potential difference between the Fermi energy of the metal andthe band edge where the majority carriers reside. From Figure 2 (b) one finds that for an n-type semiconductor the barrier height is obtainedfrom:

$$\phi_B = \Phi_M - \chi \quad \text{, for an n-type semiconductor} \tag{1.1}$$

Where $\Phi_M$ is the work function of the metal and $\chi$ is the electron affinity. The work function of selected metals as measured in vacuum can be found in Table 1. For p-type material, the barrier height is given by the difference between the valence band edge and the Fermi energy in the metal:

$$\phi_B = \frac{E_g}{q} + \chi - \Phi_M \quad \text{, for a p-type semiconductor} \tag{1.2}$$

A metal-semiconductor junction will therefore form a barrier for electrons and holes if the Fermi energy of the metal as drawn on the flatband diagram is somewhere between the conduction and valence band edge.

In addition, we define the built-in potential, $\phi_I$, as the difference between the Fermi energy of the metal and that of the semiconductor.

$$\phi_i = \Phi_M - \chi - \frac{E_c - E_{F,n}}{q} \quad , \quad \text{n-type} \tag{1.3}$$

$$\phi_i = \chi + \frac{E_c - E_{F,p}}{q} - \Phi_M \quad , \quad \text{p-type} \tag{1.4}$$

**Energy band diagram of a metal-semiconductor contact in thermal equilibrium.**

The flatband diagram, shown in Figure 2 (b), is not a thermal equilibrium diagram, since the Fermi energy in the metal differs from that in the semiconductor. Electrons in the n-type semiconductor can lower their energy by traversing the junction. As the electrons leave the semiconductor, a positive charge, due to the ionized donor atoms, stays behind. This charge creates a negative field and lowers the band edges of the semiconductor. Electrons flow into the metal until equilibrium is reached between the diffusion of electrons from the semiconductor into the metal and the drift of electrons caused by the field created by the ionized impurity atoms. This equilibrium is characterized by a constant Fermi energy throughout the structure.

**Figure 3 :** Energy band diagram of a metal-semiconductor contact in thermal equilibrium.

It is of interest to note that in thermal equilibrium, i.e. with no external voltage applied, there is a region in the semiconductor close to the junction which is depleted of mobile carriers. We call this the depletion region. The potential across the semiconductor equals the built-in potential

**Forward and reverse bias**

Operation of a metal-semiconductor junction under forward and reverse bias is illustrated with Figure 4. As a positive bias is applied to the metal (Figure 4 (a)), the Fermi energy of the metal is lowered with respectto the Fermi energy in the semiconductor. This results in a smaller potential drop across thesemiconductor.

The balance between diffusion and drift is disturbed and more electrons will diffuse towards the metal than the number drifting into the semiconductor. This leads to a positive current through the junction at a voltage comparable to the built-in potential.

**Figure 4 :** Energy band diagram of a metal-semiconductor junction under (a) forward and (b) reverse bias

As a negative voltage is applied (Figure 4 (b)), the Fermi energy of the metal is raised with respect to the Fermi energy in the semiconductor. The potential across the semiconductor now increases, yielding a larger depletion region and a larger electric field at the interface. The barrier, which restricts the electrons to the metal, is unchanged so that the flow of electrons is limited by that barrier independent of the applied voltage. The metal-semiconductor junction with positive barrier height has therefore a pronounced rectifying behavior. A large current exists under forward bias, while almost no current exists under reverse bias.

**Characteristics of Schottky Diode:**

Due to minority carrier free region, schottky diode cannot store the charge.Hence due to lack of charge storage,it can switch off very fast than a conventional diode.it can be easily switched off for the frequencies above 300MHz.The barrier at the junction for a schottky diode is less than that of normal p-n diode in both forward and reverse bias region.The barrier potential and breakdown voltage in forward bias and reverse bias region respectively are also less than p-n junction diode.The barrier potential is 0.25V as compared to

0.7V for normal diode.

**Applications:**

Due to fast switching characteristics this diode is very useful for high frequency applications such as digital computer,high speed TTl,radar systems,mixers,detectors in communication equipments and analog to digital converters.

# PRINCIPLE OF OPERATION OFSCR

A **silicon-controlled rectifier** (or **semiconductor-controlled rectifier**) is a four-layer solid state device that controls current. The name "silicon controlled rectifier" or **SCR** is General Electric's trade name for a type of thyristor. The SCR was developed by a team of power engineers led by Gordon Hall and commercialized by Frank W. "Bill" Gutzwiller in 1957.symbol of SCR is given below:

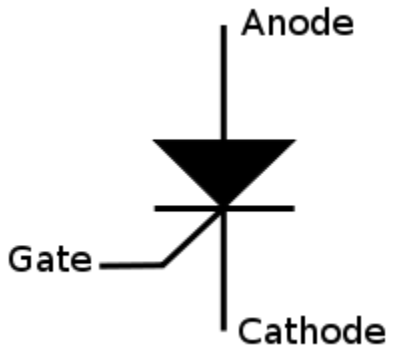



**Fig : symbol of SCR**

**Construction of SCR**

An SCR consists of four layers of alternating P and N type semiconductor materials. Silicon is used as the intrinsic semiconductor, to which the proper dopants are added. The junctions are either diffused or alloyed. The planar construction is used for low power SCRs (and all the junctions are diffused). The mesa type construction is used for high power SCRs. In this case, junction J2 is obtained by the diffusion method and then the outer two layers are alloyed to it, since the PNPN pellet is required to handle large currents. It is properly braced with tungsten or molybdenum plates to provide greater mechanical strength. One of these plates is hard soldered to a copper stud, which is threaded for attachment of heat sink. The doping of PNPN will depend ontheapplicationofSCR,sinceitscharacteristicsaresimilartothoseofthethyratron.Today,

the term thyristor applies to the larger family of multilayer devices that exhibit bistable state-change behaviour, that is, switching either ON or OFF.

The operation of a SCR and other thyristors can be understood in terms of a pair of tightly coupled bipolar junction transistors, arranged to cause the self-latching action.The following figures are construction of SCR,its two transistor model and symbol respectively

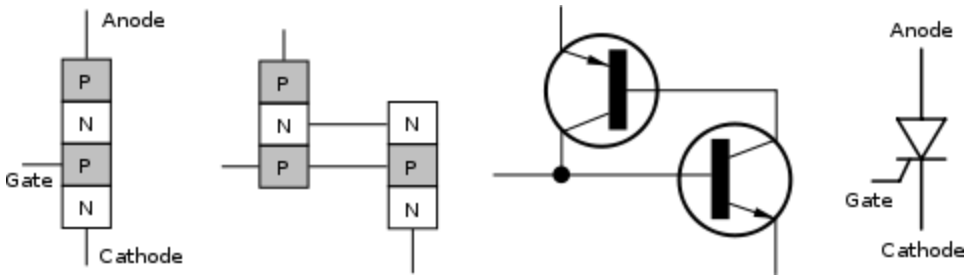
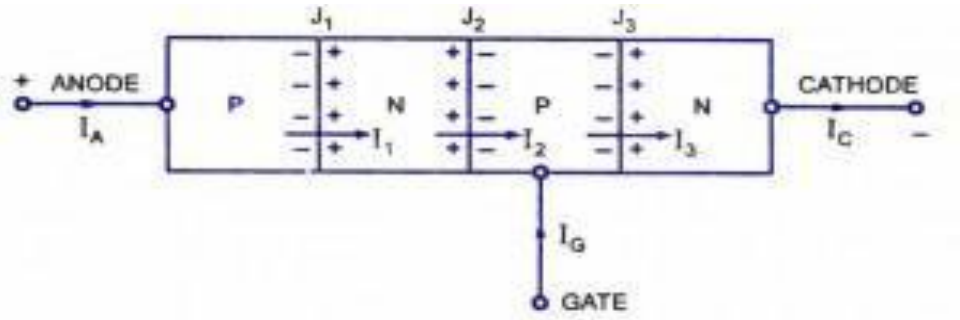



Fig: Construction,Two transistor model of SCR and symbol of SCR

## . SCR Working Principle




*Diagrammatic Representation Showing Current Flow and Voltage Bias in An SCR*

The **SCR** is a four-layer, three-junction and a three-terminal device and is shown in fig.a. The end P-region is the anode, the end N-region is the cathode and the inner P-region is the gate. The anode to cathode is connected in series with the load circuit. Essentially the device is a switch. Ideally it remains off (voltage blocking state), or appears to have an infinite impedance until both the anode and gate terminals have suitable positive voltages with respect to the cathode terminal. The thyristor then switches on and current flows and continues to conduct without further gate signals. Ideally the thyristor has zero impedance in conduction state. For switching off or reverting to the blocking state, there must be no gate signal and the anode current must be reduced to zero. Current can flow only in onedirection.

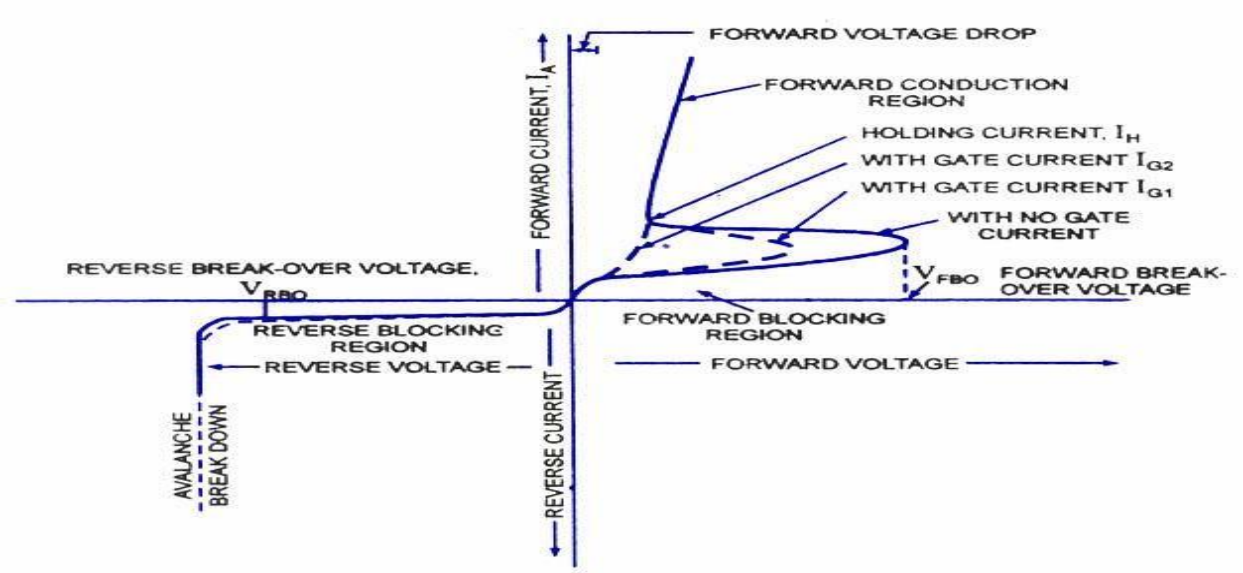
In absence of external bias voltages, the majority carrier in each layer diffuses until there is a built-in voltage that retards further diffusion. Some majority carriers have enough energy to cross the barrier caused by the retarding electric field at each junction. These carriers then become minority carriers and can recombine with majority carriers. Minority carriers in each layer can be accelerated across each junction by the fixed field, but because of absence of external circuit in this case the sum of majority and minority carrier currents must be zero.

A voltage bias, as shown in figure, and an external circuit to carry current allow internal currents which include the following terms:

The current $I_x$ is due to

- Majority carriers (holes) crossing junction$J_1$
- Minority carriers crossing junction$J_1$
- Holes injected at junction $J_2$ diffusing through the N-region and crossing junction $J_1$and
- Minority carriers from junction $J_2$ diffusing through the N-region and crossing junction $J_1$.

## V I characteristics of SCR:




*V-I Characteristics of SCR*

As already mentioned, the **SCR** is a four-layer device with three terminals, namely, the anode, the cathode and the gate. When the anode is made positive with respect to the cathode, junctions $J_1$ and $J_3$ are forward biased and junction $J_2$is reverse-biased and only the leakage current will flow through the device. The SCR is then said to be in the forward blocking state or in the forwardmodeoroffstate.Butwhenthecathodeismadepositivewithrespecttotheanode,

junctions $J_1$ and $J_3$ are reverse-biased, a small reverse leakage current will flow through the SCR and the SGR is said to be in the reverse blocking state or in reverse mode.

When the anode is positive with respect to cathode i.e. when the SCR is in forward mode, the SCR does not conduct unless the forward voltage exceeds certain value, called the forward breakover voltage, $V_{FB0}$. In non-conducting state, the current through the SCR is the leakage current which is very small and is negligible. If a positive gate current is supplied, the SCR can become conducting at a voltage much lesser than forward break-over voltage. The larger the gate current, lower the break-over voltage. With sufficiently large gate current, the SCR behaves identical to PN rectifier. Once the SCR is switched on, the forward voltage drop across it is suddenly reduced to very small value, say about 1 volt. In the conducting or on-state, the current through the SCR is limited by the external impedance.

When the anode is negative with respect to cathode, that is when the SCR is in reverse mode or in blocking state no current flows through the SCR except very small leakage current of the order of few micro-amperes. But if the reverse voltage is increased beyond a certain value, called the reverse break-over voltage, $V_{RB0}$avalanche break down takes place. Forward break-over voltage $V_{FB0}$is usually higher than reverse breakovervoltage,$V_{RBO}$.

From the foregoing discussion, it can be seen that the SCR has two stable and reversible operating states. The change over from off-state to on-state, called turn-on, can be achieved by increasing the forward voltage beyond $V_{FB0}$. A more convenient and useful method of turn-on the device employs the gate drive. If the forward voltage is less than the forward break-over voltage, $V_{FB0}$, it can be turned-on by applying a positive voltage between the gate and the cathode. This method is called the gate control. Another very important feature of the gate is that once the SCR is triggered to on-state the gate loses itscontrol.

***The switching action of gate takes place only when***

(i) SCR is forward biased i.e. anode is positive with respect to cathode,and

(ii) Suitable positive voltage is applied between the gate and thecathode.

Once the SCR has been switched on, it has no control on the amount of current flowing through it. The current through the SCR is entirely controlled by the external impedance connected in the circuit and the applied voltage. There is, however, a very small, about 1 V, potential drop across the SCR. The forward current through the SCR can be reduced by reducing the applied voltage or by increasing the circuit impedance. There is, however, a minimum forward current that must be maintained to keep the SCR in conducting state. This is called the holding current rating of SCR. If the current through the SCR is reduced below the level of holding current, the device returns to off-state or blockingstate.

The SCR can be switched off by reducing the forward current below the level of holding current which may be done either by reducing the applied voltage or by increasing the circuitimpedance.

**Note** : The gate can only trigger or switch-on the SCR, it cannot switch off.

Alternatively the SCR can be switched off by applying negative voltage to the anode (reverse mode), the SCR naturally will be switched off.

Here one point is worth mentioning, the SCR takes certain time to switch off. The time, called the turn-off time, must be allowed before forward voltage may be applied again otherwise the device will switch-on with forward voltage without any gate pulse. The turn-off time is about 15 micro-seconds, which is immaterial when dealing with power frequency, but this becomes important in the inverter circuits, which are to operate at highfrequency.

## Merits of SCR

1. Very small amount of gate drive isrequired.
2. SCRs with high voltage and current ratings areavailable.
3. On state losses of SCR areless.

## Demerits of SCR

1. Gate has no control,once SCR is turned on.
2. External circuits are required for turning it off.
3. Operationg frequencies are low.
4. Additional protection circuits are required.

## Application of SCRs

SCRs are mainly used in devices where the control of high power, possibly coupled with high voltage, is demanded. Their operation makes them suitable for use in medium to high-voltage AC power control applications, such as lamp dimming, regulators and motorcontrol.

SCRs and similar devices are used for rectification of high power AC in high-voltage directcurrent power transmission

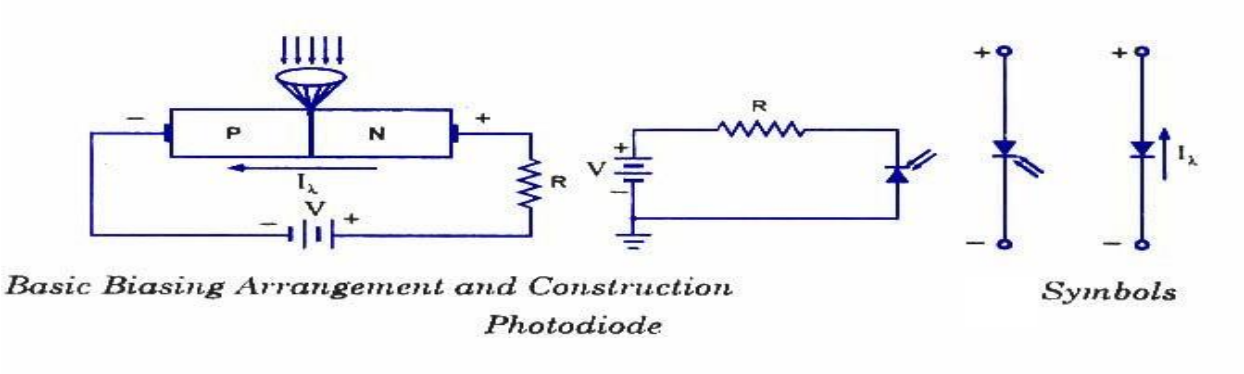
# PHOTODIODE:

The photo diode is a semiconductor p-n junction device whose region of operation is limited to the reverse biased region.The figure below shows the symbol of photodiode


Fig:Symbol for photodiode.

## Principle of operation:

A photodiode is a type of photo detector capable of converting light into either current or voltage, depending upon the mode of operation. The common, traditional solar cell used to generate electric solar power is a large area photodiode. A photodiode is designed to operate in reverse bias. The deletion region width is large.Under normal conditions it carries small reverse current due to minority charge carriers.When light is incident through glass window on the p-n junction,photons in the light bombard the p-n junction and some energy s imparted to the valence electrons.So valence electrons break covalent bonds and become free electrons.Thus more electron-hole pairs are generated.Thus total number of minority charge carriers increases and hence reverse current increases.This is the basic principle of operation of photodiode.




## Characteristics of photodiode:

When the P-N junction is reverse-biased, a reverse saturation current flows due to thermally generated holes and electrons being swept across the junction as the minority carriers. With the increase in temperature of the junction more and more hole-electron pairs are created and so the reverse saturation current $I_0$ increases. The same effect can be had by illuminating the junction. When light energy bombards a P-N junction, it dislodges valence electrons. The more light striking the junction the larger the reverse current in a diode. It is due to generation of more and more charge carriers with the increase in level of illumination. This is clearly shown in ‘ figure

for different intensity levels. The dark current is the current that exists when no light is incident. It is to be noted here that current becomes zero only with a positive applied bias equals to $V_Q$. The almost equal spacing between the curves for the same increment in luminous flux reveals that the reverse saturation current $I_0$increases linearly with the luminous flux as shown in figure. Increase in reverse voltage does not increase the reverse current significantly, because all available charge carriers are already being swept across the junction. For reducing the reverse saturation current $I_0$ to zero, it is necessary to forward bias the junction by an amount equal to barrier potential. Thus the photodiode can be used as a photoconductivedevice.

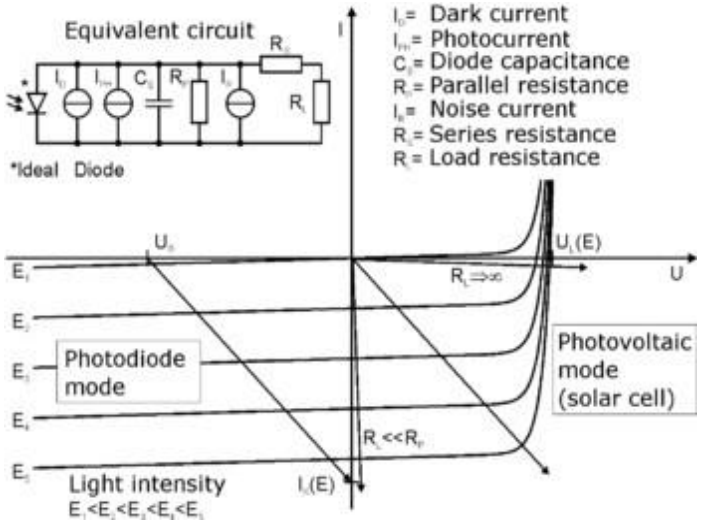



Fig: characteristics of photodiode

On removal of reverse bias applied across the photodiode, minority charge carriers continue to be swept across the junction while the diode is illuminated. This has the effect of increasing the concentration of holes in the P-side and that of electrons in the N-side But the barrier potential is negative on the P-side and positive on the N-side, and was created by holes flowing from P to N-side and electrons from N to P-side during fabrication of junction. Thus the flow of minority carriers tends to reduce the barrier potential.

When an external circuit is connected across the diode terminals, the minority carrier; return to the original side via the external circuit. The electrons which crossed the junction from P to N-side now flow out through the N-terminal and into the P-terminal This means that the device is behaving as a voltage cell with the N-side being the negative terminal and the P-side the positive terminal. Thus, the photodiode is & photovoltaic device as well as photoconductive device.

## Advantages:

The advantages of photodiode are:

1. It can be used as variable resistancedevice.

2.Highly sensitive to the light.
3.The speed of operation is veryhigh.

## Disadvantages:

1.Temperature dependent dark current.
2.poor temperature stability.
3.Current needs amplification for driving other circuits.

## Applications:

1.Alarm system.
2.counting system.

## Problems:

1.In a particular application single phase half wave rectifier using SCR is used.The average load voltage is 80V.If supply voltage is 230V,50Hz a.c.find the firing angle of the SCR.

2.In a particular application single phase half wave rectifier using SCR s used.The supply voltage is 325sin $\omega$t where $\omega$=100$\pi$rad/sec.Find the time for which SCR remains OFF ifforward breakover voltage is125V.

# . RECTIFIERS & FILTERS:

## INTRODUCTION

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c.voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulatorcircuits.

These elements constitute d.c. regulated power supply shown in the fig 1 below.

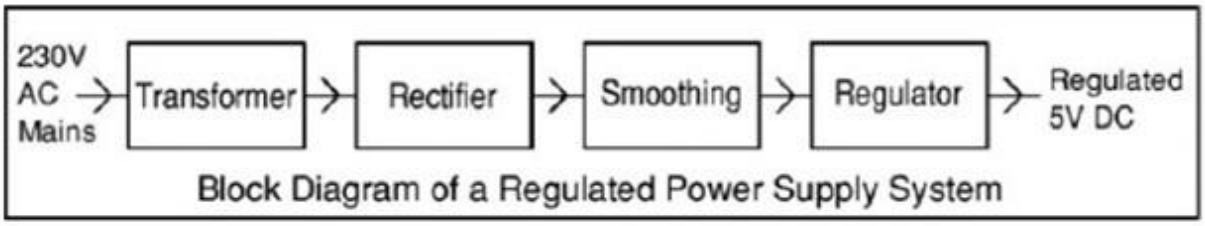



fig1 . Block diagram of Regulated D.C. Power Supply

- ✓ Transformer – steps down 230V AC mains to low voltageAC.
- ✓ Rectifier – converts AC to DC, but the DC output isvarying.
- ✓ Smoothing – smooth the DC from varying greatly to a smallripple.
- ✓ Regulator – eliminates ripple by setting DC output to a fixedvoltage.

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load. An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage Vo which is independent of the load current and variations in the input voltage ad temperature. If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

## RECTIFIER:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional Waveform, with a non-zero average component. A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Unidirectional).

**Characteristics of a Rectifier Circuit:**

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component.

A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c..Load currents: They are two types of output current. They are average or d.c. current and RMS currents.

Average or DC current: The average current of a periodic function is defined as the area of one cycle of the curve divided by the base.

It is expressed mathematically as

*i)* Average value/dc value/mean value= $\frac{Area\ over\ oneperiod}{Total\ time\ period}$

$$V_{dc} = \frac{1}{T}\int_0^T V d\,(wt)$$

ii) Effective (or) R.M.Scurrent:

The effective (or) R.M.S. current squared ofa periodic function of time is given by the area of one cycle of the curve, which represents the square of the function divided by the base.

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d\,(wt)}$$

iii) Peakfactor:

It is the ratio of peak value to Rms value

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

iv) Formfactor:

It is the ratio of Rms value to average value

$$\text{Formfactor} = \frac{Rmsvalue}{averagevalue}$$

v) RippleFactor(Γ):ItisdefinedasrationofR.M.S.valueofa.c.componenttothed.c. component in the output is known as "RippleFactor".

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

vi) Efficiency ($\eta$):

It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

$$\eta = \frac{o/p\ power}{i/p\ power}$$

vii) Peak Inverse Voltage(PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction.

viii) Transformer Utilization Factor(UTF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the Transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{p_{ac(rated)}}$$

ix) %Regulation:

The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\%\ \mathrm{Re}\ gulation = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$

For an ideal power supply, % Regulation is zero.

# CLASSIFICATION OFRECTIFIERS:

Using one or more diodes in the circuit, following rectifier circuits can be designed.

1) Half - WaveRectifier
2) Full – WaveRectifier
3) BridgeRectifier

## HALF-WAVERECTIFIER:

A Half – wave rectifier as shown in **fig 2** is one, which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.

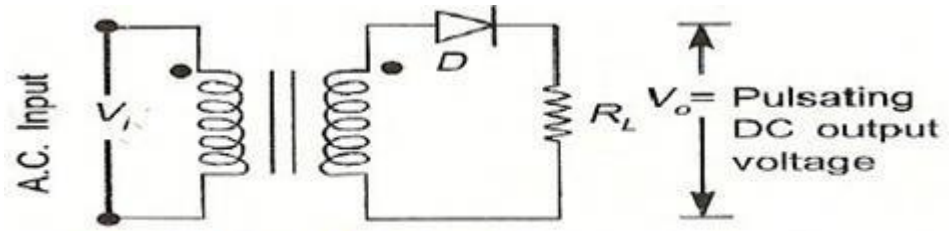



**fig 2** Basic structure of Half-Wave Rectifier

The a.c. voltage is applied to the rectifier circuit using step-down transformer-rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer

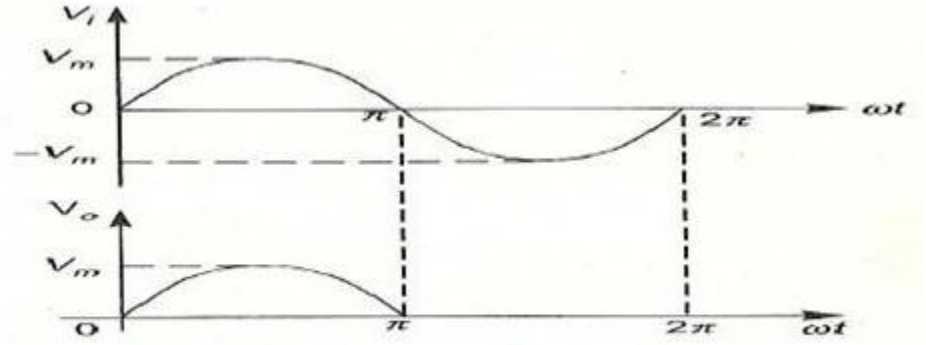



**fig 3** Input and output waveforms of a Half wave rectifier

$V=V_m \sin(wt)$

The input to the rectifier circuit, Where $V_m$ is the peak value of secondary a.c. voltage.

**Operation:**

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across $R_L$. The waveform of the diode current (or) load current is shown in **fig 3**.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not Conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half- cycle no power is delivered to the load.

**Analysis:**

In the analysis of a HWR, the following parameters are to be analyzed.

1. DC outputcurrent
2. DC Outputvoltage
3. R.M.S.Current
4. R.M.S.voltage
5. Rectifier Efficiency ($\eta$ )
6. Ripple factor ($\gamma$)
7. PeakFactor
8. %Regulation
9. Transformer Utilization Factor(TUF)

10. formfactor
11. o/p frequency

Let a sinusoidal voltage $V_i$ be applied to the input of the rectifier.

Then $V=V_m \sin(wt)$ Where $V_m$ is the maximum value of the secondary voltage. Let the diode be idealizedtopiece-wiselinearapproximationwithresistance$R_f$intheforwarddirectioni.e.,intheON state and $R_r$ (=∞) in the reverse direction i.e., in the OFF state. Now the current 'i' in the diode (or) in the load resistance $R_L$ isgivenby $V=V_m\sin(wt)$

## i) AVERAGE VOLTAGE

$$V_{dc} = \frac{1}{T}\int_0^T Vd(wt)$$

$$V_{dc} = \frac{1}{T}\int_0^{2\Pi} V(\alpha)d\alpha$$

$$V_{dc} = \frac{1}{2\Pi}\int_{\Pi}^{2\Pi} V(\alpha)d\alpha$$

$$V_{dc} = \frac{1}{2\Pi}\int_0 V_m \sin(wt)$$

$$V_{dc} = \frac{V_m}{\Pi}$$

**ii).AVERAGE CURRENT:**

$$I_{dc} = \frac{I_m}{\Pi}$$

**iii) RMS VOLTAGE:**

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_{0}^{2\Pi}(V_m sim(wt))^2\, d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

**IV) RMSCURRENT**

$$\boxed{I_{rms} = \frac{I_m}{\Pi}}$$

**V) PEAKFACTOR**

$$\textbf{Peak factor} = \frac{peakvalue}{rmsvalue}$$

$$\textbf{Peak Factor} = \frac{V_m}{(V_m/2)}$$

**Peak Factor =2**

**vi) FORMFACTOR**

$$\text{Form factor} = \frac{Rmsvalue}{averagevalue}$$

$$\text{Form factor} = \frac{(V_m/2)}{V_m/\Pi}$$

Form Factor =1.57

**vii) Ripple Factor:**

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\Gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{ac}}$$

$$\Gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$\Gamma = 1.21$$

**viii) Efficiency ($\eta$):**

$$\eta = \frac{o/ppower}{i/ppower} * 100$$

$$\eta = \frac{p_{ac}}{P_{dc}} * 100$$

$$\eta = 40.8$$

**ix) Transformer Utilization Factor(TUF):**

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. Therefore, transformer utilization factor is defined as

$$TUF = \frac{p_{dc}}{P_{ac(rated)}}$$

$$TUF = 0.286.$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized. If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver

1000 X 0.287 = 287 watts to resistance load.

**x) Peak Inverse Voltage(PIV):**

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half-wave rectifier, PIV is $V_m$.

### DISADVANTAGES OF HALF-WAVE RECTIFIER:

1. The ripple factor ishigh.
2. The efficiency islow.
3. The Transformer Utilization factor islow.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

## FULL WAVERECTIFIER:

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load RL with the help of a center-tap transformer. A center-tap transformer is the one, which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the **fig 4** below

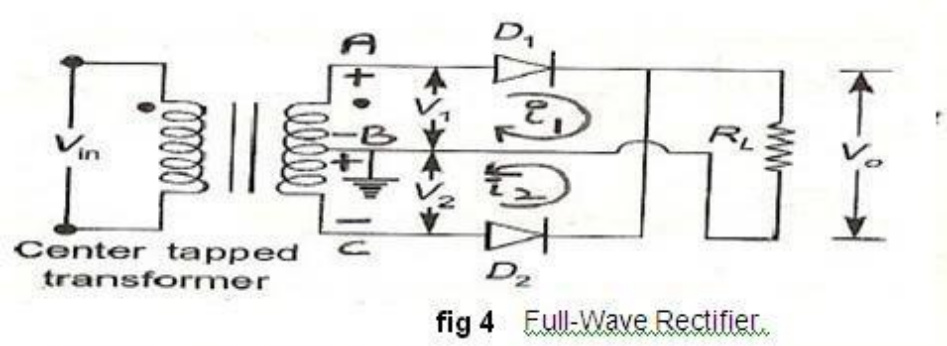



**fig 4** Full-Wave Rectifier.

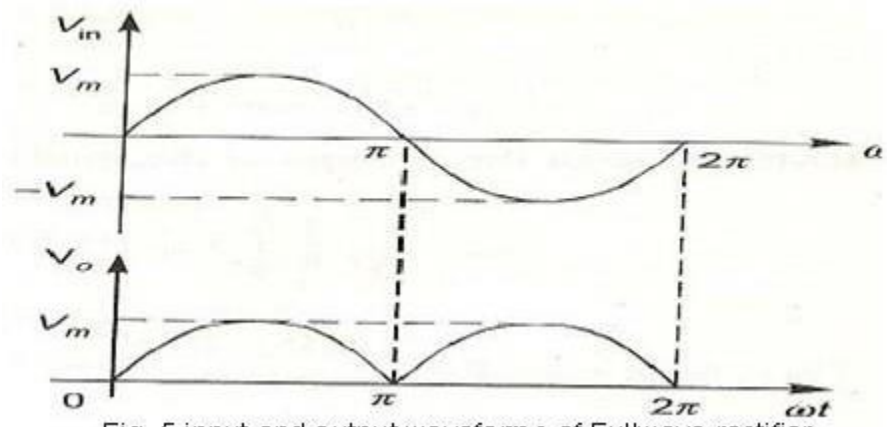


Fig. 5 input and output waveforms of Fullwave rectifier

Fig. 5 shows the input and output wave forms of the ckt.

During positive half of the input signal, anode of diode D1 becomes positive and at the same time the anode of diode D2 becomes negative. Hence D1 conducts and D2 does not conduct. The load current flows through D1 and the voltage drop across RL will be equal to the input voltage.

During the negative half cycle of the input, the anode of D1 becomes negative and the anode of D2 becomes positive. Hence, D1 does not conduct and D2 conducts. The load current flows through D2 and the voltage drop across RL will be equal to the input voltage. It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

**i) AVERAGEVOLTAGE**

$$V_{dc} = I_{dc}.R_L = \frac{2I_m}{\pi}.R_L \quad \text{We know } I_m = \frac{V_m}{R_S + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2.V_m.R_L}{\pi(R_S + R_f + R_L}$$

$$If\,(R_s + R_f) << R_L$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637V_m.$$

**ii) AVERAGECURRENT**

$$\frac{1}{2\pi}\int_0^{2\pi} id\theta = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin\theta d\theta$$

$$I_{dc} = \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\theta d\theta - \int_{\pi}^{2\pi} \sin\theta d\theta\right]$$

$$= \frac{I_m}{2\pi}[(-2)(-2)]$$

$$= \frac{I_m}{2\pi}.4 = \frac{2I_m}{\pi} = 0.637\, I_m .$$

$$\boxed{I_{dc} = 0.637 I_m.}$$

$$\therefore I_{DC}\ FWR = 2\ I_{DC}\ HWR.$$

**iii) RMSVOLTAGE:**

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d\,(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m sim(wt))\, d\,(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

**IV) RMSCURRENT**

$$\boxed{I_{rms} = \frac{2I_m}{\Pi}}$$

**V) PEAKFACTOR**

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m/2)}$$

Peak Factor =2

**vi) FORMFACTOR**

$$\text{Form factor} = \frac{Rms\ value}{averagevalue}$$

$$\text{Form factor} = \frac{(V_m/\sqrt{2})}{2V_m/\Pi}$$

Form Factor =1.11

**vii) Ripple Factor:**

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore \gamma_{FWR} = \sqrt{\left(\frac{I_m}{\sqrt{2}} / \frac{2I_m}{\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{3.1416}{2\times 1.414}\right)^2 - 1} = 0.483$$

**viii) Efficiency ($\eta$):**

$$\eta = \frac{o/ppower}{i/ppower} * 100$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

For FWR, $p_{dc} = I_{dc}^2 . R_L = \left(\frac{2}{\pi} . I_m\right)^2 . R_L$

$P_{ac} = I^2_{rms} (R_f + R_S + R_L)$

$$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_S + R_L)$$

$$\eta = \frac{\frac{I^2_m 4}{\pi^2} . R_L}{\frac{I^2 m^2}{2} . (R_f + R_s + R_L)}$$

$$If\ (R_f + R_S) << R_L$$

$$\eta = \frac{4}{\pi^2} . \frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

**ix) Transformer Utilization Factor(TUF):**

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

a) TUF (Secondary) = $\frac{P_{dc}\ delivered\ to\ load}{AC\ power\ rating\ of\ transformer\ secondary}$

b) Since both the windings are used $TUF_{FWR} = 2\ TUF_{HWR}$
= $2 \times 0.287 = 0.574$

c) TUF primary = Rated efficiency = $\frac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$

d) Average = $\frac{0.812 + 0.574}{2} = 0.693$

**x) Peak Inverse Voltage(PIV):**

It is defined as the maximum reverse voltage that a diode can withstand without destroying the

junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half-wave rectifier, PIV is 2Vm

### xi) %Regulation

$$\text{Voltage regulation} = \frac{I_{dc}(R_s + R_f)}{\frac{2V_m}{\pi} - I_{DC}(R_f + R_s)}$$

.

**Advantages**

1) Ripple factor = 0.482 (against 1.21 forHWR)
2) Rectification efficiency is 0.812 (against 0.405 forHWR)
3) Better TUF (secondary) is 0.574 (0.287 forHWR)
4) No core saturation problem

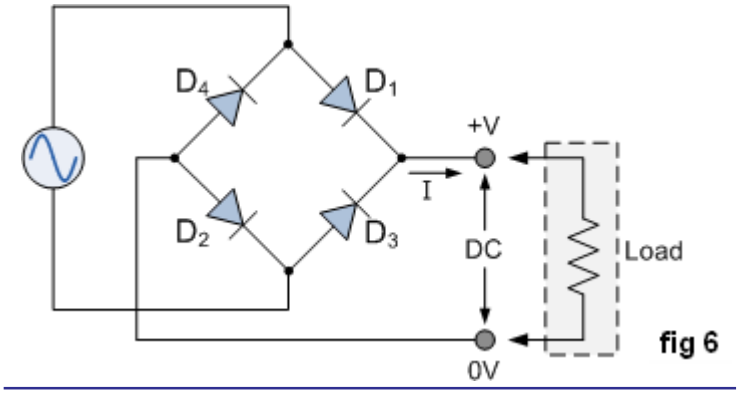
Disadvantages:

1) Requires center tappedtransformer.

## BRIDGERECTIFIER.

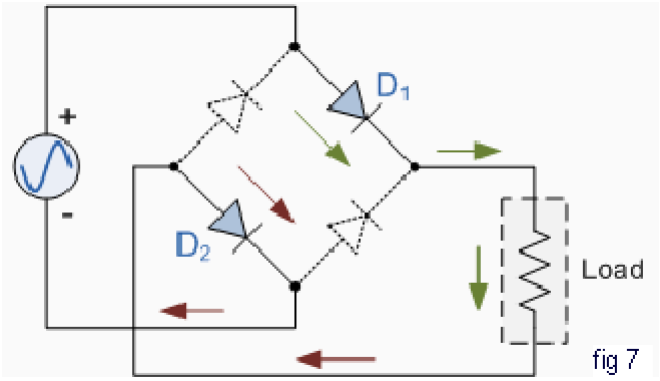
Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the **Full Wave Bridge Rectifier**. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shownbelow.

**The Diode Bridge Rectifier**




The four diodes labelled $D_1$ to $D_4$ are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below (fig 7).

## The Positive Half-cycle




## The Negative Half-cycle

During the negative half cycle of the supply, diodes D3 and D4 conduct in series (fig 8), but diodes D1 and D2 switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.

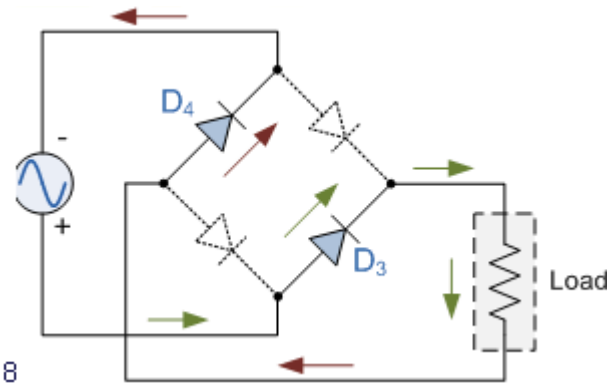


fig 8

As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC voltage across the load is $0.637V_{max}$. However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is two voltage drops ( 2 x 0.7 = 1.4V ) less than the input $V_{MAX}$ amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply)

Therefore, the following expressions are same as that of full wave rectifier.

a) Average current $I_{dc} = \frac{2I_m}{\pi}$

b) RMS current $I_{rms} = \frac{I_m}{\sqrt{2}}$

c) DC output voltage (no.load) $V_{DC}$ $\frac{2V_m}{\pi}$

d) Ripple factor $\gamma = 0.482$

e) Rectification efficiency = $\eta = 0.812$

f) DC output voltage full load.

= $V_{DCFL} = \frac{2V_m}{\pi} - I_{dc}(R_S + 2R_f)$; i.e., less by one diode loss.

TUF of both primary & secondary are 0.812 therefore TUF overall is 0.812 (better than FWR with 0.693)

**Comparison:**

| Sl. No. | Parameter | HWR | FWR | BR |
|---|---|---|---|---|
| 1 | No. of diodes | 1 | 2 | 4 |
| 2 | PIV of diodes | $V_m$ | 2 $V_m$ | $V_m$ |
| 3 | Secondary voltage (rms) | V | V-0-V | V |
| 4 | DC output voltage at no load | $\frac{V_m}{\pi}$ =0.318 $V_m$ | $\frac{2V_m}{\pi}$ =0.636 $V_m$ | $\frac{2V_m}{\pi}$ =0.636 $V_m$ |
| 5 | Ripple factor $\gamma$ | 1.21 | 0.482 | 0.482 |
| 6 | Ripple frequency | f | 2f | 2f |
| 7 | Rectification efficiency $\eta$ | 0.406 | 0.812 | 0.812 |
| 8 | TUF | 0.287 | 0.693 | 0.812 |

# FILTERS

The output of a rectifier contains dc component as well as ac component. Filters are used to minimize the undesirable ac i.e., ripple leaving only the dc component to appear at the output.

Some important filters are:

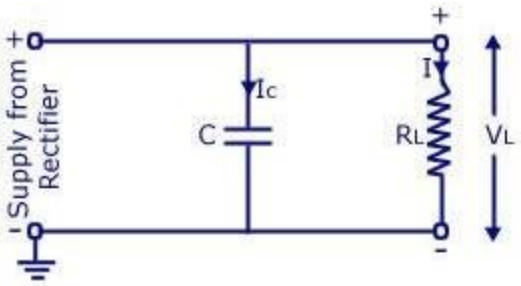
1. Inductorfilter
2. Capacitorfilter
3. LC or L sectionfilter
4. CLC or Π-typefilter

## CAPACITOR FILTER

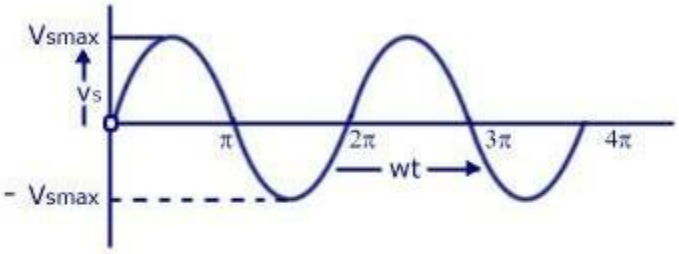
This is the most simple form of the **filter circuit**and in this arrangement a high value capacitor C is placed directly across the output terminals, as shown in figure. During the conduction period it gets charged and stores up energy to it during non-conduction period. Through this process, the time duration during which Ft is to be noted here that the capacitor C gets charged to the peak because there is no resistance (except the negligible forward resistance of diode) in the charging path. But the discharging time is quite large (roughly 100 times more than the charging time depending upon the value of RL) because it discharges through load resistanceRL.

The function of the capacitor filter may be viewed in terms of impedances. The large value capacitor C offers a low impedance shunt path to the ac components or ripples but offers high impedance to the dc component. Thus ripples get bypassed through capacitor C and only dc component flows through the load resistance RL

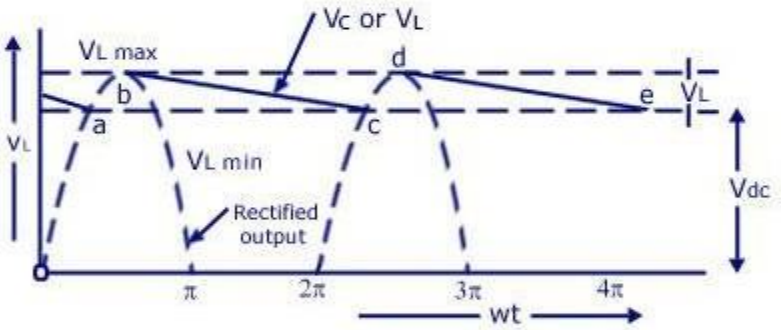
***Capacitor filter is very popular because of its low cost, small size, light weight and good characteristics.***



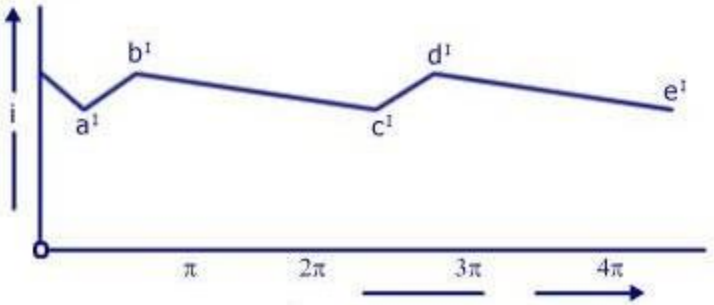

Circuit Diagram




Input voltage Waveform to Rectifier



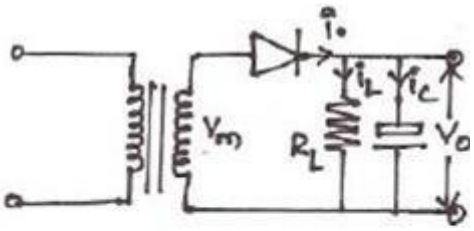

Rectified and filtered Output Voltage Waveform




Load Current Waveform

Half-wave Rectifier With Shunt Capacitor Filter

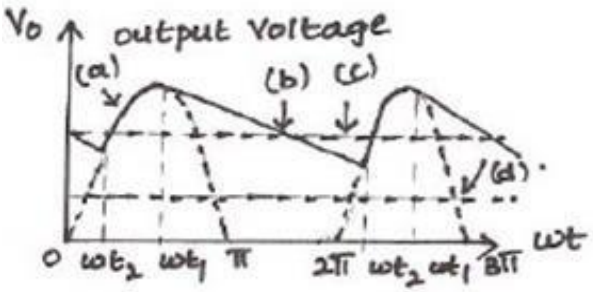
CAPACITOR FILTER WITH HWR




Cut In angle – $wt_2$

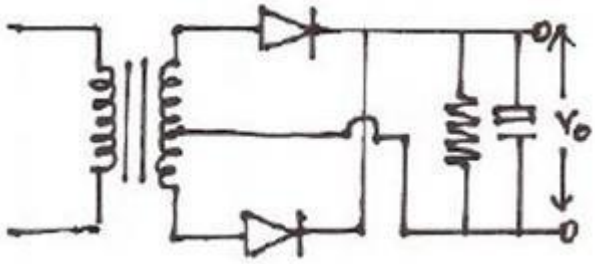
Cut out angle = $Wt_1$

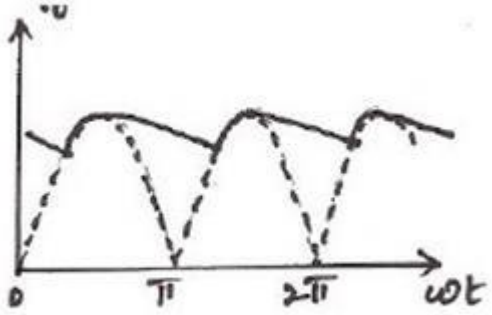
$Wt_1 = \pi - \tan^{-1} WCR_L$




(a) Capacitor charging through diode ($Wt_2 - Wt_1$)
(b) Capacitor discharging through $R_L$ ($Wt_1$ to $Wt_2$)
(c) Average (DC) voltage with fitter
(d) Average (DC) voltage without fitter.

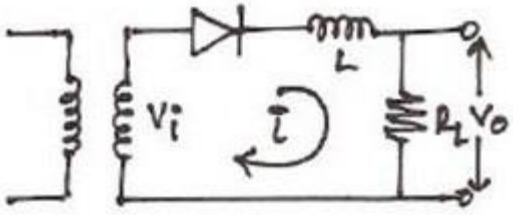
CAPACITOR FILTER WITH FWR

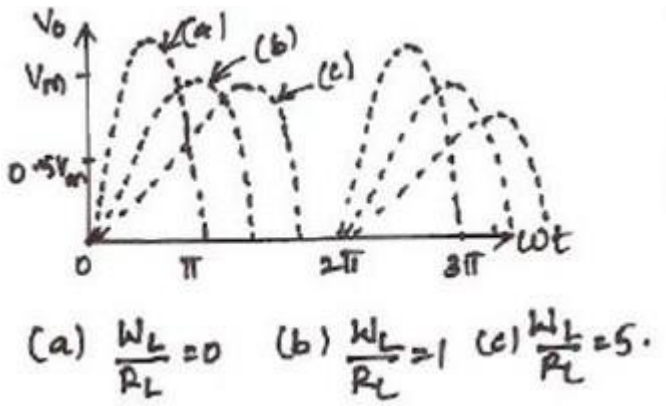



$$\text{Ripple factor } r = \frac{1}{4\sqrt{3}fCR_L}$$

Ripple freq $_{FWR}$ = 2 ripple freq $_{HWR}$.



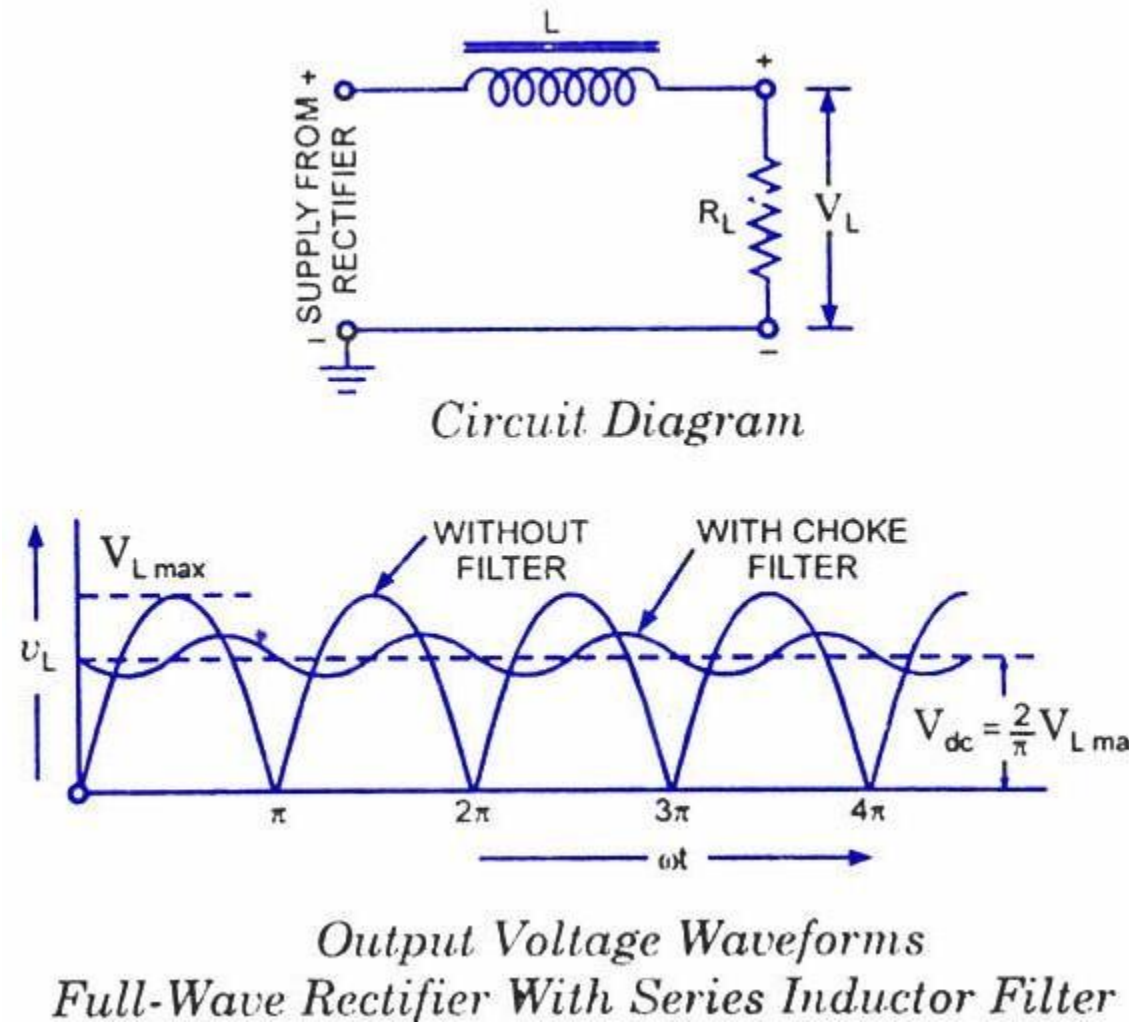



**The worthnoting points about shunt capacitor filter are:**

1. For a fixed-value filter capacitance larger the load resistance RL larger will be the discharge time constant CRL and therefore, lower the ripples and more the output voltage. On the other hand lower the load resistance (or more the load current), lower will be the outputvoltage.

2. Similarly smaller the filter capacitor, the less charge it can hold and more it will discharge. Thus the peak-to-peak value of the ripple will increase, and the average dc level will decrease. Larger the filter capacitor, the more charge it can hold and the less it will discharge. Hence the peak-to-peak value of the ripple will be less, and the average dc level will increase. But, the maximum value of the capacitance that can be employed is limited by another factor. The larger the capacitance value, the greater is the current required to charge the capacitor to a given voltage. The maximum current that can be handled by a diode is limited by the figure quoted by the manufacturer. Thus the maximum value of the capacitance, that can be used in the shunt filter capacitor islimited.

**SERIES INDUCTORFILTER.**




*Circuit Diagram*

*Output Voltage Waveforms*

*Full-Wave Rectifier With Series Inductor Filter*

In this arrangement a high value inductor or choke L is connected in series with the rectifier element and the load, as illustrated in figure. The filtering action of an inductor filter depends upon its property of opposing any change in the current flowing through it. When the output current of the rectifier increases above a certain value, energy is stored in it in the form of magnetic field and this energy is given up when the output current falls below the average value. Thus by placing a choke coil in series with the rectifier output and load, any sudden change in current that might have occurred in the circuit without an inductor is smoothed out by the presence of the inductor L.

The function of the inductor filter may be viewed in terms of impedances. The choke offers high impedance to the ac components but offers almost zero resistance to the desired dc components. Thus ripples are removed to a large extent. Nature of the output voltage without filter and with choke filter is shown in figure.

For dc (zero frequency), the choke resistance $R_c$ in series with the load resistance $R_L$ forms a voltage divider and dc voltage across the load is given as

where $V_{dc}$ is dc voltage output from a full-wave rectifier. Usually choke coil resistance Rc, is much small than $R_L$ and, therefore, almost entire of the dc voltage is available across the load resistance $R_L$.

Since the reactance of inductor increases with the increase in frequency, better filtering of the higher harmonic components takes place, so effect of third and higher harmonic voltages can be neglected.

As obvious from equation , if choke coil resistance $R_c$is negligible in comparison to load resistance $R_L$, then the entire dc component of rectifier output is available across 2 $R_L$ and isequal to — $V_{Lmax}$. The ac voltage partly drops across $X_L$ and partly over$R_L$.

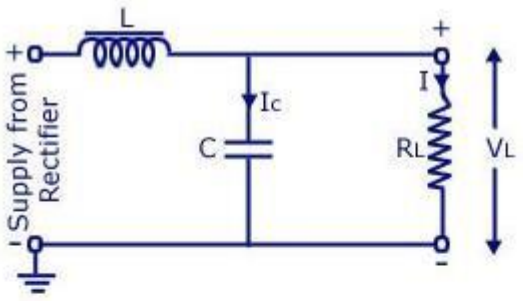
## L-SECTION FILTER:

A simple series inductor reduces both the peakand effective values of the output current and output voltage. On the other hand a simple **shunt capacitor filter**reduces the ripple voltage but increases the diode current. The diode may get damaged due to large current and at the same time it causes greater heating of supply transformer resulting in reducedefficiency.

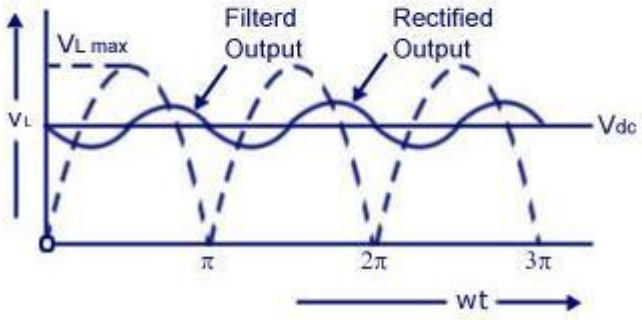
In an inductor filter, ripple factor increases with the increase in load resistance RL while in a capacitor filter it varies inversely with load resistance RL.

From economical point of view also, neither series inductor nor shunt capacitor type filters are suitable.

Practical **filter-circuits**are derived by combining the voltage stabilizing action of shunt capacitor with the current smoothing action of series choke coil. By using combination of inductor and capacitor ripple factor can be lowered, diode current can be restricted and simultaneously ripple factor can be made almost independent of load resistance (or load current). Two types of most commonly used combinations are choke-input or L-section filter-and capacitor-input or Pi-Filter.




Circuit Digram

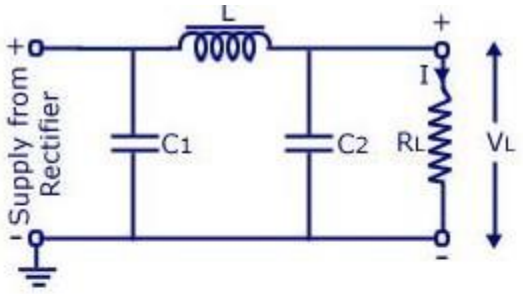



Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With Choke-Input Filter

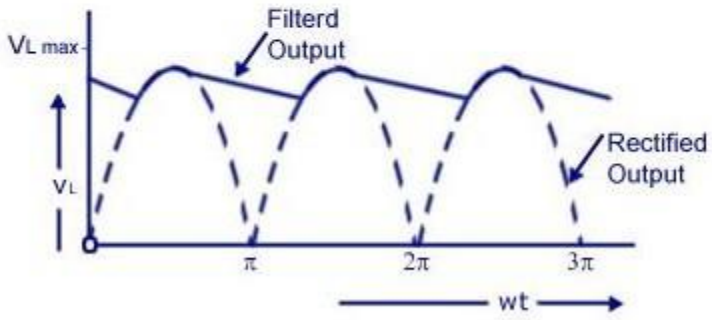
## Choke-input filter is explained below:

Choke-input filter consists of a choke L connected in series with the rectifier and a capacitor C connected across the load . This is also sometimes called the L-section filter because in this arrangement inductor and capacitor are connected, as an inverted L. ln figure only one filter section is shown. But several identical sections are often employed to improve the smoothing action. (The choke L on the input side of the filter readily allows dc to pass but opposes the flow of ac components because its dc resistance is negligibly small but ac impedance is large. Any fluctuation that remains in the current even after passing through the choke are largely by-passed around the load by the shunt capacitor because Xc is much smaller than RL. Ripples can be reduced effectively by making XL greater than Xc at ripple frequency. However, a small ripple still remains in the filtered output and this is considered negligible if it than l%. The rectified and filtered output voltage waveforms from a full-wave re with choke-input filter are shown in figure.

## **II-SECTION FILTER**:




Circuit Digram




Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With capacitor Input Filter

**Capacitor-Input or Pi-Filter.**

Such a filter consists of a shunt capacitor C1 at the input followed by an L-section filter formed by series inductor L and shunt capacitor $C_2$. This is also called the *n-filter* because the shape of the circuit diagram for this filter appears like Greek letter *n (pi)*. Since the rectifier feeds directly into the capacitor so it is also called *capacitor input filter.*

As the rectified output is fed directly into a capacitor C1. Such a filter can be used with a half-wave rectifier (series inductor and L-section filters cannot be used with half-wave rectifiers). Usually electrolytic capacitors are used even though their capacitances are large but they occupy minimum space. Usually both capacitors C1 and $C_2$ are enclosed in one metal container. The metal container serves as, the common ground for the two capacitors.

A capacitor-input or *pi*- filter is characterized by a high voltage output at low current drains. Such a filter is used, if, for a given transformer, higher voltage than that can be obtained from an L-section filter is required and if low ripple than that can be obtained from a shunt capacitor filter or L-section filter is desired. In this filter, the input capacitor C1 is selected to offer very low reactance to the ripple frequency. Hence major part of filtering is accomplished by theinput

capacitor *C1*. Most of the remaining ripple is removed by the L-section filter consisting of a choke L and capacitor $C_2$.)

The action of this filter can *best* be understood by considering the action of L-section filter, formed by L and $C_2$, upon the triangular output voltage wave from the input capacitor $C_1$ The charging and discharging action of input capacitor C1 has already been discussed. The output voltage is roughly the same as across input capacitor C1 less the dc voltage drop in inductor. The ripples contained in this output are reduced further by L-section filter. The output voltage of pi-filter falls off rapidly with the increase in load-current and, therefore, the voltage regulation with this filter is very poor.

**SALIENT FEATURES OF L-SECTION AND PI-FILTERS.**

1. In pi-filter the dc output voltage is much larger than that can be had from an L-section filter with the same inputvoltage.

2.In pi-filter ripples are less in comparison to those in shunt capacitor or L-section filter. So smaller valued choke is required in a pi-filter in comparison to that required in L-sectionfilter.

3.In pi-filter, the capacitor is to be charged to the peak value hence the rms current in supply transformer is larger as compared in case of L-sectionfilter.

4.Voltage regulation in case of pi-filter is very poor, as already mentioned. So n-filters are suitable for fixed loads whereas L-section filters can work satisfactorily with varying loads provided a minimum current ismaintained.

5.In case of a pi-filter PIV is larger than that in case of an L-sectionfilter.

**COMPARISON OF FILTERS**

1) A capacitor filter provides Vm volts at less load current. But regulation ispoor.

2) An Inductor filter gives high ripple voltage for low load currents. It is used for

high loadcurrents

3) L – Section filter gives a ripple factor independent of load current.Voltage

Regulation can be improved by use of bleeder resistance

4) Multiple L – Section filter or π filters give much less ripple than the single L –

SectionFilter.

# UNIT III

# TRANSISTORS

## INTRODUCTION

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogus to vacuum triode and is comparatively smaller in size. It is used i amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

## CONSTRUCTION OF BJT AND ITSSYMBOLS

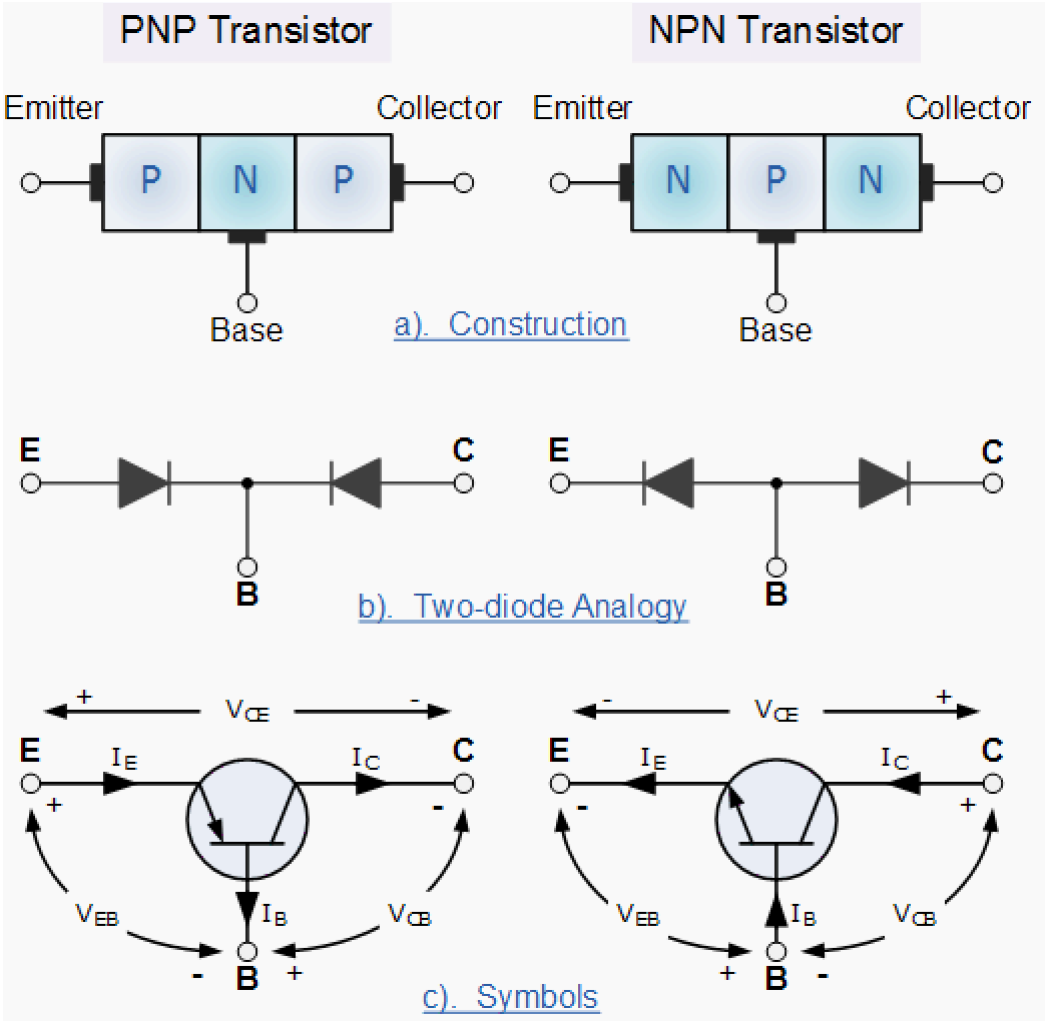
The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter ( E ), the Base ( B ) and the Collector ( C ) respectively. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they aremade.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- 1. Active Region - the transistor operates as an amplifier and Ic =β.Ib
- 2. Saturation - the transistor is "fully-ON" operating as a switch and Ic =I(saturation)
- 3. Cut-off - the transistor is "fully-OFF" operating as a switch and Ic =0

Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type(fig 1).

**Bipolar Transistor Construction**

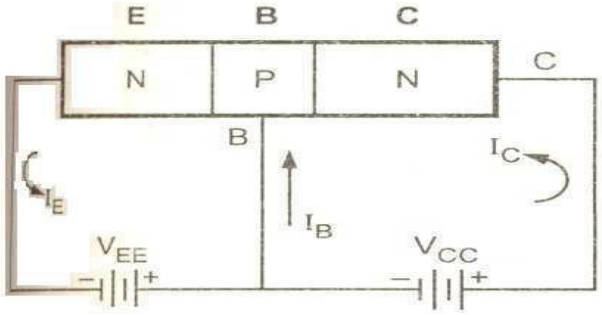



- **Fig:1**

The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol

**Transistor Operation**:

**Working of a n-p-n transistor:**



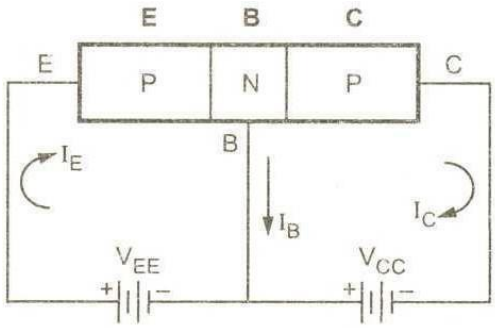

The n-p-n transistor with base to emitter junction forward biased and collector base junction reverse biased is as shown in figure.

As the base to emitter junction is forward biased the majority carriers emitted by the n-type emitter i.e., electrons have a tendency to flow towards the base which constitutes the emitter current $I_E$.

As the base is p-type there is chance of recombination of electrons emitted by the emitter with the holes in the p-type base. But as the base is very thin and lightly doped only few electrons emitted by the n-type emitter less than 5% combines with the holes in the p-type base, theRemaining more than 95% electrons emitted by the n-type emitter cross over into the collector region constitute the collectorcurrent.

**IE = IB + IC**

**Working of a p-n-p transistor:**




The p-n-p transistor with base to emitter junction is forward biased and collector to base junction reverse biased is as show in figure.

As the base to emitter junction is forward biased the majority carriers emitted by the p-type emitter i.e., holes have a tendency to flow towards the base which constitutes the emitter current $I_E$.

As the base is n-type there is a chance of recombination of holes emitted by the emitter with the electrons in the n-type base. But as the base us very thin and lightly doped only few electrons less than 5% combine with the holes emitted by the p-type emitter, the remaining 95% charge carriers cross over into the collector region to constitute thecollectorcurrent.

**IE = IB + IC**

# TRANSISTOR CURRENTCOMPONENTS:

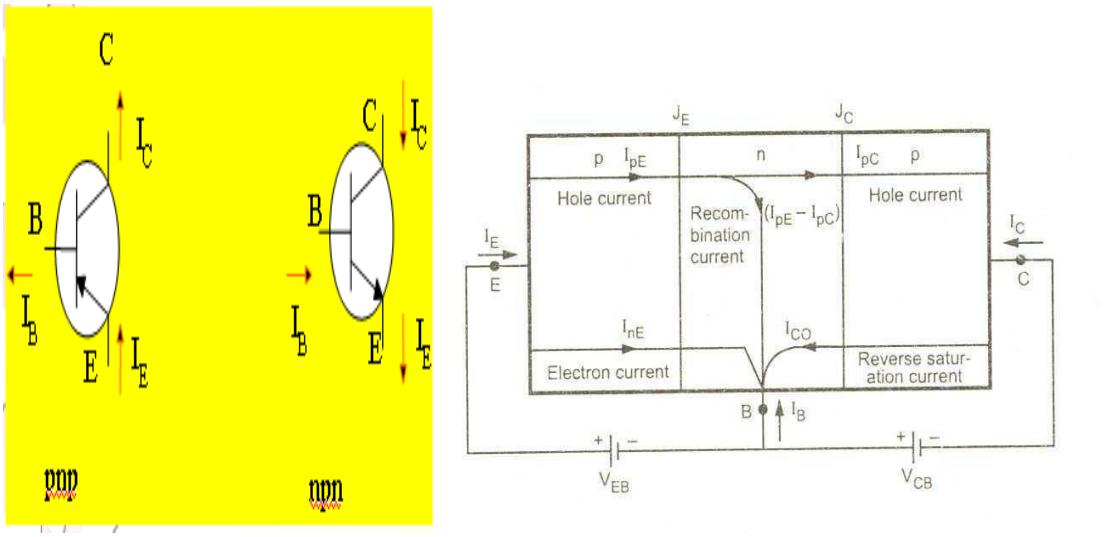



**FIG 2**

The above fig 2 shows the various current components, which flow across the forward biased emitter junction and reverse- biased collector junction. The emitter current $I_E$consists of hole current $I_{PE}$ (holes crossing from emitter into base) and electron current $I_{nE}$(electrons crossing from base into emitter).The ratio of hole to electron currents, $I_{pE/}$ $I_{nE}$ , crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n material. In a transistor, the doping of that of the emitter is made much larger than the doping of the base. This feature ensures (in p-n-p transistor) that the emitter current consists an almost entirely of holes. Such a situation is desired since the current which results from electrons crossing the emitter junction from base to emitter does not contribute carriers, which can reach thecollector.

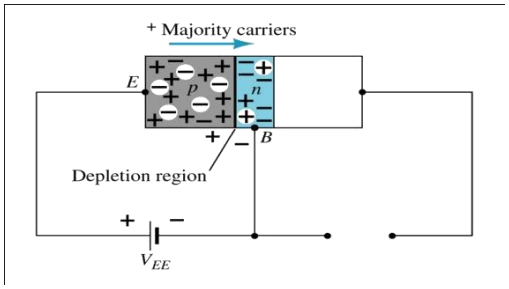
Not all the holes crossing the emitter junction $J_E$ reach the the collector junction $J_C$
Because some of them combine with the electrons in n-type base. If $I_{pC}$ is hole current at junction $J_C$ there must be a bulk recombination current ( $I_{PE-}$ $I_{pC}$ ) leaving the base.

Actually, electrons enter the base region through the base lead to supply those charges, which have been lost by recombination with the holes injected in to the base across $J_E$.If the emitter were open circuited so that $I_E$=0 then $I_{pC}$ would be zero. Under these circumstances, the base and collector current $I_C$ would equal the reverse saturation current $I_{CO.}$ If $I_E \neq 0$then

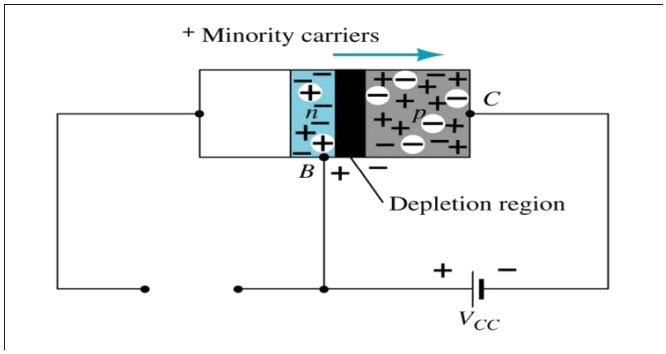
$I_C = I_{CO} - I_{pC}$

For a p-n-p transistor, $I_{CO}$ consists of holes moving across $J_{Cfrom}$ left to right (base to collector) and electrons crossing $J_C$ in opposite direction. Assumed referenced direction for $I_{CO}$ i.e. from right to left, then for a p-n-p transistor, $I_{COis}$ negative. For an n-p-n transistor, $I_{CO}$ is positive.The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

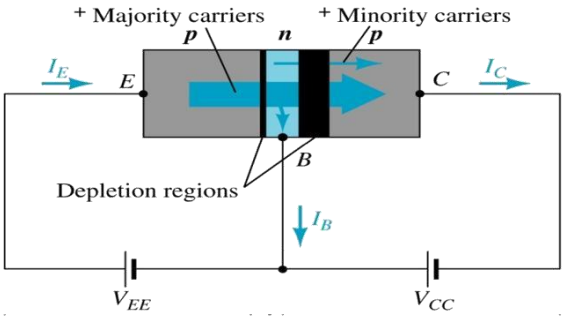
One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.




Forward-biased junction of a pnptransistor




Reverse-biased junction of a pnptransistor




Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

A very small number of carriers (+) will through n-type material to the base terminal. Resulting IB is typically in order of microamperes.

The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal

Applying KCL to the transistor :

$$I_E = I_C + I_B$$

The comprises of two components – the majority and minority carriers

$$I_C = I_{Cmajority} + I_{COminority}$$

$I_{CO}$ – $I_C$current with emitter terminal open and is called leakage current

Various parameters which relate the current components is given below

**Emitter efficiency:**

$$\gamma = \frac{currentofinjectedcar\ riersatJ_E}{totalemitt\ ercurrent}$$

$$\gamma = \frac{I_{PE}}{I_{pE}+I_{nE}} = \frac{I_{pE}}{I_{nE}}$$

**Transport Factor:**

$$\beta^* = \frac{injectedca\ rriercurrentreachingJ_C}{injectedca\ rrierncurrentatJ_E}$$

$$\beta^* = \frac{I_{pC}}{I_{nE}}$$

**Large signal current gain:**

The ratio of the negative of collector current increment to the emitter current change from zero (cut-off)to $I_E$ the large signal current gain of a common base transistor.

$$\alpha = \frac{-(I_C - I_{CO})}{I_E}$$

Since $I_C$and $I_E$ have opposite signs, then α, as defined, is always positive. Typically numerical values of α lies in the range of 0.90 to 0.995

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{nE}} * \frac{I_{pE}}{I_E} \qquad \alpha = \beta * \gamma$$

The transistor alpha is the product of the transport factor and the emitter efficiency. This statement assumes that the collector multiplication ratio $\alpha^*$ is unity. $\alpha^*$ is the ratio of total current crossing $J_C$ to hole arriving at thejunction.

## Bipolar TransistorConfigurations

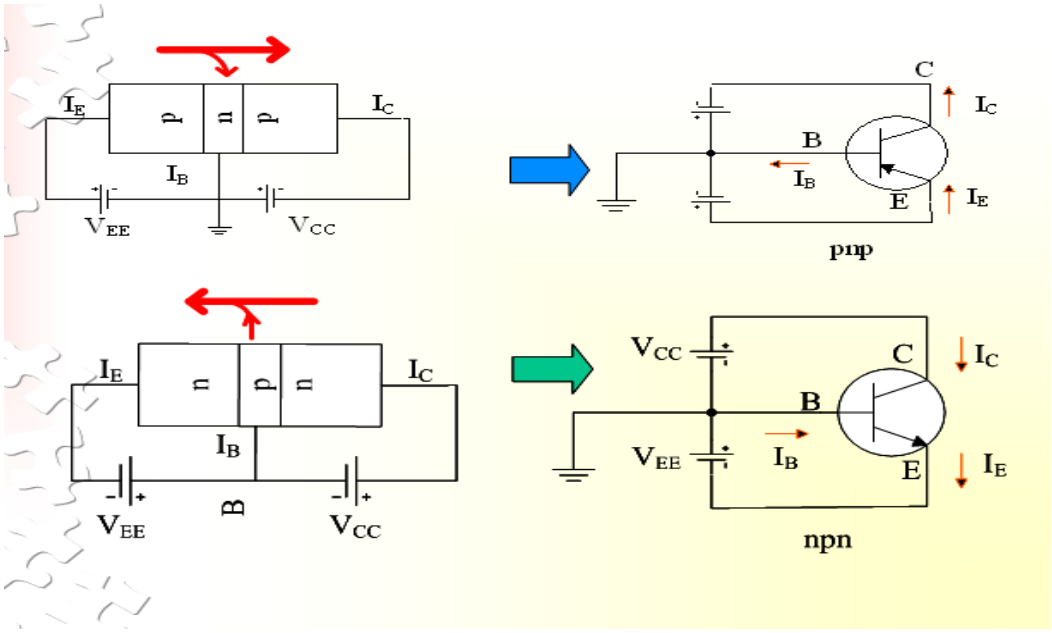
As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- 1. Common Base Configuration - has Voltage Gain but no CurrentGain.
- 2 Common Emitter Configuration - has both Current and VoltageGain.
- 3. Common Collector Configuration - has Current Gain but no VoltageGain.

## COMMON-BASECONFIGURATION

Common-base terminology is derived from the fact that the : base is common to both input and output of t configuration. base is usually the terminal closest to or at ground potential. Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriers in the n-type material. All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

Note that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch.

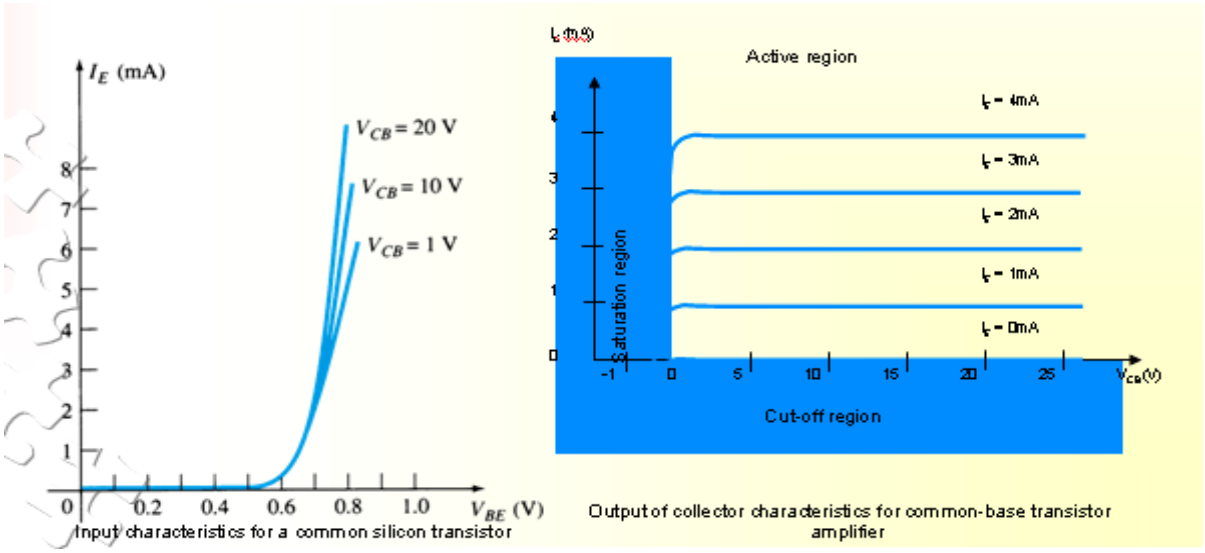



To describe the behavior of common-base amplifiers requires two set of characteristics:

1. Input or driving pointcharacteristics.
2. Output or collector characteristics

The output characteristics has 3 basicregions:

- Active region –defined by the biasingarrangements
- Cutoff region – region where the collector current is 0A
- Saturation region- region of the characteristics to the left of $V_{CB}$ =0V

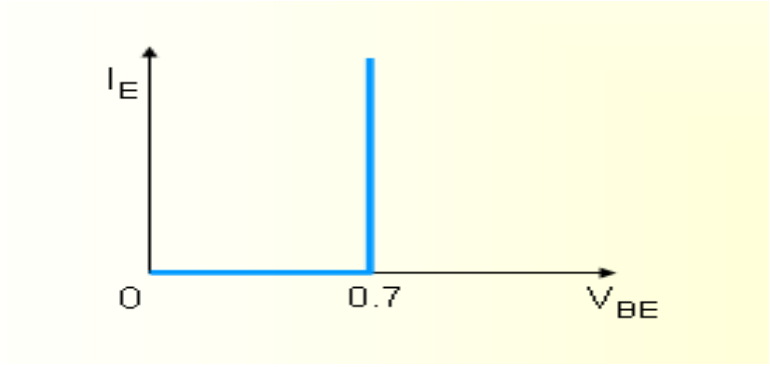


| Active region | Saturation region | Cut-off region |
|---|---|---|
| •$I_E$ increased, Ic increased<br>•BE junction forward bias and CB junction reverse bias<br>•Refer to the graf, Ic ≈ $I_E$<br>•Ic not depends on $V_{CB}$<br>•Suitable region for the transistor working as amplifier | • BE and CB junction is forward bias<br>• Small changes in $V_{CB}$ will cause big different to Ic<br>• The allocation for this region is to the left of $V_{CB}$= 0 V. | • Region below the line of $I_E$=0 A<br>• BE and CB is reverse bias<br>• no current flow at collector, only leakage current |

The curves (output characteristics) clearly indicate that a first approximation to the relationship between IE and IC in the active region is given by

$I_C \approx IE$

Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to be$V_{BE}$ = 0.7V




In the dc mode the level of $I_C$ and $I_E$ due to the majority carriers are related by a quantity called alpha

$\alpha = \alpha_{dc}$

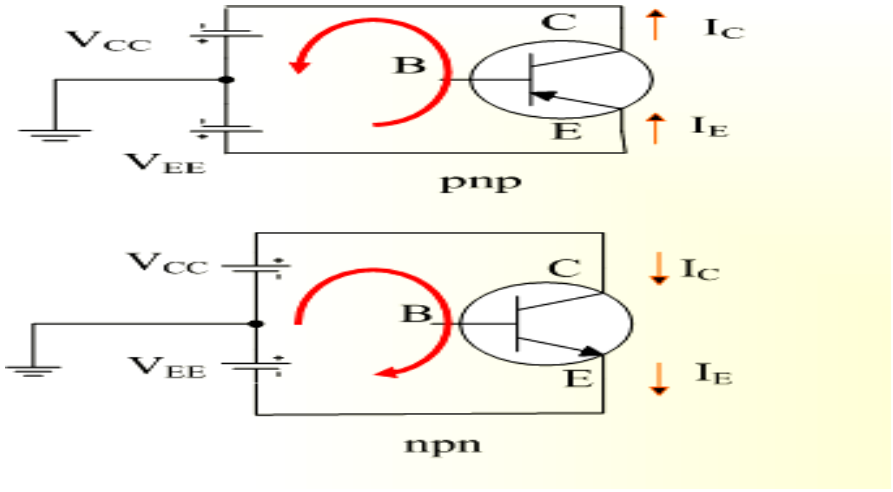
$I_C = \alpha I_E + I_{CBO}$

It can then be summarize to $I_C = \alpha I_E$ (ignore $I_{CBO}$ due to small value)

For ac situations where the point of operation moves on the characteristics curve, an ac alpha defined by $\alpha_{ac}$

Alpha a common base current gain factor that shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of α is typical from 0.9 ~ 0.998.

**Biasing:**Proper biasing CB configuration in active region by approximation $I_C \approx I_E$ ($I_B \approx 0$ uA)




# COMMON-EMITTERCONFIGURATION

It is called common-emitter configuration since : emitter is common or reference to both input and output terminals.emitter is usually the terminal closest to or at ground potential.

Almost amplifier design is using connection of CE due to the high gain for current and voltage.

Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region

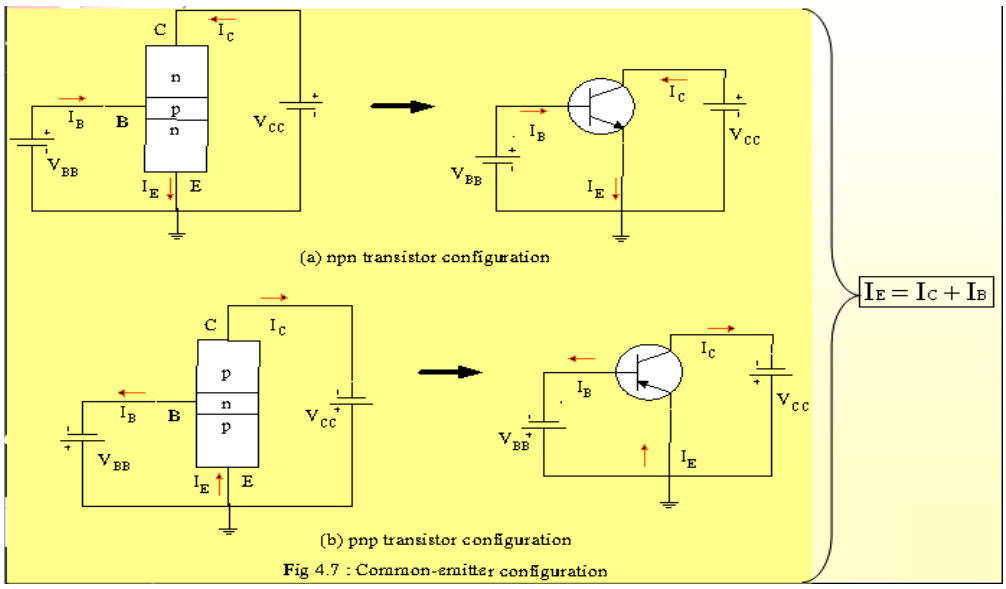


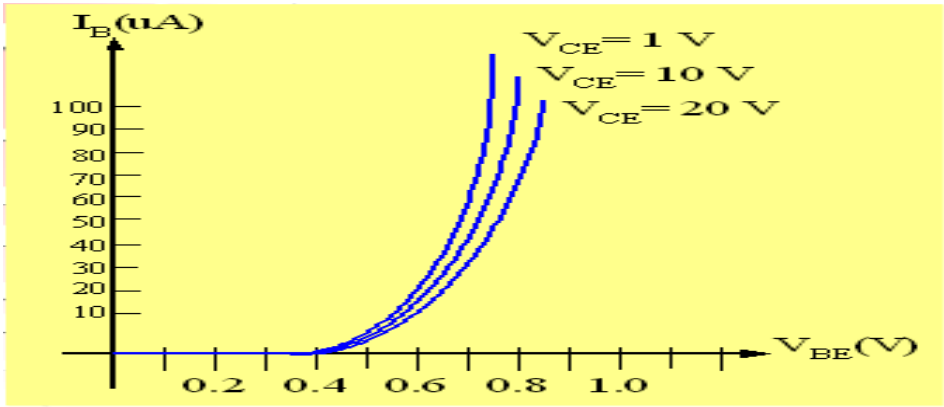

Fig 4.7 : Common-emitter configuration

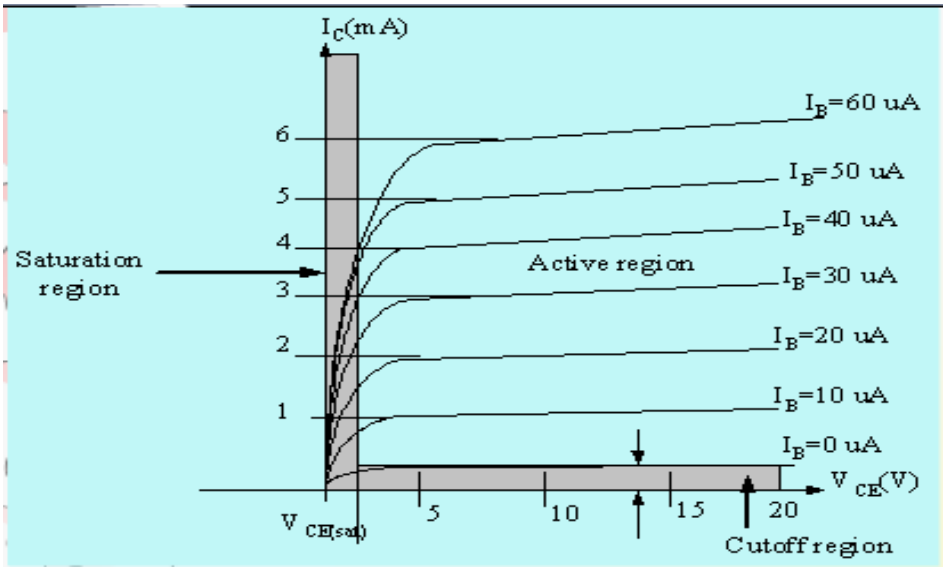
$I_B$ is microamperes compared to miliamperes of $I_C$.

$I_B$ will flow when $V_{BE}$> 0.7V for silicon and 0.3V for germanium

Before this value $I_B$ is very small and no $I_B$.

Base-emitter junction is forward bias Increasing $V_{CE}$ will reduce $I_B$ for different values.




Output characteristics for acommon-emitter npn transistor

For small $V_{CE}$ ($V_{CE}$< $V_{CESAT}$, $I_C$ increase linearly with increasing of $V_{CE}$

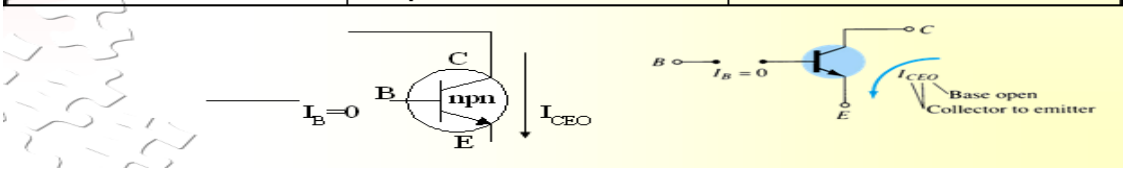
$V_{CE} > V_{CESAT}$ $I_C$ not totally depends on $V_{CE}$ → constant $I_C$

$I_B$(uA) is very small compare to $I_C$ (mA). Small increase in $I_B$ cause big increase in $I_C$

$I_B$=0 A → $I_{CEO}$ occur.

Noticing the value when $I_C$=0A. There is still some value of current flows.

| Active region | Saturation region | Cut-off region |
|---|---|---|
| • B-E junction is forward bias<br>• C-B junction is reverse bias<br>• can be employed for voltage, current and power amplification | • B-E and C-B junction is forward bias, thus the values of $I_B$ and $I_C$ is too big.<br>• The value of $V_{CE}$ is so small.<br>• Suitable region when the transistor as a logic switch.<br>• NOT and avoid this region when the transistor as an amplifier. | • region below $I_B$=0μA is to be avoided if an undistorted o/p signal is required<br>• B-E junction and C-B junction is reverse bias<br>• $I_B$=0, $I_C$ not zero, during this condition $I_C$=$I_{CEO}$ where is this current flow when B-E is reverse bias. |

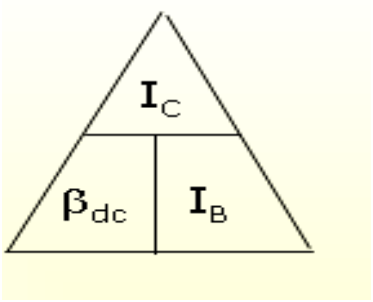



**Beta (β) or amplification factor**

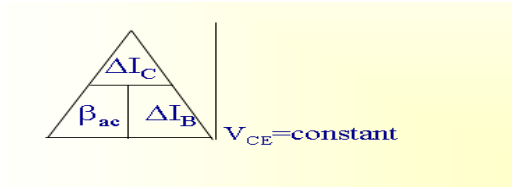
The ratio of dc collector current (IC) to the dc base current (IB) is dc beta (βdc ) which is dc current gain where IC and IB are determined at a particular operating point, Q-point (quiescent point). It's define by the following equation:

$$30 < \beta dc < 300 \rightarrow 2N3904$$

On data sheet, $\beta_{dc}$=*hfe* with *h* is derived from ac hybrid equivalent cct. FE are derived from forward-current amplification and common-emitter configuration respectively.




For ac conditions, an ac beta has been defined as the changes of collector current ($I_C$) compared to the changes of base current ($I_B$) where $I_C$ and $I_B$ are determined at operating point. On data sheet, $\beta_{ac}$=*hfe* It can defined by the following equation:




From output characteristics of commonemitter configuration, find $\beta_{ac}$ and $\beta_{dc}$ with an

Operating point at $I_B$=25 μA and $V_{CE}$ =7.5V

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{ce}\ =\ \text{constant}}$$

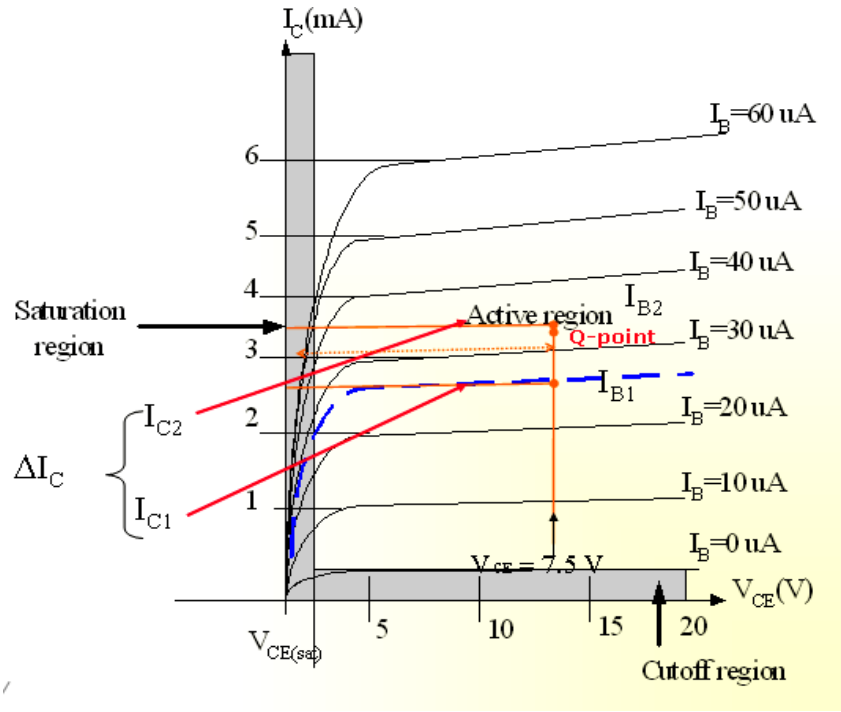
$$= \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{3.2\,m - 2.2\,m}{30\,\mu - 20\,\mu}$$

$$= \frac{1\,m}{10\,\mu} = 100$$

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$= \frac{2.7\,m}{25\,\mu}$$

$$= 108$$


$I_C$(mA)
$I_B$=60 uA
$I_B$=50 uA
$I_B$=40 uA
$I_{B2}$
$I_B$=30 uA
$I_{B1}$
$I_B$=20 uA
$I_B$=10 uA
$I_B$=0 uA
6
5
4
3
2
1
Saturation region
Active region
Q-point
$I_{C2}$
$\Delta I_C$
$I_{C1}$
$V_{CE}$ = 7.5 V
$V_{CE}$(V)
5
10
15
20
$V_{CE(sat)}$
Cutoff region

**Relationship analysis between α and β**

CASE 1

$I_E = I_C + I_B$ (1)

subtitute equ. $I_C = \beta I_B$ into (1) we get

$$I_E = (\beta + 1) I_B$$

CASE 2

known : $\alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha}$ (2)

known : $\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$ (3)

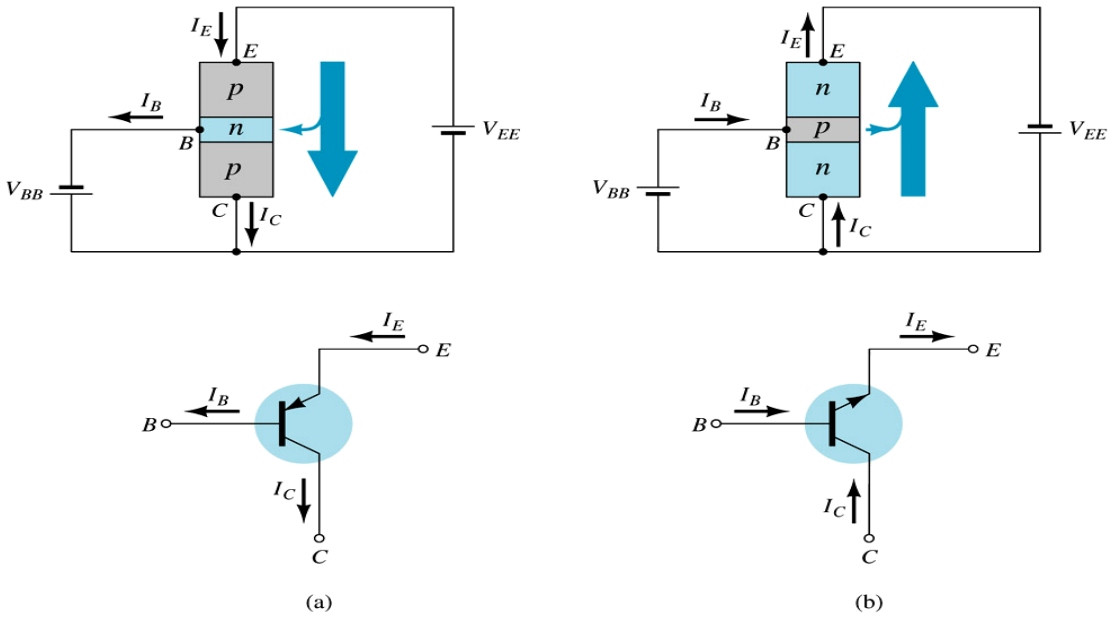
subtitute (2) and (3) into (1) we get,

$$\alpha = \frac{\beta}{\beta + 1} \quad \text{and} \quad \beta = \frac{\alpha}{1 - \alpha}$$

# COMMON – COLLECTORCONFIGURATION

Also called emitter-follower (EF). It is called common-emitter configuration since both the signal

source and the load share the collector terminal as a common connection point.The output voltage is obtained at emitter terminal. The input characteristic of common-collector configuration is similar with common-emitter. configuration.Common-collector circuit configuration is provided with the load resistor connected from emitter to ground.It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.




For the common-collector configuration, the output characteristics are a plot of $I_E$ vs $V_{CE}$ for a range of values of $I_B$.

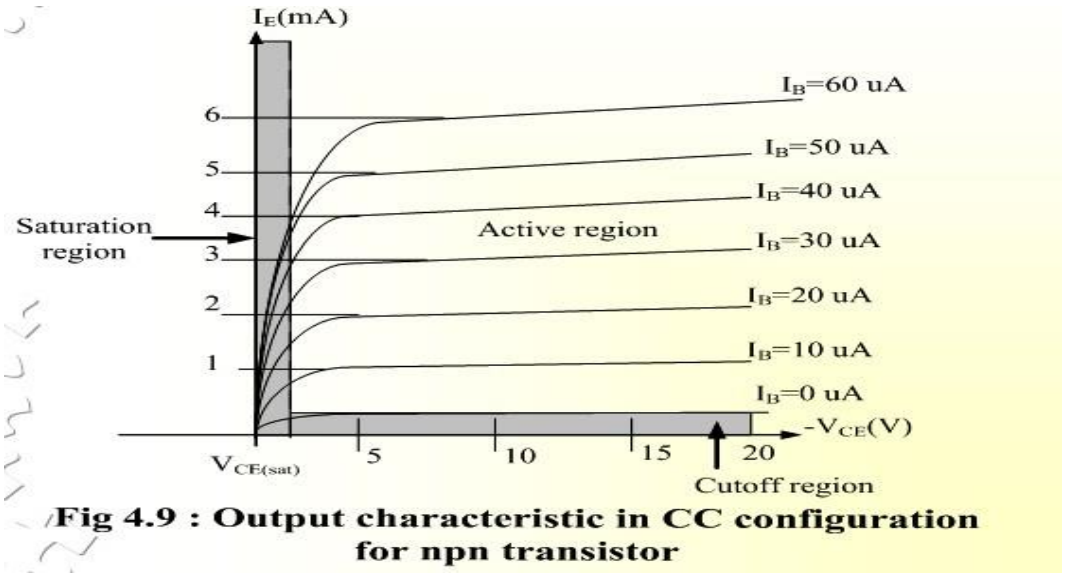



**Fig 4.9 : Output characteristic in CC configuration for npn transistor**

**Limits of opearation**

Many BJT transistor used as an amplifier. Thus it is important to notice the limits of operations.At least 3 maximum values is mentioned in data sheet.

There are:

a) Maximum power dissipation at collector: $P_{Cmax}$ or $P_D$

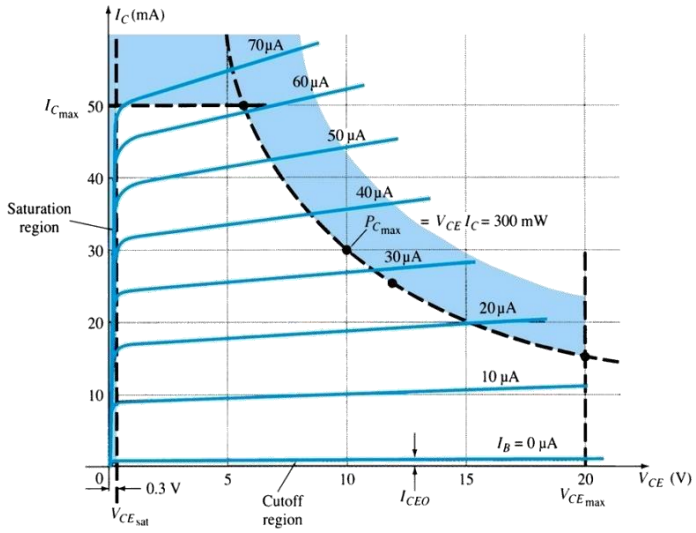
b) Maximum collector-emitter voltage: $V_{CEmax}$ sometimes named as $V_{BR(CEO)}$ or $V_{CEO}$.

c) Maximum collector current: ICmax

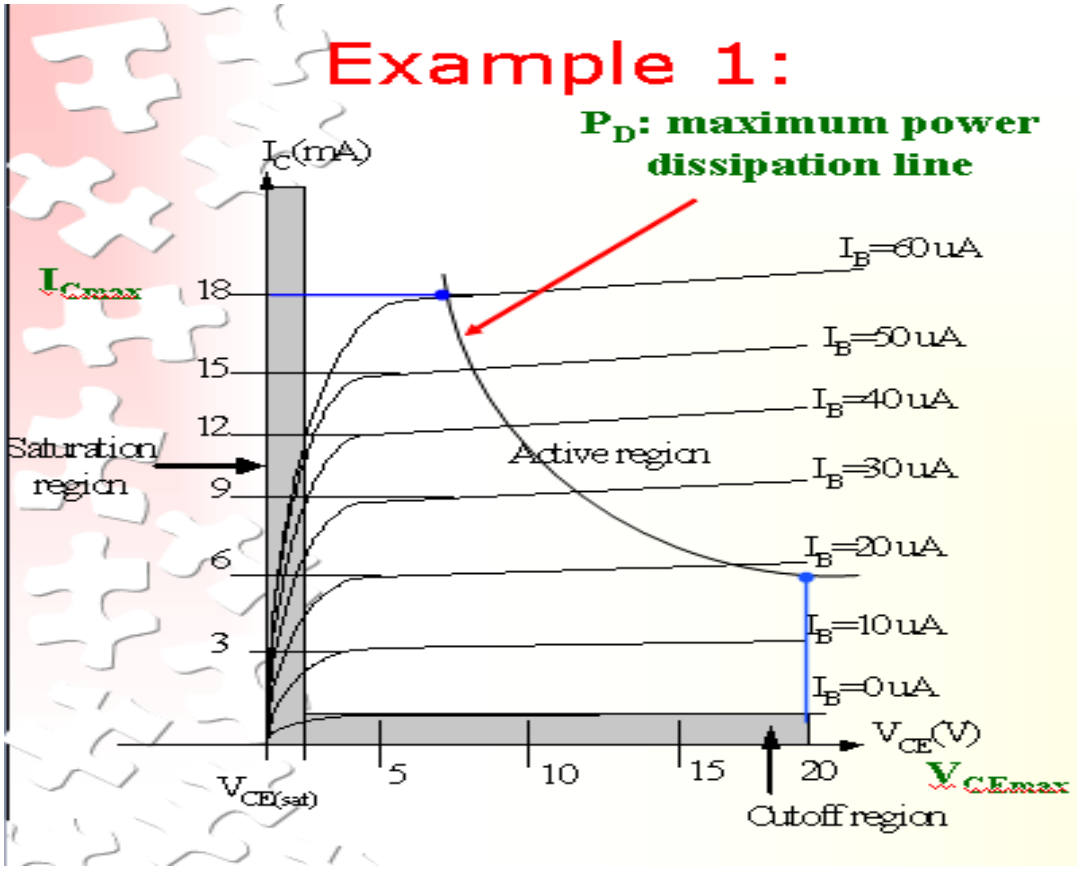
There are few rules that need to be followed for BJT transistor used as an amplifier. The rules are: transistor need to be operate in active region!

$I_C < I_{Cmax}$

$P_C < P_{Cmax}$




Note: $V_{CE}$ is at maximum and $I_C$ is at minimum ($I_{CMAX}$=$I_{CEO}$)inthe cutoff region. $I_C$is at maximum and $V_{CE}$is at minimum ($V_{CE}$max = $V_{cesat}$ = $V_{CEO}$) in the saturation region. The transistor operates in the active region between saturation andcutoff.




Refer to the fig. Example; A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

*Step1:*

The maximum collector powerdissipation,

**$P_D=I_{CMAX}$ x $V_{CEmax}$**= 18m x 20 = 360mW

*Step 2:*

At any point on the characteristics the product of and must be equal to 360 mW.

Ex. 1. If choose $I_{Cmax}$= 5 mA, substitute into the (1), we get

$V_{CEmax}I_{Cmax}$= 360 mW

$V_{CEmax}$(5 m)=360/5=7.2 V

Ex.2. If choose $V_{CEmax}$=18 V, substitute into (1), we get

$V_{CEmax}I_{Cmax}$= 360 mW

(10) $I_{CMAX}$=360m/18=<u>20 mA</u>

**Derating $P_{Dmax}$**

$P_{DMAX}$ is usually specified at 25°C.

The higher temperature goes, the less is $P_{DMAX}$

Example;A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

## *THE TRANSISTOR AS ANAMPLIFIER*

Consider the circuit fragment shown at right, which includes an *NPN* transistor connected between two power supply "*rails*" $V_{CC}$ and $V_{EE}$ (with, naturally, $V_{CC} > V_{EE}$ ). Assume that some method has been used to *bias* the transistor's base terminal at the voltage $V_B > V_{EE}$ so that the transistor's base-emitter junction is forward-biased and conductingcurrent $I_B$ as shown (we'll discuss ways of biasing the transistor in a subsequent section). What we want to determine are the relationships between the various voltages and currents, the resistor values $R_C$ and $R_E$ , and the transistor's $\beta$

We start the analysis by connecting the base and emitter voltages using the forward bias diode drop

$V_{BE} \approx 0.6$V across the base-emitter *PN* junction. As we know from our previous studyof the semiconductor diode, this voltage will be a very weak function of the base current $I_B$ , sowewillusetheworkingassumptionthatitisafixed,constantvalue.Consequently,if we know $V_B$ , then we also know $V_E$ , and vice versa. Given $V_E$ , we now know the voltage drop across the resistor $R_E$ , so we also know the current through it: $I_E = (V_E - V_{EE})/R_E$.

Knowing $I_E$ and the transistor's current gain $\beta$ immediately tells us the other two transistor currents $I_B$ and $I_C$ , since the currents are related through $\beta$ as shown in below Figure The value of $R_C$ then gives us the collector voltage $V_C$ ,since $I_C = (V_{CC} - V_C)/R_C$ .Thuswe*havesucceededinrelatingthecircuit'sstatevariables(currentsandvoltages),as we set out to do. Note that there are some conditions that must be met for our solution to be realistic: all the currents must flow in the directions shown by the arrows in Figure , and it must be the case that* $V_{EE} < V_E < V_B \leq V_C < V_{CC}$ *. If one or more of these conditions is violated by our solution, then our solution fails, and the transistor circuit is operating as a switch rather than as an amplifier (we'll discuss transistor switch circuits in the nextsection).*

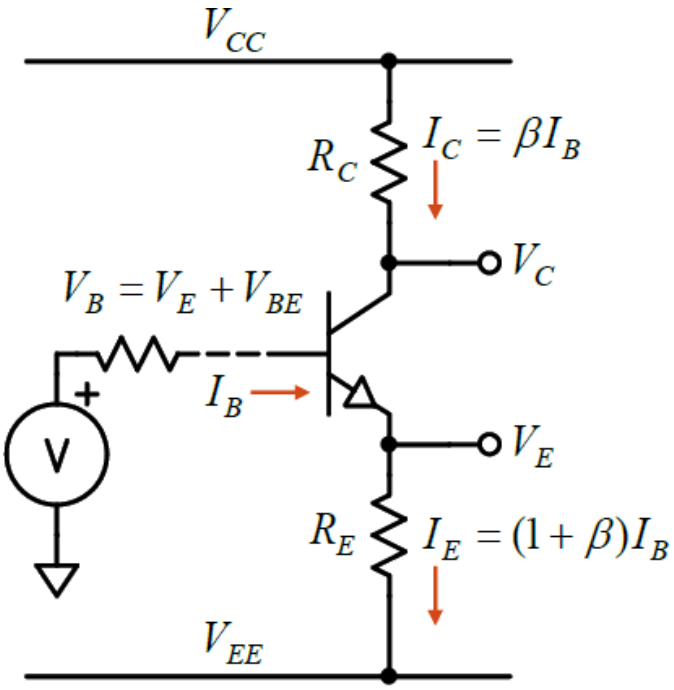



**Figure : A collector-emitter circuit fragment of an *NPN* transistor used as an amplifier.**

## Transistor as switch

If you apply a fairly large current to a transistor's base (a few mA, say), then $I_C = \beta I_B$ could be quite large. Consider the circuit in Figure 2 , for example. The transistor's base-emitter junction is clearly forward-biased by the +5V $V_{in}$ source; with $V_{BE} \approx 0.7\text{V}$, the base current would be

$$I_B = (5\text{V} - 0.7\text{V})/4.3\text{k}\Omega = 1\text{mA}$$

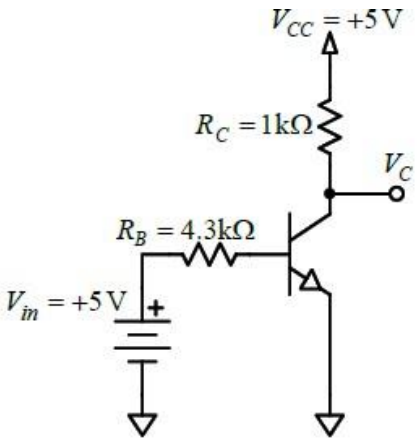



Figure 2 An *NPN switch* circuit.

If the transistor $\beta \sim 150$, then we would expect a collector current of $I_C \sim 150\text{mA}$. But the collector power supply ($V_{CC}$) is only +5V, so with $R_C = 1\text{k}\Omega$ the most current that could possibly flow into the collector is $5\text{V}/1\text{k}\Omega = 5\text{mA}$. In this case the transistor will be driven into *saturation* by the large base current, and it will reduce its collector-emitter voltage drop ($V_{CE}$) to a fraction of a volt as the collector current is maximized (given the constraints imposed by $V_{CC}$ and $R_C$). The transistor's operating state in this case is represented by the very left edge of the graph of the characteristic curves

this region has been expanded in Figure 3 Note how a relatively small base current can drive this particular transistor's collector-emitter voltage drop to a very small value if the collector current is limited by external components to much less than $\beta I_B$.

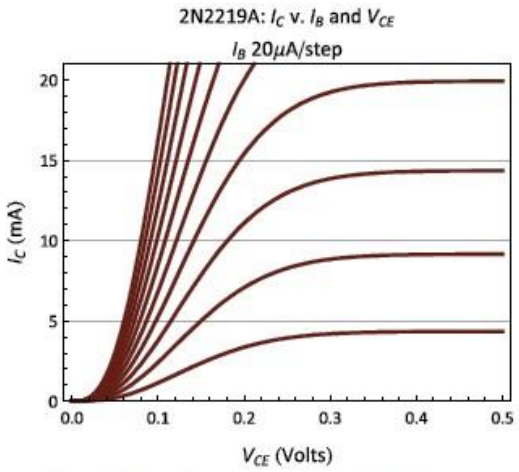



Figure 3 : *Saturation region* of the transistor characteristic curves. The left-most curve corresponds to $I_B$ = 0.2mA; note that even this relatively small base current will drive the collector-emitter voltage drop down to only about 0.1V even for collector currents as high as 20mA.

***Ensuring transistor saturation***

When using a transistor as a switch a good rule of thumb is to design the input circuit to the base so that $I_B$ will be approximately 5% to 10% of the required $I_C$, ensuring that $I_C \ll \beta I_B$. This will drive the transistor well into its saturation region, minimizing $V_C$.

# FIELD EFFECT TRANSISTOR

## INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier orswitch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no inputcurrent.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolartransistor.
4. FET is also a three terminal device, labeled as source, drain andgate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as thechannel.
7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majoritycarriers.
8. As FET has conduction through only majority carriers it is less noisy thanBJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space thanBJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signaloperation.

11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermalbreakdown.

## CLASSIFICATION OFFET:

There are two major categories of field effect transistors:

1. Junction Field EffectTransistors

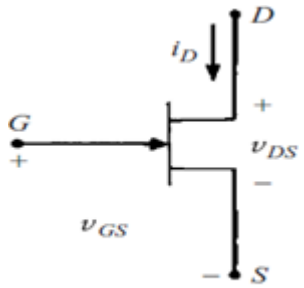
2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

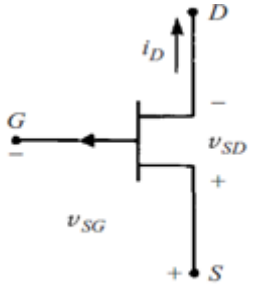
MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is of P-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.




N-channel FET

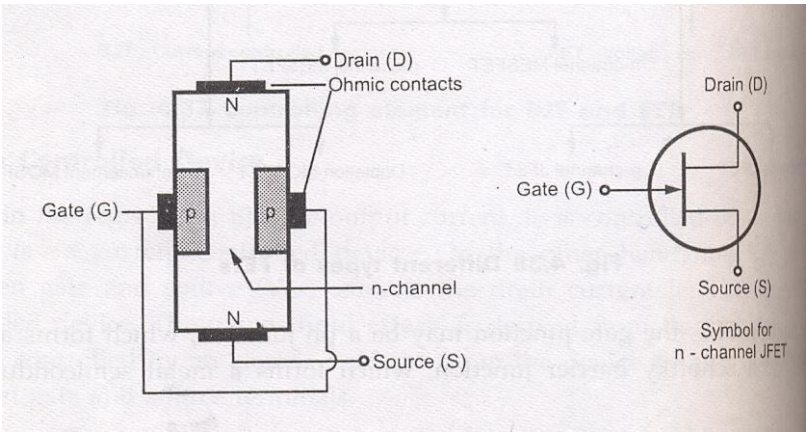



P-channel FET

# CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

**CONSTRUCTION OF N-CHANNEL JFET**




A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source . And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channelJFET.

## OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current Id flows. When the gate is biased negative with respective to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and Id is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and Id is cut offcompletely.

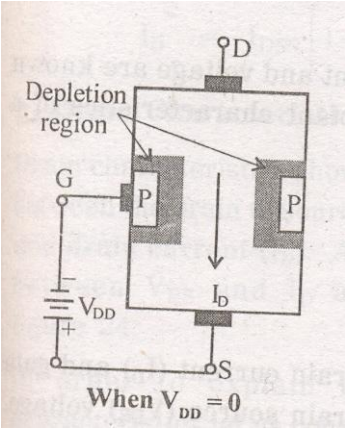
There are two ways to control the channel width

1. By varying the value ofVgs
2. And by Varying the value of Vds holding Vgsconstant

**1 By varying the value of Vgs :-**

We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of Vgs. This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reversebiasisappliedbyabatteryvoltageVgsconnectedbetweenthegateandthesource

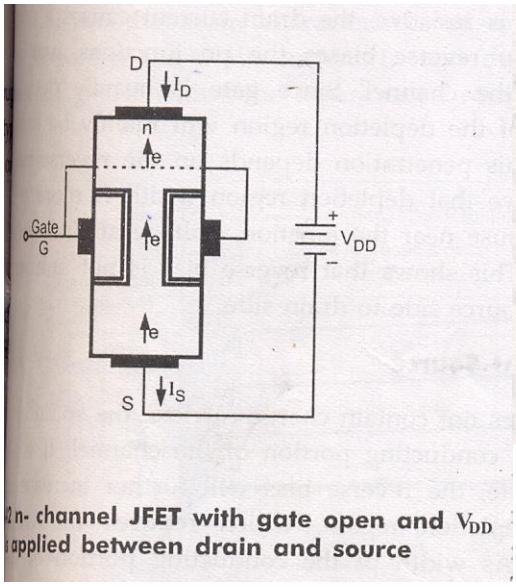
terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.



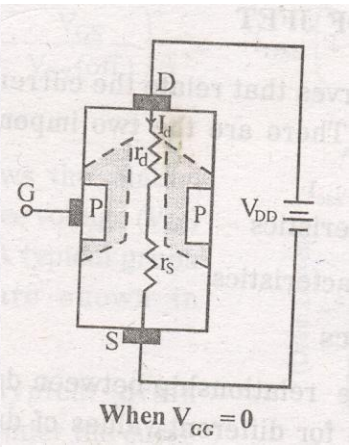

1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletionregions.
2) If both P and N regions are heavily doped then the depletion region extends symmetrically on bothsides.
3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than Pregion.
4) So when no Vds is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in thejunction.
5) Asthereversebiasvoltageisincreasesthethicknessofthedepletionregionalsoincreases.
   i.e. the effective channel width decreases .
6) By varying the value of Vgs we can vary the width of thechannel.

**2 Varying the value of Vds holding Vgs constant :-**

1) When no voltage is applied to the gate i.e. Vgs=0 , Vds is applied between source and drain the electrons will flow from source to drain through the channel constituting drain currentId .
2) With Vgs= 0 for Id= 0 the channel between the gate junctions is entirely open .In response to a small applied voltage Vds , the entire bar acts as a simple semi conductor resistor and the current Id increases linearly with Vds.
3) The channel resistances are represented as rd and rs as shown in thefig.




2 n- channel JFET with gate open and $V_{DD}$ applied between drain and source




When $V_{GG} = 0$

4) This increasing drain current Id produces a voltage drop across rd which reverse biases the gate to source junction,(rd> rs) .Thus the depletion region is formed which is not symmetrical.
5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towardssourcebecauseVrd>>Vrs.Soreversebiasishigherneardrainthanatsource.
6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage Vds is reached at which the channel is pinched off. This is the voltage where the current Id begins to level off and approach a constantvalue.
7) So, by varying the value of Vds we can vary the width of the channel holding Vgsconstant.

**When both Vgs and Vds is applied:-**

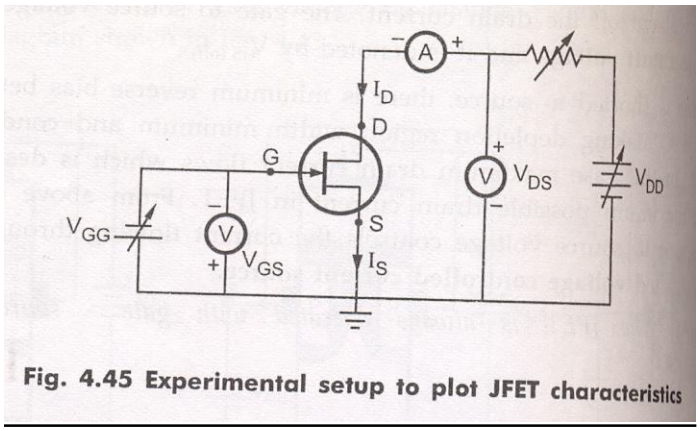


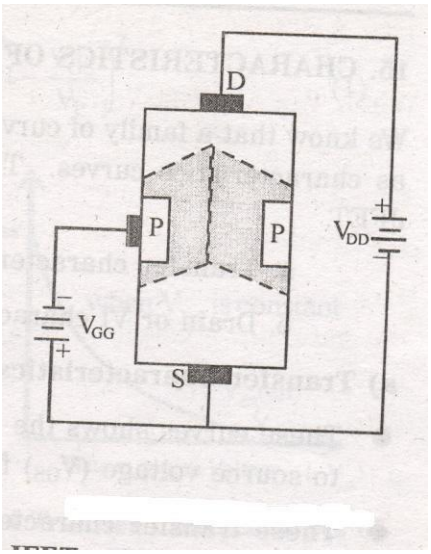

Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current Id to Zero for, if such indeed, could be the case the gate voltage Vgs is applied in the direction to provide additional reverse bias

1) When voltage is applied between the drain and source with a battery Vdd, the electrons flow from source to drain through the narrow channel existing between thedepletion

regions. This constitutes the drain current Id, its conventional direction is from drain to source.

2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated byIdss.




3) When Vgs is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
4) When Vgs is further increased a stage is reached at which to depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current toZero.

# CHARACTERISTICS OF N-CHANNEL JFET:-

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

1) Drain or VICharacteristics
2) Transfercharacteristics

**1. DrainCharacteristics:-**

Drain characteristics shows the relation between the drain to source voltage Vds and drain current Id. In order to explain typical drain characteristics let us consider the curve with Vgs= 0.V.

1) When Vds is applied and it is increasing the drain current $I_D$ also increases linearly up to kneepoint.
2) This shows that FET behaves like an ordinary resistor.This region is called as ohmicregion.
3) $I_D$ increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmicregion.

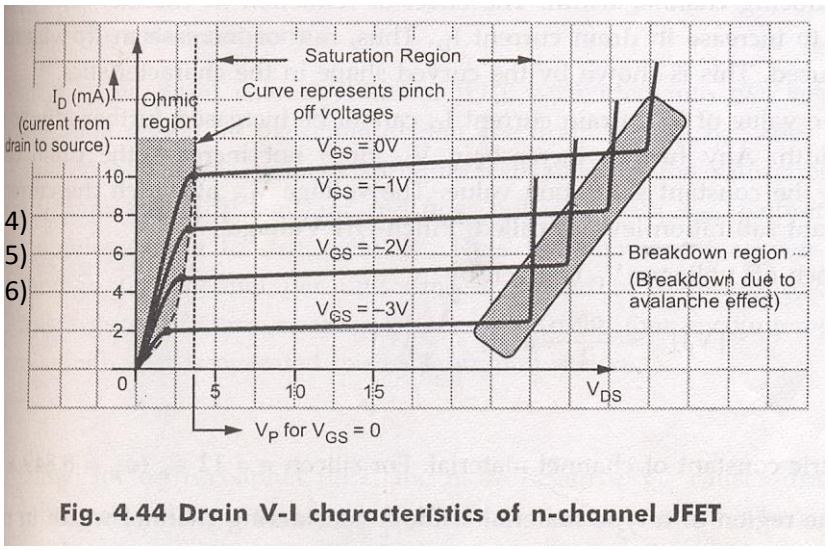



**Fig. 4.44 Drain V-I characteristics of n-channel JFET**

4)
5)
6)

4) It is because of the fact that there is an increase in $V_{DS}$ .This in turn increases the reverse bias voltage across the gate source junction .As a result of this depletion region grows in size thereby reducing the effective width of thechannel.

5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinchoff.

6) The drain to source voltage at which channel pinch off occurs is called pinch offvoltage(Vp).

**PINCH OFF Region:-**

1) This is the region shown by the curve as saturationregion.
2) It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region , the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constantinthisregion.TouseFETasan amplifieritisoperatedinthissaturationregion.
3) In this drain current remains constant at its maximum value$I_{DSS}$.

4) The drain current in the pinch off region depends upon the gate to source voltage and is given by therelation

$$I_d = I_{dss}\,[1-V_{gs/Vp}]^2$$

This is known as shokley's relation.

**BREAKDOWN REGION:-**

1) The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage isincreased.
2) It is because of the gate to source junction due to avalancheeffect.
3) The avalanche break down occurs at progressively lower value of $V_{DS}$ because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gatejunction
   This causes
   1. The maximum saturation drain current issmaller
   2. The ohmic region portiondecreased.
4) It is important to note that the maximum voltage $V_{DS}$ which can be applied to FET is the lowest voltage which causes available breakdown.

**2. TRANSFERCHARACTERISTICS:-**

These curves shows the relationship between drain current $I_D$ and gate to source voltage $V_{GS}$ for different values of$V_{DS}$.

1) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitablevalue.
2) Plot the graph between gate to source voltage along the horizontal axis and current $I_D$on the vertical axis. We shall obtain a curve likethis.

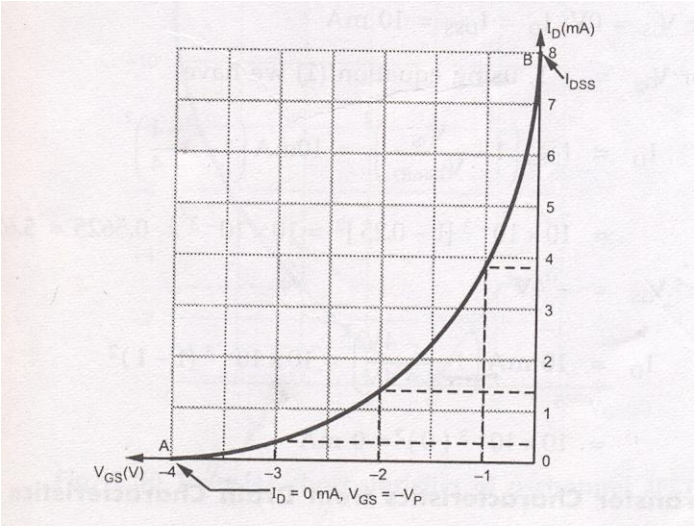



**Fig. 4.48 Transfer characteristics of n-channel JFET**

3) As we know that if $V_{gs}$ is more negative curves drain current to reduce . where $V_{gs}$ is made sufficiently negative, $I_d$ is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of $V_{gs}$at the cutoff point is designed as$V_{gsoff}$

4) The upper end of the curve as shown by the drain current value is equal to $I_{dss}$ that is when $V_{gs}$ = 0 the drain current ismaximum.

5) While the lower end is indicated by a voltage equal to$V_{gsoff}$
6) If$Vg_s$continuouslyincreasing,thechannelwidth isreduced, then$I_d$=0
7) It may be noted that curve is part of the parabola; it may be expressedas

$I_d=I_{dss}[1-V_{gs}/V_{gsoff}]^2$

**DIFFERENCE BETWEEN $V_p$ AND $V_{gsoff}$ –**

$V_p$ is the value of $V_{gs}$ that causes the JFET to become constant current component, It is measured at $V_{gs}$ =0V and has a constant drain current of $I_d=I_{dss}$ .Where $V_{gsoff}$ is the value of $V_{gs}$ that reduces $I_d$ to approximately zero.

**Why the gate to source junction of a JFET be always reverse biased ?**

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component.

There is one more important characteristic of JFET reverse biasing i.e. J FET 's have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physicalarea.

# JFETPARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are obtained from the characteristiccurves.

A C Drain resistance($r_d$):

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal,when the JFET is operating in the pinch off or saturation region.It is given by the ratio of small change in drain to source voltage $\Delta V_{ds}$ to the corresponding change in drain current $\Delta I_d$ for a constant gate to source voltage $V_{gs.}$

Mathematically it is expressed as $r_d=\Delta V_{ds}/\Delta I_d$ where $V_{gs}$ is held constant.

TRANCE CONDUCTANCE ($g_m$):

It is also called forward transconductance . It is given by the ratio of small change in drain current ($\Delta I_d$) to the corresponding change in gate to source voltage ($\Delta V_{ds}$)

Mathematically the transconductance can be written as

$$g_m=\Delta I_d/\Delta V_{ds}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage ($\Delta V_{ds}$) to the corresponding change in gate to source voltage ($\Delta V_{gs}$)for a constant drain current ($I_d$).

Thus $\mu=\Delta V_{ds}/\Delta V_{gs}$ when $I_d$ held constant

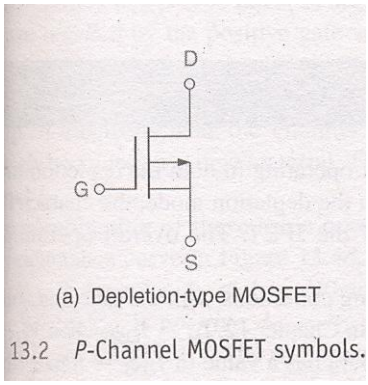
The amplification factor μ may be expressed as a product of transconductance ($g_m$)and ac drain resistance ($r_d$)

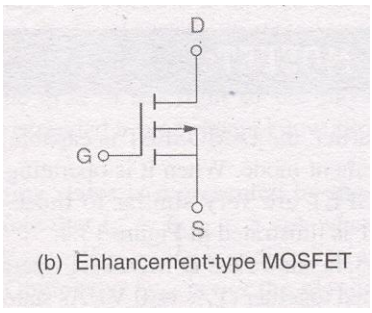
$\mu=\Delta V_{ds}/\Delta V_{gs}=g_m\, r_d$

# MOSFET:-

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.




(a) DepletiontypeMOSFET (b) Enhancement typeMOSFET

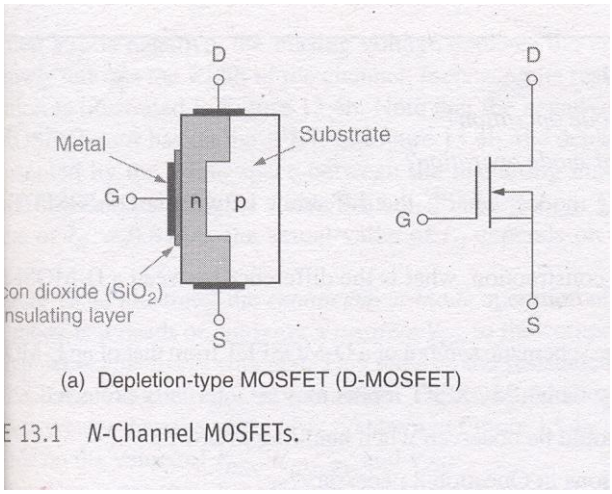
**Both of them are P- channel**

Here are two basic types of MOSFETS

(1) Depletiontype (2) Enhancement type MOSFET.

D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

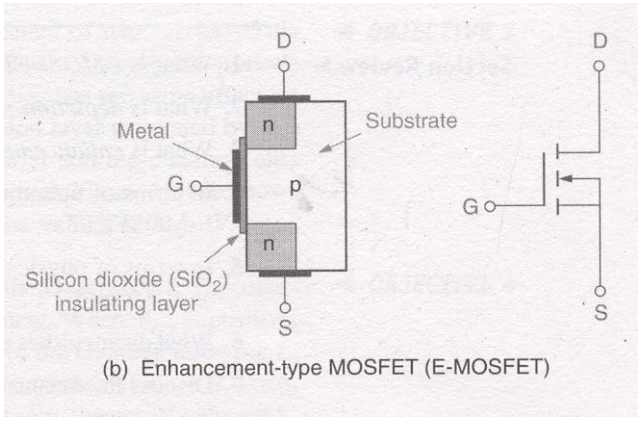
The construction difference between the two is shown in the fig given below.




(a) Depletion-type MOSFET (D-MOSFET)

E 13.1 *N*-Channel MOSFETs.

As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)




(b) Enhancement-type MOSFET (E-MOSFET)

The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drainterminals.

Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of $SIO_2$ a glass like insulating material. The gate material is made up of metal conductor .Thus going from gate to substrate, we can have metal oxide semi conductor which is where the term MOSFET comes from.

Since the gate is insulated from the rest of the component, the MOSFET is sometimes referred to as an insulated gate FET orIGFET.

The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source.

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing in represents an N-channel device, while an arrow pointing out represents p-channeldevice.

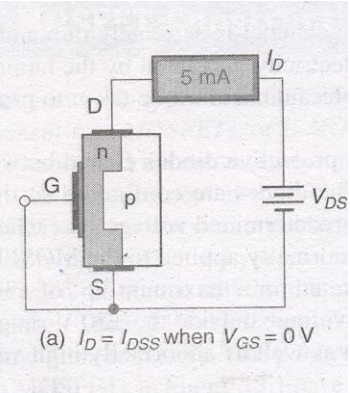
**CONSTRUCTION OF AN N-CHANNEL MOSFET:-**

The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections , which will act as source and drain. A thin layer of insulation silicon dioxide ($SIO_2$) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region.Metal contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal.The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer ofsio2

Is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10 10 to 10power 15ohms) for MOSFET.

## DEPLETION MOSFET

The basic structure of D –MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current $I_{DSS}$ flows foe zero gate to source voltage, Vgs=0.




**Depletion mode operation:-**

1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shortedtogether($V_{GS}$=0V)

2) At this stage $I_D$= $I_{DSS}$ where $V_{GS}$=0V, with this voltage $V_{DS}$, an appreciable drain current $I_{DSS}$ flows.

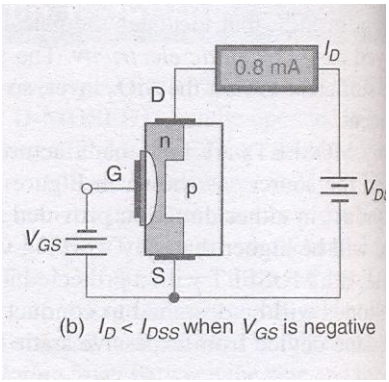
3) If the gate to source voltage is made negative i.e. $V_{GS}$ is negative .Positive charges are induced in the channel through the SIO2 of the gatecapacitor.

4) Since the current in a FET is due to majority carriers(electrons for an N-type material) , the inducedpositivechargesmakethechannellessconductiveandthedraincurrentdropsasVgs is made morenegative.

5) The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletionMOSFET.

6) That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel , increasing itsresistance.

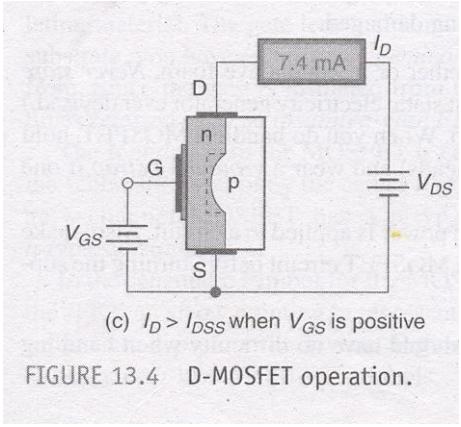
7) Note that negative Vgs has the same effect on the MOSFET as it has on theJFET.




8) As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width.Asaresult,Id<Idss.TheactualvalueofIDdependsonthevalueofIdss,Vgs(off)andVgs.

**Enhancement mode operation of the D-MOSFET:-**

1) This operating mode is a result of applying a positive gate to source voltage Vgs to the device.
2) When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value ofIDSS
3) When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gatevoltage.
4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gatevoltage.
5) With the build up of electrons near the channel , the area to the right of the physical channel effectively becomes an N typematerial.
6) The extended n type channel now allows more current, Id>Idss




(c) $I_D > I_{DSS}$ when $V_{GS}$ is positive

FIGURE 13.4 D-MOSFET operation.

**Characteristics of Depletion MOSFET:-**

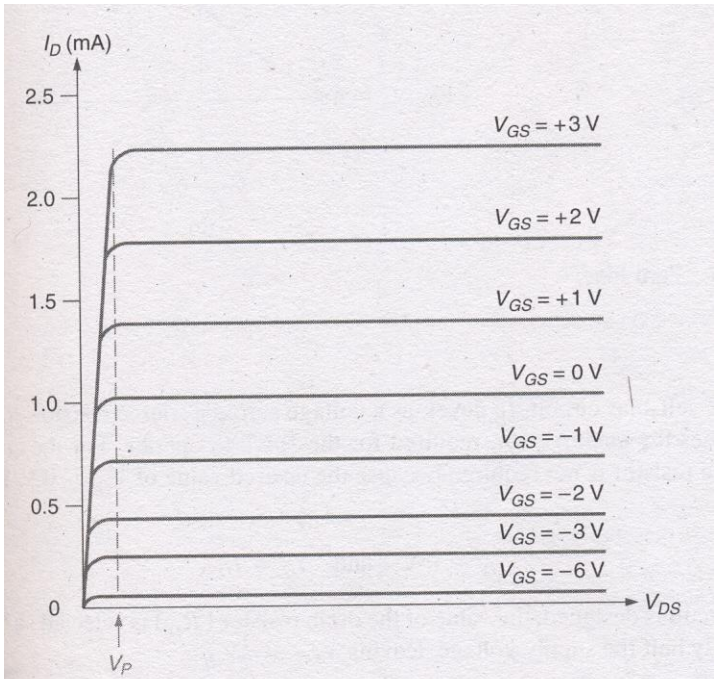
The fig. shows the drain characteristics for the N channel depletion type MOSFET

1) The curves are plotted for both Vgs positive and Vgs negativevoltages
.
2) When Vgs=0 and negative the MOSFET operates in depletion mode when Vgs is positive ,the MOSFET operates in the enhancementmode.
3) The difference between JFET and D MOSFET is that JFET does not operate for positive values ofVgs.

4) When Vds=0, there is no conduction takes place between source to drain, if Vgs<0 and Vds>0 then Id increaseslinearly.

5) But as Vgs,0 induces positive charges holes in the channel, and controls the channel width. Thustheconductionbetweensourceto drainismaintainedasconstant,i.e.Idisconstant.

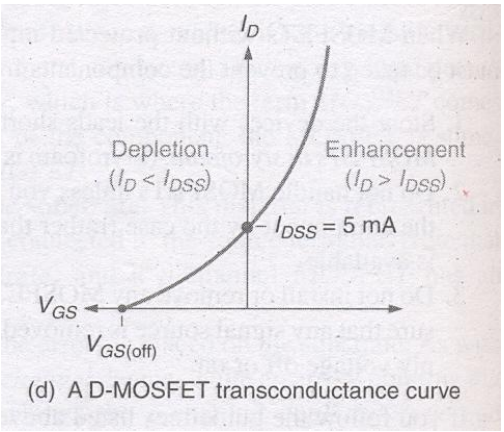
6) If Vgs>0 the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown inFig




6 MOSFET drain curves.

**TRANSFER CHARACTERISTICS:-**

The combination of 3 operating states i.e. Vgs=0V, VGs<0V, Vgs>0V is represented by the D MOSFET transconductance curve shown in Fig.




(d) A D-MOSFET transconductance curve

1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.

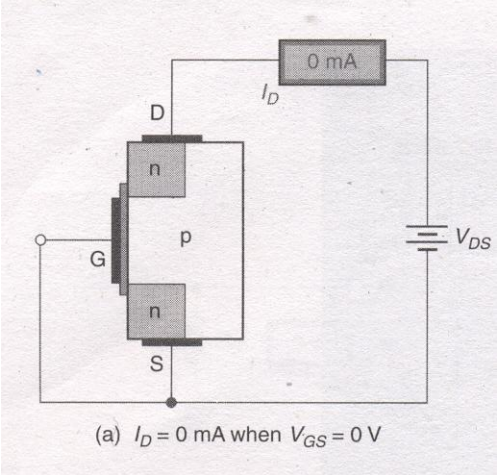
2) This curve extends for the positive values ofVgs

3) Note that Id=Idss for Vgs=0V when Vgs is negative,Id< Idss when Vgs= Vgs(off) ,Id is reduced to approximately omA.Where Vgs is positive Id>Idss.So obviously Idss is not the maximum possible value of Id for aMOSFET.

4) ThecurvesaresimilartoJFETso thettheD MOSFEThavethesametransconductance equation.

# E-MOSFETS

The E MOSFET is capable of operating only in the enhancement mode.The gate potential must be positive w.r.t to source.




1) when the value of Vgs=0V, there is no channel connecting the source and drain materials.

2) As aresult , there can be no significant amount of draincurrent.

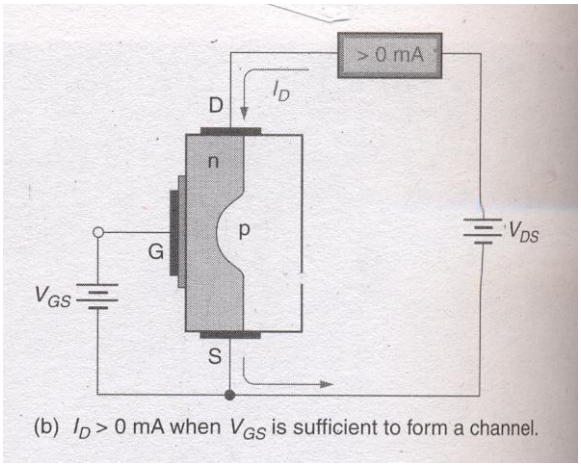
3) When Vgs=0, the Vdd supply tries to force free electrons from source to drain but the presence of p-region does not permit the electrons to pass through it. Thus there is no drain current atVgs=0,

4) If Vgs is positive, it induces a negative charge in the p type substrate just adjacent to the SIO2layer.

5) As the holes are repelled by the positive gate voltage, the minority carrier electrons attracted toward this voltage. This forms an effective N type bridge between source and drain providing a path for draincurrent.

6) This +ve gate voltage forma a channel between the source anddrain.

7) This produces a thin layer of N type channel in the P type substarate.This layer of free electrons is called N type inversionlayer.



(b) $I_D > 0$ mA when $V_{GS}$ is sufficient to form a channel.

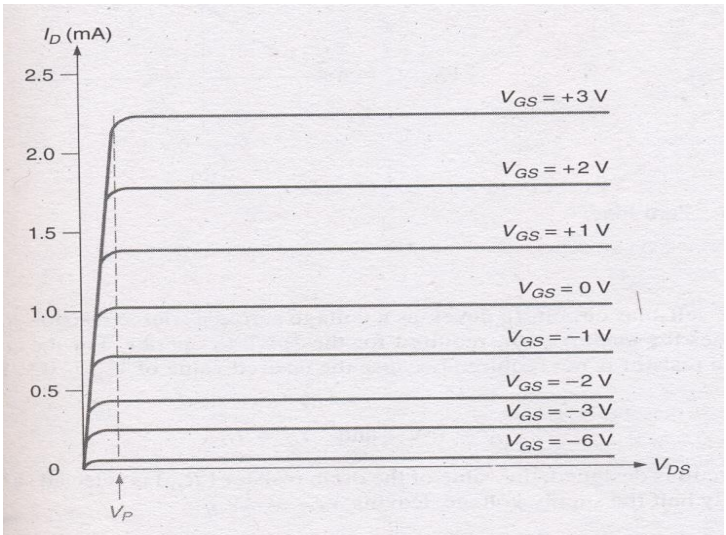
8) The minimum Vgs which produces this inversion layer is called threshold voltage and is designated by Vgs(th).This is the point at which the device turns on is called the threshold voltageVgs(th)
9) When the voltage Vgs is <Vgs (th) no current flows from drain tosource.

10) How ever when the voltage Vgs > Vgs (th) the inversion layer connects the drainto source and we get significant values ofcurrent.

## CHARACTERISTICS OF E MOSFET:-

### 1. DRAINCHARACTERISTICS

The volt ampere drain characteristics of an N-channel enhancement mode MOSFET are given in the fig.



6 MOSFET drain curves.

**2.TRANSFER CHARACTERISTICS:-**

1) The current Idss at Vgs≤ 0 is very small beinf of the order of a few nanoamps.
2) As Vgs is made +ve , the current Id increases slowly at forst, and then much more rapidly with an increase inVgs.
3) The standard transconductance formula will not work for the EMOSFET.
4) To determine the value of ID at a given value of VGs we must use the following relation

$$Id = K[V_{gs} - V_{gs(Th)}]^2$$

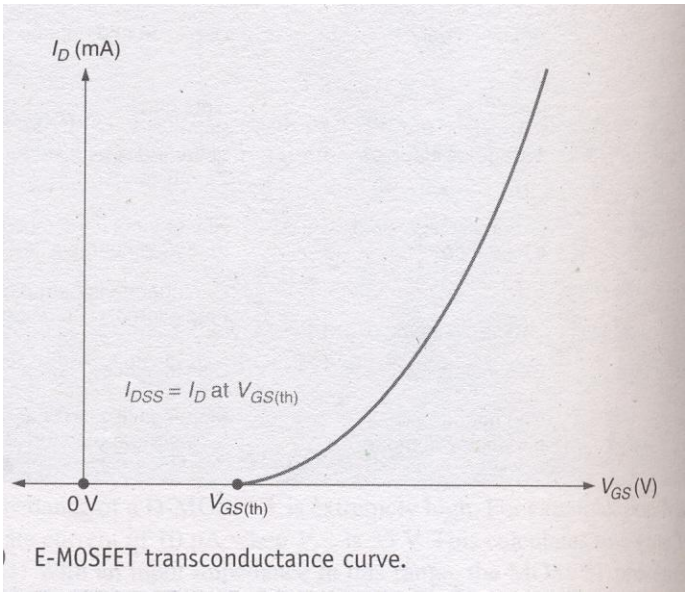
Where K is constant for the MOSFET . found as

$$K = \frac{Id(on)}{[vgs(on) - Vgs(Th)]2}$$

From the data specification sheets, the 2N7000 has the following ratings.

Id(on)= 75mA(minimum).

And Vgs(th)=0.8(minimum)



E-MOSFET transconductance curve.

# APPLICATION OFMOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave ,made up of two dc levels (or logic levels). These logic levels are 0V and+5V.

A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities , and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely ofMOSFETs.

# COMPARISON OF MOSFET WITHJFET

a. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of thechannel.

b. IntheJFETthetransverseelectricfieldacrossthe reversebiasedPNjunction controls the conductivity of thechannel.

c. The gate leakage current in a MOSFET is of the order of $10^{-12}$A. Hence the input resistance of a MOSFET is very high in the order of $10^{10}$ to $10^{15}$ Ω. The gate leakage current of a JFET is of the order of $10^{-9}$A., and its input resistance is of the order of$10^{8}$Ω.

d. The output characteristics of the JFET are flatter than those of the MOSFET, and hence the drain resistance of a JFET (0.1 to 1MΩ) is much higher than that of a MOSFET (1 to50kΩ).

e. JFETs are operated only in the depletion mode. The depletion typeMOSFET may be operated in both depletion and enhancementmode.

f. Comparing to JFET, MOSFETs are easier tofabricate.

g. Special digital CMOS circuits are available which involve near zero power dissipation and very low voltage and current requirements. This makesthem suitable for portablesystems.

# UNIJUNCTION TRANSISTOR(UJT):

Another device whose construction is similar to that of the FET is shown in the figure.

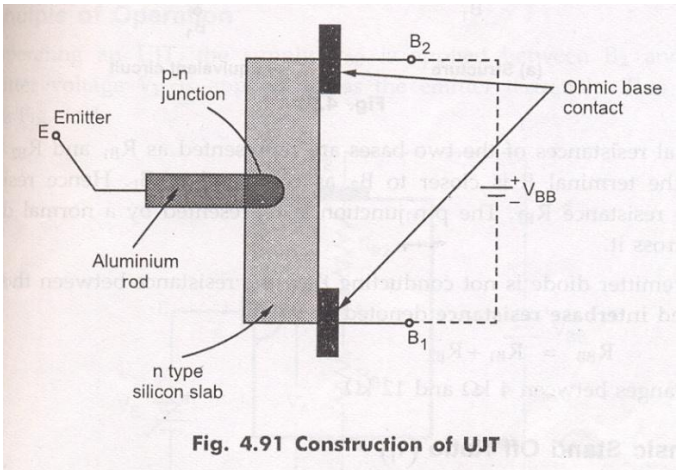


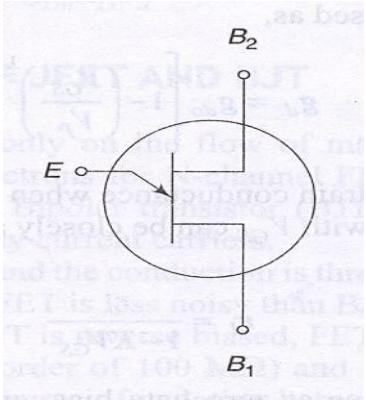

Fig. 4.91 Construction of UJT

It is a three terminal device, having two layers.It consists of a slab of lightly doped N-type silicon material. The two base contacts are attached to both ends of this N-type surface. These are denoted as B1 and B2 respectively.

A P-type material is used to form a pn junction at the boundary of the aluminium rod and N-type slab. The N-type is lightly doped while P-type is heavily doped. That is N-type provides high resistivity and P-type provides low resistivity.

This device was originally described in the literature as the double-base diode, but is now commercially available under the designation Uni Junction transistor (UJT).

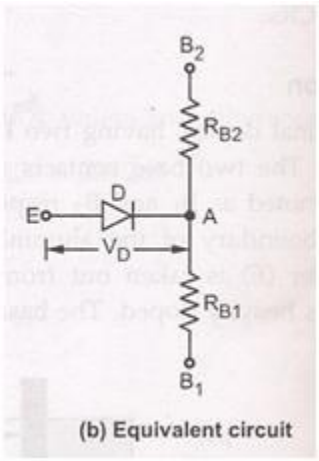
The standard symbol for this device is shown in the fig.




Here the emitter arrow is inclined and points toward B1 and This emitter arrow which is at an angle to the vertical line representing N-type material. This arrow indicates the direction of flow of conventional current when UJT is forward biased.

**EQUIVALENT CIRCUIT OF UJT**

The circuit of UJT is shown in the fig.




In the construction ,the terminal emitter is closer to $B_2$ as compared to $B_1$.

If we see the equivalent circuit of UJT, The internal resistances of the two bases are represented as $R_{b1}$and $R_{b2}$. Hence $R_{b1}$ is greater than $R_{b2}$. The pn junction is represented by a

normal diode with $V_d$ as the drop acrossit. When the emitter diode is not conducting then the resistance between the two bases $B_1$ and $B_2$is called interbase resistance denotes$R_{bb}$

$$R_{bb}=R_{b1}+R_{b2}$$

Its value ranges from 4kΩ to 12kΩ

**Intrinsic stand off ratio (η)**

Consider UJT as shown in the fig. to which supply $V_{bb}$ is connected. With $I_e=0$, That is emitter diode is not conducting ,

$$R_{bb}=R_{b1}+R_{b2}$$

Then the voltage drop across $R_{b1}$ can be obtained by using potential divider rule.

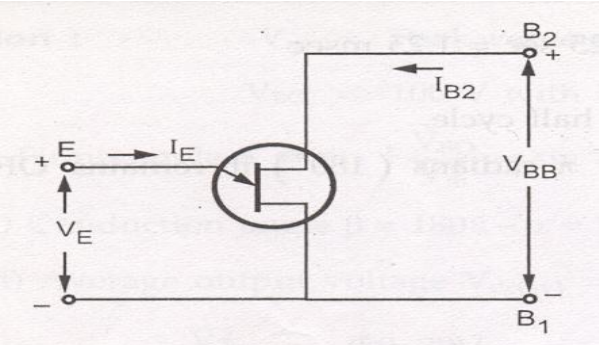
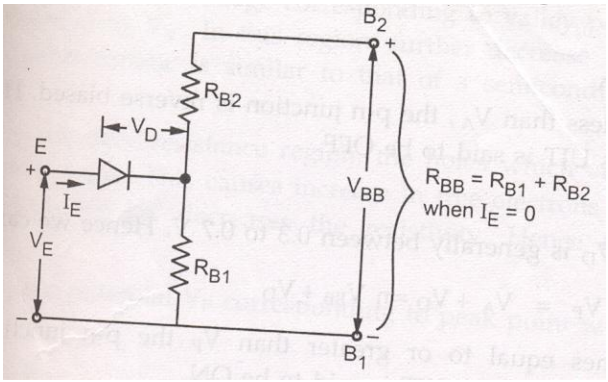



**Fig. 4.91(a) Symbol of UJT**

Replacing with its equivalent circuit




$R_{bb}=R_{b1}+R_{b2}$

When $I_e=0$

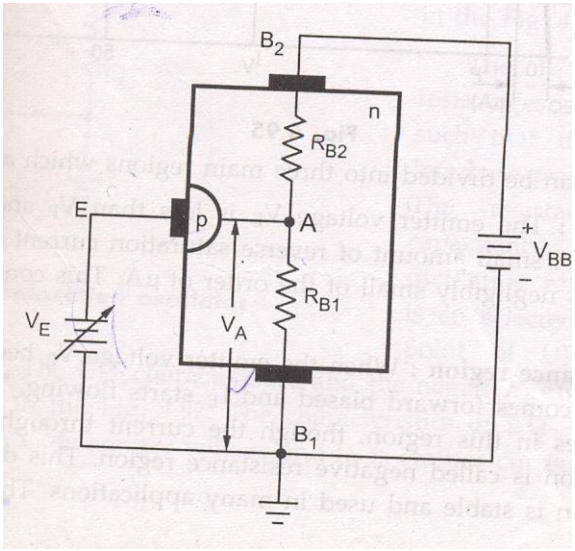
$V_{RB1}=\left(\frac{RB1}{RB1+RB2}\right) V_{BB} = \eta.V_{BB}$ When$I_e=0$

η = Intrinsic stand offratio= $\left(\frac{RB1}{RB1+RB2}\right)$ when Ie=0

$\eta = (\frac{RB1}{RBB})$ when $I_e=0$

The value of η is from 0.5 to 0.8 the voltage $V_{rb1}$ is called intrinsic stand off voltage, because it keeps the emitter diode reverse biased for all emitter voltages less than $V_{rb1}$.

**Operation**




1.The supply $V_{bb}$ is applied between $B_2$ and $B_1$.

2. Variable emitter voltage $V_e$ is applied across the emitterterminals.

3. If $V_e$ is varied , potential of A is decided by η and is equal to $\eta V_{bb}$

$$V_a = V_{rb1} = \eta V_{bb}$$

Case 1: If $V_e < V_a$

As long as $V_e < V_a$, the pn junction is reverse biased. Hence emitter current $I_e$ will not flow. Thus UJT is said to be off.

Case 2: if $V_e > V_p$

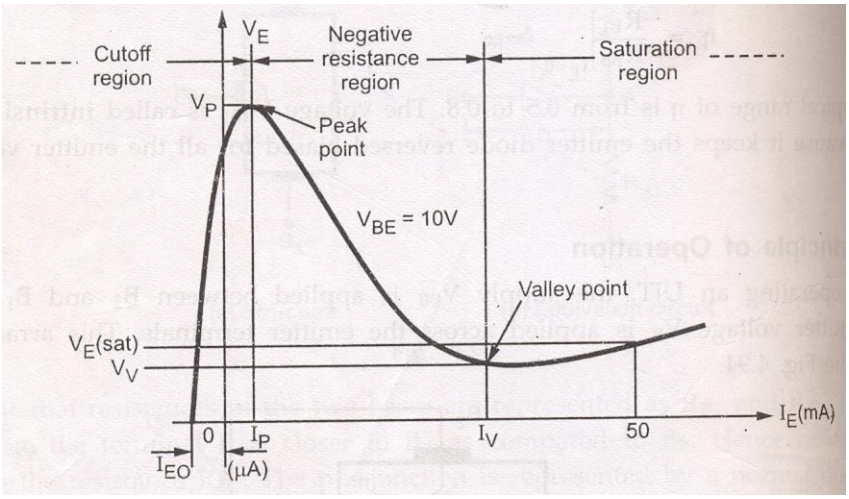
The diode drop $V_d$ is generally between 0.3 to 0.7v.

We can write $V_p = V_a + V_d = \eta V_{bb} + V_d$

When $V_e$ becomes equal to or greater than $V_p$ the pn junction becomes forward biased and current $I_e$ flows. Thus UJT is said to be ON.

**VI Characteristics**

1.The graph of $I_e$ against emitter voltage plotted for a particular value of $V_{bb}$ is called the characteristics of UJT.




The characteristics can be divided in to three main regions.

1.cutoff 2. Negative resistance region 3. Saturationregion.

1.cut off: The $V_e < V_p$ and the pn junction is reverse biased . A small amount of reverse saturation current $I_{e0}$ flows through the device which is negligibly small of the order of micro amps. This condition remains till the peakpoint.

2. Negative resistance region: When emitter voltage $V_e$becomes equal to $V_p$ then p n junction becomes forward biased and $I_e$starts flowing. The voltage across the device decreases in this region though the current through the device increases. Hence the region is called negative resistance region. This decreases the resistance $R_{b1}$. This region is stable and used in many applications. This region continues till valleypoint.

3. Saturation region: The region to the right of the valley point is called saturation region. In the valley point, the resistance changes from negative to positive. The resistance remains positive in the saturationregion.

As $V_{bb}$ increases , the potential $V_p$ corresponding to peak point will increase.

## Applications of UJT

The UJT is mainly used in the triggering of other devices such as SCR. It is also used in the sawtooth wave generators and some timing circuits. The most popular application of UJT is as a relaxation oscillator to obtain short pulses for triggering ofSCRs.

The relaxation oscillator using UJT which is ment for generating sawtooth waveform. It consists of a UJT and a capacitor , which is charged through emitter resistor as the supply voltage $V_{bb}$ is switched 0N.

# UNIT IV

# BIASING AND COMPENSATION TECHNIQUES

## NEED FOR TRANSISTORBIASING:

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region . To establish an operating point (proper values of collector current $I_c$and collector to emitter voltage $V_{CE}$) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasingckt.

There are four conditions to be met by a transistor so that it acts as a faithful ampr:

1) Emitter base junction must be forward biased ($V_{BE}$=0.7Vfor Si, 0.2V for Ge) and collector base junction must be reverse biased for all levels of i/psignal.
2) $V_{ce}$ voltage should not fall below $V_{CE(sat)}$ (0.3V for Si, 0.1V for Ge) for any part of the i/p signal.For$V_{CE}$lessthan$V_{CE(sat)}$thecollectorbasejunctionisnotprobablyreversebiased.
3) The value of the signal $I_c$ when no signal is applied should be at least equal to the max. collector current t due to signalalone.
4) Max. rating of the transistor $I_{c(max)}$, $V_{CE(max)}$ and $P_{D(max)}$ should not be exceeded at any value of i/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, $I_c$=0, $V_{CE}$ =0. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region .It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents

Hence operating point for a transistor amplifier is selected to be in the middle of active region.

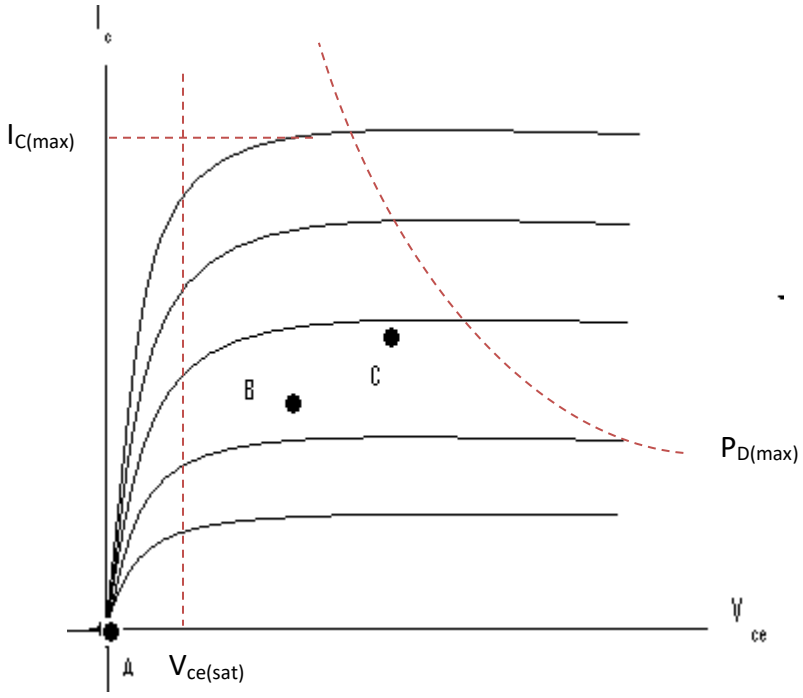



**fig1**

## DC LOADLINE:

Referring to the biasing circuit of fig 4.2a, the values of $V_{CC}$ and $R_C$ are fixed and Ic and $V_{CE}$ are dependent on$R_B$.

Applying Kirchhoff's voltage law to the collector circuit in fig. 4.2a, we get

$$Vcc = IcRc + Vce$$

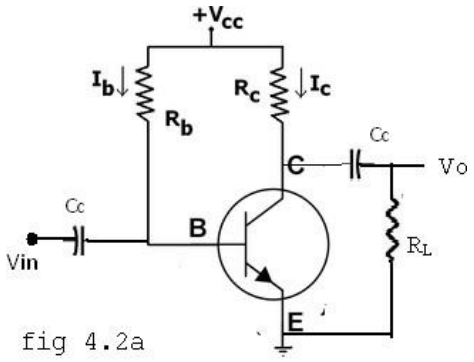



fig 4.2a

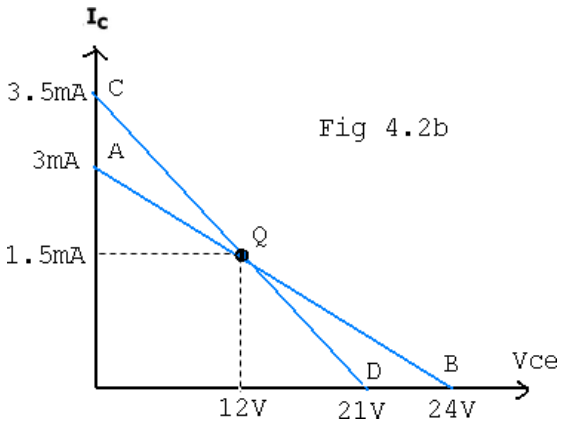



Fig 4.2b

The straight line represented by AB in fig4.2b is called the dc load line. The coordinates of the end point A are obtained by substituting $V_{CE}$ =0 in the above equation. Then $Ic = \frac{Vcc}{Rc}$. Therefore The coordinates of A are $V_{CE}$ =0 and $Ic = \frac{Vcc}{Rc}$.

The coordinates of B are obtained by substituting Ic=0 in the above equation. Then Vce = Vcc. Therefore the coordinates of B are $V_{CE}$ =Vcc and Ic=0. Thus the dc load line AB can be drawn if the values of Rc and Vcc areknown.

As shown in the fig4.2b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

1) Reverse saturation current, Ico, which doubles for every 10°C raise intemperature
2) Base emitter Voltage ,VBE, which decreases by 2.5 mV per°C
3) Transistor current gain, $h_{FE}$ or β which increases withtemperature.

If base current $I_B$ is kept constant since $I_B$is approximately equal to Vcc/RB. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current Ic for a given $I_B$. Hence , in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completelyunsatisfactory.

## AC LOADLINE:

Afterdrawingthedcloadline,theoperatingpointQisproperlylocatedatthecenterof the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pas through the operating point Q. The effective ac load resistance $R_{ac}$, is a combination of $R_C$ parallel to$R_L$i.e. $R_{ac} = R_L \,||\, R_C$. So the slope of theac

load line CQDwillbe $\left(\frac{-1}{R_{ac}}\right)$. To draw the ac load line, two end points, I.e. $V_{CE(max)}$ and $I_{C(max)}$ when the signal is applied arerequired.

$V_{CE(\max)} = V_{CEQ} + I_{CQ}R_{ac}$, which locates point D on theVceaxis.

$I_{c(\max))} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C on the $I_C$axis.

By joining points c and D, ac load line CD is constructed. As $R_C > R_{ac}$, The dc load line is less steep than ac load line.

## STABILITY FACTOR(S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, $I_C$ also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which $I_C$ is stabilized with varying $I_C$ is measured by a stability factor S

$$S = \frac{\partial I_c}{\partial I_{co}} \approx \frac{dI_c}{dI_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}}, \quad \beta \text{ and } I_B \text{ constant}$$

ForCEconfiguration$I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiate the above equation w.r.t $I_C$ , Weget

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{dI_{co}}{dI_c}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\therefore S = \frac{1+\beta}{1-\beta\frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

**Stability factor S' and S'':**

S' is defined as the rate of change of $I_C$ with $V_{BE}$, keeping $I_C$ and $V_{BE}$constant.

$$S' = \frac{\partial I_c}{\partial V_{BE}}$$

S'' is defined as the rate of change of $I_C$ with β, keeping $I_{CO}$ and $V_{BE}$constant.

$$S'' = \frac{\partial I_c}{\partial \beta}$$

## METHODS OF TRANSISTORBIASING:

### 1) Fixed bias (base bias)

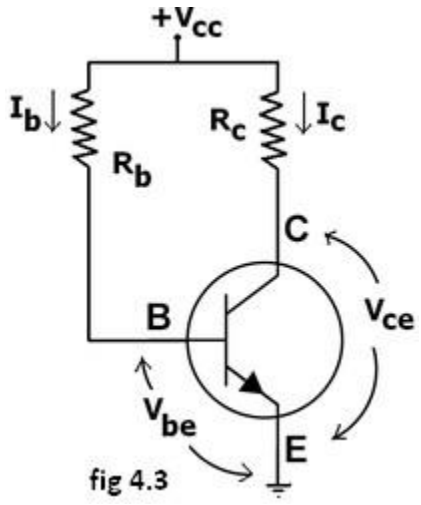


fig 4.3

This form of biasing is also called *base bias*. In the fig 4.3 shown, the single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$V_{cc} = I_B R_B + V_{be}$

Therefore, $I_B = (V_{cc} - V_{be})/R_B$

Since the equation is independent of current $I_CR$, $dI_{B/}/dI_CR = 0$ and the stability factor is given by the equation….. reduces to

$$S=1+\beta$$

Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used for biasing.

For a given transistor, $V_{be}$ does not vary significantly during use. As $V_{cc}$ is of fixed value, on selection of $R_B$, the base current $I_B$ is fixed. Therefore this type is called *fixed bias* type of circuit.

Also for given circuit, $V_{cc} = I_CR_C + V_{ce}$

Therefore, $V_{ce} = V_{cc} - I_CR_C$

**Merits:**

- Itissimpletoshifttheoperatingpointanywhereintheactiveregionbymerely changing the base resistor($R_B$).
- A very small number of components arerequired.

**Demerits:**

- Thecollectorcurrentdoesnotremainconstantwithvariationintemperature or power supply voltage. Therefore the operating point isunstable.
- Changes in $V_{be}$ will change $I_B$ and thus cause $R_E$ to change. This in turn will alter the gain of thestage.
- When the transistor is replaced with another one, considerable change inthe value of β can be expected. Due to this change the operating point willshift.

## 2) EMITTER-FEEDBACKBIAS:

The emitter feedback bias circuit is shown in the fig 4.4. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

$V_{Rb} = V_{CC} - I_eR_e - V_{be}$.

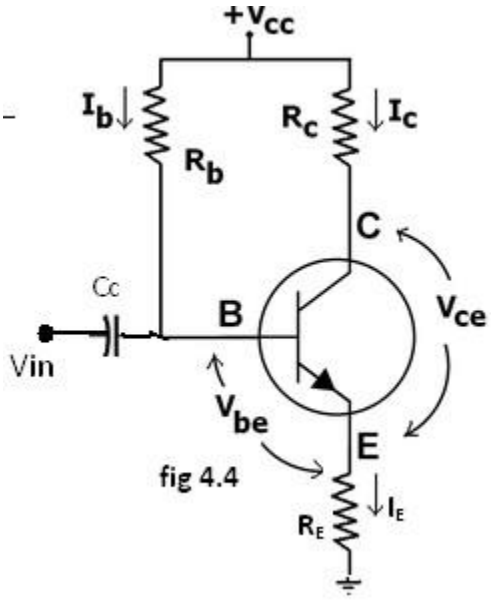


fig 4.4

From Ohm's law, the base current is

$I_b = V_{Rb} / R_b$.

The way feedback controls the bias point is as follows. If $V_{be}$ is held constant and temperature increases, emitter current increases. However, a larger $I_e$ increases the emitter voltage $V_e = I_eR_e$, which in turn reduces the voltage $V_{Rb}$ across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because $I_c = ß\ I_B$. Collector current and emitter current are related by $I_c = \alpha\ I_e$ with $\alpha \approx 1$, so increase in emitter current with temperature is opposed, and operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in $I_C$ (corresponding to change in β-value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

$I_B = (V_{CC} - V_{be})/(R_B + (\beta+1)R_E)$.

**Merits:**

The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

**Demerits:**

- In this circuit, to keep $I_C$ independent of β the following condition must bemet:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if ( β + 1 )$R_E$>> $R_B$.

- Asβ-valueisfixedforagiventransistor,thisrelationcan besatisfiedeitherby keeping $R_E$ very large, or making $R_B$ verylow.

- If $R_E$ is of large value, high $V_{CC}$ is necessary. This increases cost as well as precautions necessary whilehandling.
- If $R_B$ is low, a separate low voltage supply should be used in the basecircuit. Using two supplies of different voltages isimpractical.

- In addition to the above, $R_E$ causes ac feedback which reduces the voltage gainof theamplifier.

## 3) COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:

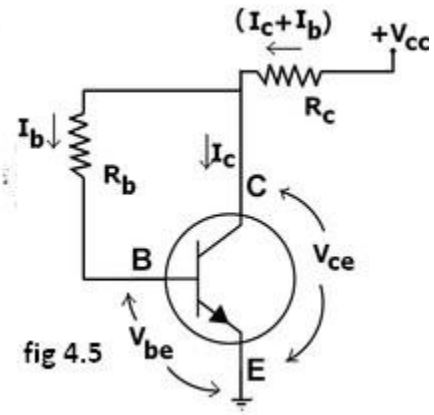


fig 4.5

This configuration shown in fig 4.5 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor $R_B$ is connected to the collector instead of connecting it to the DC source $V_{cc}$. So any thermal runaway will induce a voltage drop across the $R_C$ resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage $V_{R_b}$across the base resistor $R_b$is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}} .$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, andso

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current $I_b$ is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If $V_{be}$ is held constant and temperature increases, then the collector current $I_c$ increases. However, a larger $I_c$ causes the voltage drop across resistor $R_c$ to increase, which in turn reduces the voltage $V_{R_b}$across the base resistor $R_b$. A lower base-resistor voltage drop reduces the base current $I_b$, which results in less collector current $I_c$. Because an increase in collector current with temperature is opposed, the operating point is keptstable.

**Merits:**

- Circuit stabilizes the operating point against variations in temperature and β(i.e. replacement oftransistor)

**Demerits:**

- In this circuit, to keep $I_c$ independent of β, the following condition must bemet:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$$\beta R_c \gg R_b.$$

- As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping $R_c$ fairly large or making $R_b$ verylow.

- If $R_c$ is large, a high $V_{cc}$ is necessary, which increases cost as well as precautions necessary whilehandling.
- If $R_b$ is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in activemode.

- The resistor $R_b$ causes an AC feedback, reducing thevoltage gainof the amplifier. This undesirable effect is a trade-off for greaterQ-pointstability.

**Usage:** The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

## 4) COLLECTOR –EMITTER FEEDBACKBIAS:

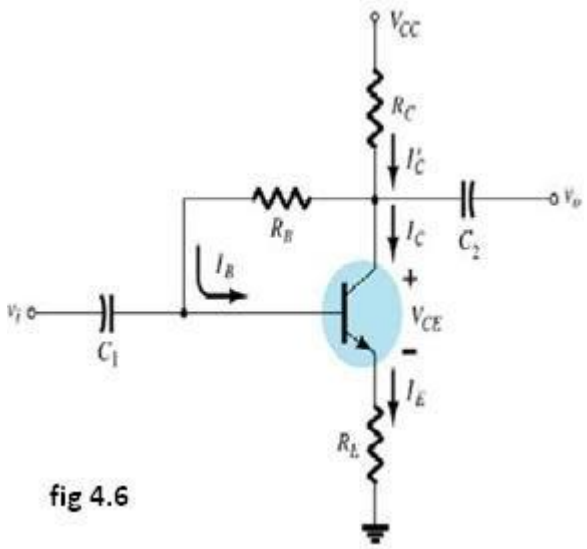



fig 4.6

The above fig4.6 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is provided by connecting an emitter Re from emitter to ground. Both feed backs are used to

control collector current and base current IB in the opposite direction to increase the stability as compared to the previous biasingcircuits.

## 5) VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTERBIAS:

The voltage divider as shown in the fig 4.7 is formed using external resistors $R_1$ and $R_2$. The voltage across $R_2$ forward biases the emitter junction. By proper selection of resistors $R_1$and $R_2$, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitterresistor.

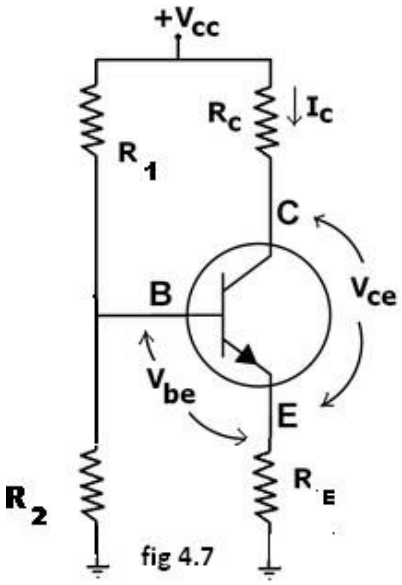


fig 4.7

In this circuit the base voltage is given by:

$$V_B = \text{voltageacross } R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1+R_2)} \text{ provided } I_B << I_2 = V_B/R_2.$$

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$
$$V_2 = \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$
$$V_2 = V_{BE} + I_E R_E$$
$$I_E = \frac{V_2 - V_{BE}}{R_E}$$
$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \because I_C \cong I_E$$
$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of ? thus the stability is excellent. In all practical cases the value of VBE is quite small in comparison to the V2, so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellentstability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$
$$\because I_C \cong I_E$$
$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1+\beta)(R_{eq}+R_E)}{R_{eq}+R_E(1+\beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1+\beta)\left(1+\frac{R_{eq}}{R_E}\right)}{\frac{R_{eq}}{R_E}+1+\beta}$$

If Req/RE is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1+\beta}{1+\beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since Req/RE cannot be ignored as compared to 1.

**Merits:**

- Unlike above circuits, only one dc supply isnecessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift intemperature.

**Demerits:**

- In this circuit, to keep $I_C$ independent of β the following condition must bemet:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the caseif $(\beta+1)R_E >> R_1 \parallel R_2$

where $R_1$ || $R_2$ denotes the equivalent resistance of $R_1$ and $R_2$ connected in parallel.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping $R_E$ fairly large, or making $R_1||R_2$ very low.

- If $R_E$ is of large value, high $V_{CC}$ is necessary. This increases cost as well as precautions necessary whilehandling.
- If $R_1$ || $R_2$ is low, either $R_1$ is low, or $R_2$ is low, or both are low. A low $R_1$ raises $V_B$ closer to $V_C$, reducing the available swing in collector voltage, and limiting how large $R_C$can be made without driving the transistor out of active mode. A low $R_2$lowers $V_{be}$, reducingthe

allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.

- AC as well as DC feedback is caused by $R_E$, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussedbelow.

**Usage:** The circuit's stability and merits as above make it widely used for linear circuits.

## BIAS COMPENSATION USING DIODE ANDTRANSISTOR:

The various biasing circuits considered use some type of negative feedback to stabilize the operation point. Also, diodes, thermistors and sensistors can be used to compensate for variations in current.

### DIODE COMPENSATION:

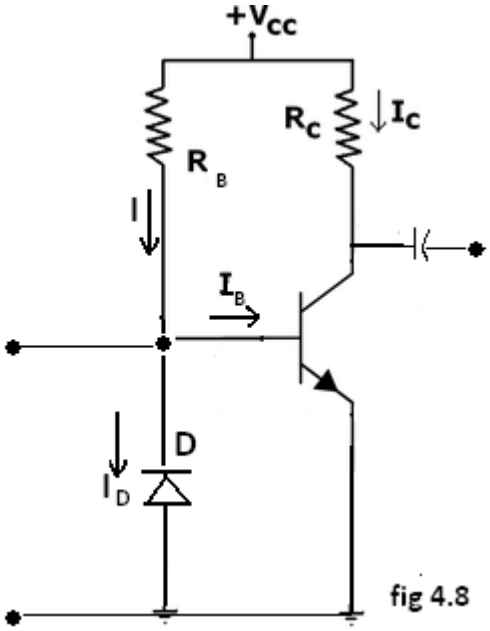



fig 4.8

The following fig4.8 shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in collector saturation current $I_{CO}$. The diode is of the same material as the transistor and it is reverse biased by e the emitter-base junction

voltage $V_{BE}$, allowing the diode reverse saturation current $I_O$ to flow through diode D. The base current $I_B$=I-$I_O$.

As long as temperature is constant, diode D operates as a resistor. As the temperature increases, $I_{CO}$ of the transistor increases. Hence, to compensate for this, the base current $I_B$ should be decreased.

The increase in temperature will also cause the leakage current $I_O$ through D to increase and thereby decrease the base current $I_B$. This is the required action to keep Ic constant.

This type of bias compensation does not need a change in Ic to effect the change in $I_C$, as both $I_O$ and $I_{CO}$ can track almost equally according to the change in temperature.

## THERMISTOR COMPENSATION:

The following fig4.9 a thermistor $R_T$, having a negative temperature coefficient is connected in parallel with $R_2$. The resistance of thermistor decreases exponentially with increase of temperature. An increase of temperature will decrease the base voltage $V_{BE}$, reducing $I_B$ and$I_C$.

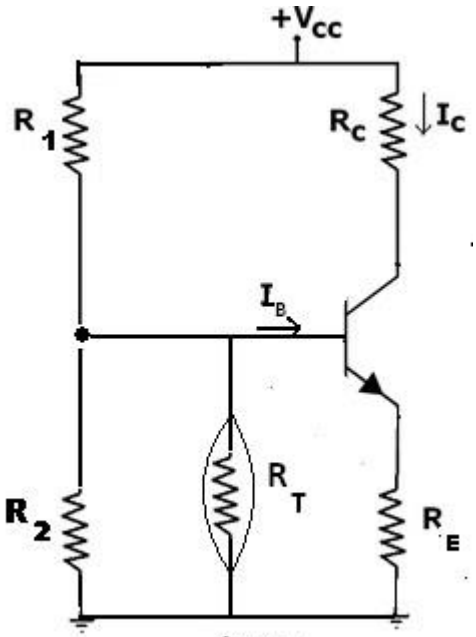



fig 4.9

## SENSISTOR COMPENSATION:

In the following fig4.10 shown a sensistor Rs having a positive temperature coefficient is connected across $R_1$ or $R_E$. Rs increases with temperature. As the temperature increases, the equivalent resistance of the parallel combination of R1 and Rs also increases and hence $V_{BE}$

decreases, reducing $I_B$ and Ic. This reduced Ic compensates for increased Ic caused by the increase in $V_{BE}$, $I_{CO}$ and β due to temperature.

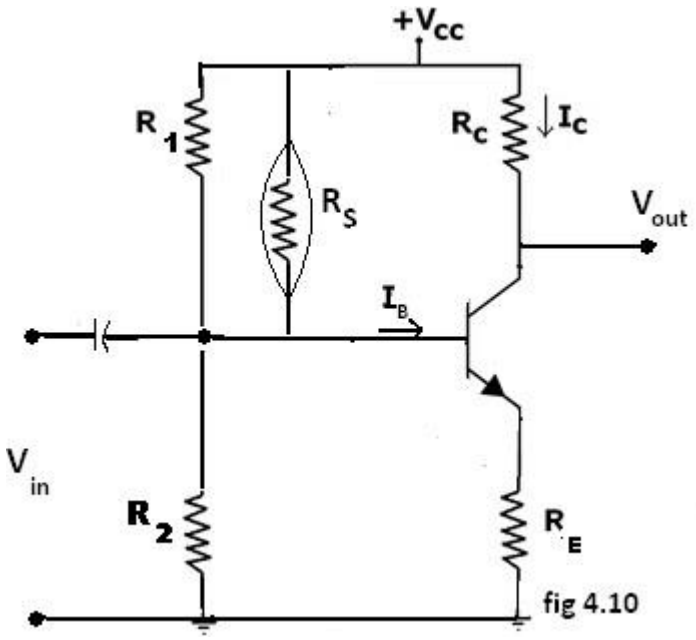



fig 4.10

## THERMAL RUNAWAY AND THERMALSTABILITY:

### THERMAL RUNAWAY:

The collector current for the CE circuit is given by $I_C = \beta I_B + (1+\beta)I_{CO}$.The three variables in the equation, β, $I_B$, and $I_{CO}$increases with rise in temperature. In particular, the reverse saturation current or leakage current $I_{CO}$changes greatly with temperature. Specifically itdoublesforevery10°Criseintemperature.Thecollectorcurrentcausesthecollectorbase junction temperature to rise which in turn, increase $I_{CO}$, as a result $I_C$will increase still further, which will further rise the temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to *"thermal runaway"*. Consequently, the ratings of the transistor are exceeded which may destroy the transistoritself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current $I_B$ is made to decrease automatically with rise in temperature, then the decrease in $\beta I_B$ will compensate for increaseinthe $(1+\beta)I_{CO}$ , keeping $I_C$almostconstant.

## THERMAL RESISTANCE

Consider transistor used in a circuit where the ambient temperature of the air around the transistor is $T_A{}^oC$ and the temperature of the collector-base junction of the transistor is $T_J{}^oC$.

Due to heating within the transistor $T_J$ is higher than $T_A$. As the temperature difference $T_J$- $T_A$ is greater,thepowerdissipatedinthetransistor,$P_D$willbegreater,i.e,$T_J$-$T_A$ $\propto P_D$

The equation can be written as $T_J$- $T_A = \Theta P_D$. , where $\Theta$is the constant of proportionality and is called the Thermal resistance. Rearranging the above equation $\Theta = T_J - T_A / P_D$. Hence $\Theta$is measured in $^oC/W$ which may be as small as 0.2 $^oC/W$ for a high power transistor that has an efficient heat sink or up to $1000^oC/W$ for small signal, low power transistor which have no coolingprovision.

As Θ represents total thermal resistance from a transistor junction to the ambient temperature, it is referred to as $\Theta_{J-A}$. However, for power transistors, thermal resistance is given form junction to case,$\Theta_{J-C}$.

The amount resistance from junction to ambience is considered to consist of 2 parts.

$$\Theta_{J-A} = \Theta_{J-C} - \Theta_{C-A}.$$

Which indicates the heat dissipated in the junction must make its way to the surrounding air through two series paths from junction to case and from case to air. Hence the power dissipated.

$$P_D=(T_J-T_A)/\Theta_{J-A}$$

$$=(T_J-T_A)/(\Theta_{J-C}+\Theta_{C-A})$$

$\Theta_{J-C}$ is determined by the type of manufacture of the transistor and how it is located I the case, but $\Theta_{C-A}$ is determined by the surface area of the case or flange and its contact with air. If the effective surface area of the transistor case could be increased, the resistance to heat flows, or could be increased $\Theta_{C-A}$, could be decreased. This can be achieved by the use of a heat sink.

The heat sink is a relatively large, finned, usually black metallic heat conducting device in close contact with transistor case or flange. Many versions of heat sink exist depending upon the shape and size of the transistor. Larger the heat sink smaller is the thermal resistance $\Theta_{HS-A}$.

This thermal resistance is not added to $\Theta_{C-A}$ in series, but is instead in parallel with it and if

$\Theta_{HS-A}$ is much less than $\Theta_{C-A}$, then $\Theta_{C-A}$ will be reduced significantly, thereby improving the dissipation capability of the transistor. Thus

$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} || \Theta_{HS-A}$.

## CONDITION FOR THERMALSTABILITY:

For preventing thermal runaway, the required condition I the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition. Hence the condition to be satisfied to avoid thermal runaway is given by

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\Theta}$$

If the circuit is properly designed, then the transistor cannot runaway below a specified ambient temperature or even under any conditions.

In the self biased circuit the transistor is biased in the active region. The power generated at the junction without any signal is

$$P_C = I_C V_{CB} \approx I_C V_{CE}$$

Let us assume that the quiescent collector and the emitter currents are equal. Then

$$P_C = I_C V_{CC} - I_C^2 (R_E + R_C) \quad \text{.....(1)}$$

The condition to prevent thermal runaway can be writtenas

$$\frac{\partial P_C}{\partial I_C}\frac{\partial I_C}{\partial T_j} < \frac{1}{\Theta} \quad \text{.....(2)}$$

As Θ and $\frac{\partial I_C}{\partial T_j}$ are positive, $\frac{\partial P_C}{\partial I_C}$ should be negative in order to satisfy the above condition.

Differentiating equation (1) w.r.t $I_C$ weget

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C (R_E + R_C) \quad \text{.....(3)}$$

Hence to avoid thermal runaway it is necessary that

$$I_C > \frac{V_{CC}}{2(R_E + R_C)} \quad \text{.....(4)}$$

SinceVCE=VCC-IC(RE+RC) then eq(4) implies that VCE<VCC/2. IF the inequality of eq(4) is not satisfied and VCE<VCC/2, then from eq(3), $\frac{\partial P_C}{\partial I_C}$is positive., and the corresponding eq(2) should be satisfied. Other wise thermal runaway willoccur.

## BIASING FET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage $V_{GS}$ and drain current $I_D$ which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuitsThe main difference between JFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

1) Selfbias
2) Voltage dividerbias.

## SELFBIAS

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate. A self bias circuit is shown in the fig. Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative $V_{GS}$ for an N channel JFET and a positive $V_{GS}$ for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig. The gate resistor $R_G$ doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V .$R_G$ is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor $R_S$ makes gate source junction reverse biased.

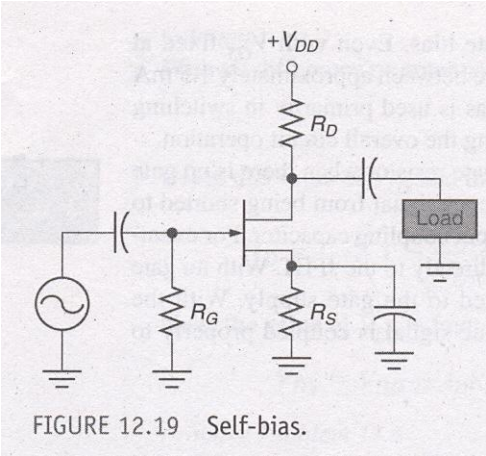


FIGURE 12.19 Self-bias.

For the dc analysis coupling capacitors are open circuits.

For the N channel FET in Fig (a)

$I_S$ produces a voltage drop across $R_S$ and makes the source positive w.r.t ground. In any JFET circuit all the source current passes through the device to the drain circuit .This is due to the fact that there is no significant gatecurrent.

We can define source current as $I_S = I_D$

($V_G$ =0 because there is no gate current flowing in $R_G$ So $V_G$ across $R_G$ is zero)

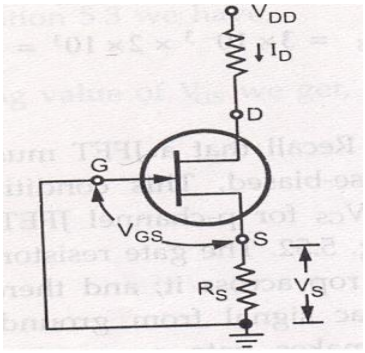
$V_G$ =0 then $V_S = I_S R_S = I_D R_S$

$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$

**DC analysis of self Bias:-**

In the following DC analysis, the N channel J FET shown in the fig. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor $R_G$ by a short circuit equivalent.:. $I_G$ = 0.The relation between $I_D$ and $V_{GS}$ is given by




$$Id = Idss\left[1 - \frac{Vgs}{Vp}\right]^2$$

$V_{GS}$ for N channel JFET is =-id Rs

Substuting this value in the above equation

$$Id = Idss\left[1 - \frac{(-IdRs)}{Vp}\right]^2$$

$$Id = Idss\left[1 + \frac{(IdRs)}{Vp}\right]^2$$

For the N-chanel FET in the above figure

Is produces a voltage drop across Rs and makes the source positive w.r.t ground in any JFET circuit all the sourcecurrent passesthroughthedevicetodraincircuitthisisduetothefactthatthereisnosignificant gate current. Therefore we can define source current as Is=Id and Vg=0then

Vs= Is Rs =IdRs

Vgs=Vg-Vs=0-IdRs=-IdRs

**Drawing the self biasline:-**

Typical transfer characteristics for a self biased JFET are shown in the fig.

The maximum drain current is 6mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

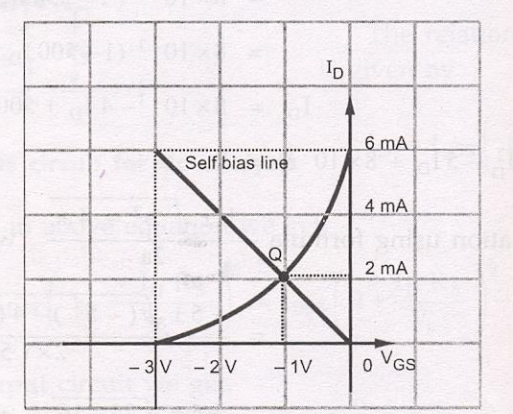



**Fig. 5.55 Transfer characteristics**

Now using the equation $V_{GS} = -I_D R_S$ and assuming $R_S$ of any suitable value we can draw the self bias line.

Let us assume RS = 500Ω

With this Rs , we can plot two points corresponding to $I_D = 0$ and Id = $I_{DSS}$

for $I_D = 0$

$V_{GS} = -I_D R_S$

$V_{GS} = 0X (500.Ω) = 0V$

So the first point is (0 ,0)

( $I_d$, $V_{GS}$)

For $I_D = I_{DSS} = 6mA$

$V_{GS} = (-6mA)(500\ \Omega) = -3V$

So the 2nd Point will be (6mA,-3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line.The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point , the $I_D$ is slightly > than 2mA and $V_{GS}$ is slightly > -1V. The Q point for the self bias JFET depends on the value of Rs.If Rs is large, Q point far down on the transconductance curve ,$I_D$ is small, when Rs is small Q point is far up on the curve , $I_D$ is large.

## VOLTAGE DIVIDERBIAS:-

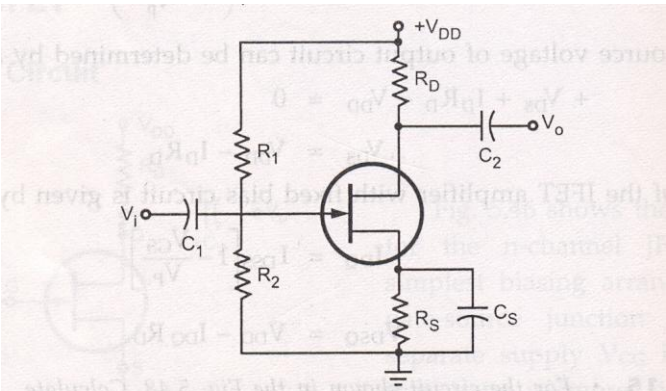



**Fig. 5.49 Voltage divider bias for n-channel JFET**

The fig. shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltageis

$V_S = I_D R_S$

The gate voltage is set by resistors R1 and R2 as expressed by the following equation using the voltage divider formula.

$$Vg=\left(\frac{R2}{(R1+R2)}\right)Vdd$$

For dc analysis

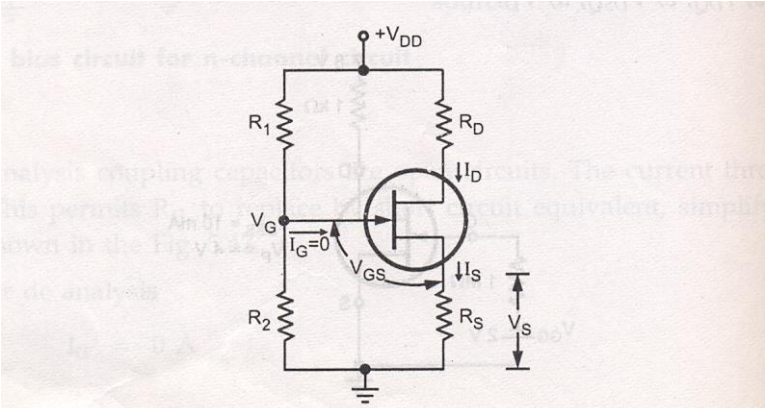



**Fig. 5.50 Simplified voltage divider circuit for dc analysis**

Applying KVL to the input circuit

$V_G - V_{GS} - V_S = 0$

$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$

$V_{GS} = V_G - I_D R_S \quad \because I_S = I_D$

Applying KVL to the input circuit we get

$V_{DS} + I_D R_D + V_S - V_{DD} = 0$

$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$

$V_{DS} = V_{DD} - I_D ( R_D + R_S )$

The Q point of a JFET amplifier , using the voltage divider biasis

$I_{DQ} = I_{DSS}[1 - V_{GS}/V_P]2$

$V_{DSQ} = V_{DD} - I_D ( R_D + R_S)$

# UNIT V

# BJT AND FET AMPLIFIERS

## 5.0 Introduction

characteristics of an active device such as BJT are non-linear. The analysis of a non-linear device is complex. Thus to simplify the analysis of the BJT, its operation is restricted to the linear V-I characteristics around the Q-point i.e. in the active region. This approximation ispossible only with small input signals. With small input signals transistor can be replaced with small signal linear model. This model is also called small signal equivalentcircuit.

## 5..1Two –Port Devices and Network Parameters

**Small signal low frequency transistor Models:**

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

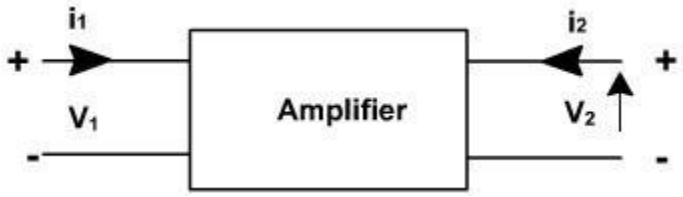



**Fig. 1**

A two-port network is represented by four external variables: voltage $V_1$ and current $I_1$ at the input port, and voltage $V_2$ and current $I_2$ at the output port, so that the two-port network can be treated as a black box modeled by the relationships between the four variables,$V_1$,$V_2$, $I_1$,$I_2$ . Out of four variables two can be selected as are independent variables and two are dependent variables.The dependent variables can be expressed interns of independent variables. This leads to various two port parameters out of which the following three areimportant:

1. Impedance parameters (z-parameters)
2. Admittance parameters (y-parameters)
3. Hybrid parameters(h-parameters)

## z-parameters

A two-port network can be described by z-parameters as

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Where

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0}$$

Input impedance with output port open circuited

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

Reverse transfer impedance with input port open circuited

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0}$$

Forward transfer impedance with output port open circuited

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}$$

Output impedance with input port open circuited

## Y-parameters

A two-port network can be described by Y-parameters as

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0}$$

Input admittance with output port short circuited

$$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0}$$

Reverse transfer admittance with input port short circuited

$$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0}$$

Forward transfer admittance with output port short circuited

$$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0}$$

Output admittance with input port short circuited

## Hybrid parameters(h-parameters)

If the input current I1 and output voltage V2 are taken as independent variables, the dependent variables V1 and I2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Where $h_{11}$, $h_{12}$, $h_{21}$, $h_{22}$ are called as hybrid parameters.

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0}$$

Input impedence with o/p port short circuited

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$$

Forward voltage transfer ratio with o/p port short circuited

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

**output impedence with i/p port open circuited**

# THE HYBRID MODEL FOR TWO PORTNETWORK:

Based on the definition of hybrid parameters the mathematical model for two pert networks known as h-parameter model can be developed. The hybrid equations can be written as:

$V_1 = h_i I_1 + h_r V_2$

$I_2 = h_f I_1 + h_o V_2$

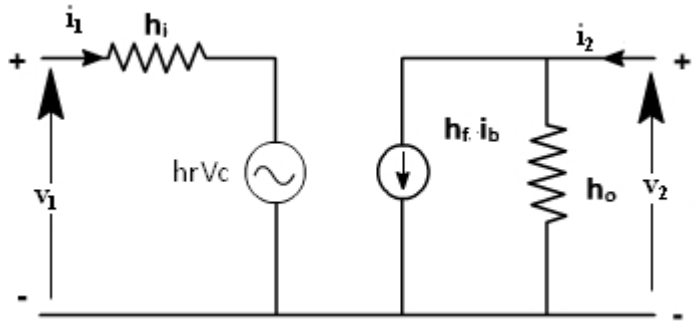
(The following convenient alternative subscript notation is recommended by the **IEEE Standards**:

***i*=11=input** ***o* = 22 =output**

***f* =21 = forward transfer *r* = 12 = reverse transfer)**

We may now use the four h parameters to construct a mathematical model of the device of Fig.(1). The hybrid circuit for any device indicated in Fig.(2). We can verify that the model of Fig.(2) satisfies above equations by writing Kirchhoff'svoltage and current laws for inputand

output ports.




If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. $h_{fe}$ ,$h_{ib}$ are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in **fig. 2**.

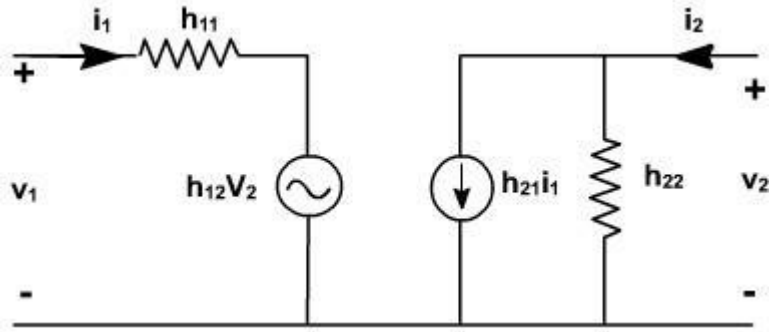



Fig. 2

## 5.2.1 TRANSISTOR HYBRID MODEL:

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in fig. 3. The variables, $i_B$, $i_C$ ,$v_C$, and $v_B$ represent total instantaneous currents and voltages $i_B$ and $v_C$ can be taken as independent variables and $v_B$, $I_C$ as dependent variables.

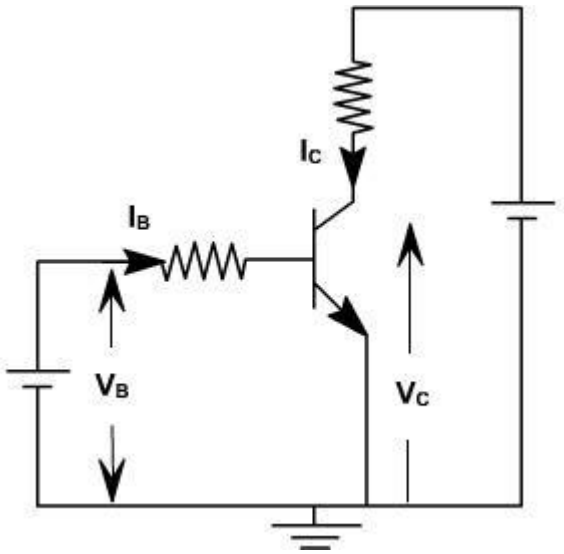



Fig. 3

$V_B = f1\ (i_B, v_C)$

$I_C = f2\ (i_B, v_C)$.

Using Taylor 's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} \Delta v_C$$

$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The $\Delta v_B$, $\Delta v_C$, $\Delta i_B$, $\Delta i_C$ represent the small signal (incremental) base and collector current and voltage and can be represented as $v_B$, $i_C$, $i_B$, $v_C$

$$\therefore v_b = h_{ie}\, i_B + h_{re}\, v_C$$

$$i_C = h_{fe}\, i_B + h_{oe}\, v_b$$

where

$$h_{ie} = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_c} = \left.\frac{\partial v_B}{\partial i_B}\right|_{v_c}; \qquad h_{re} = \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

$$h_{fe} = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_c} = \left.\frac{\partial i_C}{\partial i_B}\right|_{v_c}; \qquad h_{oe} = \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

The model for CE configuration is shown in fig. 4.

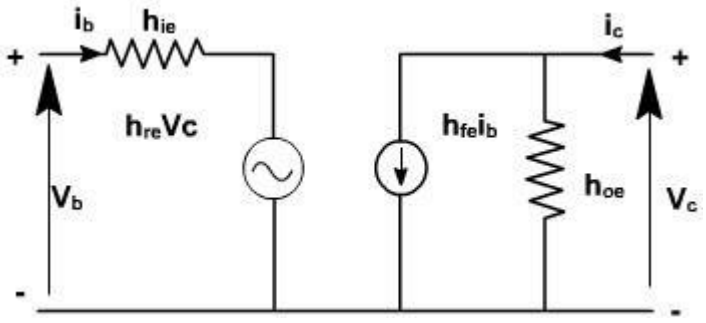



Fig. 4

To determine the four h-parameters of transistor amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. **Fig. 5**, shows the output characteristics of CE amplifier.

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{b2} - i_{b1}}$$

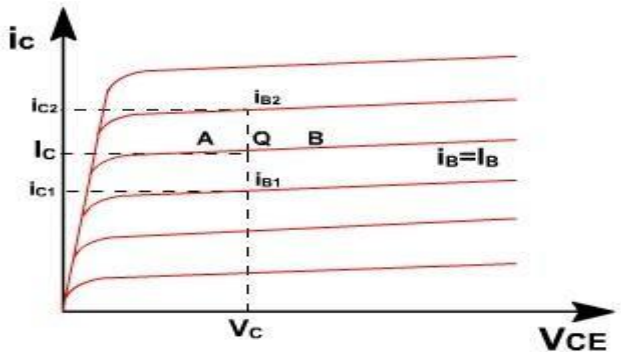



Fig. 5

The current increments are taken around the quiescent point Q which corresponds to $i_B = I_B$ and to the collector voltage $V_{CE} = V_C$

$$h_{oe} = \left.\frac{\partial i_C}{\partial V_C}\right|_{i_B}$$

The value of $h_{oe}$ at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \left.\frac{\Delta V_B}{\Delta i_B}\right|_{V_C}$$

$h_{ie}$ is the slope of the appropriate input on **fig. 6**, at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left.\frac{\Delta V_B}{\Delta V_C}\right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

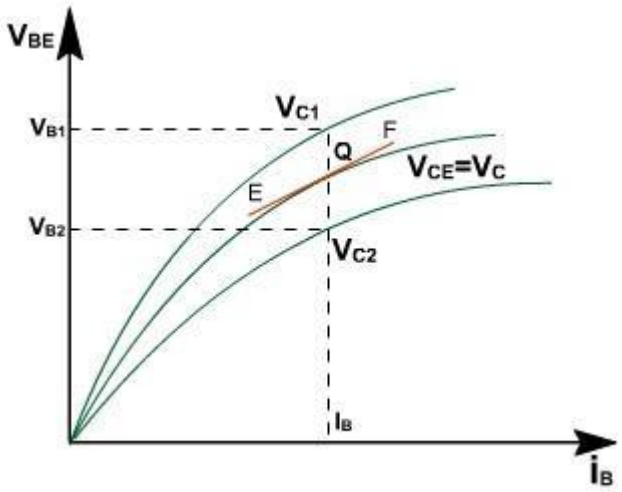



**Fig. 6**

A vertical line on the input characteristic represents constant base current. The parameter hre can be obtained from the ratio ($V_{B2}$– $V_{B1}$ ) and ($V_{C2}$– $V_{C1}$ ) for at Q.

Typical CE h-parametersof transistor 2N1573 are given below:

$h_{ie}$ = 1000 ohm.
$h_{re}$ = 2.5 * 10 –4
$h_{fe}$ = 50
$h_{oe}$=25 □□A /V

# ANALYSIS OF A TRANSISTOR AMPLIFIER USING H-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in **fig. 1**and to bias the transistor properly.

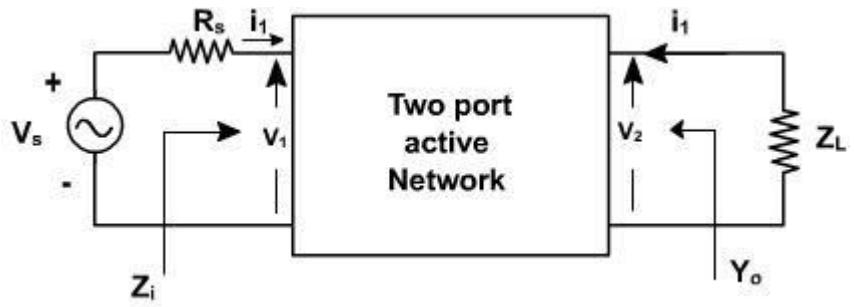



**Fig. 1**

Consider the two-port network of CE amplifier. $R_S$ is the source resistance and $Z_L$ is the load impedence h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in **fig. 2**. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedence, voltage gain, and output impedence.

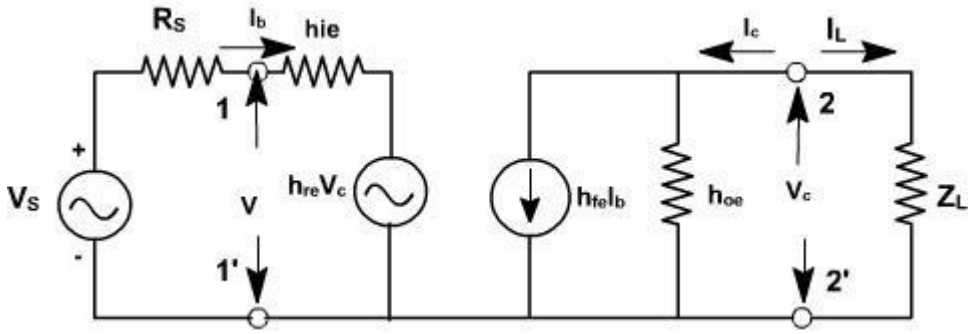



**Fig. 2**

## Currentgain:

For the transistor amplifier stage, $A_i$ is defined as the ratio of output to input currents.

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

## Inputimpedence:

The impedence looking into the amplifier input terminals ( 1,1' ) is the input impedence $Z_i$

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

## Voltagegain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_C}{V_b} = - \frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

## OutputAdmittance:

It is defined as

$$Y_0 = \left.\frac{I_c}{V_c}\right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe}\frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0$.

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re}\, h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance ($R_S$) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i\right)$$

$$= A_V \cdot \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_I\, Z_L}{Z_i + R_s}$$

$A_v$ is the voltage gain for an ideal voltage source ($R_v = 0$).

Consider input source to be a current source $I_S$ in parallel with a resistance $R_S$ as shown in **fig. 3**.

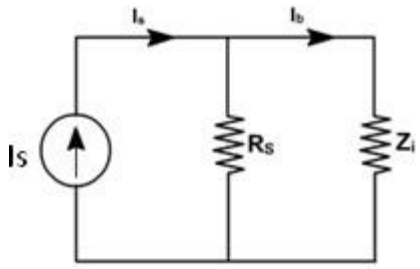



**Fig. 3**

In this case, overall current gain $A_{IS}$ is defined as

$$A_{I_s} = \frac{I_L}{I_s}$$

$$= -\frac{I_c}{I_s}$$

$$= -\frac{I_c}{I_b} * \frac{I_b}{I_s} \qquad \left(I_b = \frac{I_s * R_s}{R_s + Z_i}\right)$$

$$= A_I \cdot \frac{R_s}{R_s + Z_i}$$

$$\text{If } R_s \to \infty, \quad A_{I_s} \to A_I$$

**h-parameters**

**To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture data sheet. The manufacture data sheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example fig.4hrc in terms of CE parameter can be obtained as follows.**

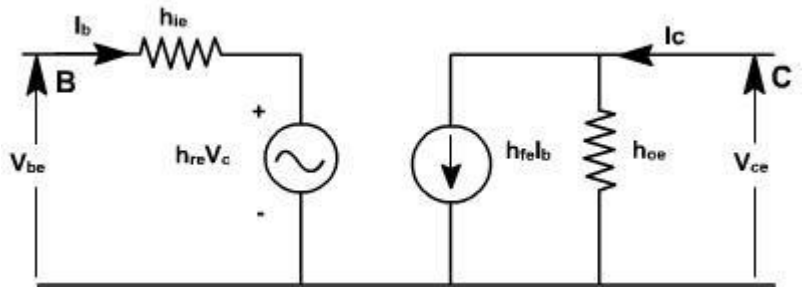



**Fig. 4**

**For CE transistor configuaration**

**Vbe = hie Ib + hre Vce**

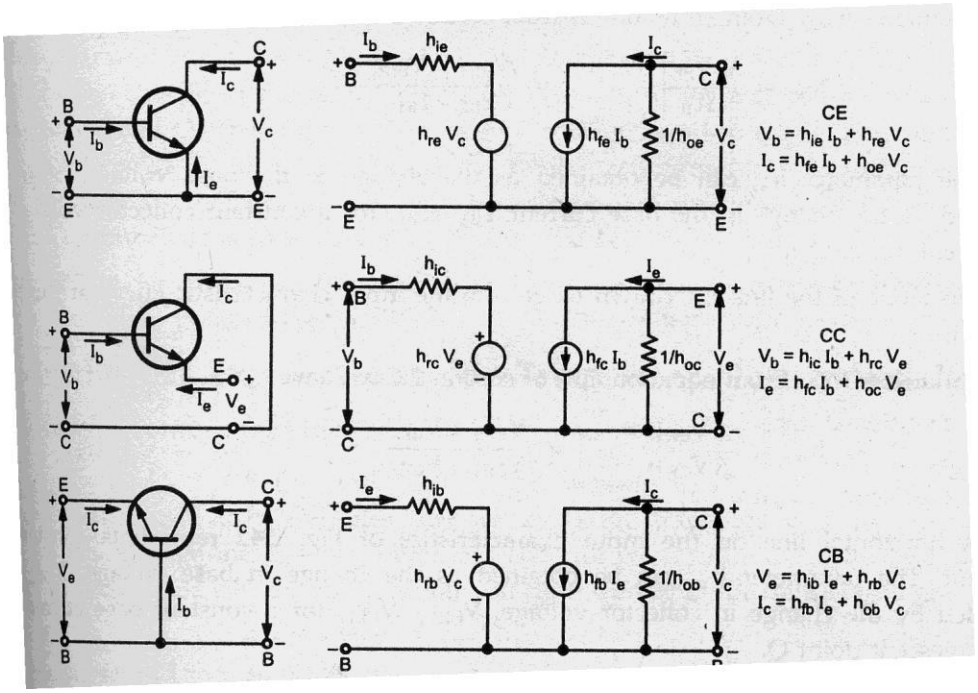
**Ic = h fe Ib + hoe Vce**

**The circuit can be redrawn like CC transistor configuration as shown in fig. 5.**

**Vbc = hie Ib + hrc Vec**

**Ic = hfe Ib + hoe Vec**

**hybrid model for transistor in three different configurations**




Typical h-parameter values for a transistor

| Parameter | CE | CC | CB |
|---|---|---|---|
| $h_i$ | 1100 Ω | 1100 Ω | 22 Ω |
| $h_r$ | $2.5 \times 10^{-4}$ | 1 | $3 \times 10^{-4}$ |
| $h_f$ | 50 | -51 | -0.98 |
| $h_o$ | 25 µA/V | 25 µA/V | 0.49 µA/V |

## Analysis of a Transistor amplifier circuit using h-parameters

A transistor amplifier can be constructed by connecting an external load and signal source and biasing the transistor properly.

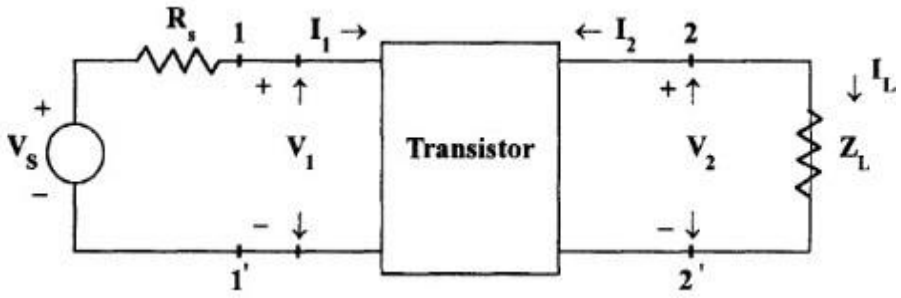



Fig.1.4 Basic Amplifier Circuit

The two port network of Fig. 1.4 represents a transistor in any one of its configuration. It is assumed that h-parameters remain constant over the operating range.The input is sinusoidal and $I_1$,$V_1$,$I_2$ and $V_2$ are phase quantities

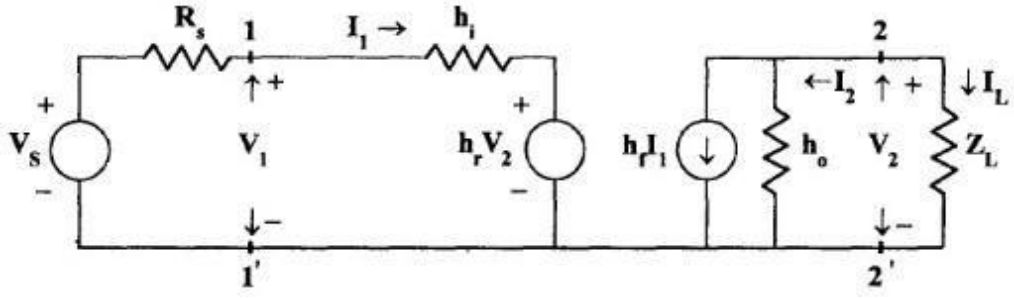



Fig. 1.5 Transistor replaced by its Hybrid Model

**Current Gain or Current Amplification ($A_i$)**

For transistor amplifier the current gain $A_i$ is defined as the ratio of output current to input current,i.e,

$$A_i = I_L / I_1 = -I_2 / I_1$$

From the circuit ofFig

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$

$I_2 = h_f I_1 - I_2 Z_L h_o$

$I_2 + I_2 Z_L h_o = h_f I_1$

$I_2( 1 + Z_L h_o) = h_f I_1$

$A_i = -I_2 / I_1 = - h_f / ( 1 + Z_L h_o)$

Therefore,

$A_i = - h_f / ( 1 + Z_L h_o)$

**Input Impedence ($Z_i$)**

In the circuitofFig , $R_S$is the signal source resistance .The impedence seen when looking into the amplifier terminals $(1,1^{'})$ is the amplifier input impedence$Z_i$,

$Z_i = V_1 / I_1$

From the input circuit of Fig $V_1 = h_i I_1 + h_r V_2$

$Z_i = ( h_i I_1 + h_r V_2) / I_1$

$= h_i + h_r V_2 / I_1$

Substituting

$V_2 = -I_2 Z_L = A_1 I_1 Z_L$

$Z_i = h_i + h_r A_1 I_1 Z_L / I_1$

$= h_i + h_r A_1 Z_L$

Substituting for $A_i$

$Z_i = h_i - h_f h_r Z_L / (1 + h_o Z_L)$

$= h_i - h_f h_r Z_L / Z_L(1/Z_L + h_o)$

Taking the Load admittance as $Y_L = 1/ Z_L$

$Z_i = h_i - h_f h_r / (Y_L + h_o)$

**Voltage Gain or Voltage Gain Amplification Factor($A_v$)**

The ratio of output voltage $V_2$ to input voltage $V_1$ give the voltage gain of the transistor i.e,

$$A_v = V_2 / V_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$A_v = A_1 I_1 Z_L / V_1 = A_i Z_L / Z_i$$

**Output Admittance ($Y_o$)**

$Y_o$ is obtained by setting $V_S$ to zero, $Z_L$ to infinity and by driving the output terminals from a generator $V_2$. If the current $V_2$ is $I_2$ then $Y_o = I_2/V_2$ with $V_S=0$ and $R_L = \infty$.

From the circuit of fig

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by $V_2$,

$I_2 / V_2 = h_f I_1/V_2 + h_o$

With $V_2 = 0$, by KVL in input circuit,

$$R_S I_1 + h_i I_1 + h_r V_2 = 0$$

$$(R_S + h_i) I_1 + h_r V_2 = 0$$

Hence, $I_2 / V_2 = -h_r / (R_S + h_i)$

$= h_f (-h_r/( R_S + h_i)+h_o$

$Y_o = h_o - h_f h_r/( R_S + h_i)$

The output admittance is a function of source resistance. If the source impedence is resistive then $Y_o$ is real.

**Voltage Amplification Factor($A_{vs}$) taking into account the resistance ($R_s$) of the source**

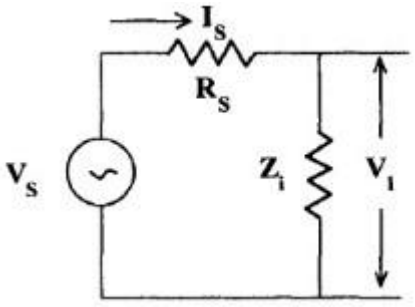



Fig. 5.6 Thevenin's Equivalent Input Circuit

This overall voltage gain $A_{vs}$ is given by

$$A_{vs} = V_2 / V_S = V_2V_1 / V_1V_S = A_v V_1 / V_S$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 5.6

$V_1 = V_S Z_i / (Z_{i+} R_S)$

$V_1 / V_S = Z_i / ( Z_i + R_S)$

Then, $A_{vs} = A_v Z_i / ( Z_i + R_S)$

Substituting $A_v = A_i Z_L / Z_i$

$A_{vs} = A_i Z_L / ( Z_i + R_S)$

$A_{vs} = A_i Z_L R_S / ( Z_i + R_S) R_S$

$A_{vs} = A_{is} Z_L / R_S$

**Current Amplification ($A_{is}$) taking into account the sourse Resistance($R_S$)**

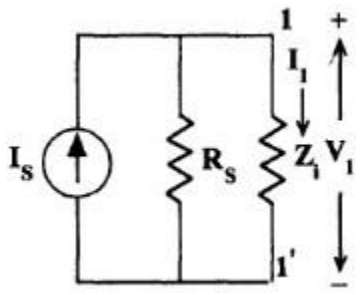



Fig. 1.7 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of $A_{is}$ is shown in Fig. 1.7

OverallCurrentGain, $A_{is} = -I_2 / I_S = -I_2 I_1 / I_1 I_S = A_i I_1 / I_S$

FromFig.1.7 $I_1 = I_S R_S / (R_S + Z_i)$

$I_1 / I_S = R_S / (R_S + Z_i)$

andhence, $A_{is} = A_i R_S / (R_S + Z_i)$

**Operating Power Gain ($A_P$)**

The operating power gain $A_P$ of the transistor is definedas

$A_P = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = A_i A_i Z_L / Z_i A_P$

$= A^2 (Z_i / Z_L)$ i

**Small Signal analysis of a transistor amplifier**

| | |
|---|---|
| $A_i = - h_f / ( 1 + Z_L h_o)$ | $A_v = A_i Z_L / Z_i$ |
| $Z_i = h_i + h_r A_1 Z_L = h_i - h_f h_r / (Y_L + h_o)$ | $A_{vs} = A_v Z_i / ( Z_i + R_S) = A_i Z_L / ( Z_i + R_S)$ $= A_{is} Z_L / R_S$ |
| $Y_o = h_o - h_f h_r / ( R_S + h_i) = 1 / Z_o$ | $A_{is} = A_i R_S / (R_S + Z_i) = A_{vs} = A_{is} R_S / Z_L$ |

**Simplified common emitter hybrid model:**

In most practical cases it is appropriate to obtain approximate values of $A_V$ , $A_i$ etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. **Fig. 4**shows the CE amplifier equivalent circuit in terms of h-parameters Since $1 / h_{oe}$ in parallel with $R_L$ is approximately equal to $R_L$ if $1 / h_{oe} >> R_L$ then $h_{oe}$ may be neglected. Under these conditions.

$I_c = h_{fe} I_B$ .

$h_{re} v_c = h_{re} I_c R_L = h_{re} h_{fe} I_b R_L$ .

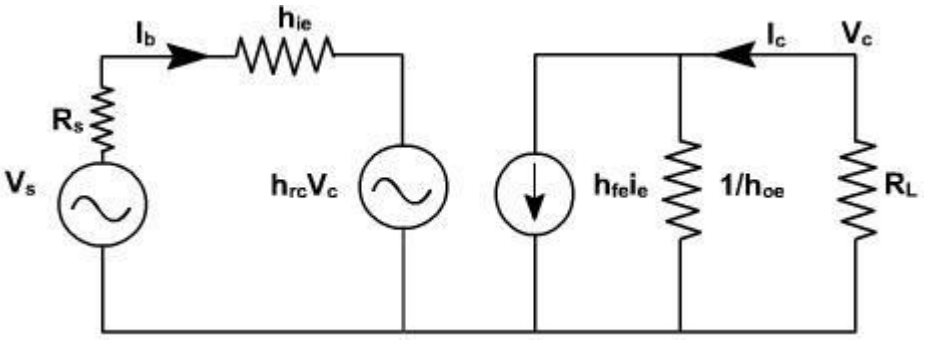



**Fig. 4**

Since $h_{fe}.h_{re} = 0.01$(approximately), this voltage may be neglected in comparison with $h_{ic} I_b$ drop across $h_{ie}$ provided $R_L$ is not very large. If load resistance $R_L$ is small than hoe and $h_{re}$ can be neglected.

$$A_I = -\frac{h_{fe}}{1+h_{oe} R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_V = \frac{A_I R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie}}$$

Output impedence seems to be infinite. When $V_s = 0$, and an external voltage is applied at the output we fined $I_b = 0$, $I_C = 0$. True value depends upon $R_S$ and lies between 40 K and 80K.

On the same lines, the calculations for CC and CB can be done.

**CE amplifier with an emitter resistor:**

The voltage gain of a CE stage depends upon $h_{fe}$. This transistor parameter depends upon temperature, aging and the operating point. Moreover, $h_{fe}$ may vary widely from device to device, even for same type of transistor. To stabilize voltage gain $A_V$ of each stage, it should be

independent of $h_{fe}$. A simple and effective way is to connect an emitter resistor $R_e$ as shown in **fig. 5**. The resistor provides negative feedback and provide stabilization.

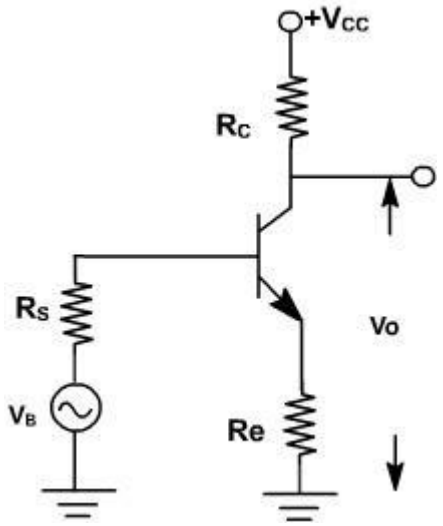



**Fig. 5**

**An approximate analysis of the circuit can be made using the simplified model.**

$$\text{Current gain } A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe}\, I_b}{I_b}$$
$$= -h_{fe}$$

It is unaffected by the addition of $R_C$.

Input resistance is given by

$$R_i = \frac{V_i}{I_b}$$
$$= \frac{h_{ie}\, I_b + (1+h_{fe})\, I_b\, R_e}{I_b}$$
$$= h_{ie} = (1+h_{fe})\, R_e$$

The input resistance increases by $(1+h_{fe})R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe}\, R_L}{h_{ie} + (1+h_{fe})R_e}$$

Clearly, the addition of $R_e$ reduces the voltage gain.

If $(1+h_{fe})R_e >> h_{ie}$ and $h_{fe} >> 1$

then

$$A_v = \frac{-h_{fe}\, R_L}{(1+h_{fe})R_e} \approx -\frac{R_L}{R_e}$$

**Subject to above approximation $A_V$ is completely stable. The output resistance is infinite for the approximatemodel.**

## Comparison of Transistor Amplifier Configuration

The characteristics of three configurations are summarized in Table .Here the quantities $A_i$,$A_v$,$R_i$,$R_o$ and $A_P$ are calculated for a typical transistor whose h-parameters are given in table .The values of $R_L$ and $R_s$ are taken as 3KΩ.

Table: Performance schedule of three transistor configurations

| *Quantity* | *CB* | *CC* | *CE* |
|---|---|---|---|
| $A_I$ | 0.98 | 47.5 | -46.5 |
| $A_V$ | 131 | 0.989 | -131 |
| $A_P$ | 128.38 | 46.98 | 6091.5 |
| $R_i$ | 22.6 Ω | 144 kΩ | 1065 Ω |
| $R_o$ | 1.72 MΩ | 80.5 Ω | 45.5 kΩ |

The values of current gain, voltage gain, input impedance and output impedance calculated as a function of load and source impedances

## Characteristics of Common Base Amplifier

(i) Current gain is less than unity and its magnitude decreases with the increase ofload resistance $R_L$,
(ii) Voltage gain $A_V$is high for normal values of$R_L$,
(iii) The input resistance $R_i$is the lowest of all the three configurations,and
(iv) The output resistance $R_o$is the highest of all the threeconfigurations.

*Applications* The CB amplifier is not commonly used for amplification purpose. It is used for

(i) Matching a very low impedancesource
(ii) As a non inverting amplifier to voltage gain exceedingunity.

(iii) For driving a high impedanceload.

(iv) As a constant currentsource.

**Characteristics of Common Collector Amplifier**

(i) For low $R_L$(< 10 kΩ), the current gain $A_i$is high and almost equal to that of aCE amplifier.

(ii) The voltage gain $A_V$is less thanunity.

(iii) The input resistance is the highest of all the threeconfigurations.

(iv) The output resistance is the lowest of all the threeconfigurations.

*Applications* The CC amplifier is widely used as a buffer stage between a high impedance source and a low impedance load.

**Characteristics of Common Emitter Amplifier**

(i) The current gain $A_i$is high for $R_L$< 10kΩ.

*(ii)* The voltage gain is high for normal values of load resistance$R_L$.

(iii) The input resistance $R_i$ismedium.

(iv) The output resistance $R_o$is moderatelyhigh.

*Applications*: CE amplifier is widely used for amplification.

**Simplified common emitter hybrid model:**

In most practical cases it is appropriate to obtain approximate values of $A_V$ , $A_i$ etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. **Fig 1. 8**shows the CE amplifier equivalent circuit in terms of h-parameters Since $1 / h_{oe}$ in parallel with $R_L$ is approximately equal to $R_L$ if $1 / h_{oe} >> R_L$ then $h_{oe}$ may be neglected. Under these conditions.

$I_c = h_{fe} I_B$ .

$h_{re} v_c = h_{re} I_c R_L = h_{re} h_{fe} I_b R_L$ .

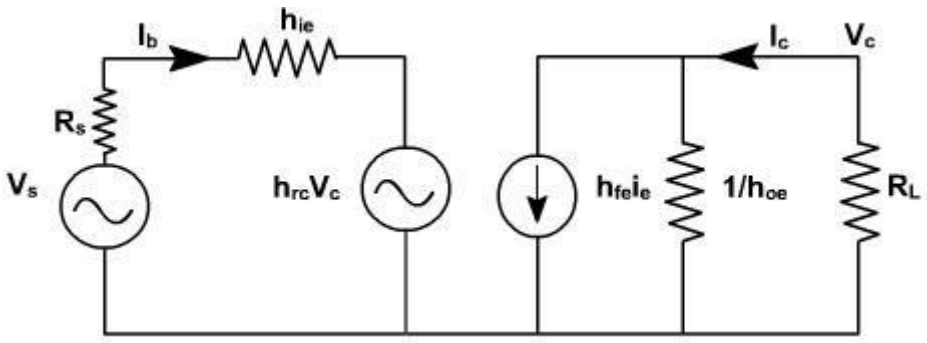



**Fig 1.8**

Since $h_{fe}.h_{re}$ » 0.01, this voltage may be neglected in comparison with $h_{ic}$ $I_b$ drop across $h_{ie}$ provided $R_L$ is not very large. If load resistance $R_L$ is small than hoe and $h_{re}$ can be neglected.

$$A_I = -\frac{h_{fe}}{1+h_{oe}\,R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_V = \frac{A_I\,R_L}{R_i} = -\frac{h_{fe}\,R_L}{h_{ie}}$$

Output impedence seems to be infinite. When $V_s = 0$, and an external voltage is applied at the output we fined $I_b = 0$, $I_C = 0$. True value depends upon $R_S$ and lies between 40 K and 80K.

On the same lines, the calculations for CC and CB can be done.

**CE amplifier with an emitter resistor:**

The voltage gain of a CE stage depends upon $h_{fe}$. This transistor parameter depends upon temperature, aging and the operating point. Moreover, $h_{fe}$ may vary widely from device to device, even for same type of transistor. To stabilize voltage gain $A_V$ of each stage, it should be independent of $h_{fe}$. A simple and effective way is to connect an emitter resistor $R_e$ as shown in **fig.1.9**. The resistor provides negative feedback and provide stabilization.

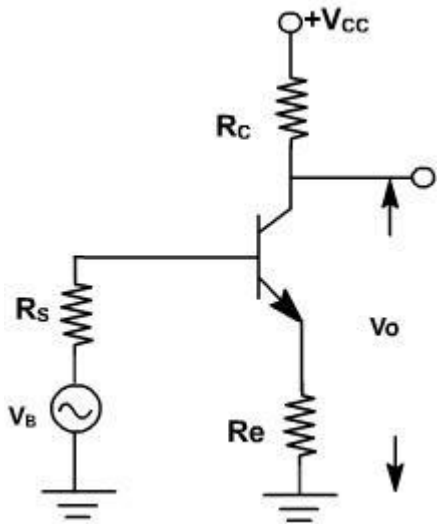



**Fig.1.9**

An approximate analysis of the circuit can be made using the simplified model.

$$\text{Current gain } A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe}\, I_b}{I_b}$$
$$= -h_{fe}$$

It is unaffected by the addition of $R_C$.

Input resistance is given by

$$R_i = \frac{V_i}{I_b}$$
$$= \frac{h_{ie}\, I_b + (1+h_{fe})\, I_b\, R_e}{I_b}$$
$$= h_{ie} = (1+h_{fe})\, R_e$$

The input resistance increases by $(1+h_{fe})R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe}\, R_L}{h_{ie} + (1+h_{fe})R_e}$$

Clearly, the addition of $R_e$ reduces the voltage gain.

If $(1+h_{fe})R_e >> h_{ie}$ and $h_{fe} >> 1$

then

$$A_v = \frac{-h_{fe}\, R_L}{(1+h_{fe})R_e} \approx -\frac{R_L}{R_e}$$

Subject to above approximation $A_V$ is completely stable. The output resistance is infinite for the approximate model.

**Common Base Amplifier:**

The common base amplifier circuit is shown in **Fig. 1.** The $V_{EE}$ source forward biases the emitter diode and $V_{CC}$ source reverse biased collector diode. The ac source $v_{in}$is connected to emitter through a couplingcapacitor so that it blocks dc. This ac voltage produces small fluctuation in currents and voltages. The load resistance $R_L$is also connected to collector through coupling capacitor so the fluctuation in collector base voltage will be observed across$R_L$.

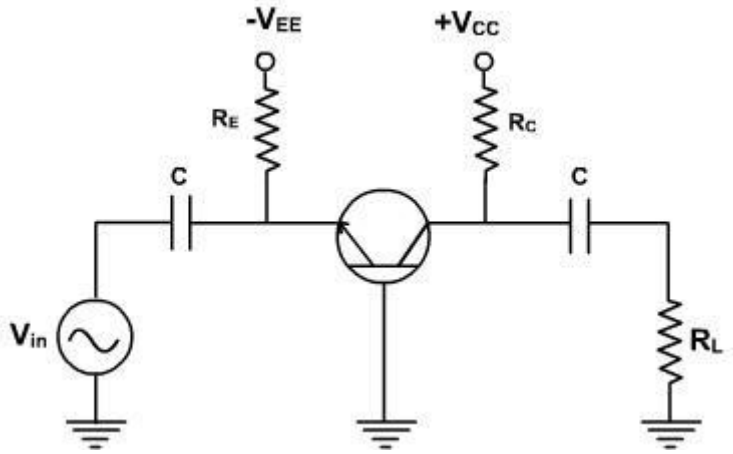



**Fig. 1**

The dc equivalent circuit is obtained by reducing all ac sources to zero and opening all capacitors. The dc collector current is same as $I_E$ and $V_{CB}$ is given by

$V_{CB} = V_{CC} - I_C R_C$.

These current and voltage fix the Q point. The ac equivalent circuit is obtained by reducing all dc sources to zero and shorting all coupling capacitors. $r'_e$ represents the ac resistance of the diode as shown in **Fig.2**.

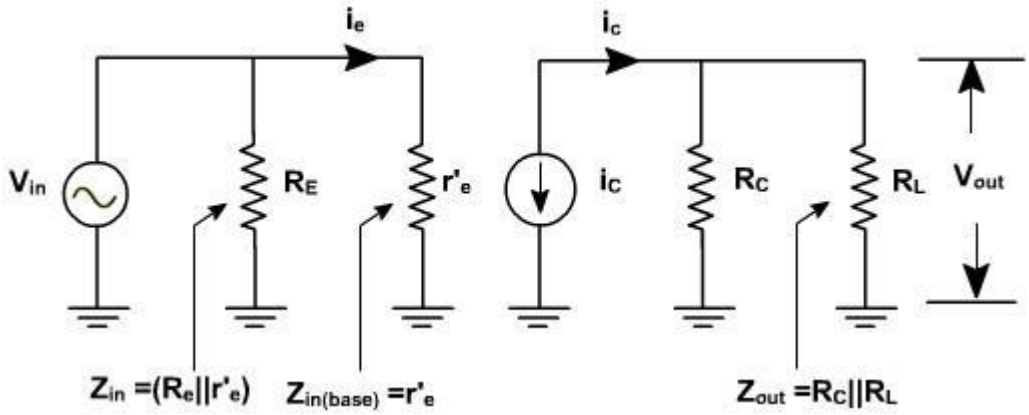



**Fig. 2**

**Fig. 3**, shows the diode curve relating $I_E$ and $V_{BE}$. In the absence of ac signal, the transistor operates at Q point (point of intersection of load line and input characteristic). When the ac

signal is applied, the emitter current and voltage also change. If the signal is small, the operating point swings sinusoidally about Q point (A to B).

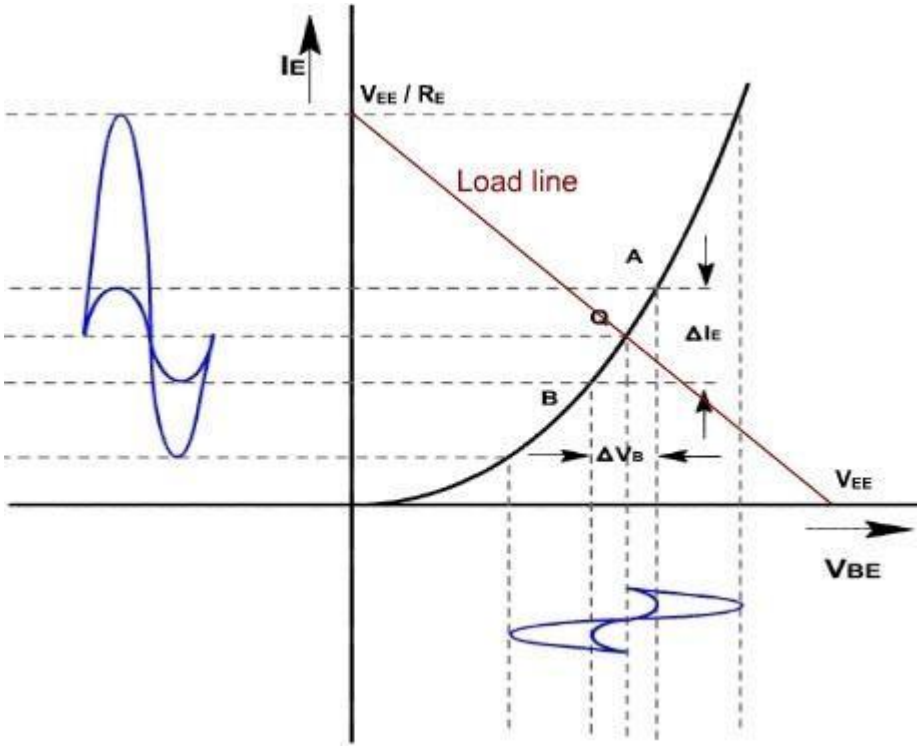



**Fig .3**

If the ac signal is small, the points A and B are close to Q, and arc A B can be approximated by a straight line and diode appears to be a resistance given by

$$r'_e = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{\text{small change}}$$

$$= \frac{V_{be}}{i_e} = \frac{\text{ac voltage across base and emitter}}{\text{ac current through emitter}}$$

If the input signal is small, input voltage and current will be sinusoidal but if the input voltage is large then current will no longer be sinusoidal because of the non linearity of diode curve. The emitter current is elongated on the positive half cycle and compressed on negative half cycle. Therefore the output will also be distorted.

$r'_e$ is the ratio of $\Delta V_{BE}$ and $\Delta I_E$ and its value depends upon the location of Q. Higher up the Q point small will be the value of r' e because the same change in $V_{BE}$ produces large change in $I_E$. The slope of the curve at Q determines the value of $r'_e$. From calculation it can be proved that.

$r'_e = 25mV / I_E$

**Common BaseAmplifier**

**Proof:**

In general, the current through a diode is given by

$$I = I_{CO}(e^{\frac{qV}{KT}} - 1)$$

Where q is he charge on electron, V is the drop across diode, T is the temperature and K is a constant.

On differentiating w.r.t V, we get,

$$\frac{dI}{dV} = I_{co} * e^{\frac{qV}{KT}} * \frac{q}{KT}$$

The value of (q / KT) at 25°C is approximately 40.

$$\frac{dI}{dV} = 40 * I_{co} * e^{\frac{qV}{KT}}$$

Therefore,

$$= 40 * (I + I_{co})$$

or,

$$\frac{dV}{dI} = \frac{1}{40 * (I + I_{co})} \approx \frac{1}{40 * I}$$

$$\text{Therefore, ac resistance of the emitter diode} = \frac{dV}{dI} = \frac{25mV}{I} \text{ Ohms}$$

To a close approximation the small changes in collector current equal the small changes in emitter current. In the ac equivalent circuit, the current '$i_C$' is shown upward because if '$i_e$' increases, then '$i_C$' also increases in the same direction.

## Voltage gain:

Since the ac input voltage source is connected across $r'_e$. Therefore, the ac emitter current is given by

$i_e = V_{in} / r'_e$

or, $V_{in} = ier'_e$

The output voltage is given by $V_{out} = i_c (R_C \parallel R_L)$

$$\text{Therefore, voltage gain } A_V = \frac{v_{out}}{v_{in}} = \frac{(R_C \parallel R_L)}{r'_e} = \frac{rc}{r}$$

Under open circuit condition $v_{out} = i_c R_c$

$$\text{Therefore, voltage gain in open circuit condition} = A_V = \frac{R_C}{r'_e}$$

## Example-1

Find the voltage gain and output of the amplifier shown in **fig. 4**, if input voltage is 1.5mV.

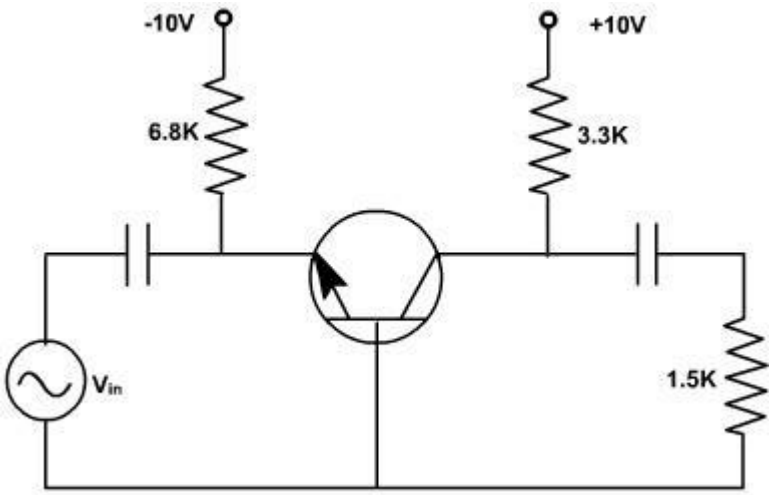



**Fig. 4**

**Solution:**

The emitter dc current I E is given by $I_E = \frac{10 - 0.7}{6.8k} = 1.37mA$

Therefore, emitter ac resistance = $A_V = \frac{r_c}{r'_e} = \frac{3.3k \parallel 1.5k}{18.2\Omega}$

or, $A_V = 56.6$

and, $V_{out}$ = 1.5 x 56.6 = 84.9 mV

## Example-2

Repeat example-1 if ac source has resistance R s = 100 W .

**Solution:**

The ac equivalent circuit with ac source resistance is shown in fig. 5.

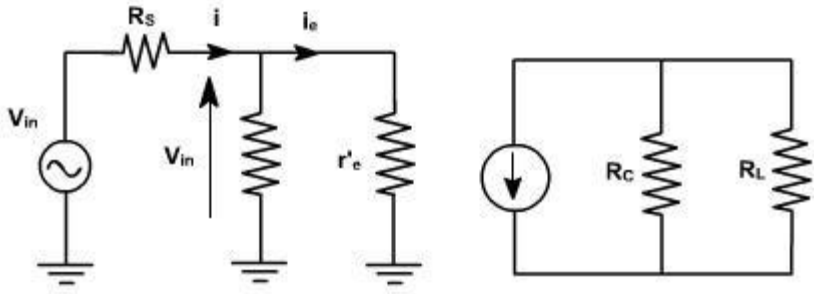



**Fig. 5**

The emitter ac current is given by $i_e = \frac{v_{in}}{R_s + (R_E \| r_e')} \times \frac{R_E}{R_E + r_e'}$

or, $i_e = \frac{v_{in}}{(R_s + r_e')R_E + R_s r_e'} \times R_E ; \frac{v_{in}}{R_s + r_e'}$

Therefore, voltage gain of the amplifier = $A_V = \frac{v_{out}}{v_{in}} = \frac{i_c r_c}{i_e (R_s + r'_e)} = \frac{r_c}{R_s + r_e'}$

$$A_V = \frac{3.3k \| 1.5k}{100\Omega + 18.2\Omega} = 8.71$$

and, $V_{out}$ = 1.5 x 8.71 =13.1mV

**Small Signal CE Amplifiers:**

CE amplifiers are very popular to amplify the small signal ac. After a transistor has been biased with a Q point near the middle of a dc load line, ac source can be coupled to the base. This produces fluctuations in the base current and hence in the collector current of the same shape and frequency. The output will be enlarged sine wave of same frequency.

The amplifier is called linear if it does not change the wave shape of the signal. As long as the input signal is small, the transistor will use only a small part of the load line and the operation will be linear.

On the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut off. This clips the peaks of the input and the amplifier is no longer linear.

The CE amplifier configuration is shown in **fig. 1**.

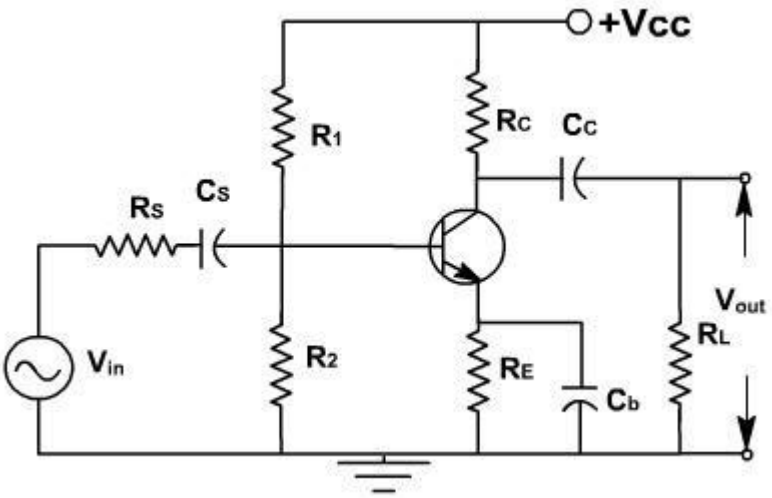



**Fig. 1**

The coupling capacitor ($C_C$ ) passes an ac signal from one point to another. At the same time it does not allow the dc to pass through it. Hence it is also called blocking capacitor.

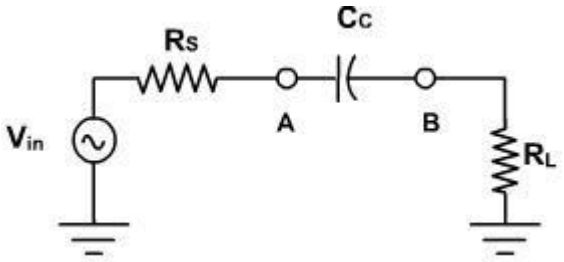



**Fig. 2**

For example in **fig. 2**, the ac voltage at point A is transmitted to point B. For this series reactance $X_C$ should be very small compared to series resistance $R_S$. The circuit to the left of A may be a source and a series resistor or may be the Thevenin equivalent of a complex circuit. Similarly $R_L$ may be the load resistance or equivalent resistance of a complex network. The current in the loop is given by

$$i = \frac{v_{in}}{\sqrt{(R_S + R_L)^2 + X_C^2}}$$

$$= \frac{v_{in}}{\sqrt{R^2 + X^2}}$$

As frequencyincreases, $X_C \left( = \frac{1}{2\pi fc} \right)$ decreases, and current increases until it reaches to its maximum value $v_{in}$ / R. Therefore the capacitor couples the signal properly from A to Bwhen $X_C$<< R. The size of the coupling capacitor depends upon the lowest frequency to be coupled. Normally, for lowest frequency$X_C$ □ □0.1R is taken as designrule.

The coupling capacitor acts like a switch, which is open to dc and shorted for ac.

The bypass capacitor $C_b$is similar to a coupling capacitor, except that it couples an ungrounded point to a grounded point. The $C_b$ capacitor looks like a short to an ac signal and therefore emitter is said ac grounded. A bypass capacitor does not disturb the dc voltage at emitterbecause it looks open to dc current. As a designrule $X_{Cb}$ □ $0.1R_E$ at Analysis of CEamplifier:

In a transistor amplifier, the dc source sets up quiescent current and voltages. The ac source then produces fluctuations in these current and voltages. The simplest way to analyze this circuit is to split the analysis in two parts: dc analysis and ac analysis. One can use superposition theorem for analysis .

## AC & DC Equivalent Circuits:

For dc equivalent circuit, reduce all ac voltage sources to zero and open all ac current sources and open all capacitors. With this reduced circuit shown in **fig. 3**dc current and voltages can be calculated.

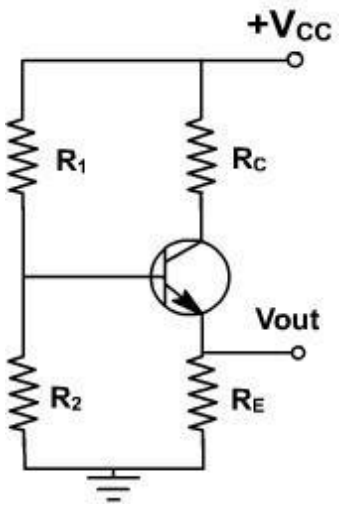


**Fig. 3**

For ac equivalent circuits reduce dc voltage sources to zero and open current sources and short all capacitors. This circuit is used to calculate ac currents and voltage as shown in **fig. 4**.

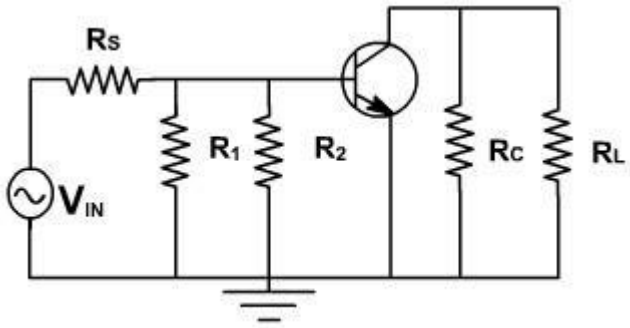



**Fig. 4**

The total current in any branch is the sum of dc and ac currents through that branch. The total voltage across any branch is the sum of the dc voltage and ac voltage across that branch.

## Phase Inversion:

Because of the fluctuation is base current; collector current and collector voltage also swings above and below the quiescent voltage. The ac output voltage is inverted with respect to the ac input voltage, meaning it is $180^{o}$ out of phase with input.

During the positive half cycle base current increase, causing the collector current to increase. This produces a large voltage drop across the collector resistor; therefore, the voltage output decreases and negative half cycle of output voltage is obtained. Conversely, on the negative half cycle of input voltage less collector current flows and the voltage drop across the collector resistor decreases, and hence collector voltage increases we get the positive half cycle of output voltage as shown in **fig. 5**.

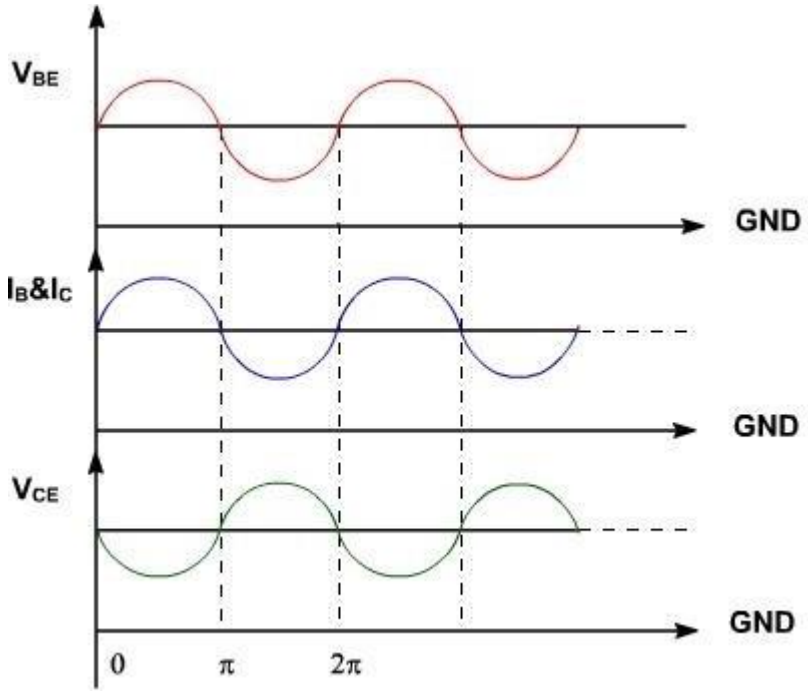



**Fig. 5**

lowest frequency.

**AC Load line:**

Consider the dc equivalent circuit **fig. 1**.

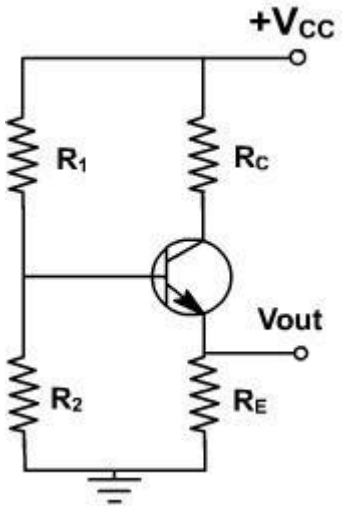



**Fig. 1**

Assuming $I_C = I_C(approx)$, the output circuit voltage equation can be written as

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

and $$I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E}$$

and $$I_C = 0, \quad V_{CE} = V_{CC}$$

The slop of the d.c load lineis $-\frac{1}{R_C + R_E}$.

When considering the ac equivalent circuit, the output impedance becomes $R_C \parallel R_L$ which is less than $(R_C + R_E)$.

In the absence of ac signal, this load line passes through Q point. Therefore ac load line is a line of slope $(-1 / ( R_C \parallel R_L) )$ passing through Q point. Therefore, the output voltage fluctuations will now be corresponding to ac load line as shown in **fig. 2**. Under this condition, Q-point is not in the middle of load line, therefore Q-point is selected slightly upward, means slightly shifted to saturation side.

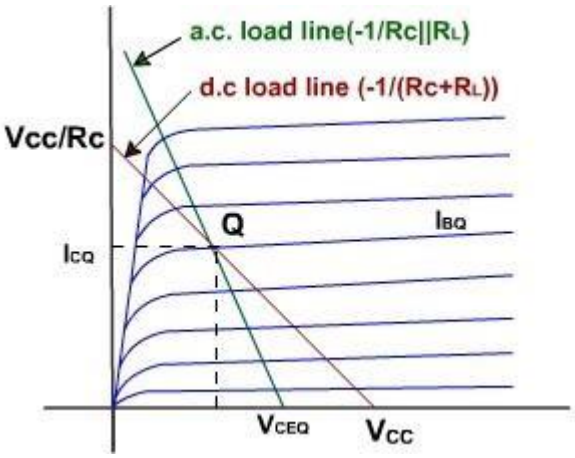



**Fig. 2**

## Analysis of CEamplifier

### Voltage gain:

To find the voltage gain, consider an unloaded CE amplifier. The ac equivalent circuit is shown in **fig. 3**. The transistor can be replaced by its collector equivalent model i.e. a current source and emitter diode which offers ac resistance $r'_e$.

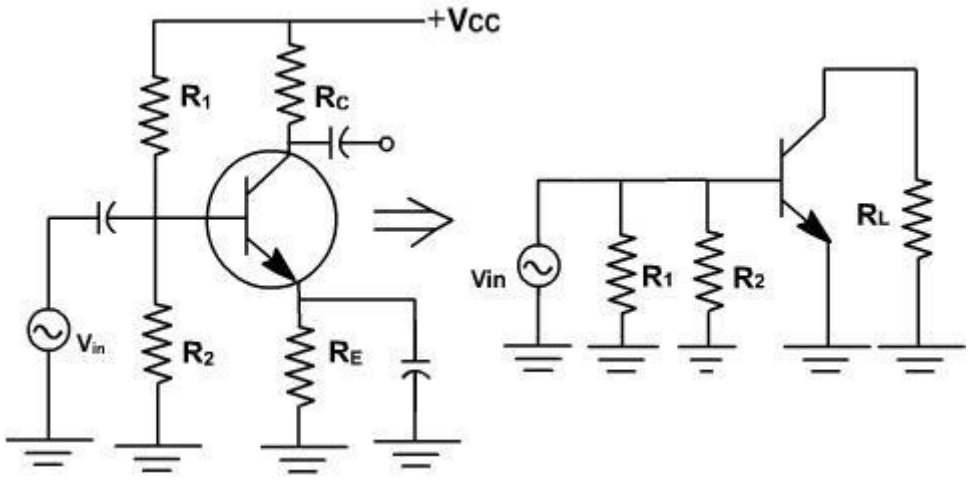



**Fig. 3**

The input voltage appears directly across the emitter diode.

Therefore emitter current $i_e = V_{in} / r'_e$.

Since, collector current approximately equals emitter current and $i_C = i_e$ and $v_{out} = - i_e R_C$ (The minus sign is used here to indicate phase inversion)

Further $v_{out} = - (V_{in} R_C) / r'_e$

Therefore voltage gain $A = v_{out} / v_{in} = -R_C / r'_e$

The ac source driving an amplifier has to supply alternating current to the amplifier. The input impedance of an amplifier determines how much current the amplifier takes from the ac source.

In a normal frequency range of an amplifier, where all capacitors look like ac shorts and other reactance are negligible, the ac input impedance is defined as

$z_{in} = v_{in} / i_{in}$

Where $v_{in}$, $i_{in}$ are peak to peak values or rms values

The impedance looking directly into the base is symbolized $z_{in(base)}$ and is given by

$Z_{in(base)} = v_{in} / i_b$ ,

Since, $v_{in} = i_e$

$r'_e z_{in\,(base)} = r'_e$.

From the ac equivalent circuit, the input impedance $z_{in}$ is the parallel combination of $R_1$ , $R_2$ and $r'_e$.

$Z_{in} = R_1||R_2 \;\; || \sqsupset r'_e$

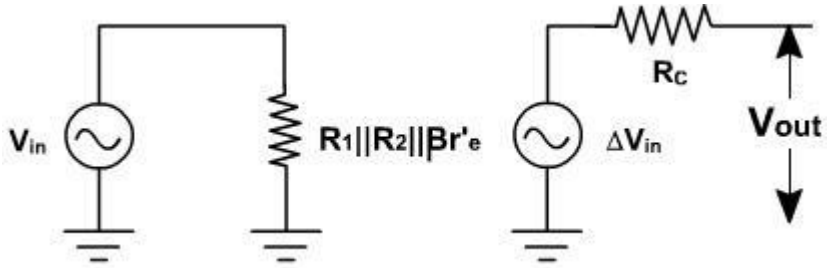
The Thevenin voltage appearing at the output is

$v_{out} = Av_{in}$

The Thevenin impedance is the parallel combination of $R_C$and the internal impedance of the current source. The collector current source is an ideal source, therefore it has an infinite internal impedance.

$z_{out} = R_C$.

The simplified ac equivalent circuit is shown in **fig. 4**.




**Analysis of CE amplifier**
**Example-1:**

**Select R1 and R2 for maximum output voltage swing in the circuit shown in fig. 5.**

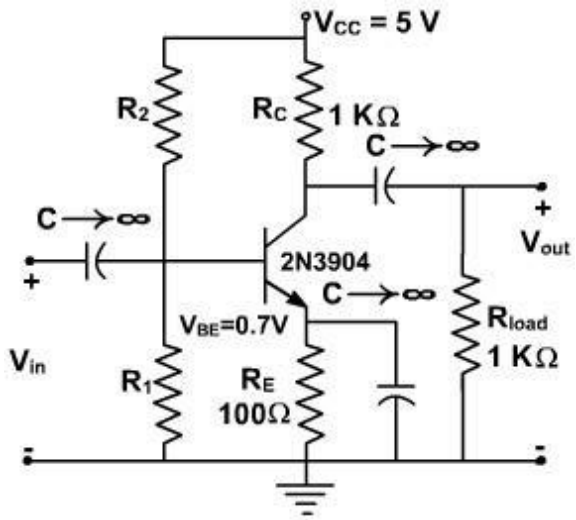


**Fig. 5**

**Solution:**

**We first determine ICQ for the circuit**

$$R_{ac} = R_C \parallel R_{load} = 500$$
$$R_{dc} = R_E + R_C = 1100$$
$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{5}{500 + 1100} = 3.13 \text{ mA}$$

**For maximum swing,**

**V'CC = 2 VCEQ**

**The quiescent value for VCE is the given by**

**VCEQ= (3.13 mA) (500 W ) = 1.56 V**

**The intersection of the ac load line on the vCE axis is V'CC = 3.13V. From the manufacturer's specification, β for the 2N3904 is 180. RB is set equal to 0.1 βRE. So,**

**RB = 0.1(180 )(100) = 1.8 K W**

**VBB = (3.13 x 10-3) (1.1 x 100) + 0.7 = 1.044 V**

**Since we know VBB and RB, we find R1 and R2,**

$$R_1 = \frac{R_B}{1 - V_{BB} / V_{CC}} = \frac{1800}{1 - 1.044 / 5} = 2.28 \text{ K}\Omega$$
$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = \frac{1800 \times 5}{1.044} = 8.62 \text{ K}\Omega$$

**The maximum output voltage swing, ignoring the non-linearity's at saturation and cutoff, would then be**

$$\text{Max collector current swing} = 2 I_{CQ} (R_C \parallel R_{load})$$
$$= 2 (3.13 \text{ mA}) (500 \ \Omega) = 3.13 \text{ V}$$

**The load lines are shown on the characteristics of fig. 6.**

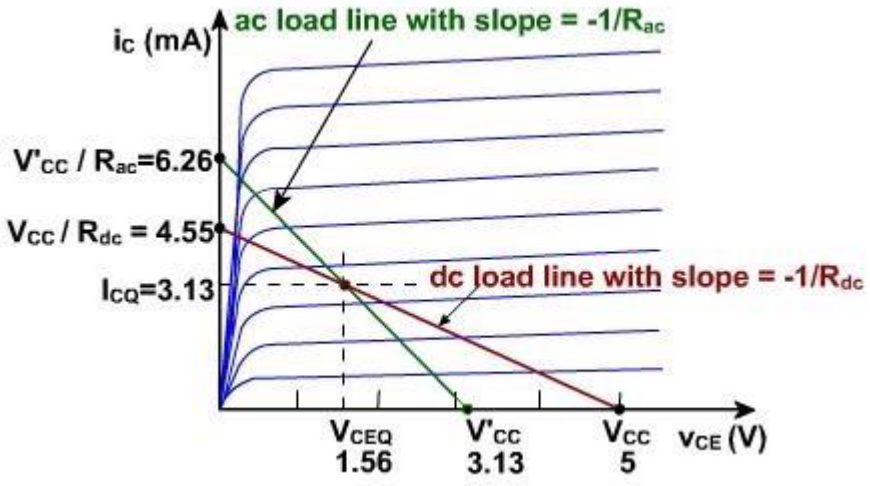



**Fig. 6**

**The maximum power dissipated by the transistor is calculated to assure that it does not exceed the specifications. The maximum average power dissipated in the transistor is**

**P(transistor)= VCEQ ICQ = (1.56 (V)) (3.13 mA) =4.87 mW**

**This is well within the 350 mW maximum given on the specification sheet. The maximum conversion efficiency is**

$$\eta = \frac{P_{out}(ac)}{P_{VCC}(dc)} = \frac{\left(3.13 \times 10^{-3}/2\right)^2 \times 1000/2 \times 100}{5 \times 3.13 \times 10^{-3} + 5^2/10.9 \times 10^3} = 6.84\%$$

**The swamped Amplifier:**

The ac resistance of the emitter diode r'e equals 25mV / IE and depends on the temperature. Any change in r'e will change the voltage gain in CE amplifier. In some applications, a change in voltage is acceptable. But in many applications we need a stable voltage gain is required.

To make it stable, a resistance rE is inserted in series with the emitter and therefore emitter is no longer ac grounded. fig .7.

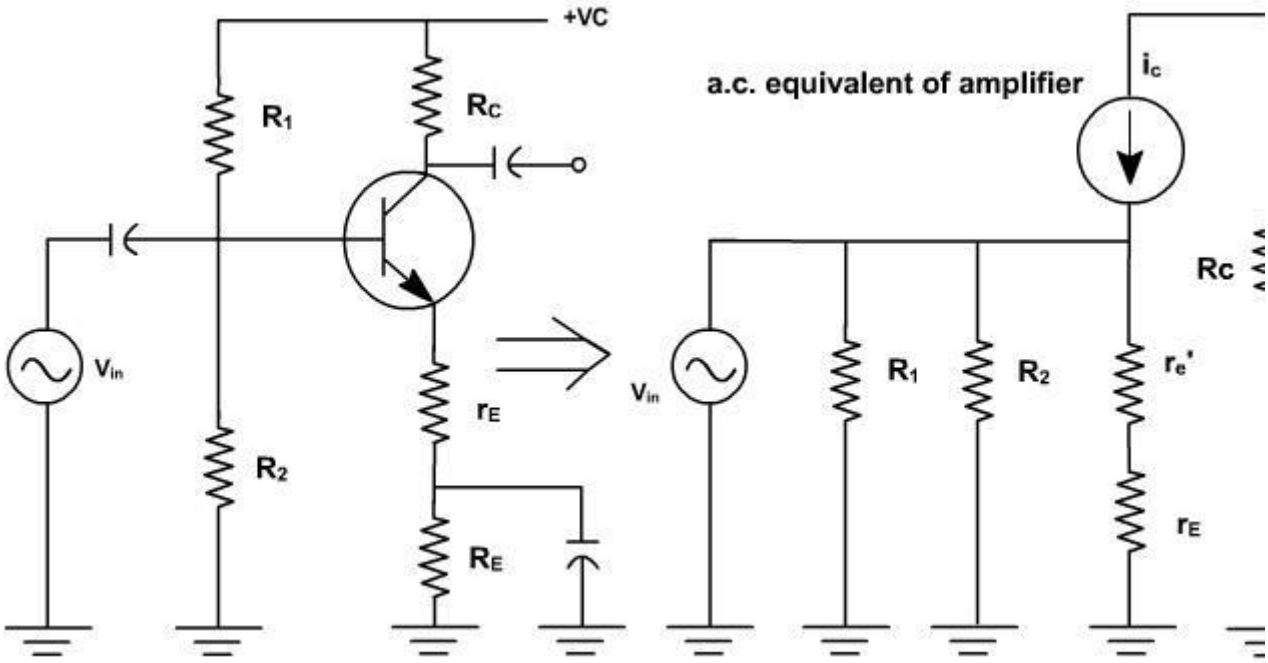



**Fig. 7**

Because of this the ac emitter current flows through rE and produces an ac voltage at the emitter. If rE is much greater than r'e almost all of the ac input signal appears at the emitter, and the emitter is bootstrapped to the base for ac as well as for dc.

In this case, the collector circuit is given by

$$i_C = \frac{V_{in}}{r'_e + r_E}$$

and $V_{out} = -i_C R_C$

Therefore,

$$A = \frac{V_{out}}{V_{in}} = -\frac{i_C R_C}{i_C (r'_e + r_E)}$$

$$= -\frac{R_C}{(r'_e + r_E)}$$

**Now r'e has a less effect on voltage gain, swamping means rE >> r'e If swamping is less, voltage gain varies with temperature. If swamping is heavy, then gain reduces very much.**

**Design of Amplifier :**

Example -1 (Common Emitter Amplifier Design)

Design a common-emitter amplifier with a transistor having a β =200 and VBE = 0.7 V. Obtain an overall gain of |A V | ≥ 100 and maximum output voltage swing. Use the CE configuration shown in fig. 1with two power supplies. Rsource is the resistance associated with the source, vsource. Let Rsource= 100 Ohms. The output load is 2KΩ. Determine the resistor values of the bias circuitry, the maximum undistorted output voltage swing, and the stage voltage gain.

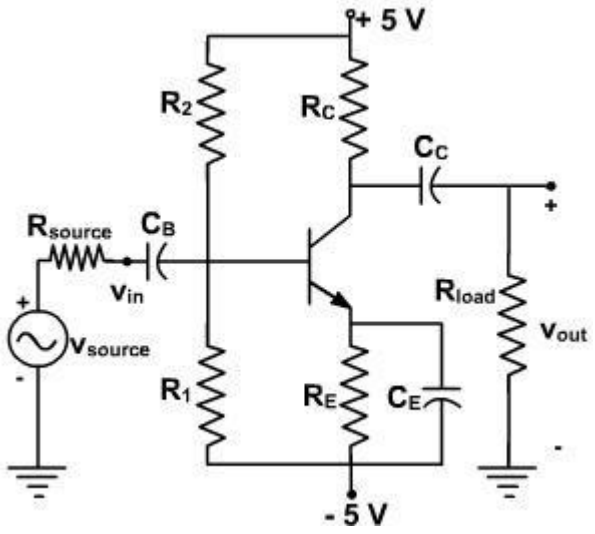



Fig. 1

Solution:

The maximum voltage across the amplifier is 10 V since the power supply can be visualized as a 10V power supply with a ground in the center. In this case, the ground has no significance to the operation of the amplifier since the input and output are isolated from the power supplies by capacitors.

We will have to select the value for RC and we are really not given enough information to do so. Let choose RC = Rload.

We don't have enough information to solve for RB – we can't use the bias stability criterion since we don't have the value of RE either. We will have to (arbitrarily) select a value of RB or RE. If this leads to a contradiction, or “bad” component values (e.g., unobtainable resistor values), we can come back and modify our choice. Let us select a value for RE that is large enough to obtain a reasonable value of VBB, Selecting RE as 400Ω will not appreciably reduce the collector current yet it will help in maintaining a reasonable value of VBB. Thus,

RB = 0.1 β RE = 0.1 (200)(400) = 8 K Ω

To insure that we have the maximum voltage swing at the output, we will use

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{10}{1000 + 2400} = 2.94 \text{ mA}$$

$$V_{BB} = V_{BE} + I_{CQ}\,(R_B/\beta + R_E) = 0.7 + 2.9 \times 10^{-3}\left(\frac{8000}{200} + 400\right) = 1.99 \text{ V}$$

Note that we are carrying out our calculations to four places so that we can get accuracy to three places. The bias resistors are determined by

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{8000}{1 - 1.99/10} = 9.99 \text{ K}\Omega$$

$$R_2 = R_B \frac{V_{CC}}{V_{BB}} = 8000\left(\frac{10}{1.99}\right) = 40.2 \text{ K}\Omega$$

Since we designed the bias circuit to place the quiescent point in the middle of the ac load line, we can use

Vout(undistorted p-p) 1.8 (2.94 x 10-3 ) (2 K Ω || 2 K Ω ) =5.29 V

Now we can determine the gain of the amplifier itself.

$$|A_v| = g_m\,(R_C \,||\, R_{load}) = \frac{2.94 \times 10^{-3} \times 1000}{26 \times 10^{-3}}$$

Using voltage division, we can determine the gain of the overall circuit.

The value of Rin can be obtained as

$$R_{in} = r_\pi \,||\, R_B = 1.77\text{k}\Omega \,||\, 8\text{k}\Omega = 1.45 \text{ k}\Omega$$

Thus the overall gain of the amplifier is

$$|A_v| \text{ overall} = \left|\frac{v_{out}}{v in} = 113\right| \times \frac{R_{in}}{R_{in} + R_{source}} = 106$$

This shows that the common-emitter amplifier provides high voltage gain. However, it is very noisy, it has a low input impedance, and it does not have the stability of the emitter resistor common emitter a

Design ofAmplifier

Example-2 (Emitter-Resistor Amplifier Design)

Design an emitter-resistor amplifier as shown in fig. 2to drive a 2 KΩ load using a pnp silicon transistor, $V_{CC}$ = -24V, β = 200, $A_v$ = -10, and $V_{BE}$ = -0.7 V. Determine all element valuesand calculate $A_i$, $R_{in}$, $I_{CQ}$ and the maximum undistorted symmetrical output voltage swing forthree

values of $R_C$ as given below:

1. $R_C = R_{load}$
2. $R_C = 0.1R_{load}$
3. $R_C = 10R_{load}$

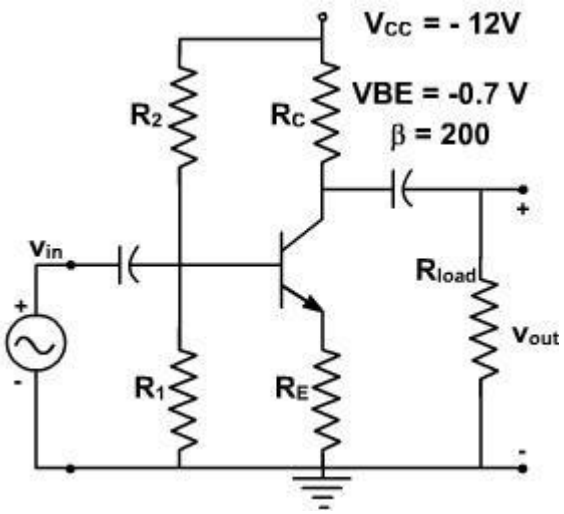



Fig. 2

Solution:

(a) $R_C = R_{load}$

We use the various equations derived in previous lecture in order to derive the parameters of the circuit.

From the voltage gain, we can solve for $R'_E$.

$$A_v = -10 = -\frac{R_{load} \,||\, R_C}{r_e + R_E} = -\frac{2K\Omega \,||\, 2K\Omega}{r_e + R_E}$$

So $R'_E = r_e + R_E = 100\ \Omega$

We can find the quiescent value of the collector current $I_C$ form the collector-emitter loop using the equation for the condition of maximum output swing.

$$I_{CQ} = \frac{V_{CC}}{R_{dc} + R_{ac}} = -7.5\ mA$$

Therefore, $r_E' = \frac{25 \times 10^{-3}}{7.5 \times 10^{-3}} = 3.33\Omega$

This is small enough that we shall ignore it to find that $R_E = 100\ \Omega$. Since we now know $\beta$ and $R_E$. We can use the design guideline.

$R_B = 0.1\ \beta\ R_E = 2\ k\ \Omega$

As designed earlier, the biasing circuitry can be designed in the same manner and given by

$V_{BB} = -1.52\ V$

$R_1 = 2.14\ K\ \Omega$

$R_2 = 3.6\ K\ \Omega$

The maximum undistorted symmetrical peak to peak output swing is then

$V_{out}\ (P\text{-}P) = 1.8\ I_{CQ}\ (R_{load} \parallel R_C) = 13.5\ V$

Thus current gain $A_i = -9.1$

and input impedance $R_{in} = 1.82\ K\ \Omega$

(b) $R_C = 0.1R_{load}$

we repeat the steps of parts (a) to find

| | |
|---|---|
| $R_C = 200\ \Omega$ | $R_i = 390\ \Omega$ |
| $I_{CQ} = -57.4\ mA$ | $R_2 = 4.7K\ \Omega$ |
| $r'_e = 0.45\ \Omega$ | $v_{out}(p\text{-}p) = 18.7\ V$ |
| $R_B = 360\ \Omega$ | $A_i = -1.64$ |
| $V_{BB} = -1.84\ V$ | $R_{in} = 327\ \Omega$ |

(C) $R_C = 10R_{load}$

Once again, we follow the steps of part (a) to find

| | |
|---|---|
| $R_C = 20\ K\ \Omega$ | $R_1 = 3.28K\ \Omega$ |
| $I_{CQ} = -1.07\ mA$ | $R_2 = 85.6K\ \Omega$ |
| $r'_e = 24.2\ \Omega$ | $v_{out}(p\text{-}p) = 3.9\ V$ |

$R_B = 3.64K\ \Omega$ $A_i = -14.5$

$V_{BB} = -0.886\ V$ $R_{in} = 2.91K\ W$

We now compare the results obtained Table-I for the purpose of making the best choice for $R_C$.

| | $I_{CQ}$ | $A_i$ | $R_{in}$ | $v_{out}$(p-p) |
|---|---|---|---|---|
| $R_C = R_{load}$ | -7.5 mA | -9.1 | 1.82K W | 13.5 V |
| $R_C = 0.1\ R_{load}$ | -57.4 mA | -1.64 | 327 W | 20.8 V |
| $R_C = 10\ R_{load}$ | -1.07mA | -14.5 | 2.91W | 3.9 V |

Table - 1 Comparsion for the three selections of $R_C$

It indicates that of the three given ratios of $R_C$ to $R_{load}$, $R_C = R_{load}$ has the most desirable performance in the CE amplifier stage.

It can be used as a guide to develop a reasonable designs. In most cases, this choice will provide performance that meets specifications. In some applications, it may be necessary to do additional analysis to find the optimum ratio of $R_C$ to $R_{load}$.

mplifier.

Design ofAmplifier

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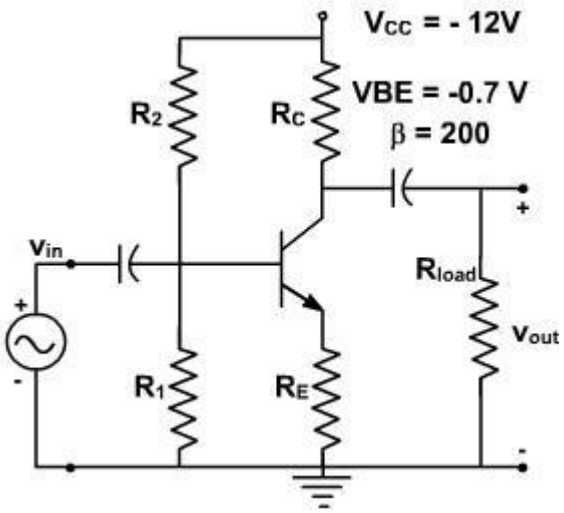


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It can be used as a guide to develop a reasonable designs. In most cases, this choice will provide performance that meets specifications. In some applications, it may be necessary to do additional analysis to find the optimum ratio of $R_C$ to $R_{load}$.

## Design ofAmplifier

Example- 3 (Capacitor-Coupled Emitter-Resistor Amplifier Design)

Design an emitter-resistor amplifier as shown in fig. 3with $A_V$ =-10, β =200 and R load = 1K Ω. A pnp transistor is used and maximum symmetrical output swing is required.

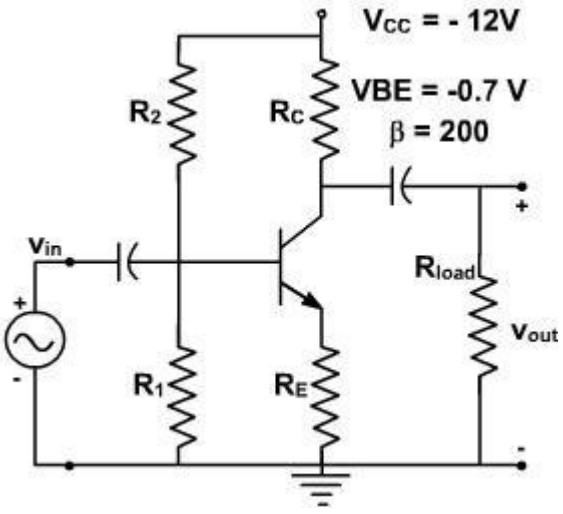



Fig. 3

Solution:

As designed earlier, we shall chose $R_C = R_{load} = 10\ k\Omega$.

The voltage gain is given by $A_v = \frac{R_{load} \parallel R_C}{R'_E}$

where $R'_E = R_E + r'_e$.

Substituting $A_V$, $R_{load}$ and $R_C$ in this equation, we find $R'_E = 50\ \Omega$.

We need to know the value of $r'_e$ to fine $R_E$. We first find $R_{ac}$ and $R_{dc}$, and then calculate the Q point as follows (we assume $r'_e$ is small, so $R_E = R'_E$)

$R_{ac} = R_E + R_C \parallel R_{load} = 550\ \Omega$

$R_{dc} = R_E + R_C = 1050\ \Omega$

Now, the first step is to calculate the quiescent collector current needed to place the Q-point into the center of the ac load line (i.e., maximum swing). The equation is

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = -7.5 \text{ mA}$$

The quantity, $r'_e$ , is found as follows

$$r_e' = \frac{25(\text{mV})}{|I_{CQ}|} = \frac{25(\text{mV})}{7.5(\text{mA})} = 3.33\Omega$$

Then

$R_E = 50 - r_e = 46.67\ \Omega$

If there were a current gain or input resistance specification for this design, we would use it to solve for the value of $R_B$. Since is no such specification, we use the expression

$R_B = 0.1\ \beta\ R_E = 0.1\ (200)\ (46.6) = 932\ \Omega$

Then continuing with the design steps,

$$A_i = \frac{-R_B}{R_B / \beta + r_E' + R_B} \cdot \frac{R_C}{R_C + R_{load}} = -8.50$$

$V_{CEQ} = V_{CC} - (R_C + R'_E)\ I_{CQ} = -4.125\ \text{V}$

and

$$V_{BB} = I_{CQ}\left(R_E + \frac{R_E}{\beta}\right) + V_{BE} = -1.08\ V$$

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = 1.02\ K\Omega$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = 10.3\ K\Omega$$

$$R_{in} = \frac{R_B(r_e + R_E)}{R_B/\beta + r_e + R_E} = 8.51\Omega$$

$$R_O = R_C = 1\ K\Omega$$

The last equality assumes that $r_O$ is large compared to $R_C$.

The maximum undistorted peak to peak output swing is given by

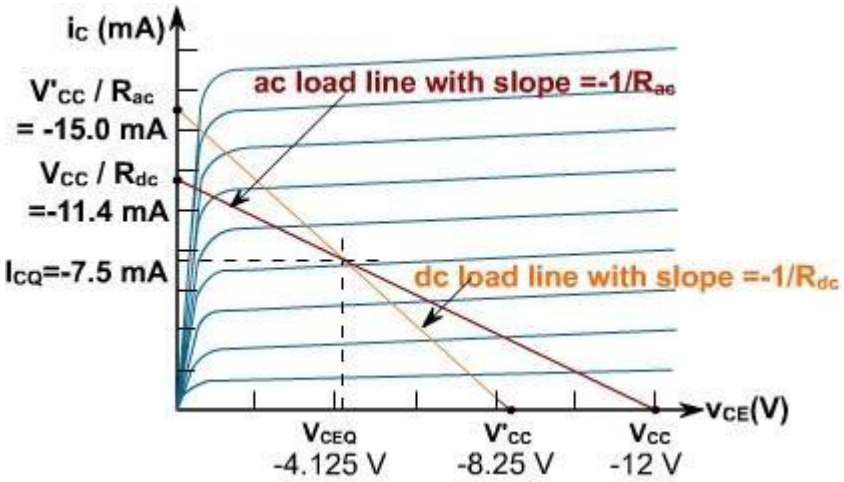
$1.8 \mid I_{CQ} \mid ( R_C \parallel R_{load} ) = 1.8 ( 0.0075 ) ( 500 ) = 6.75$ V

The power delivered into the load and the maximum power dissipated by the transistor are found as

$$P_{Load} = \frac{1}{2}\left(I_{CQ}\frac{R_C}{R_C + R_{load}}\right)^2 R_{load} = \frac{I_{CQ}^2 R_{load}}{8} = 7\ mW$$

$$P_{transistor} = V_{CEQ}I_{CQ} = (-4.125V)(-7.5mA) = 31\,mW$$

The load lines for this circuit are shown in fig. 4.




**Common Collector Amplifier:**

If a high impedance source is connected to low impedance amplifier then most of the signal is dropped across the internal impedance of the source. To avoid this problem common collector

amplifier is used in between source and CE amplifier. It increases the input impedence of the CE amplifier without significant change in input voltage.

Fig. 1, shows a common collector (CC) amplifier. Since there is no resistance in collector circuit, therefore collector is ac grounded. It is also called grounded collector amplifier. When input source drives the base, output appears across emitter resistor. A CC amplifier is like a heavily swamped CE amplifier with a collector resistor shorted and output taken across emitter resistor.

$v_{out} = v_{in} - v_{BE}$

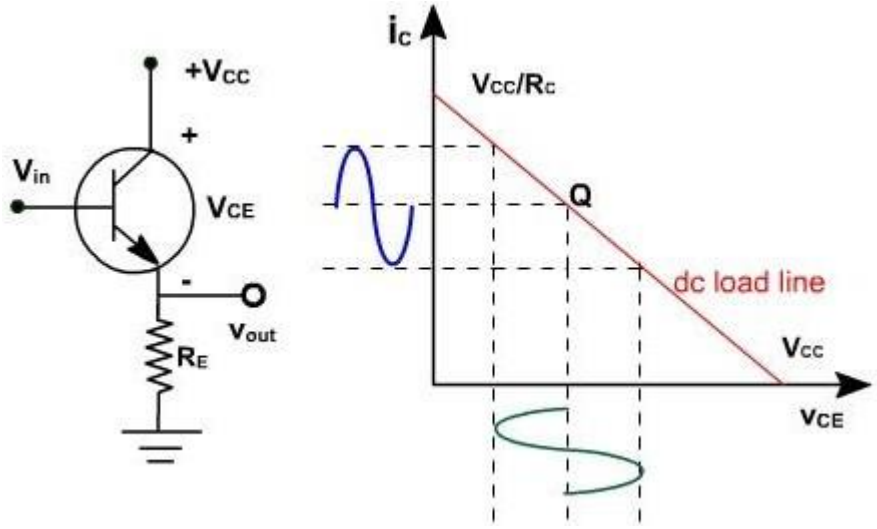



Fig. 1

Therefore, this circuit is also called emitter follower, because $V_{BE}$ is very small. As $v_{in}$ increases, $v_{out}$ increases.

If $v_{in}$ is 2V, $v_{out}$ = 1.3V

If $v_{in}$ is 3V, $v_{out}$ = 2.3V.

Since $v_{out}$ follows exactly the $v_{in}$ therefore, there is no phase inversion between input and output.

The output circuit voltage equation is given by

$V_{CE} = V_{CC} – I_E R_E$

Since $I_E = \square I_C$

$I_C = (V_{CC} – V_{CE}) / R_E$

This is the equation of dc load line. The dc load line is shown in Fig.1.

**Common CollectorAmplifier:**

Voltage gain:

Fig. 2, shows an emitter follower driven by a small ac voltage. The input is applied at the base of transistor and output is taken across the emitter resistor. Fig. 3, shows the ac equivalent circuit of the amplifier. The emitter is replaced by ac resistance $r'_e$.

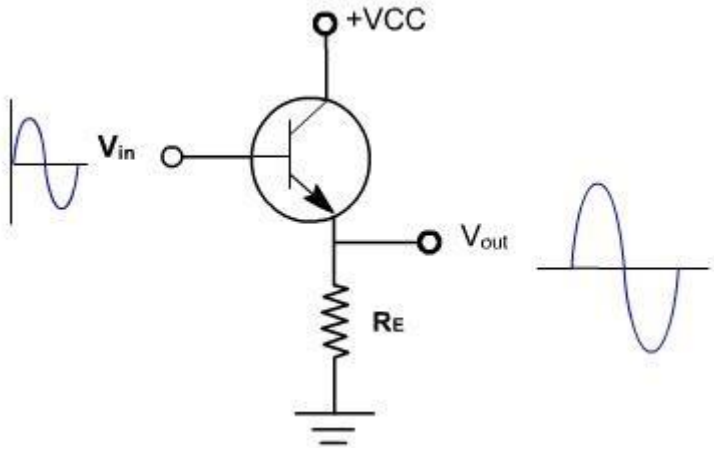



Fig. 2

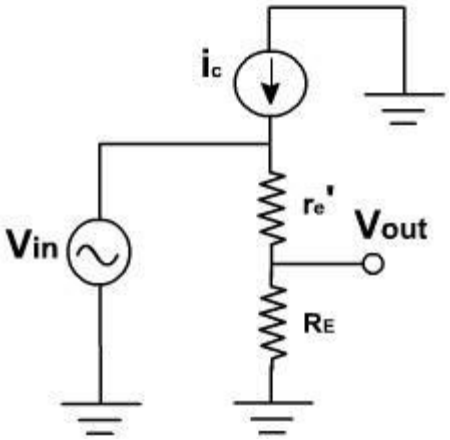



Fig. 3

The ac output voltage is given by

$v_{out} = R_E i_e$

and, $v_{in} = i_e (R_E + r'_e)$

Therefore, $A = R_E / (R_E + r'_e)$

Since $r'_e << R_E$

$\square Av = \square 1$. (approx)

Therefore, it is a unity gain amplifier. The practical emitter follower circuit is shown in Fig. 4.

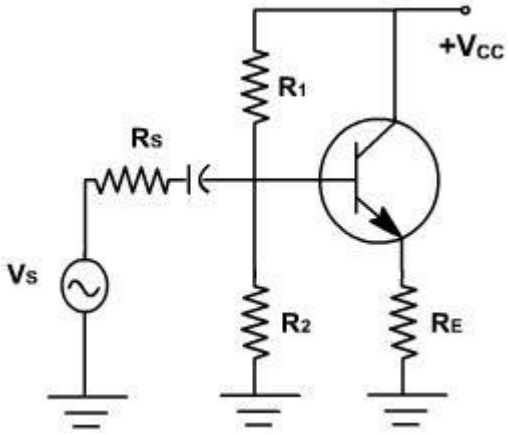



Fig. 4

The ac source ($v_S$) with a series resistance $R_S$ drives the transistor base. Because of the biasing resistor and input impedance of the base, some of the ac signal is lost across the source resistor.

The ac equivalent circuit is shown in Fig. 5.

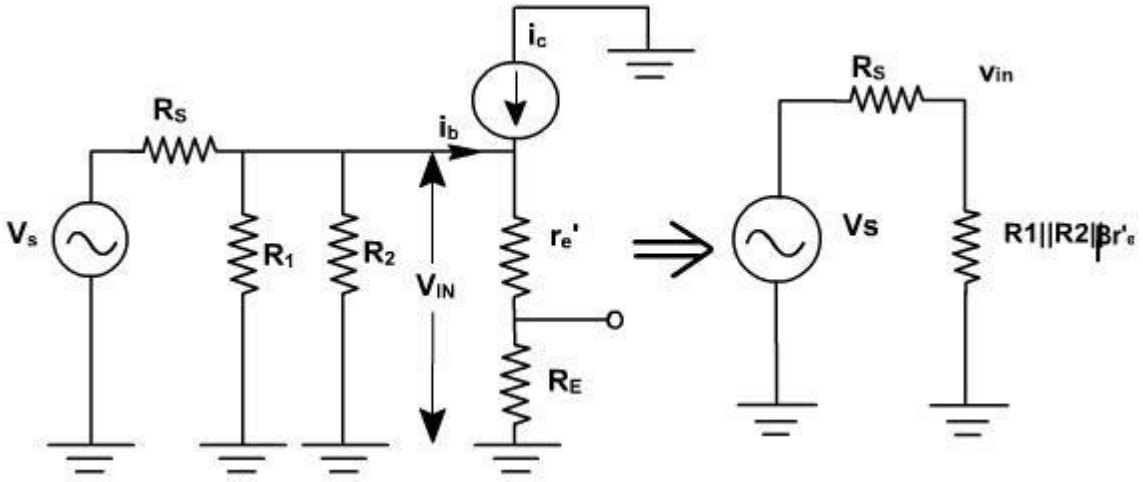



Fig. 5

The input impedance at the base is given by

$$Z_{in(base)} = \frac{v_{in}}{i_B}$$
$$= \frac{i_e(r'_e + R_E)}{i_b}$$
$$= \frac{\beta i_b(r'_e + R_E)}{i_b}$$
$$= \beta(r'_e + R_E)$$

Since $r'_e$ is very small in comparison with $R_E$

$$\therefore Z_{in(base)} \approx \beta R_E$$

The total input impedance of an emitter follower includes biasing resistors in parallel with input impedance of the base.

$z_{in} = R_1 \parallel R_2 \parallel (r'_e + R_E)$

Since $R_E$ is very large as compared to $R_1$ and $R_2$.

Thus, $z_{in} \approx R_1 \parallel R_2$

Therefore input impedance is very high.

Applying Thevenin's theorem to the base circuit of Fig. 5, it becomes a source $v_{in}$ and a series resistance ($R_1 \parallel R_2 \parallel R_S$) as shown in Fig. 6.

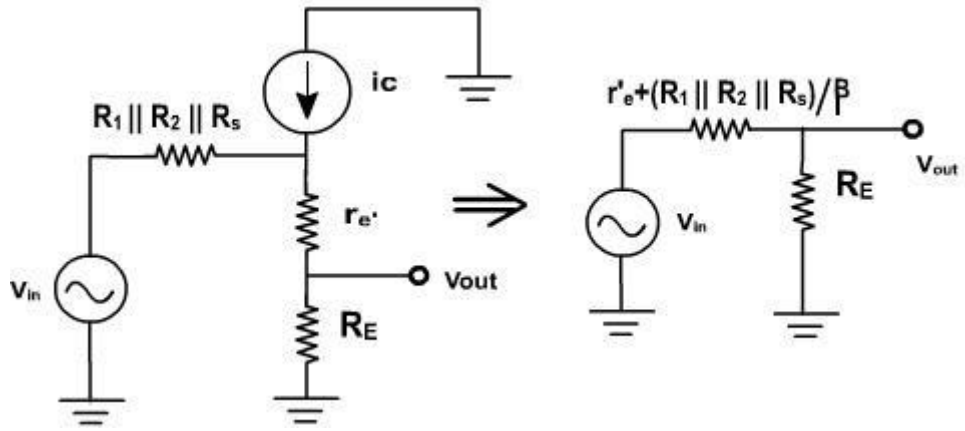



Fig. 6

$$v_{in} = (R_1 \| R_2 \| R_S) + i_e\ (r'_e + R_E)$$

$$\text{or,} \quad i_e = \frac{V_{in}}{R_E + r'_e + \dfrac{R_1 \| R_2 \| R_S}{\beta}}$$

The emitter resistor $R_E$ is driven by an ac source with output impedance of

$$Z_{out} = r'_e + \frac{R_1 \| R_2 \| R_S}{\beta}$$

The impedance of the amplifier seen from the output terminal is given by

$$Z = R_E \| \ r'_e + \frac{R_1 \| R_2 \| R_S}{\beta}$$

The ouput voltage is given by

$$V_{out} = A v_{in}$$

$$= \frac{R_E}{R_E + r'_e + \dfrac{R_1 \| R_2 \| R_S}{\beta}} v_{in}$$

$$\approx v_{in} \quad (\text{if } R_E \text{ is very larage})$$

**Common CollectorAmplifier**

**Example 1:**

Find the Q-point of the emitter follower circuit of **fig. 7**with $R_1$ = 10 KΩ and $R_2$ = 20 KΩ. Assume the transistor has a β of 100 and input capacitor C is very-very large.

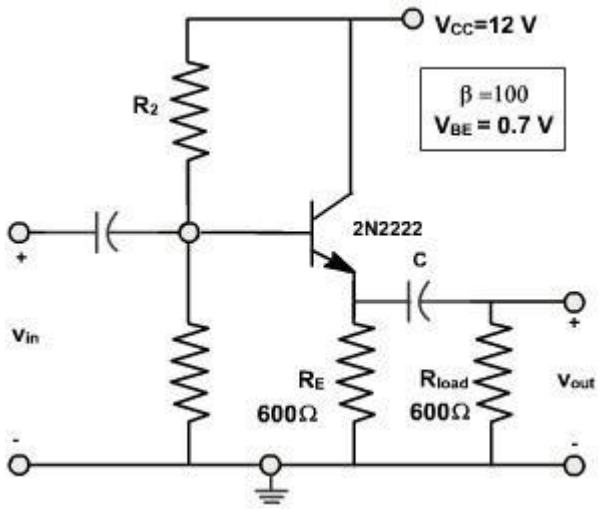



**Fig. 7**

**Solution:**

We first find the Thevenin's equivalent of the base bias circuitry.

$R_B = R_1 \parallel R_2 = 6.67\ K\ \Omega$

$$V_{BB} = \frac{R_1 V_{CC}}{R_1 + R_2} = \frac{12(10^4)}{30x10^3} = 4\ V$$

From the bias equation we have

$$I_C = I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E} = \frac{4 - 0.7}{6670/100 + 600} = 4.95\ mA$$

**Example - 2**

Find the output voltage swing of the circuit of **fig. 7**.

**Solution:**

The Q-Point location has already been calculated in **Example-1**. We found that the quiescent collector current is 4.95 mA.

The Output voltage swing = 2 **.** $I_C$ peak **.** ($R_E \parallel R_{Load}$) = $2(4.95 \times 10^{-3})$ (300) = 2.97V

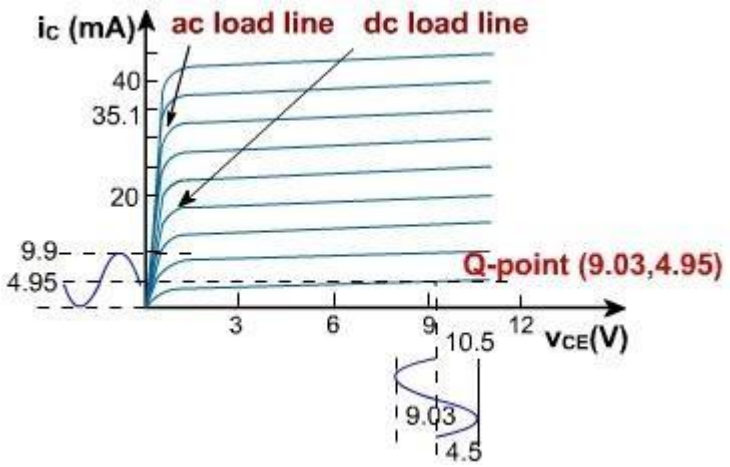
This is less than the maximum possible output swing. Continuing the analysis,

$V_{CEQ} = V_{CC} - I_{CQ} R_E = 9.03$ V

$V'_{CC} = V_{CEQ} + I_{CQ} (R_E \parallel R_{Load}) = 10.5$ V

$$I'_{CC} = \frac{10.5}{300} = 35.1 \text{ mA}$$

The load lines for this problem are shown in **Fig. 8**.




**CLASSIFICATION OF AMPLIFIERS:**

A circuit that increases the amplitude of the given input signal is an amplifier.A small ac signal fed to the amplifier is obtained as a larger ac signal of the same frequency at the output.Amplifiers constitute an essential part of radio,television and other communication circuits.Depending on the nature and level of amplification and the impedance matching requirements different types of amplifiers can be considered and they are discussed in this chapter.

Amplifiers can be classified as follows:

1.Based on the transistor configuration

(a) Common emitteramplifier

(b) Common baseamplifier

(c ) Common emitter amplifier

2. Based on the active devices

   (a) BJTamplifier

   (b) FETamplifier

3. Based on the Q-point(operatingcondition)

   (a) Class Aamplifier

   (b) Class Bamplifier

   (c) Class Camplifier

   (d) Class AB amplifier

4. Based on the number ofstages

   (a) Single stageamplifiers

   (b) Multistageamplifiers

5. Based on theoutput

   (a)Voltage amplifiers

   (b)Power amplifiers

6. Based on the frequency response

   (a)Audio frequency(AF) amplifier

   (b)Intermediate Frequencyamplifier(IF)

   (c )Radio Frequencyamplifier(RF)

7. Based on thebandwidth

   (a) Narrow band amplifier(normally RF amplifier)

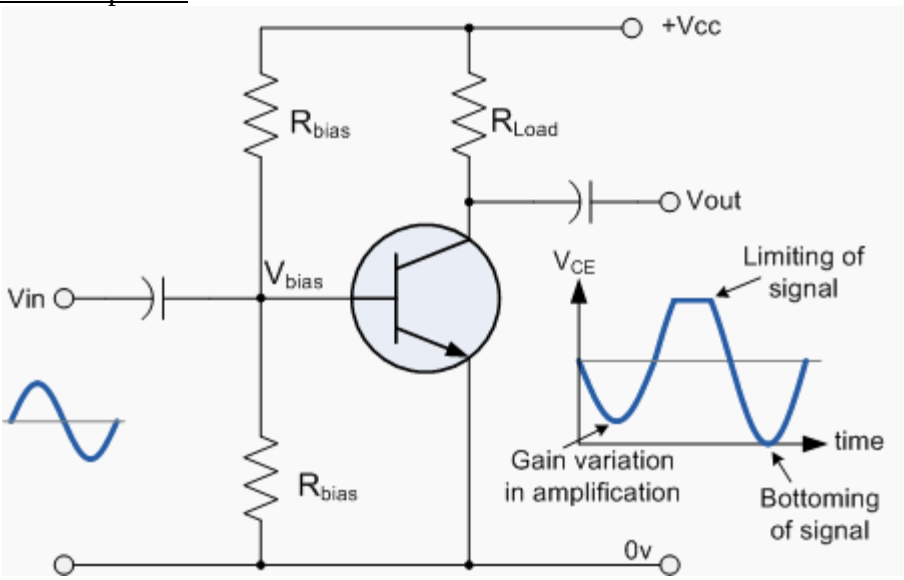
(b) Wide band amplifier(normally videoamplifier)

**Distortion in amplifiers:**

## Amplifier Distortion

From the previous tutorials we learnt that for a signal amplifier to work correctly it requires some form of DC Bias on its Base or Gate terminal so that it amplifies the input signal over its entire cycle with the bias "Q-point" set as near to the middle of the load line as possible. This then gave us a "Class-A" type amplification with the most common configuration being Common Emitter for Bipolar transistors and Common Source for unipolar transistors. We also saw that the Power, Voltage or Current Gain, (amplification) provided by the amplifier is the ratio of the peak input value to its peak output value. However, if we incorrectly design our amplifier circuit and set the biasing Q-point at the wrong position on the load line or apply too large an input signal, the resultant output signal may not be an exact reproduction of the original input signal waveform. In other words the amplifier will suffer from distortion. Consider the common emitter amplifier circuit below.

Common Emitter Amplifier




Distortion of the signal waveform may take place because:

1. Amplification may not be taking place over the whole signal cycle due to incorrectbiasing.

2. The input signal may be too large, causing the amplifier tolimit.

3. The amplification may not be linear over the entire frequency range ofinputs.

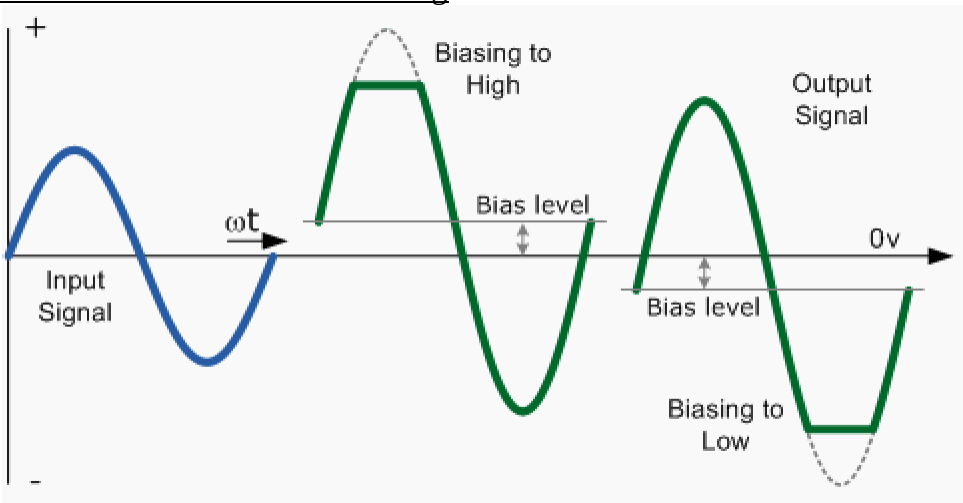
This means then that during the amplification process of the signal waveform, some form of Amplifier Distortion has occurred.

Amplifiers are basically designed to amplify small voltage input signals into much larger output signals and this means that the output signal is constantly changing by some factor or value times the input signal for all input frequencies. We saw previously that this multiplication factor is called the Beta, β value of the transistor. Common emitter or even common source type transistor circuits work fine for small AC input signals but suffer from one major disadvantage, the bias Q-point of a bipolar amplifier depends on the same Beta value which may vary from transistors of the same type, ie. the Q-point for one transistor is not necessarily the same as the Q-point for another transistor of the same type due to the inherent manufacturing tolerances. If this occurs the amplifier may not be linear and Amplitude Distortion will result but careful choice of the transistor and biasing components can minimise the effect of amplifierdistortion.

Amplitude Distortion

Amplitude distortion occurs when the peak values of the frequency waveform are attenuated causing distortion due to a shift in the Q-point and amplification may not take place over the whole signal cycle. This non-linearity of the output waveform is shown below.

Amplitude Distortion due to Incorrect Biasing



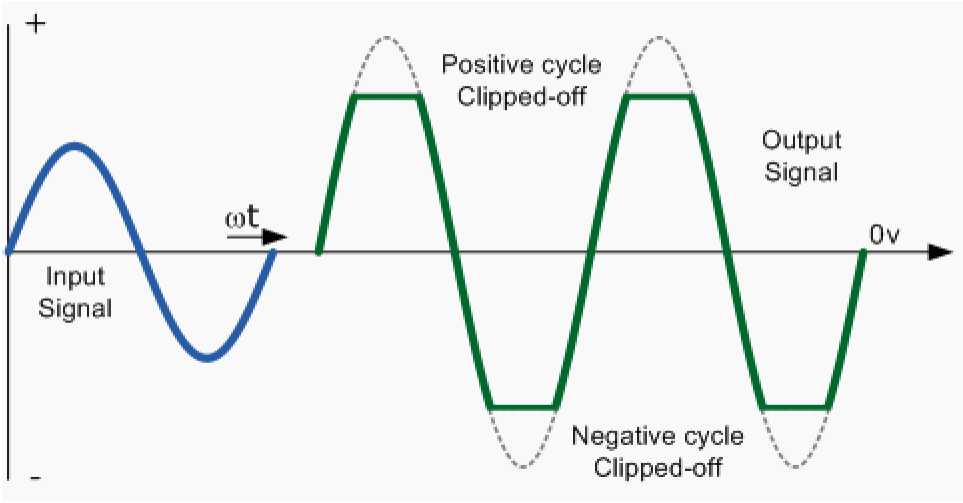

If the bias is correct the output waveform should look like that of the input waveform only bigger, (amplified). If there is insufficient bias the output waveform will look like the one on the right with the negative part of the output waveform "cut-off". If there is too much bias the output

waveform will look like the one on the left with the positive part "cut-off". When the bias voltage is too small, during the negative part of the cycle the transistor does not conduct fully so the output is set by the supply voltage. When the bias is too great the positive part of the cycle saturates the transistor and the output drops almost to zero.

Even with the correct biasing voltage level set, it is still possible for the output waveform to become distorted due to a large input signal being amplified by the circuits gain. The output voltage signal becomes clipped in both the positive and negative parts of the waveform an no longer resembles a sine wave, even when the bias is correct. This type of amplitude distortion is called Clipping and is the result of "Over-driving" the input of the amplifier.

When the input amplitude becomes too large, the clipping becomes substantial and forces the output waveform signal to exceed the power supply voltage rails with the peak (+ve half) and the trough (-ve half) parts of the waveform signal becoming flattened or "Clipped-off". To avoid this the maximum value of the input signal must be limited to a level that will prevent this clipping effect as shown above.

Amplitude Distortion due to Clipping




Amplitude Distortion greatly reduces the efficiency of an amplifier circuit. These "flat tops" of the distorted output waveform either due to incorrect biasing or over driving the input do not contribute anything to the strength of the output signal at the desired frequency. Having said all that, some well known guitarist and rock bands actually prefer that their distinctive sound is highly distorted or "overdriven" by heavily clipping the output waveform to both the +ve and -ve power supply rails. Also, excessive amounts of clipping can also produce an output which resembles a "square wave" shape which can then be used in electronic or digital circuits.

We have seen that with a DC signal the level of gain of the amplifier can vary with signal amplitude, but as well as Amplitude Distortion, other types of distortion can occur with AC signals in amplifier circuits, such as Frequency Distortion and Phase Distortion.

## Frequency Distortion

Frequency Distortion occurs in a transistor amplifier when the level of amplification varies with frequency. Many of the input signals that a practical amplifier will amplify consist of the required signal waveform called the "Fundamental Frequency" plus a number of different frequencies called "Harmonics" superimposed onto it. Normally, the amplitude of these harmonics are a fraction of the fundamental amplitude and therefore have very little or no effect on the output waveform. However, the output waveform can become distorted if these harmonic frequencies increase in amplitude with regards to the fundamental frequency. For example, consider the waveform below:

## Frequency Distortion due to Harmonics

In the example above, the input waveform consists a the fundamental frequency plus a second harmonic signal. The resultant output waveform is shown on the right hand side. The frequency distortion occurs when the fundamental frequency combines with the second harmonic to distort the output signal. Harmonics are therefore multiples of the fundamental frequency and in our simple example a second harmonic was used. Therefore, the frequency of the harmonic is 2 times the fundamental, 2 x f or 2f. Then a third harmonic would be 3f, a fourth, 4f, and so on. Frequency distortion due to harmonics is always a possibility in amplifier circuits containing reactive elements such as capacitance or inductance.

## Phase Distortion

Phase Distortion or Delay Distortion occurs in a non-linear transistor amplifier when there is a time delay between the input signal and its appearance at the output. If we call the phase change between the input and the output zero at the fundamental frequency, the resultant phase angle delay will be the difference between the harmonic and the fundamental. This time delay will depend on the construction of the amplifier and will increase progressively with frequency within the bandwidth of the amplifier. For example, consider the waveform below:

Phase Distortion due to Delay

Any practical amplifier will have a combination of both "Frequency" and "Phase" distortion together with amplitude distortion but in most applications such as in audio amplifiers or power amplifiers, unless the distortion is excessive or severe it will not generally affect the operation of the system.

# FET AMPLIFIERS

## 5.4.0 INTRODUCTION

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain and high input impedence. Because of high input impedence and other characteristics of JFETs they are preferred over BJTs for certain types of applications.

There are 3 basic FET circuit configurations:

i)Common Source

ii)Common Drain

iii)Common Gain

Similar to BJT CE,CC and CB circuits, only difference is in BJT large output collector current is controlled by small input base current whereas FET controls output current by means of small input voltage. In both the cases output current is controlled variable.

FET amplifier circuits use voltage controlled nature of the JFET. In Pinch off region, $I_D$ depends only on $V_{GS}$.

## Common Source (CS)Amplifier

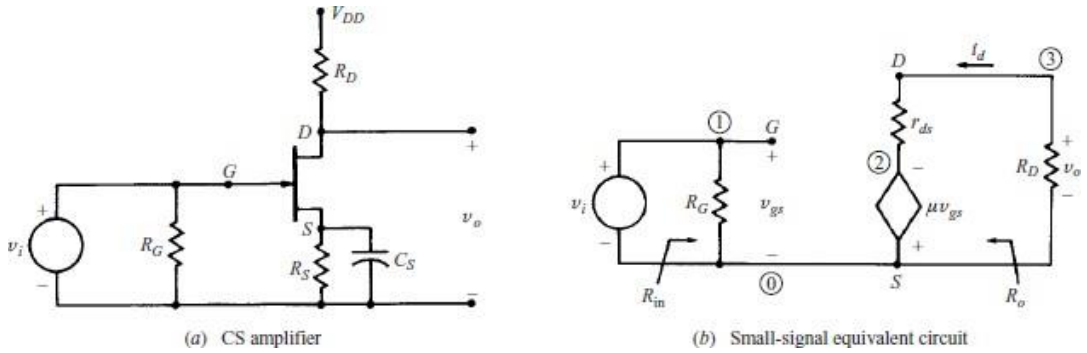



Fig. 7.1 (a) CS Amplifier (b) Small-signal equivalent circuit

A simple Common Source amplifier is shown in Fig. 7.1(a) and associated small signal equivalent circuit using voltage-source model of FET is shown in Fig. 7.1(b)

**Voltage Gain**

Source resistance ($R_S$) is used to set the Q-Point but is bypassed by $C_S$ for mid-frequency operation. From the small signal equivalent circuit ,the output voltage

$$V_O = -R_D \mu V_{gs}(R_D + r_d)$$

Where $V_{gs} = V_i$ , the input voltage,

Hence, the voltage gain,

$$A_V = V_O / V_i = -R_D \mu (R_D + r_d)$$

**Input Impedence**

From Fig. 7.1(b) Input Impedence is

$$Z_{i} = R_G$$

For voltage divider bias as in CE Amplifiers of BJT

$$R_G = R_1 \parallel R_2$$

**Output Impedance**

Output impedance is the impedance measured at the output terminals with the input voltage $V_I$ = 0

From the Fig. 7.1(b) when the input voltage $V_i = 0$, $V_{gs} = 0$ and hence

$$\mu V_{gs} = 0$$

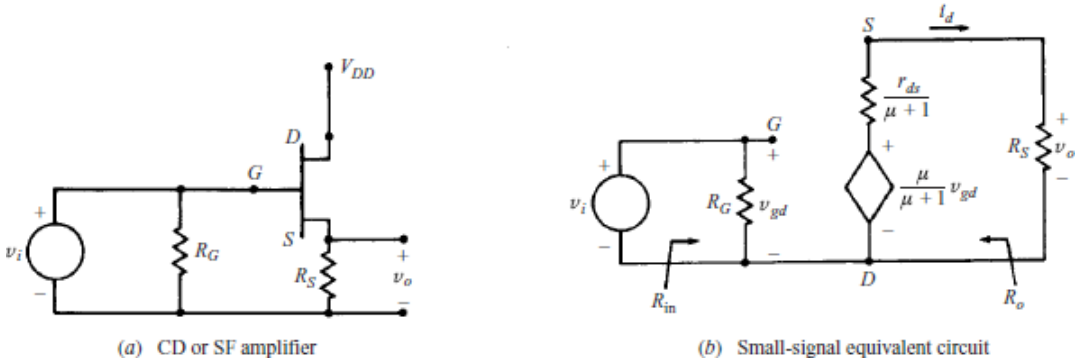
The equivalent circuit for calculating output impedence is given in Fig. 7.2.

Output impedence $Z_o = r_d \parallel R_D$

Normally $r_d$ will be far greater than $R_D$ . Hence $Z_o \approx R_D$

## Common DrainAmplifier

A simple common drain amplifier is shown in Fig. 7.2(a) and associated small signal equivalent circuit using the voltage source model of FET is shown in Fig. 7.2(b).Since voltage $V_{gd}$ is more easily determined than $V_{gs}$, the voltage source in the output circuit is expressed in terms of $V_{gs}$ and Thevenin's theorem.




(a) CD or SF amplifier (b) Small-signal equivalent circuit

Fig. 7.2 (a)CD Amplifier (b)Small-signal equivalent circuit

**Voltage Gain**

The output voltage,

$$V_O = R_S \mu V_{gd} / (\mu + 1) R_S + r_d$$

Where $V_{gd} = V_i$ the inputvoltage.

Hence, the voltage gain,

$$A_v = V_O / V_i = R_S \mu / (\mu + 1) R_S + r_d$$

**Input Impedence**

From Fig. 7.2(b), Input Impedence $Z_i = R_G$

**Output Impedence**

From Fig. 7.2(b), Output impedence measured at the output terminals with input voltage $V_i = 0$ can be calculated from the following equivalent circuit.

As $V_i = 0$: $V_{gd} = 0$: $\mu v_{gd} / (\mu + 1) = 0$

Output Impedence

$$Z_O = r_d / (\mu + 1) \parallel R_S$$

When $\mu \gg 1$

$$Z_O = ( r_d / \mu) \parallel R_S = (1/g_m) \parallel R_S$$

## BIASINGFET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage $V_{GS}$ and drain current $I_D$ which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuitsThe main difference between JFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

1. Selfbias
2. Voltage dividerbias.

## 5.5.1. SELF BIAS:-

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate.

A self bias circuit is shown in the fig 7.3

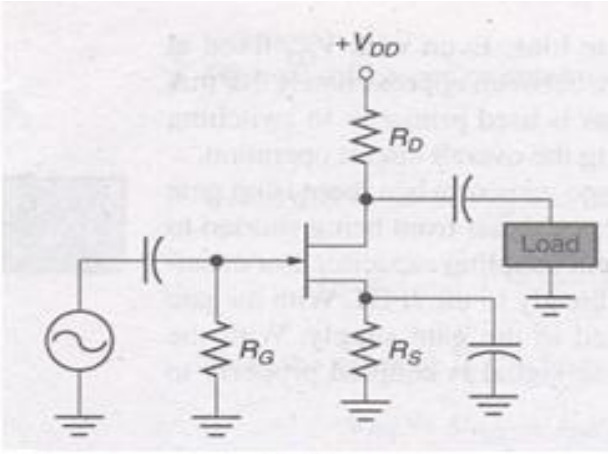



fig 7.3

Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative $V_{GS}$ for an N channel JFET and a positive $V_{GS}$ for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig 7.3. The gate resistor $R_G$ doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V .$R_G$ is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor $R_S$ makes gate source junction reversebiased.

**DC analysis of self Bias:-**

In the following DC analysis , the N channel J FET shown in the fig7.4. is used for illustration.

ForDCanalysiswecanreplacecouplingcapacitorsbyopencircuitsand we canalsoreplace the resistor $R_G$ by a short circuitequivalent.

:. $I_G = 0$

The relation between $I_D$ and $V_{GS}$ is given by

$$Id=Idss[1-\frac{Vgs}{Vp}]^2$$

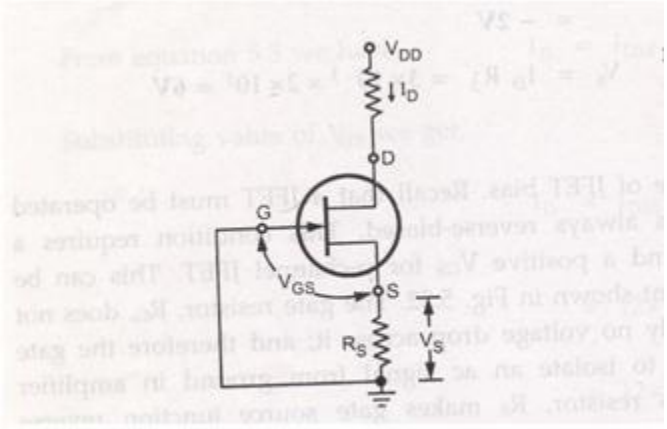



fig 7.4

$V_{GS}$ for N channel JFET is =-id Rs

Substuting this value in the above equation

$$Id=Idss[1-\frac{(-IdRs)}{Vp}]^2$$

$$Id=Idss[1+\frac{(IdRs)}{Vp}]^2$$

For the N-chanel FET in the above figure

Is produces a voltage drop across Rs and makes the source positive w.r.t ground

in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current

therefore we can define source current as Is=Id and Vg=0 then

Vs= Is Rs =IdRs

Vgs=Vg-Vs=0-IdRs=-IdRs

**Drawing the self bias line:-**

Typical transfer characteristics for a self biased JFET are shown in the fig7.5.

The maximum drain current is 6mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

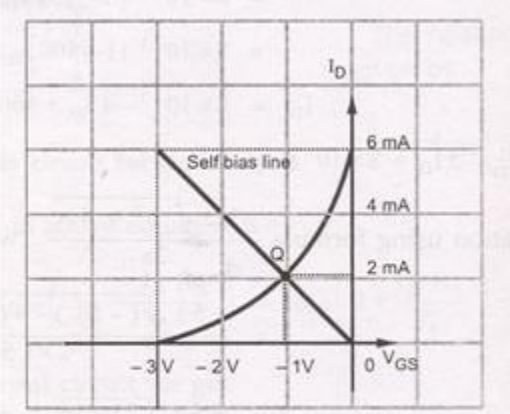



fig 7.5 Transfer characteristics

Now using the equation $V_{GS} = -I_D R_S$ and assuming $R_S$ of any suitable value we can draw the self bias line.

Let us assume RS = 500Ω

With this Rs , we can plot two points corresponding to $I_D = 0$ and Id = $I_{DSS}$

for $I_D = 0$

$V_{GS} = -I_D R_S$

$V_{GS} = 0X (500.Ω) = 0V$

So the first point is (0 ,0)

( $I_d$, $V_{GS}$)

For $I_D = I_{DSS} = 6mA$

$V_{GS} = (-6mA) (500 Ω) = -3V$

So the 2nd Point will be (6mA,-3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line. The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point , the $I_D$ is slightly > than 2mA and $V_{GS}$ is slightly > -1V. The Q point for the self bias JFET depends on the value of Rs.If Rs is large, Q point far down on the transconductance curve ,$I_D$ is small, when Rs is small Q point is far up on the curve , $I_D$ is large.

## 5.5.2 VOLTAGE DIVIDER BIAS:-

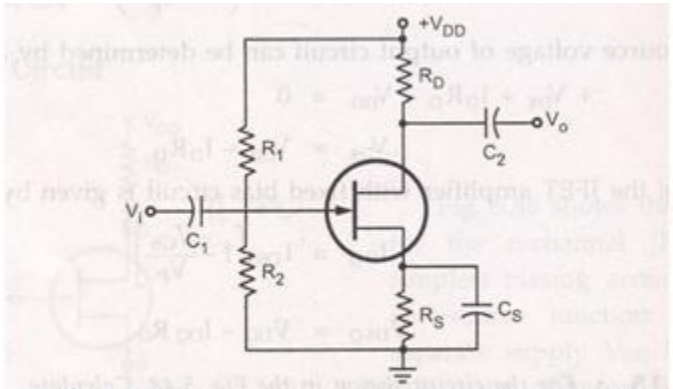



fig 7.6 **Voltage divider bias for n-channel JFET**

The fig7.6 shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltageis

$V_S = I_D R_S$

The gate voltage is set by resistors R1 and R2 as expressed by the following equation using the voltage divider formula.

$$Vg=\left(\frac{R2}{(R1+R2)}\right)Vdd$$

For dc analysis fig 7.7

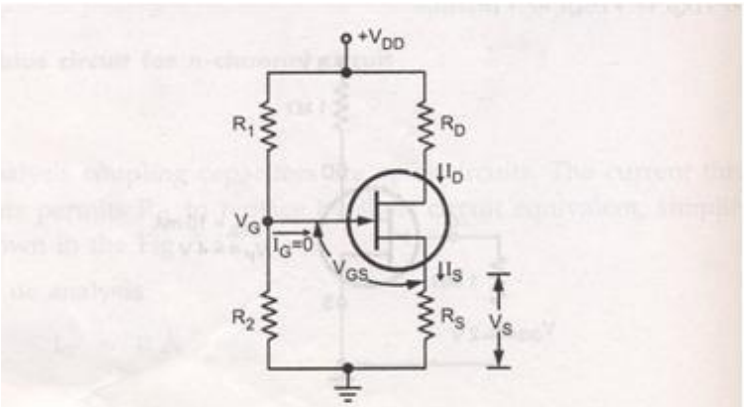



fig 7.7 **Simplified voltage divider circuit for dc analysis**

Applying KVL to the input circuit

$V_G - V_{GS} - V_S = 0$

$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$

$V_{GS} = V_G - I_D R_S \quad \therefore I_S = I_D$

Applying KVL to the input circuit we get

$V_{DS} + I_D R_D + V_S - V_{DD} = 0$

$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$

$V_{DS} = V_{DD} - I_D ( R_D + R_S )$

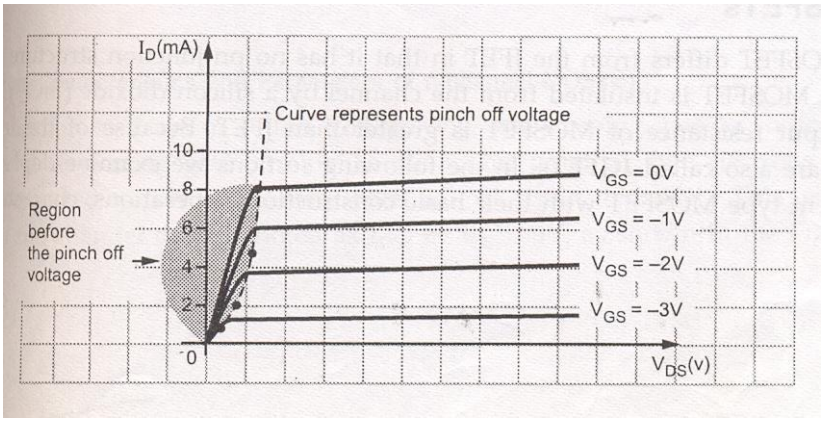
The Q point of a JFET amplifier , using the voltage divider biasis

$I_{DQ} = I_{DSS}[1 - V_{GS}/V_P]2$

$V_{DSQ} = V_{DD} - I_D ( R_D + R_S)$

## 5.6 JFET AS A VVR OR VDR:-

Let us consider the drain characteristics of FET as shown in the fig.




In this characteristics we can see that in the region before pinch off voltage, drain characteristics are linear, i.e. FET operation is linear. In this region the FET is useful as a voltage controlled resistor,i.e. the drain to source resistance is controlled by the bias voltage $V_{GS}$.( In this region only FET behaves like an ordinary resistor This resistances can be varied by $V_{GS}$ ) .The operation of FET in the region is useful in

most linear applications of FET.In such an application the FET is also referred to as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

The drain to source conductance ( rd )

$g_d=\frac{Id}{Vds}$ for small values of $V_{DS}$ which may also be expressed as

$$g_d=g_{d0}(1-(\frac{Vgs}{Vp})^{1/2})$$

Where $g_{d0}$ is the value of drain conductance

When the variation of the rd with VGS can be closely approximated by the expression

rd= $(\frac{r0}{1-KVgs})$ Where ro = drain resistance at zero gate bias.K = a constant, dependent uponFET type.

## 5.6.1 APPLICATION OF VVR

The VVR property of FET can be used to vary the voltage gain of a multistage amplifier A, as the signal level is increased. This action is called AGC automatic gain control. A typical arrangement is shown in the fig.

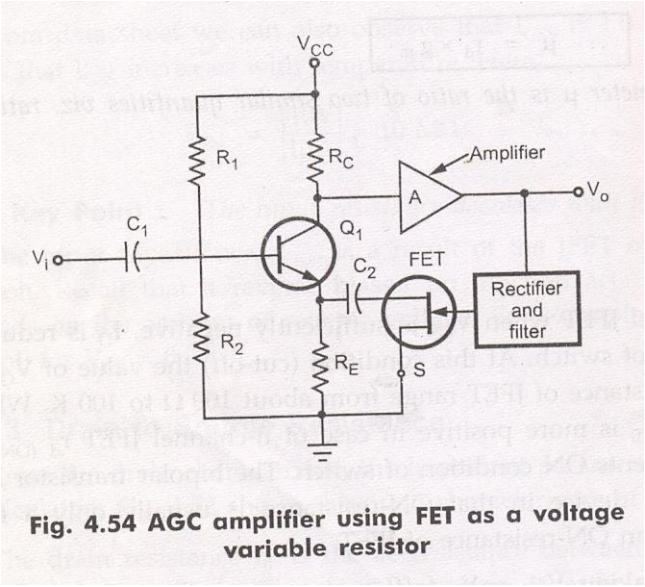



**Fig. 4.54 AGC amplifier using FET as a voltage variable resistor**

Here maximum value of signal is taken rectified; filter to produce a DC voltage proportional to the output signal level. This voltage is applied to the gate of JFET, this causing the resistance between drain and source to change. As this resistance is connected across $R_E$, so effective $R_E$ also changes

according to change in the drain to source resistance. When output signal level increases, the drain to source resistance rd increases, increasing effective $R_E$. Increase in $R_E$ causes the gain of transistor Q1 to decrease, reducing the output signal. Exactly reverse process takes place when output signal level decreased.

:: The output signal level is maintained constant. It is to be noted that the DC bias conditions of Q1 are not affected by JFET since FET is isolated from Q1 by capacitor C2