LECTURE NOTES

ON

DIGITAL AND PULSE CIRCUITS

B.Tech IV semester (IARE-R16)

Prepared By
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DIGITAL AND PULSE CIRCUITS

IV Semester: EEE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC019	Foundation	3	1	-	3	30	70	100
Contact Classes: 45	Tutorial Classes: 15	Practical Classes: Nil				Total Classes: 60		

OBJECTIVES:

This course should enable the student to:

I. Understand basics, different binary codes in digital electronic circuits and be able to convert between different codes.

II. Implement minimization techniques and state machines using flip-flops.

III. Implement and design logical operations using large scale integration and medium scale integration devices.

IV. Discuss the concept of sequential circuits and analyze sequential systems.

V. Design finite state machine and algorithmic state machines charts and memories.

UNIT-I	BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS	Classes:08

Introduction of binary numbers: Complements of numbers, codes, binary codes, binary code decimal code and its properties, unit distance codes, alpha numeric codes, error detecting and correcting codes; Boolean algebra: Basic theorems and properties, switching functions, canonical and standard form.

UNIT-II	MINIMIZATION TECHNIQUES AND DESIGN OF MSI	Classes:10

Minimization with theorem: Karnaugh map method, five variable map, prime and essential implications, don‘t care map entries, tabular method, partially specified expressions; combination all design: Arithmetic circuits, comparator, multiplexers, code converters, hazards and hazard free relations.

UNIT-III	SEQUENTIAL CIRCUITS DESIGN	Classes: 08

Basic differences between combinational and sequential logic circuits, binary cell, fundamentals of sequential machine operation, D Flip Flop, T Flip Flop, J K Flip Flop, design procedure for conversion of Flip Flops, conversion from one type of Flip-Flop to another, timing and triggering consideration, clock skew.

Counters: Design of single mode counter, ripple counter, ring counter, shift register, shift register sequences, ring counter using shift register.

UNIT-IV	FEEDBACK AMPLIFIERS AND OSCILLATORS	Classes: 10

Feedback Amplifiers: Concepts of feedback, classification of feedback amplifiers, general characteristics of negative feedback amplifiers, effect of feedback on amplifier characteristics, voltage series, voltage shunt; Current series; Current shunt feedback configurations, illustrative examples; Oscillators: Classification of oscillators, condition for oscillations, RC phase shift oscillators; Generalized analysis of LC oscillators: Hartley and Colpitts oscillators, Wien Bridge and crystal oscillators, stability of oscillators.

UNIT-V	SINGLE STAGE AMPLIFIERS AND MULTISTAGE AMPLIFIERS	Classes: 09

Single Stage Amplifiers: Classification of amplifiers, distortion in amplifiers, analysis of CE, CC and CB configurations with simplified hybrid model, analysis of CE amplifier with emitter resistance and emitter follower, Miller‘s theorem and its dual design of single stage RC coupled amplifier using BJT; Multistage amplifiers: Analysis of cascaded RC coupled BJT amplifiers, cascade amplifier, darlington pair, different coupling schemes used in amplifiers RC coupled amplifiers, transformer coupled amplifier, direct coupled amplifier.

Text Books:

1. M Morris Mano, Michael D Ciletti, –Digital Design", Pearson Education / PHI, 3rd Edition, 2008.
2. Fletcher W I, –An Engineering Approach to Digital Design‖, Prentice Hall India Learning Private Limited, 1990.
3. Zvi Kohavi, –Switching and Finite Automata Theory‖, Tata McGraw-Hill, 3rd Edition, 2004.
4. John M Yarbrough, –Digital logic applications and design‖, Thomson publications, 1st Edition, 2006.
5. J Millman, C C Halkias, –Integrated Electronics‖, Tata McGraw -Hill, 2008.

Reference Books:

1. Fredriac J Hill, Gerald R Peterson, –Introduction to Switching Theory and Logic Design‖, 3rd Edition, 2008.
2. Thomas L Floyd, –Digital Fundamentals‖, Pearson Publications, 10th Edition, 2013.
3. Roth, –Fundamentals of Logic Design‖, Thomson Publications,7th Edition, 2004
4. Comer, –Digital Logic and State machine Design‖, Oxford Publications, 3rd Edition, 2013.
5. Rashid, –Electronic Circuit Analysis‖, Cengage Publishers, 12th Edition,2013
6. Robert L Boylestad, Louis Nashelsky, –Electronic Devices and Circuits Theory‖, PHI, 9th Edition, 2008.

Web References:

1. https://www.mcsbzu.blogspot.com
2. https://www.books.askvenkat.com
3. https://www.web02.gonzaga.edu
4. https://www.daenotes.com
5. https://www.worldclassprogramme.com
6. https://www.cse.psu.edu

E-Text Books:

1. https://www.springer.com/us/book/9780387285931
2. https://www.books.askvenkat.com/2016/01/switching-theory-and-logic-design-textbook-by-anandkumar.html
3. https://www.freebookcentre.net/Electronics/Electronic-Circuits-Books.html

Course Home Page:

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UNIT 1

BOOLEAN ALGEBRA AND SWITCHING FUNCTIONS

- Philosophy of number systems
- Complement representation of negative numbers
- Binary arithmetic
- Binary codes
- Error detecting & error correcting codes _ Hamming codes

HISTORY OF THE NUMERAL SYSTEMS:

A **numeral system** (or **system of numeration**) is a linguistic system and mathematical notation for representing numbers of a given set by symbols in a consistent manner. For example, It allows the numeral "11" to be interpreted as the binary numeral for *three*, the decimal numeral for *eleven*, or other numbers in different bases. Ideally, a numeral system will:

- Represent a useful set of numbers (e.g. all whole numbers, integers, or real numbers)
- Give every number represented a unique representation (or at least a standard representation) – Reflect the algebraic and arithmetic structure of the numbers.

For example, the usual decimal representation of whole numbers gives every whole number a unique representation as a finite sequence of digits, with the operations of arithmetic (addition, subtraction, multiplication and division) being present as the standard algorithms of arithmetic. However, when decimal representation is used for the rational or real numbers, the representation is no longer unique: many rational numbers have two numerals, a standard one that terminates, such as 2.31, and another that recurs, such as 2.309999999... . Numerals which terminate have no non-zero digits after a given position. For example,numerals like **2.31 and 2.310 are taken** to be the same, except in the experimental sciences, where greater precision is denoted by the trailing zero.

The most commonly used system of numerals is known as Hindu-Arabic numerals.Great Indian mathematicians Aryabhatta of Kusumapura (5th Century) developed the place value notation.

Brahmagupta (6th Century) introduced the symbol zero.

BINARY

The ancient Indian writer Pingala developed advanced mathematical concepts for describing prosody, and in doing so presented the first known description of a binary numeral system.A full set of 8 trigrams and 64 hexagrams, analogous to the 3-bit and 6-bit binary numerals, were known to the ancient Chinese in the classic text *I Ching*. An arrangement of the hexagrams of the *I Ching*, ordered according to the values of the corresponding binary numbers (from 0 to 63), and a method for

generating thesame, was developed by the Chinese scholar and philosopher Shao Yong in the 11th century

In 1854, British mathematician George Boole published a landmark paper detailing an algebraic system of logic that would become known as Boolean algebra. His logical calculus was to become instrumental in the design of digital electronic circuitry. In 1937, Claude Shannon produced his master's thesis at MIT that implemented Boolean algebra and binary arithmetic using electronic relays and switches for the first time in history. Entitled *A SymbolicAnalysis of Relay and Switching Circuits*, Shannon's thesis essentially founded practical digital circuit design.

Binary codes

Binary codes are codes which are represented in binary system with modification from the original ones.

- Weighted Binary codes
- Non Weighted Codes

Weighted binary codes are those which obey the positional weighting principles, each position of the number represents a specific weight. The binary counting sequence is an example.

Decimal	BCD 8421	Excess-3	84-2-1	2421	5211	Bi-Quinary 5043210			5	0	4	3	2	1	0
0	0000	0011	0000	0000	0000	0100001		0		X					X
1	0001	0100	0111	0001	0001	0100010		1		X				X	
2	0010	0101	0110	0010	0011	0100100		2		X			X		
3	0011	0110	0101	0011	0101	0101000		3		X		X			
4	0100	0111	0100	0100	0111	0110000		4		X	X				
5	0101	1000	1011	1011	1000	1000001		5	X						X
6	0110	1001	1010	1100	1010	1000010		6	X					X	
7	0111	1010	1001	1101	1100	1000100		7	X				X		
8	1000	1011	1000	1110	1110	1001000		8	X			X			
9	1001	1111	1111	1111	1111	1010000		9	X		X				

Reflective Code

A code is said to be reflective when code for 9 is complement for the code for 0, and so is for 8 and 1 codes, 7 and 2, 6 and 3, 5 and 4. Codes 2421, 5211, and excess-3 are reflective, whereas the 8421 code is not.

Sequential Codes

A code is said to be sequential when two subsequent codes, seen as numbers in binary

representation, differ by one. This greatly aids mathematical manipulation of data. The 8421 and Excess-3 codes are sequential, whereas the 2421 and 5211 codes are not.

Non weighted codes

Non weighted codes are codes that are not positionally weighted. That is, each position within the binary number is not assigned a fixed value. Ex: Excess-3 code

Excess-3 Code

Excess-3 is a non weighted code used to express decimal numbers. The code derives its name from the fact that each binary code is the corresponding 8421 code plus 0011(3).

Gray Code

The gray code belongs to a class of codes called minimum change codes, in which only one bit in the code changes when moving from one code to the next. The Gray code is non-weighted code, as the position of bit does not contain any weight. The gray code is a reflective digital code which has the special property that any two subsequent numbers codes differ by only one bit. This is also called a unitdistance code. In digital Gray code has got a special place.

Decimal Number	Binary Code	Gray Code	Decimal Number	Binary Code	Gray Code
0	0000	0000	8	1000	1100
1	0001	0001	9	1001	1101
2	0010	0011	10	1010	1111
3	0011	0010	11	1011	1110
4	0100	0110	12	1100	1010
5	0101	0111	13	1101	1011
6	0110	0101	14	1110	1001
7	0111	0100	15	1111	1000

Binary to Gray Conversion

- Gray Code MSB is binary code MSB.
- Gray Code MSB-1 is the XOR of binary code MSB and MSB-1.
- MSB-2 bit of gray code is XOR of MSB-1 and MSB-2 bit of binary code.
- MSB-N bit of gray code is XOR of MSB-N-1 and MSB-N bit of binary code.**Error detection codes**

1) Parity bits

A **parity bit** is a bit that is added to a group of source bits to ensure that the number of set bits (i.e., bits with value 1) in the outcome is even or odd. It is a very simple scheme that can be used to detect single or any other odd number (i.e., three, five, etc.) of errors in the output. An even number of flipped bits will make the parity bit appear correct even though the data is erroneous.

2) Checksums

A **checksum** of a message is a modular arithmetic sum of message code words of a fixed word length (e.g.,byte values). The sum may be negated by means of a one's-complement prior to transmission to detect errorsresulting in all-zero messages.Checksum schemes include parity bits, check digits, and longitudinal redundancy checks. Some checksum schemes, such as the Luhn algorithm and the Verhoeff algorithm, are specifically designed to detect errorscommonly introduced by humans in writing down or remembering identification numbers.

3) Cyclic redundancy checks (CRCs)

A **cyclic redundancy check (CRC)** is a single-burst-error-detecting cyclic code and non-secure hash function designed to detect accidental changes to digital data in computer networks. It is characterized by specification of a so-called *generator polynomial*, which is used as the divisor in a polynomial long division over a finite field, taking the input data as the dividend, and where the remainder becomes the result.Cyclic codes have favorable properties in that they are well suited for detecting burst errors. CRCs are particularly easy to implement in hardware, and are therefore commonly used in digital networks and storage devices such as hard disk drives.Even parity is a special case of a cyclic redundancy check, where the single-bit CRC is generated by the divisor *x*+1.

NUMBER BASE CONVERSIONS

Any number in one base system can be converted into another base system Types

1) decimal to any base
2) Any base to decimal
3) Any base to Any base

Decimal number: $123.45 = 1\,10^2 + 2\,10^1 + 3\,10^0 + 4\,10^{-1} + 5\,10^{-2}$

Base *b* number: $N = a_{q-1}b^{q-1} + \cdots + a_0 b^0 + \cdots + a_{-p}b^{-p}$

$b > 1, \quad 0 <= a_i <= b-1$

Integer part: $a_{q-1}a_{q-2} \cdots a_0$

Fractional part: $a_{-1}a_{-2} \cdots a_{-p}$

Most significant digit: a_{q-1}

Least significant digit: a_{-p}

Binary number (*b*=2): $1101.01 = 1\,2^3 + 1\,2^2 + 0\,2^1 + 1\,2^0 + 0\,2^{-1} + 1\,2^{-2}$

Representing number *N* in base *b*: $(N)_b$

Complement of digit *a*: $a' = (b-1)-a$

Decimal system: 9's complement of 3 = 9-3 = 6

Binary system: 1's complement of 1 = 1-1 = 0

Fractional number:

$$(N)_{b_1} = a_{-1}b_2^{-1} + a_{-2}b_2^{-2} + \cdots + a_{-p}b_2^{-p}$$

$$b_2 \cdot (N)_{b_1} = a_{-1} + a_{-2}b_2^{-1} + \cdots + a_{-p}b_2^{-p+1}$$

Example: Convert $(0.3125)_{10}$ to base 8

0.3125 × 8 = 2.5000 hence $a_{-1} = 2$

0.5000 × 8 = 4.0000 hence $a_{-2} = 4$

Thus, $(0.3125)_{10} = (0.24)_8$

Decimal to Binary

Example: Convert $(432.354)_{10}$ to binary

Q_i	r_i
216	$0 = a_0$
108	$0 = a_1$
54	$0 = a_2$
27	$0 = a_3$
13	$1 = a_4$
6	$1 = a_5$
3	$0 = a_6$
1	$1 = a_7$
	$1 = a_8$

$0.354 \cdot 2 = 0.708$ hence $a_{-1} = 0$
$0.708 \cdot 2 = 1.416$ hence $a_{-2} = 1$
$0.416 \cdot 2 = 0.832$ hence $a_{-3} = 0$
$0.832 \cdot 2 = 1.664$ hence $a_{-4} = 1$
$0.664 \cdot 2 = 1.328$ hence $a_{-5} = 1$
$0.328 \cdot 2 = 0.656$ hence $a_{-6} = 0$
$a_{-7} = 1$
etc.

Thus, $(432.354)_{10} = (110110000.0101101\ldots)_2$

Octal To Binary

Example: Convert $(123.4)_8$ to binary

$(123.4)_8 = (001\ 010\ 011.100)_2$

Example: Convert $(1010110.0101)_2$ to octal

$(1010110.0101)_2 = (001\ 010\ 110.010\ 100)_2 = (126.24)_8$

Error Detection and Correction Codes

- No communication channel or storage device is completely error-free
- As the number of bits per area or the transmission rate increases, more errors occur. • Impossible to detect or correct 100% of the errors

Hamming Codes

1. One of the most effective codes for error-recovery
2. Used in situations where random errors are likely tooccur

3. Error detection and correction increases in proportion to the number of parity bits (error- checking bits) added to the end of the information bits

code word = information bits + parity bits

Hamming distance: the number of bit positions in which two code words differ.

10001001

10110001

* * *

Minimum Hamming distance or D(min) : determines its error detecting and correcting capability.

4. Hamming codes can always detect D(min) – 1 errors, but can only correct half of those errors.

EX.

Data Bits	Parity Bit	Code Word
00	0	000
01	1	011
10	1	101
11	0	110

000* 100
001 101*
010 110*
011* 111

5. Single parity bit can only detect error, not correct it

6. Error-correcting codes require more than a single parity bit EX. 0 0 0 0 0

0 1 0 1 1

1 0 1 1 0

1 1 1 0 1

Minimum Hamming distance = 3

Can detect up to 2 errors and correct 1 error

Cyclic Redundancy Check

1. Let the information byte F = 1001011
2. The sender and receiver agree on an arbitrary binary pattern P. Let P = 1011.
3. Shift F to the left by 1 less than the number of bits in P. Now, F = 1001011000.
4. Let F be the dividend and P be the divisor. Perform –modulo 2 division.
5. After performing the division, we ignore the quotient. We got 100 for the remainder, which becomes the actual CRC checksum.

6. Add the remainder to F, giving the message M: 1001011 + 100 = 1001011100 = M

M is decoded and checked by the message receiver using the reverse process.

```
       1010100
    ___________
1011 | 1001011100
       1011
       001001
        1001
        0010
        001011
          1011
          0000          ← Remainder
```

UNIT-II

MINIMIZATION TECHNIQUES AND DESIGN OF MSI

- **Fundamental postulates of Boolean algebra**
- **Basic theorems and properties**
- **Switching functions**
- **Canonical and Standard forms**
- **Algebraic simplification digital logic gates, properties of XOR gates**
- **Universal gates**
- **Multilevel NAND/NOR realizations**

Boolean Algebra: Boolean algebra, like any other deductive mathematical system, may be defined with aset of elements, a set of operators, and a number of unproved axioms or postulates. A *set* of elements is anycollection of objects having a common property. If **S** is a set and ***x*** and ***y*** are certain objects, then **x Î S**denotes that ***x*** is a member of the set **S**, and ***y*** Ï**S** denotes that ***y*** is not an element of **S**. A set with adenumerable number of elements is specified by braces: **A** = {1,2,3,4}, *i.e.* the elements of set **A** are thenumbers 1, 2, 3, and 4. A *binary operator* defined on a set S of elements is a rule that assigns to each pair ofelements from S a unique element from S._ Example: In *a***b*=*c*, we say that * is a binary operator if it specifies a rule for finding *c* from the pair (*a*,*b*)and also if *a*, *b*, *c* Î S.

CLOSURE: The Boolean system is *closed* with respect to a binary operator if for every pair of Boolean values,it produces a Boolean result. For example, logical AND is closed in the Boolean system because it accepts only Boolean operands and produces only Boolean results.

_ A set *S* is closed with respect to a binary operator if, for every pair of elements of *S*, the binary operator specifies a rule for obtaining a unique element of *S*.

_ For example, the set of natural numbers N = {1, 2, 3, 4, … 9} is closed with respect to the binary operator plus (+) by the rule of arithmetic addition, since for any *a*, *b* Î N we obtain a unique *c* Î N by the operation *a* + *b* = c.

ASSOCIATIVE LAW:

A binary operator * on a set *S* is said to be associative whenever (*x* * *y*) * *z* = *x* * (*y* * *z*) for all *x*, *y*, *z* Î S, forall Boolean values x, y and z.

COMMUTATIVE LAW:A binary operator * on a set *S* is said to be commutative whenever x * *y* = *y* * *x* for all *x*, *y*, *z* ϵ S

IDENTITY ELEMENT:A set ***S*** is said to have an identity element with respect to a binary operation * on S if there exists an element *e* ϵ S with the property *e* * *x* = *x* * *e* = *x* for every *x* ϵ S

BASIC IDENTITIES OF BOOLEAN ALGEBRA

- *Postulate 1(Definition)*: A Boolean algebra is a closed algebraic system containing a set *K* of two or more elements and the two operators · and + which refer to logical AND and logical OR •$x + 0 = x$
- $x \cdot 0 = 0$
- $x + 1 = 1$
- $x \cdot 1 = 1$
- $x + x = x$
- $x \cdot x = x$
- $x + x' = x$
- $x \cdot x' = 0$
- $x + y = y + x$
- $xy = yx$
- $x + (y + z) = (x + y) + z$
- $x (yz) = (xy) z$
- $x (y + z) = xy + xz$
- $x + yz = (x + y)(x + z)$
- $(x + y)' = x' y'$
- $(xy)' = x' + y'$
- $(x')' = x$

DeMorgan's Theorem

(a) $(a + b)' = a'b'$

(b) $(ab)' = a' + b'$

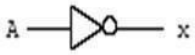
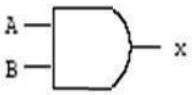
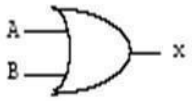
Generalized DeMorgan's Theorem (a) $(a + b + \ldots z)' = a'b' \ldots z'$

(b) $(a.b \ldots z)' = a' + b' + \ldots z$

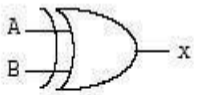
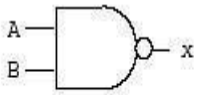
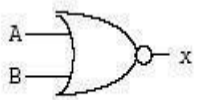
LOGIC GATES

Formal logic: In formal logic, a statement (proposition) is a declarative sentence that is either true(1) or false (0). It is easier to communicate with computers using formal logic.

- Boolean variable: Takes only two values – either true (1) or false (0). They are used as basic units of formal logic.
- Boolean algebra: Deals with binary variables and logic operations operating on those variables.
- Logic diagram: Composed of graphic symbols for logic gates. A simple circuit sketch that represents inputs and outputs of Boolean functions

Name	Graphic symbol	Algebraic function	Truth table	
Inverter		x = A'	A | x 0 | 1 1 | 0	
AND		x = AB	A B | x 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1	True if both are true.
OR		x = A + B	A B | x 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1	True if either one is true.

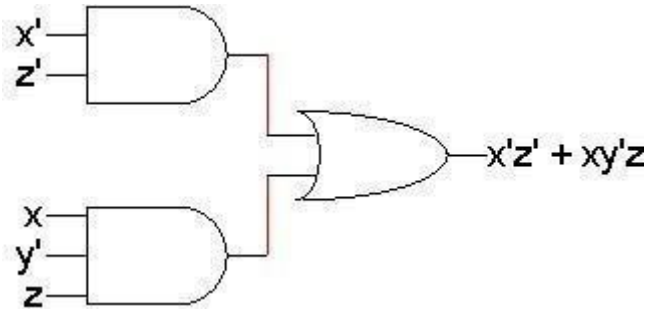
- Other common gates include:

Name	Graphic symbol	Algebraic function	Truth table	
Exclusive-OR (XOR)		x = A ⊕ B = A'B + AB'	A B | x 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0	Parity check: True if only one is true.
NAND		x = (AB)'	A B | x 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0	Inversion of AND.
NOR		x = A + B	A B | x 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0	Inversion of OR.

Minimization of switching functions is to obtain logic circuits with least circuit complexity. This goal is very difficult since how a minimal function relates to the implementation technology is important. For example, If we are building a logic circuit that uses discrete logic made of small scale Integration ICs(SSIs) like 7400 series, in which basic building block are constructed and are available for use. The goal of minimization would be to reduce the number of ICs and not the logic gates. For example, If we require two 6 and gates and 5 Or gates,we would require 2 AND ICs(each has 4 AND gates) and one OR IC. (4 gates). On the other hand if the same logic could be implemented with only 10 nand gates, we require only 3 ICs. Similarly when we design logic on Programmable device, we may implement the design with certain number of gates and remaining gates may not be used.

Whatever may be the criteria of minimization we would be guided by the following:

- Boolean algebra helps us simplify expressions and circuits
- Karnaugh Map: A graphical technique for simplifying a Boolean expression into eitherform:
  - minimal sum of products (MSP)
  - minimal product of sums (MPS)
- Goal of thesimplification.
  - There are a minimal number of product/sum terms oEach term has a minimal number of literals
- Circuit-wise, this leads to a *minimal* two-levelimplementation



A Two-Variable Karnaugh Map

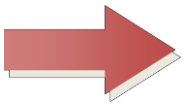
- A two-variable function has four possible minterms. We can re-arrange these minterms intoa Karnaugh map

x	y	minterm

Y 0	0	x‘y‘
0	1	x‘y
1	0	xy‘
1	1	xy

0 1

0
X 1



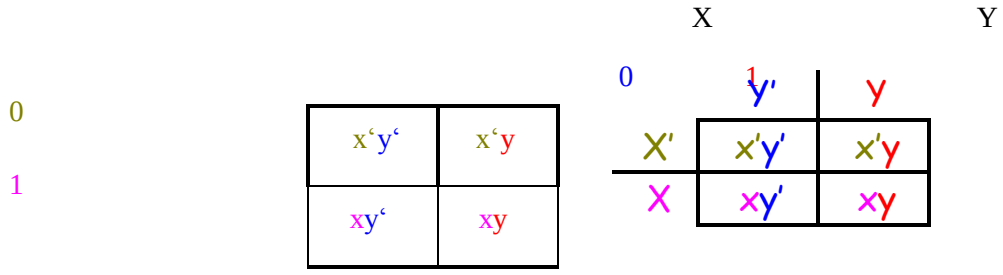
x‘y‘	x‘y
xy‘	xy

-

Now we can easily see which minterms contain common literals

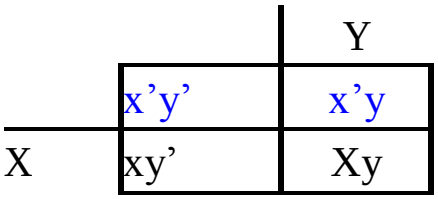
– Minterms on the left and right sides contain y‘ and y respectively

– Minterms in the top and bottom rows contain x‘ and x respectively



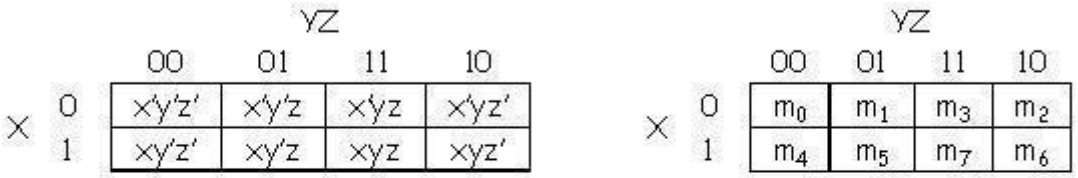
ap Simplification

- Imagine a two-variable sum of minterms x‘y‘ + x‘y
- Both of these minterms appear in the top row of a Karnaugh map, which means that they both contain the literal x‘

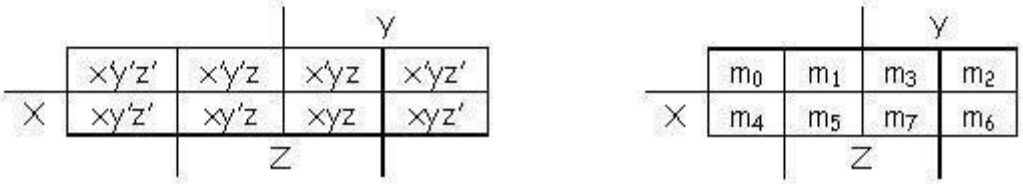


- What happens if you simplify this expression using Boolean algebra?
- x‘y‘ + x‘y= x‘(y‘ + y) [Distributive]
- = x‘ ⊔ 1 [y + y‘ = 1]
- = x‘ [x _ 1 = x]

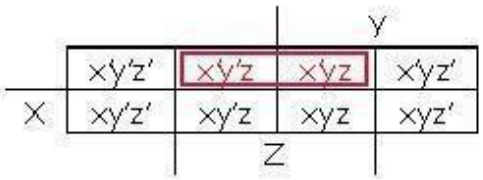
- For a three-variable expression with inputs x, y, z, the arrangement of minterms is more tricky:



- Another way to label the K-map (use whichever you like):

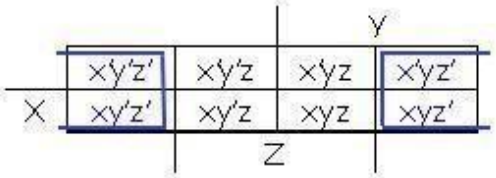


- With this ordering, any group of 2, 4 or 8 adjacent squares on the map contains common literals that can be factored out



$$
\begin{aligned}
& x'y'z + x'yz \\
= \; & x'z(y' + y) \\
= \; & x'z \bullet 1 \\
= \; & x'z
\end{aligned}
$$

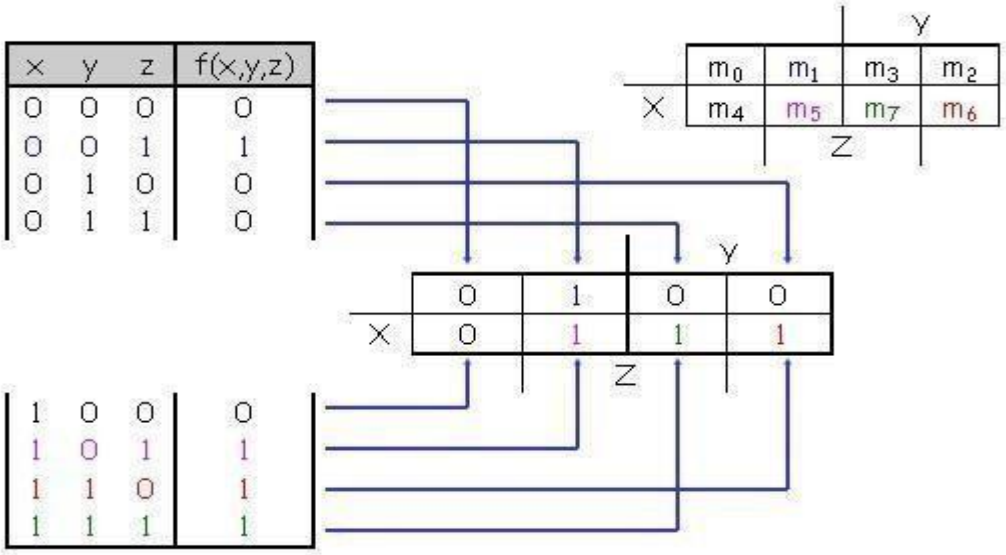
- "Adjacency" includes wrapping around the left and right sides:



$$
\begin{aligned}
& x'y'z' + xy'z' + x'yz' + xyz' \\
= \; & z'(x'y' + xy' + x'y + xy) \\
= \; & z'(y'(x' + x) + y(x' + x)) \\
= \; & z'(y'+y) \\
= \; & z'
\end{aligned}
$$

- We'll use this property of adjacent squares to do our simplifications.

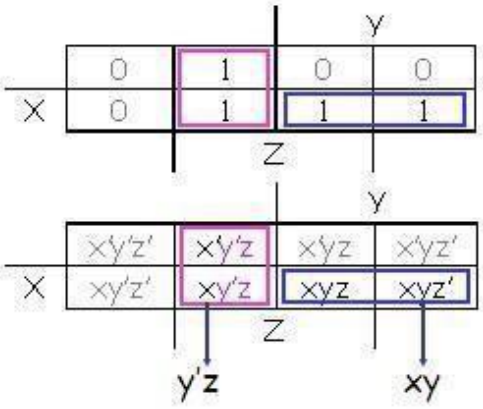
  - We can fill in the K-map directly from a truth table
    - The output in row *i* of the table goes into square m_i of the K-map
    - Remember that the rightmost columns of the K-map are "switched"



K-maps From Truth Tables

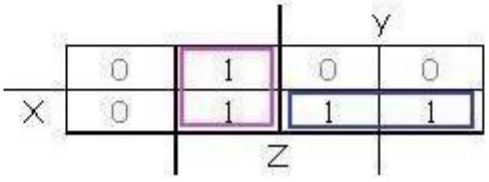
Reading the MSP from the K-map

- You can find the minimal SoP expression
  - Each rectangle corresponds to one product term
  - The product is determined by finding the common literals in that rectangle



$F(x,y,z) = y'z + xy$

- The most difficult step is grouping together all the 1s in the K-map
  - Make rectangles around groups of one, two, four or eight 1s
  - All of the 1s in the map should be included in at least one rectangle
  - Do *not* include any of the 0s
  - Each group corresponds to one product term



Simplify $m_0+m_2+m_5+m_8+m_{10}+m_{13}$

K-map Simplification of SoP Expressions

- Let's consider simplifying f(x,y,z) = xy + y'z + xz
- You should convert the expression into a sum of minterms form,
  - The easiest way to do this is to make a truth table for the function, and then read off the minterms
  - You can either write out the literals or use the minterm shorthand
- Here is the truth table and sum of minterms for our example:

x	y	z	f(x,y,z)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$f(x,y,z) = x'y'z + xy'z + xyz' + xyz$$
$$= m_1 + m_5 + m_6 + m_7$$

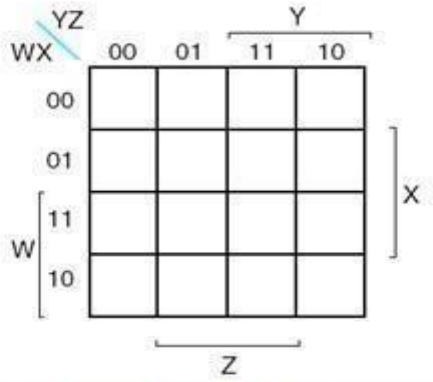
- You can also convert the expression to a sum of minterms with Boolean algebra
  - Apply the distributive law in reverse to add in missing variables.
  - Very few people actually do this, but it's occasionally useful.

$$\begin{aligned} xy + y'z + xz &= (xy \bullet 1) + (y'z \bullet 1) + (xz \bullet 1) \\ &= (xy \bullet (z' + z)) + (y'z \bullet (x' + x)) + (xz \bullet (y' + y)) \\ &= (xyz' + xyz) + (x'y'z + xy'z) + (xy'z + xyz) \\ &= xyz' + xyz + x'y'z + xy'z \\ &= m_1 + m_5 + m_6 + m_7 \end{aligned}$$

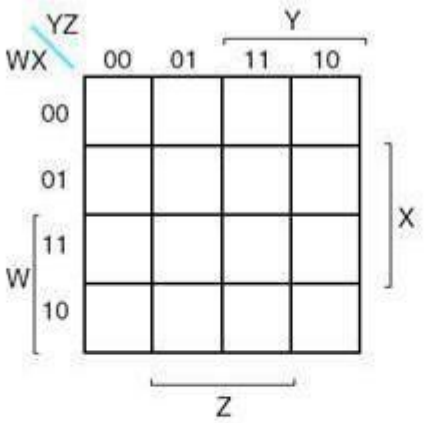
- In both cases, we're actually "unsimplifying" our example expression
  - The resulting expression is larger than the original one!
  - But having all the individual minterms makes it easy to combine them together with the K-map

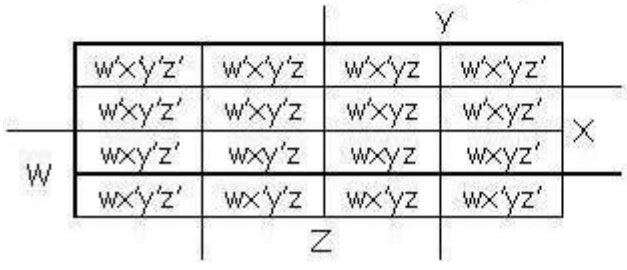
Simplify $m_0+m_2+m_5+m_8+m_{10}+m_{13}$

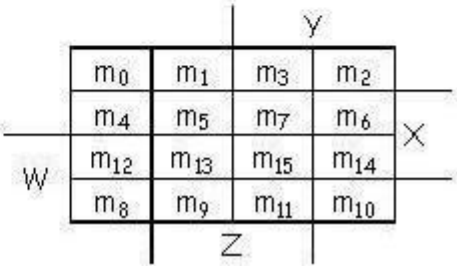
- We can do four-variable expressions too!
  - The minterms in the third and fourth columns, *and* in the third and fourth rows, are switched around.
  - Again, this ensures that adjacent squares have common literals



- Grouping minterms is similar to the three-variable case, but:
  - You can have rectangular groups of 1, 2, 4, 8 or 16 minterms
  - You can wrap around *all four* sides

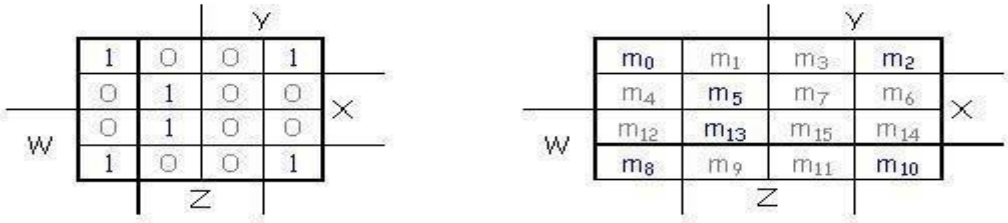




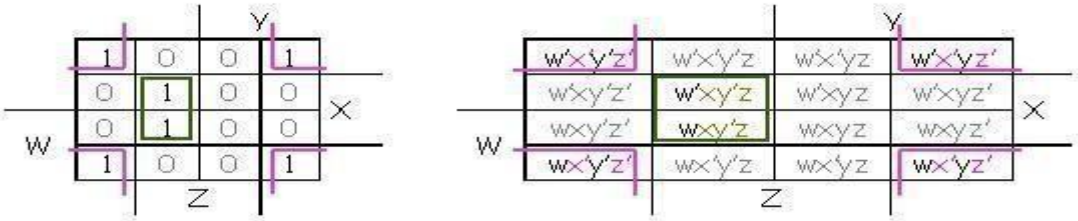


Simplify $m_0+m_2+m_5+m_8+m_{10}+m_{13}$

- The expression is already a sum of minterms, so here's the K-map:



- We can make the following groups, resulting in the MSP x'z' + xy'z

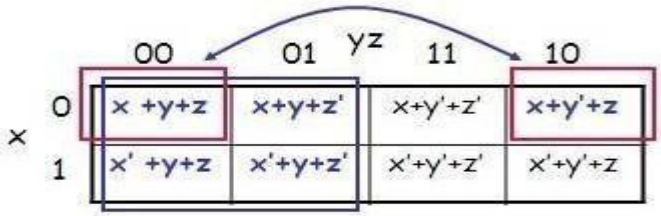


PoS Optimization

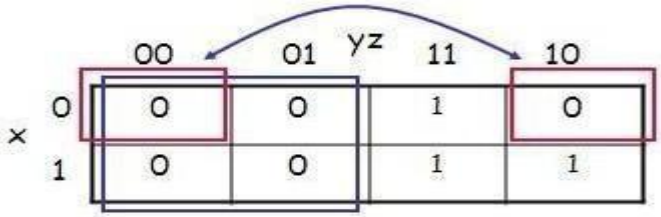
- Maxterms are grouped to find minimal PoS expression

x \ yz	00	01	11	10
0	x +y+z	x+y+z'	x+y'+z'	x+y'+z
1	x' +y+z	x'+y+z'	x'+y'+z'	x'+y'+z

- F(W,X,Y,Z)= Π M(0,1,2,4,5)

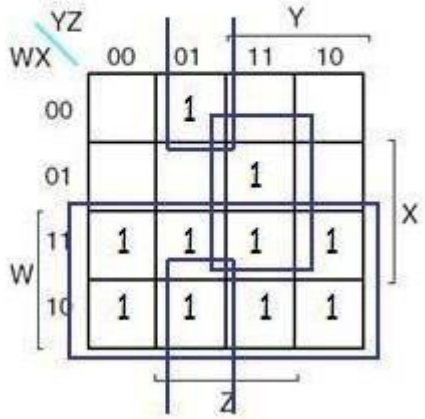


F(W,X,Y,Z)= Y . (X + Z)



SoP Optimization from PoS

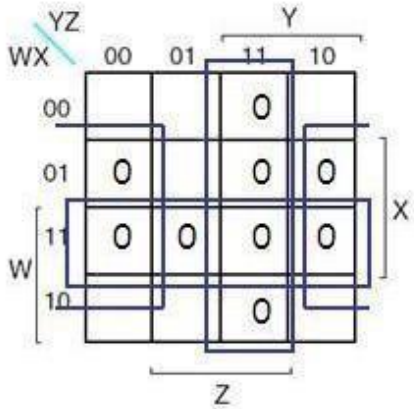
$$F(W,X,Y,Z) = \prod M(0,2,3,4,5,6)$$
$$= \Sigma m(1,7,8,9,10,11,12,13,14,15)$$



$$F(W,X,Y,Z) = W + XYZ + X'Y'Z$$

PoS Optimization from SoP

$$F(W,X,Y,Z) = \Sigma m(0,1,2,5,8,9,10)$$
$$= \prod M(3,4,6,7,11,12,13,14,15)$$



$$F(W,X,Y,Z) = (W' + X')(Y' + Z')(X' + Z)$$

Or,

$$F(W,X,Y,Z) = X'Y' + X'Z' + W'Y'Z$$

Which one is the minimal one?

Don’t care

- You don’t always need all 2^n input combinations in an n-variable function
  - If you can guarantee that certain input combinations never occur
  - If some outputs aren’t used in the rest of the circuit
- We mark don’t-care outputs in truth tables and K-maps with Xs.

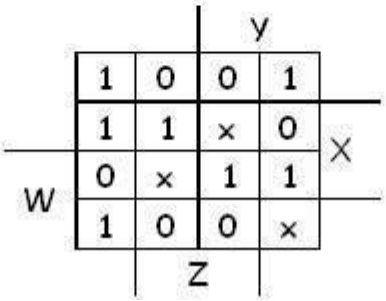
x	y	z	f(x,y,z)
0	0	0	0
0	0	1	1
0	1	0	X
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	X
1	1	1	1

- Within a K-map, each X can be considered as either 0 or 1. You should pick the interpretation that allows for the most simplification.

- Find a MSP for

$$f(w,x,y,z) = \Sigma m(0,2,4,5,8,14,15), d(w,x,y,z) = \Sigma m(7,10,13)$$

This notation means that input combinations wxyz = 0111, 1010 and 1101 (corresponding to minterms m_7, m_{10} and m_{13}) are unused.



K-map Summary

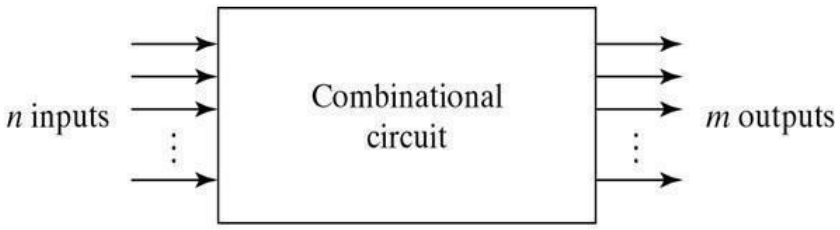
- K-maps are an alternative to algebra for simplifying expressions
  - The result is a MSP/MPS, which leads to a minimal two-level circuit
  - It‘s easy to handle don‘t-care conditions
  - K-maps are really only good for manual simplification of small expressions...
  - Things to keep in mind:
  - Remember the correct order of minterms/maxterms on the K-map
  - When grouping, you can wrap around all sides of the K-map, and your groups can overlap
  - Make as few rectangles as possible, but make each of them as large as possible. This leads to fewer, but simpler, product terms
  - There may be more than one valid solution

UNIT-III

SEQUENTIAL CIRCUITS DESIGN

Combinational Logic

- Logic circuits for digital systems may be combinational or sequential.
- A combinational circuit consists of input variables, logic gates, and output variables.



For n input variables,there are 2^n possible combinations of binary input variables .For each possible input Combination ,there is one and only one possible output combination.A combinational circuit can be described by m Boolean functions one for each output variables.Usually the input s comes from flip-flops and outputs goto flip-flops.

Design Procedure:

1. The problem is stated
2. The number of available input variables and required output variables isdetermined. 3.The input and output variables are assigned lettersymbols.

4.The truth table that defines the required relationship between inputs and outputs is derived. 5.The simplified Boolean function for each output is obtained.
6.The logic diagram is drawn.

Adders:

Digital computers perform variety of information processing tasks,the one is arithmetic operations.And the most basic arithmetic operation is the addition of two binary digits.i.e, 4 basic possible operations are:

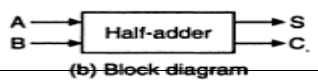
0+0=0,0+1=1,1+0=1,1+1=10

The first three operations produce a sum whose length is one digit, but when augends and addend bits are equal to 1,the binary sum consists of two digits.The higher significant bit of this result is called a carry.A combinational circuit that performs the addition of two bits is called a half- adder. One that performs the addition of 3 bits (two significant bits & previous carry) is called a full adder.& 2 half adder can employ as a full-adder.

The Half Adder: A Half Adder is a combinational circuit with two binary inputs (augends and addend bits and two binary outputs (sum and carry bits.) It adds the two inputs (A and B) and produces the sum (S) and the carry (C) bits. It is an arithmetic operation of addition of two single bit words.

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(a) Truth table



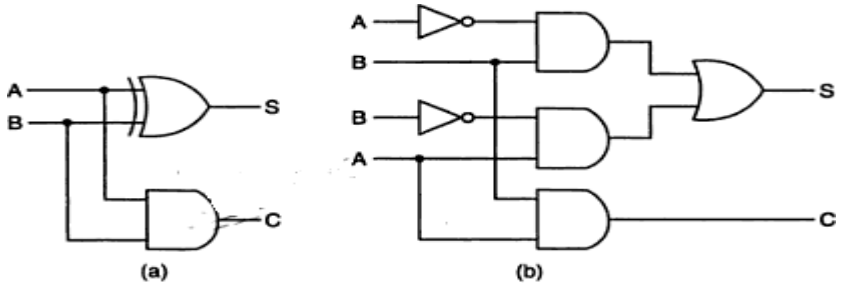
(b) Block diagram

The Sum(S) bit and the carry (C) bit, according to the rules of binary addition, the sum (S) is the X-OR of A and B (It represents the LSB of the sum). Therefore,

S=A+ $A \oplus B$

The carry (C) is the AND of A and B (it is 0 unless both the inputs are 1).Therefore, C=AB

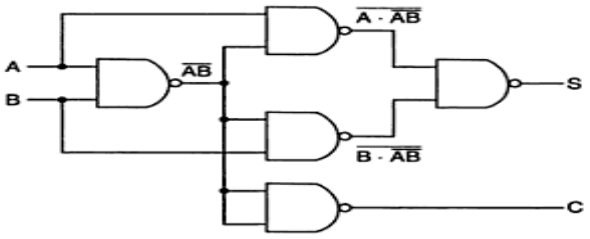
A half-adder can be realized by using one X-OR gate and one AND gate a



Logic diagrams of half-adder

NAND LOGIC:

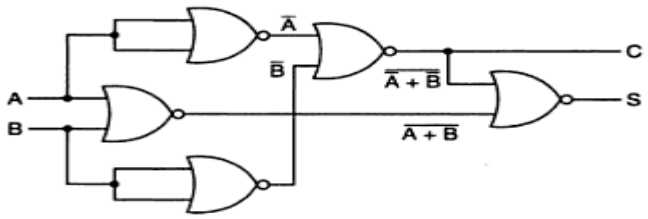
$$S = A\bar{B} + \bar{A}B = A\bar{B} + A\bar{A} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$
$$= A \cdot \overline{A\bar{B}} + B \cdot \overline{A\bar{B}}$$
$$= \overline{A \cdot \overline{A\bar{B}}} \cdot \overline{B \cdot \overline{A\bar{B}}}$$
$$C = AB = \overline{\overline{AB}}$$



Logic diagram of a half-adder using only 2-input NAND gates.

NOR Logic:

$$S = A\bar{B} + \bar{A}B = A\bar{B} + A\bar{A} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$
$$= (A + B)(\bar{A} + \bar{B})$$
$$= \overline{\overline{A + B} + \overline{\bar{A} + \bar{B}}}$$
$$C = AB = \overline{\overline{AB}} = \overline{\bar{A} + \bar{B}}$$



Logic diagram of a half-adder using only 2-input NOR gates.

The Full Adder:

A Full-adder is a combinational circuit that adds two bits and a carry and outputs a sum bit and a carry bit. To add two binary numbers, each having two or more bits, the LSBs can be added by using a half-adder.

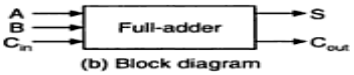
The carry resulted from the addition of the LSBs is carried over to the next significant column and added to the two bits in that column. So, in the second and higher columns, the two data bits of that column and the carry bit generated from the addition in the previous column need to be added.

The full-adder adds the bits A and B and the carry from the previous column called the carry-in C_{in} and outputs the sum bit S and the carry bit called the carry-out C_{out}. The variable S gives the value of the least significant bit of the sum. The variable C_{out} gives the output carry.The

eight rows under the input variables designate all possible combinations of 1s and 0s that these variables may have. The 1s and 0s for the output variables are determined from the arithmetic sum of the input bits. When all the bits are 0s , the output is 0. The S output is equal to 1 when only 1 input is equal to 1 or when all the inputs are equal to 1. The C_{out} has a carry of 1 if two or three inputs are equal to 1.

Inputs			Sum	Carry
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a) Truth table



(b) Block diagram

Full-adder.

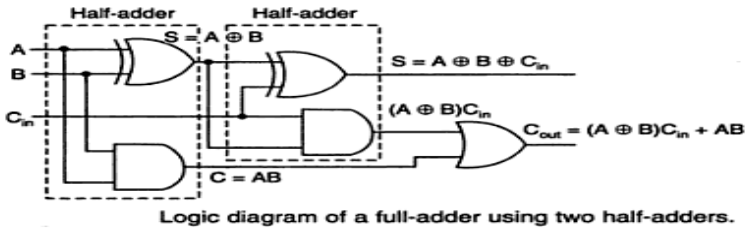
From the truth table, a circuit that will produce the correct sum and carry bits in response to every possible combination of A,B and C_{in} is described by

$$S = A\bar{B}\bar{C}_{in} + \bar{A}B\bar{C}_{in} + \bar{A}\bar{B}C_{in} + ABC_{in}$$

and

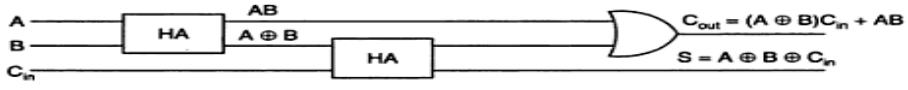
$$C_{out} = AC_{in} + BC_{in} + AB$$

The sum term of the full-adder is the X-OR of A,B, and C_{in}, i.e, the sum bit the modulo sum of the data bits in that column and the carry from the previous column. The logic diagram of the full-adder using two X-OR gates and two AND gates (i.e, Two half adders) and one OR gate is



Logic diagram of a full-adder using two half-adders.

The block diagram of a full-adder using two half-adders is



Block diagram of a full-adder using two half-adders.

Even though a full-adder can be constructed using two half-adders, the disadvantage is that the bits must propagate through several gates in accession, which makes the total propagation delay greater than that of the full-adder circuit using AOI logic.

The Full-adder neither can also be realized using universal logic, i.e., either only NAND gates or only NOR gates as

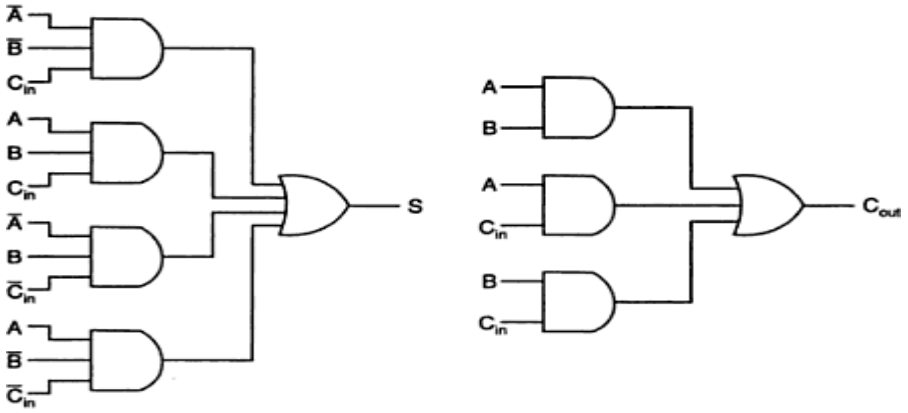
$$A \oplus B = \overline{\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}}$$

Then

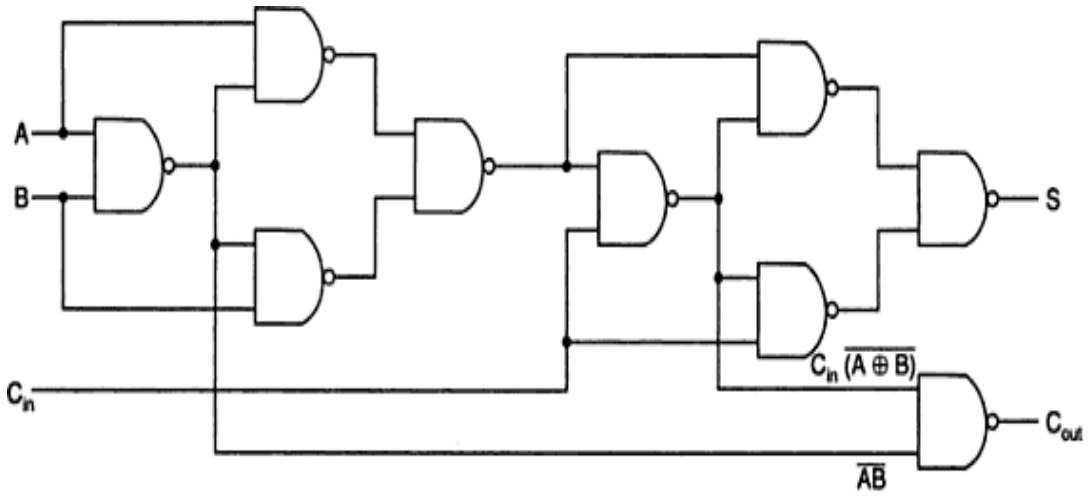
$$S = A \oplus B \oplus C_{in} = \overline{\overline{(A \oplus B) \cdot \overline{(A \oplus B)C_{in}}} \cdot \overline{C_{in} \cdot \overline{(A \oplus B)C_{in}}}}$$

NAND Logic:

$$C_{out} = C_{in}(A \oplus B) + AB = \overline{\overline{C_{in}(A \oplus B)} \cdot \overline{AB}}$$



Sum and carry bits of a full-adder using AOI logic.



Logic diagram of a full-adder using only 2-input NAND gates.

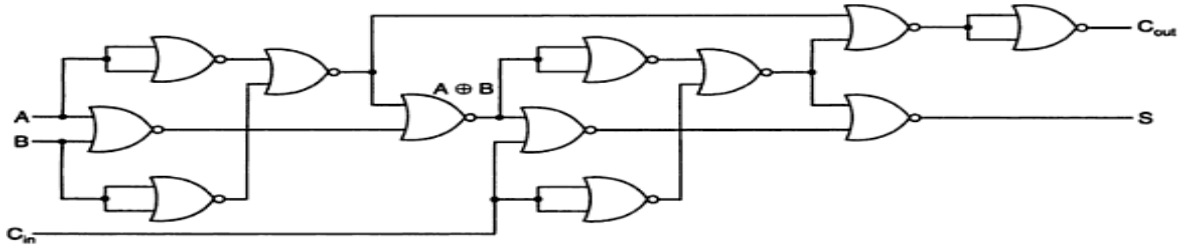
NOR Logic:

$$A \oplus B = \overline{\overline{(A + B)} + \overline{\overline{A} + \overline{B}}}$$

Then

$$S = A \oplus B \oplus C_{in} = \overline{\overline{(A \oplus B) + \overline{C}_{in}} + \overline{\overline{(A \oplus B) + \overline{C}_{in}}}}$$

$$C_{out} = AB + C_{in}(A \oplus B) = \overline{\overline{A} + \overline{B}} + \overline{\overline{C}_{in} + \overline{A \oplus B}}$$



Logic diagram of a full-adder using only 2-input NOR gates.

Subtractors:

The subtraction of two binary numbers may be accomplished by taking the complement of the subtrahend and adding it to the minuend. By this, the subtraction operation becomes an addition operation and instead of having a separate circuit for subtraction, the adder itself can be used to perform subtraction. This results in reduction of hardware. In subtraction, each subtrahend bit of the number is subtracted from its corresponding significant minuend bit to form a difference bit. If the minuend bit is smaller than the subtrahend bit, a 1 is borrowed from the next significant position., that has been borrowed must be conveyed to the next higher pair of bits by means of a signal coming out (output) of a given stage and going into (input) the next higher stage.

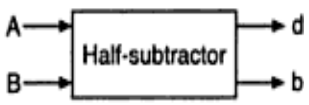
The Half-Subtractor:

A Half-subtractor is a combinational circuit that subtracts one bit from the other and produces the difference. It also has an output to specify if a 1 has been borrowed. . It is used to subtract the LSB of the subtrahend from the LSB of the minuend when one binary number is subtracted from the other.

A Half-subtractor is a combinational circuit with two inputs A and B and two outputs d and b. d indicates the difference and b is the output signal generated that informs the next stage that a 1 has been borrowed. When a bit B is subtracted from another bit A, a difference bit (d) and a borrow bit (b) result according to the rules given as

Inputs		Outputs	
A	B	d	b
0	0	0	0
1	0	1	0
1	1	0	0
0	1	1	1

(a) Truth table



(b) Block diagram

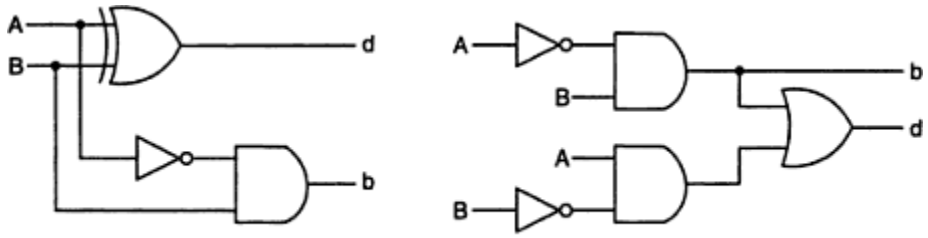
Half-subtractor.

The output borrow b is a 0 as long as A≥B. It is a 1 for A=0 and B=1. The d output is the result of the arithmetic operation2b+A-B.

A circuit that produces the correct difference and borrow bits in response to every possible combination of the two 1-bit numbers is , therefore ,

d=A+ $A \oplus B$ and b=B

That is, the difference bit is obtained by X-OR ing the two inputs, and the borrow bit is obtained by ANDing the complement of the minuend with the subtrahend.Note that logic for this exactly the same as the logic for output S in the half-adder.



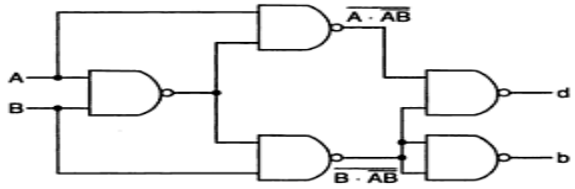
Logic diagrams of a half-subtractor.

A half-substractor can also be realized using universal logic either using only NAND gates or using NOR gates as:

NAND Logic:

$$d = A \oplus B = \overline{\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}}$$

$$b = \overline{A}B = B(\overline{A} + \overline{B}) = B(\overline{AB}) = \overline{B \cdot \overline{AB}}$$



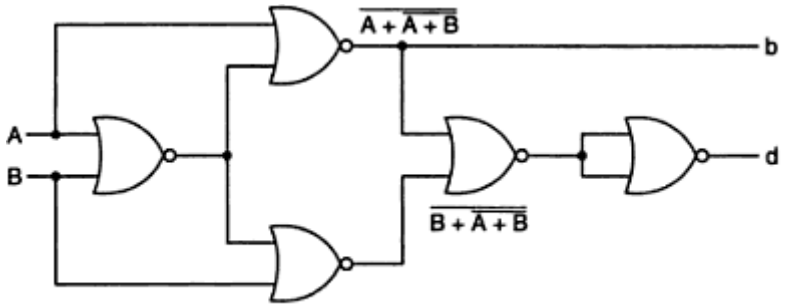
Logic diagram of a half-subtractor using only 2-input NAND gates.

NOR Logic:

$$d = A \oplus B = A\overline{B} + \overline{A}B = A\overline{B} + B\overline{B} + \overline{A}B + A\overline{A}$$

$$= \overline{B}(A + B) + \overline{A}(A + B) = \overline{\overline{B} + \overline{A + B}} + \overline{\overline{A} + \overline{A + B}}$$

$$d = \overline{A}B = \overline{A}(A + B) = \overline{\overline{A}(A + B)} = \overline{A + (\overline{A + B})}$$



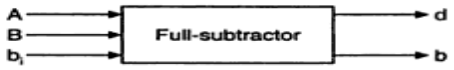
Logic diagram of a half-subtractor using only 2-input NOR gates.

The Full-Subtractor:

The half-subtractor can be only for LSB subtraction. IF there is a borrow during the subtraction of the LSBs, it affects the subtraction in the next higher column; the subtrahend bit is subtracted from the minuend bit, considering the borrow from that column used for the subtraction in the preceding column. Such a subtraction is performed by a full-subtractor. It subtracts one bit (B) from another bit (A) , when already there is a borrow b_i from this column for the subtraction in the preceding column, and outputs the difference bit (d) and the borrow bit(b) required from the next d and b. The two outputs present the difference and output borrow. The 1s and 0s for the output variables are determined from the subtraction of A-B-b_i.

Inputs			Difference	Borrow
A	B	b_i	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(a) Truth table



(b) Block diagram

Full-subtractor.

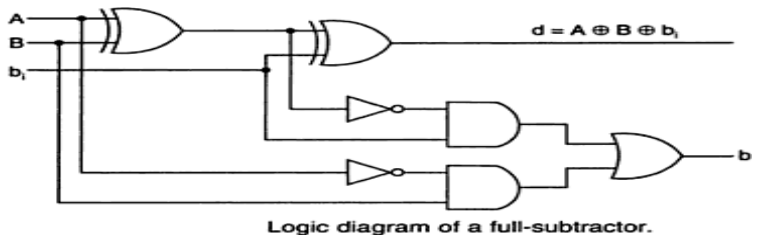
From the truth table, a circuit that will produce the correct difference and borrow bits in response to every possiblecombinations of A,B and b_i is

$$d = \bar{A}\bar{B}b_i + \bar{A}B\,\bar{b}_i + A\bar{B}\,\bar{b}_i + ABb_i$$
$$= b_i(AB + \bar{A}\bar{B}) + \bar{b}_i(A\bar{B} + \bar{A}B)$$
$$= b_i(\overline{A \oplus B}) + \bar{b}_i(A \oplus B) = A \oplus B \oplus b_i$$

and

$$b = \bar{A}\bar{B}b_i + \bar{A}B\,\bar{b}_i + \bar{A}Bb_i + ABb_i = \bar{A}B(b_i + \bar{b}_i) + (AB + \bar{A}\bar{B})b_i$$
$$= \bar{A}B + (\overline{A \oplus B})b_i$$

A full-subtractor can be realized using X-OR gates and AOI gates as



Logic diagram of a full-subtractor.

The full subtractor can also be realized using universal logic either using only NAND gates or using NOR gates as:

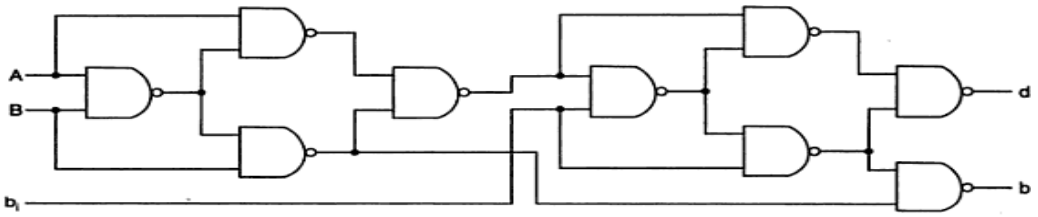
NAND Logic:

$$d = A \oplus B \oplus b_i = \overline{\overline{(A \oplus B) \oplus b_i}} = \overline{\overline{(A \oplus B)\overline{(A \oplus B)b_i}} \cdot \overline{b_i\overline{(A \oplus B)b_i}}}$$

$$b = \bar{A}B + b_i(\overline{A \oplus B}) = \overline{\bar{A}B + b_i(\overline{A \oplus B})}$$

$$= \overline{\overline{\bar{A}B} \cdot \overline{b_i(\overline{A \oplus B})}} = \overline{\overline{B(\bar{A} + \bar{B})} \cdot \overline{b_i(\bar{b}_i + (\overline{A \oplus B}))}}$$

$$= \overline{\overline{B \cdot \overline{AB}} \cdot \overline{b_i[\overline{b_i \cdot (A \oplus B)}]}}$$



Logic diagram of a full-subtractor using only 2-input NAND gates.

NOR Logic:

$$d = A \oplus B \oplus b_i = \overline{\overline{(A \oplus B) \oplus b_i}}$$

$$= \overline{(A \oplus B)b_i + (\overline{A \oplus B})\bar{b}_i}$$

$$= \overline{[(A \oplus B) + (\overline{A \oplus B})\bar{b}_i][b_i + (\overline{A \oplus B})\bar{b}_i]}$$

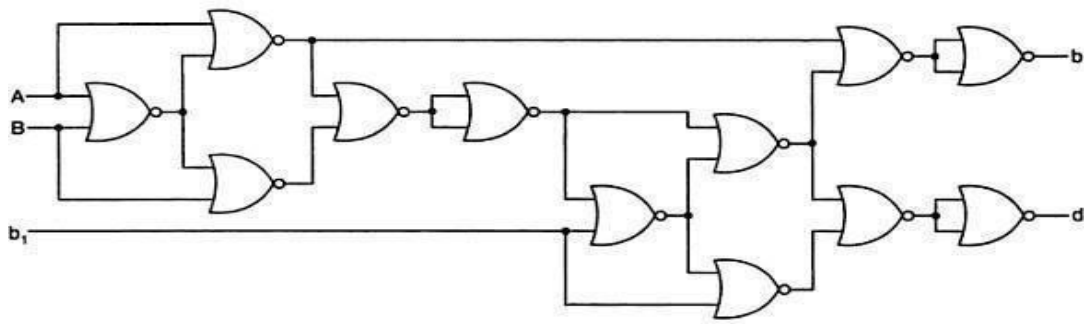
$$= \overline{(A \oplus B) + \overline{(A \oplus B) + b_i}} + \overline{b_i + \overline{(A \oplus B) + b_i}}$$

$$= \overline{\overline{(A \oplus B) + \overline{(A \oplus B) + b_i}} + \overline{b_i + \overline{(A \oplus B) + b_i}}}$$

$$b = \bar{A}B + b_i(\overline{A \oplus B})$$

$$= \bar{A}(A + B) + (\overline{A \oplus B})[(A \oplus B) + b_i]$$

$$= \overline{\overline{A + \overline{(A + B)}} + \overline{(A \oplus B) + \overline{(A \oplus B) + b_i}}}$$

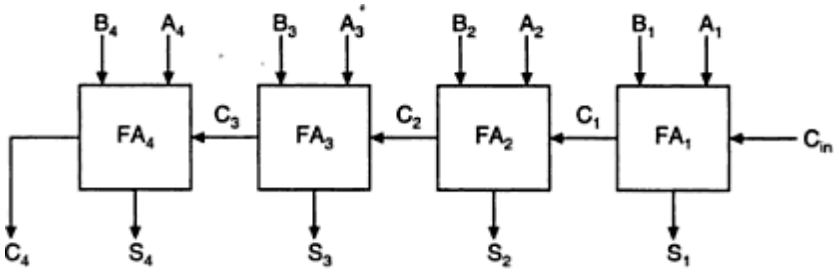


Logic diagram of a full subtractor using only 2-input NOR gates.

Binary Parallel Adder:

A binary parallel adder is a digital circuit that adds two binary numbers in parallel form and produces the arithmetic sum of those numbers in parallel form. It consists of full adders connected in a chain , with the output carry from each full-adder connected to the input carry of the next full-adder in the chain.

The interconnection of four full-adder (FA) circuits to provide a 4-bit parallel adder. The augends bits of A and addend bits of B are designated by subscript numbers from right to left, with subscript 1 denoting the lower –order bit. The carries are connected in a chain through the full-adders. The input carry to the adder is C_{in} and the output carry is C_4. The S output generates the required sum bits. When the 4-bit full-adder circuit is enclosed within an IC package, it has four terminals for the augends bits, four terminals for the addend bits, four terminals for the sum bits, and two terminals for the input and output carries. AN n-bit parallel adder requires n-full adders. It can be constructed from 4-bit, 2-bit and 1-bit full adder ICs by cascading several packages. The output carry from one package must be connected to the input carry of the one with the next higher –order bits. The 4-bit full adder is a typical example of an MSI function.



Logic diagram of a 4-bit binary parallel adder.

Ripple carry adder:

In the parallel adder, the carry –out of each stage is connected to the carry-in of the next stage. The sum and carry-out bits of any stage cannot be produced, until sometime after the carry-in of that stage occurs. This is due to the propagation delays in the logic circuitry,

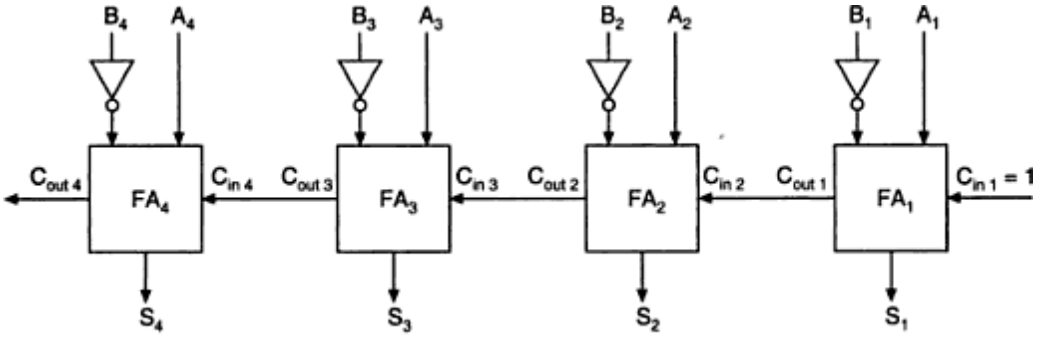
which lead to a time delay in the addition process. The carry propagation delay for each full- adder is the time between the application of the carry-in and the occurrence of the carry-out.

The 4-bit parallel adder, the sum (S_1) and carry-out (C_1) bits given by FA_1 are not valid, until after the propagation delay of FA_1. Similarly, the sum S_2 and carry-out (C_2) bits given by FA_2 are not valid until after the cumulative propagation delay of two full adders (FA_1 and FA_2) , and so on. At each stage ,the sum bit is not valid until after the carry bits in all the preceding stages are valid. Carry bits must propagate or ripple through all stages before the most significant sum bit is valid. Thus, the total sum (the parallel output) is not valid until after the cumulative delay of all the adders.

The parallel adder in which the carry-out of each full-adder is the carry-in to the next most significant adder is called a ripple carry adder.. The greater the number of bits that a ripple carry adder must add, the greater the time required for it to perform a valid addition. If two numbers are added such that no carries occur between stages, then the add time is simply the propagation time through a single full-adder.

4- Bit Parallel Subtractor:

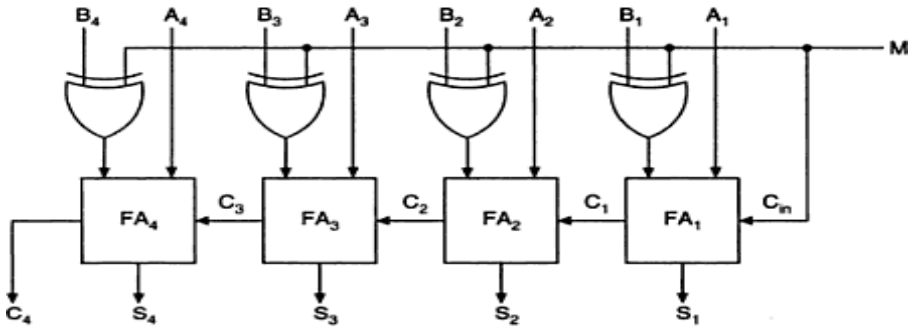
The subtraction of binary numbers can be carried out most conveniently by means of complements , the subtraction A-B can be done by taking the 2_s complement of B and adding it to A . The 2_s complement can be obtained by taking the 1_s complement and adding 1 to the least significant pair of bits. The 1_s complement can be implemented with inverters as



Logic diagram of a 4-bit parallel subtractor.

Binary-Adder Subtractor:

A 4-bit adder-subtractor, the addition and subtraction operations are combined into one circuit with one common binary adder. This is done by including an X-OR gate with each full-adder. The mode input M controls the operation. When M=0, the circuit is an adder, and when M=1, the circuit becomes a subtractor. Each X-OR gate receives input M and one of the inputs of B. When M=0,.The full-adder receives the value of B , the input carry is 0 and the circuit performs A+B. whenand C_1=1. The B inputs are complemented and a 1 is through the input carry. The circuit performs the operation A plus the 2_s complement of B.



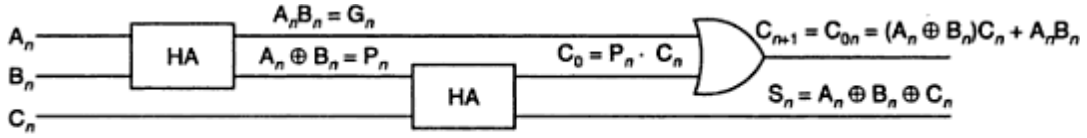
Logic diagram of a 4-bit binary adder-subtractor.

The Look-Ahead –Carry Adder:

In parallel-adder,the speed with which an addition can be performed is governed by the time required for the carries to propagate or ripple through all of the stages of the adder. The look-ahead carry adder speeds up the process by eliminating this ripple carry delay. It examines all the input bits simultaneously and also generates the carry-in bits for all the stages simultaneously.

The method of speeding up the addition process is based on the two additional functions of the full-adder, called the carry generate and carry propagate functions.

Consider one full adder stage; say the nth stage of a parallel adder as shown in fig. we know that is made by two half adders and that the half adder contains an X-OR gate to produce the sum and an AND gate to produce the carry. If both the bits A_n and B_n are 1s, a carry has to be generated in this stage regardless of whether the input carry C_{in} is a 0 or a 1. This is called generated carry, expressed as $G_n = A_n.B_n$ which has to appear at the output through the OR gate as shown in fig.



A full adder (*n*th stage of a parallel adder).

Thereis another possibility of producing a carry out. X-OR gate inside the half-adder

at the input produces an intermediary sum bit- call it P_n –which is expressed as $P_n = A_n \oplus B_n$. Next P_n and C_n are added using the X-OR gate inside the second half adder to produce the final

sum bit and $S_n = P_n \oplus C_n$ where $P_n = A_n \oplus B_n$ and output carry$C_0 = P_n.C_n = (A_n \oplus B_n)C_n$ which becomes carry for the (n+1) th stage.

Consider the case of both P_n and C_n being 1. The input carry C_n has to be propagated to the output only if P_n is 1. If P_n is 0, even if C_n is 1, the and gate in the second half-adder will inhibit C_n . the carry out of the nth stage is 1 when either $G_n=1$ or $P_n.C_n=1$ or both G_n and $P_n.C_n$ are equal to 1.

For the final sum and carry outputs of the nth stage, we get the following Boolean expressions.

$$S_n = P_n \oplus C_n \text{ where } P_n = A_n \oplus B_n$$
$$C_{on} = C_{n+1} = G_n + P_nC_n \text{ where } G_n = A_n \cdot B_n$$

Observe the recursive nature of the expression for the output carry at the nth stage which becomes the input carry for the (n+1)st stage .it is possible to express the output carry of a higher significant stage is the carry-out of the previous stage.

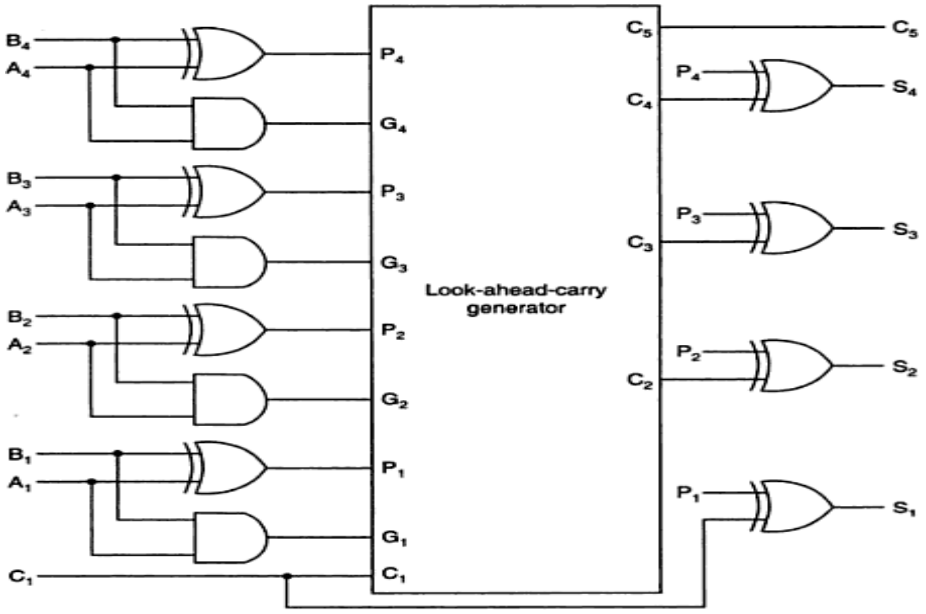
Based on these , the expression for the carry-outs of various full adders are as follows,

$$C_1 = G_0 + P_0 \cdot C_0$$
$$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0$$
$$C_3 = G_2 + P_2 \cdot C_2 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0$$
$$C_4 = G_3 + P_3 \cdot C_3 = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

The general expression for n stages designated as 0 through $(n-1)$ would be

$$C_n = G_{n-1} + P_{n-1} \cdot C_{n-1} = G_{n-1} + P_{n-1} \cdot G_{n-2} + P_{n-1} \cdot P_{n-2} \cdot G_{n-3} + \ldots + P_{n-1} \cdot \ldots P_0 \cdot C_0$$

Observe that the final output carry is expressed as a function of the input variables in SOP form. Which is two level AND-OR or equivalent NAND-NAND form. Observe that the full look-ahead scheme requires the use of OR gate with (n+1) inputs and AND gates with number of inputs varying from 2 to (n+1).



Logic diagram of a 4-bit look-ahead-carry adder.

2's complement Addition and Subtraction using Parallel Adders:

Most modern computers use the 2_s complement system to represent negative numbers and to perform subtraction operations of signed numbers can be performed using only the addition operation ,if we use the 2_s complement form to represent negative numbers.

The circuit shown can perform both addition and subtraction in the 2_s complement. This adder/subtractor circuit is controlled by the control signal ADD/SUB_. When the ADD/SUB_ level is HIGH, the circuit performs the addition of the numbers stored in registers A and B. When the ADD/Sub_ level is LOW, the circuit subtract the number in register B from the number in register A. The operation is:

When ADD/SUB_ is a 1:

1. AND gates 1,3,5 and 7 are enabled , allowing B_0,B_1,$B_2$and B_3 to pass to the OR gates 9,10,11,12 . AND gates 2,4,6 and 8 are disabled , blocking B_0_,B_1_,B_2_, and B_3_ from reaching the OR gates 9,10,11 and 12.

2. The two levels B_0 to B_3 pass through the OR gates to the 4-bit parallel adder, to be added to the bits A_0 to A_3. The sum appears at the output S_0 to S_3

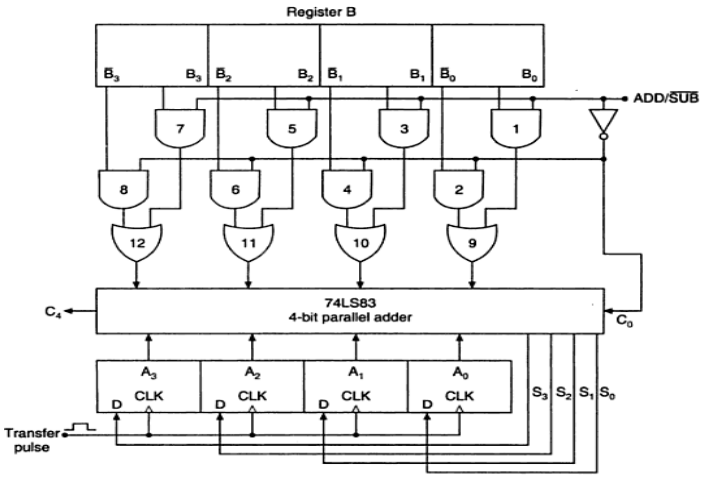
3. Add/SUB_ =1 causes no carry into the adder. When ADD/SUB_ is a 0:

1. AND gates 1,3,5 and 7 are disabled , allowing B_0,B_1,$B_2$and B_3 from reaching the OR gates 9,10,11,12 . AND gates 2,4,6 and 8 are enabled , blocking B_0_,B_1_,B_2_, and B_3_ from reaching the OR gates.

2. The two levels B_0_ to B_3_ pass through the OR gates to the 4-bit parallel adder, to be added to the bits A_0 to A_3.The C_0 is now 1.thus the number in register B is converted to its 2_s complement form.

3. The difference appears at the output S_0 toS_3.

Adders/Subtractors used for adding and subtracting signed binary numbers. In computers , the output is transferred into the register A (accumulator) so that the result of the addition or subtraction always end up stored in the register A This is accomplished by applying a transfer pulse to the CLK inputs of register A.



Logic diagram of a parallel adder/subtractor using 2's complement system.

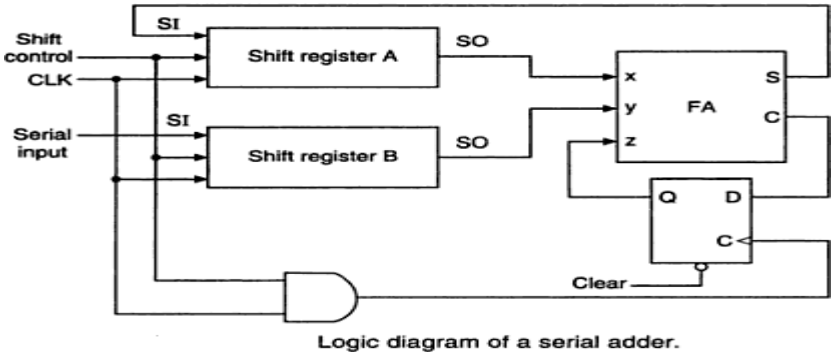
Serial Adder:

A serial adder is used to add binary numbers in serial form. The two binary numbers to be added serially are stored in two shift registers A and B. Bits are added one pair at a time through a single full adder (FA) circuit as shown. The carry out of the full-adder is transferred to a D flip- flop. The output of this flip-flop is then used as the carry input for the next pair of significant bits. The sum bit from the S output of the full-adder could be transferred to a third shift register. By shifting the sum into A while the bits of A are shifted out, it is possible to use one register for storing both augend and the sum bits. The serial input register B can be used to transfer a new binary number while the addend bits are shifted out during the addition.

The operation of the serial adder is:

Initially register A holds the augend, register B holds the addend and the carry flip-flop is cleared to 0. The outputs (SO) of A and B provide a pair of significant bits for the full-adder at x and y. The shift control enables both registers and carry flip-flop , so, at the clock pulse both registers are shifted once to the right, the sum bit from S enters the left most flip-flop of A , and the output carry is transferred into flip-flop Q . The shift control enables the registers for a number of clock pulses equal to the number of bits of the registers. For each succeeding clock pulse a new sum bit is transferred to A, a new carry is transferred to Q, and both registers are shifted once to the right. This process continues until the shift control is disabled. Thus the addition is accomplished by passing each pair of bits together with the previous carry through a single full adder circuit and transferring the sum, one bit at a time, into register A.

Initially, register A and the carry flip-flop are cleared to 0 and then the first number is added from B. While B is shifted through the full adder, a second number is transferred to it through its serial input. The second number is then added to the content of register A while a third number is transferred serially into register B. This can be repeated to form the addition of two, three, or more numbers and accumulate their sum in register A.



Logic diagram of a serial adder.

Difference between Serial and Parallel Adders:

The parallel adder registers with parallel load, whereas the serial adder uses shift registers. The number of full adder circuits in the parallel adder is equal to the number of bits in the binary numbers, whereas the serial adder requires only one full adder circuit and a carry flip- flop. Excluding the registers, the parallel adder is a combinational circuit, whereas the serial adder is a sequential circuit. The sequential circuit in the serial adder consists of a full-adder and a flip-flop that stores the output carry.

BCD Adder:

The BCD addition process:

1. Add the 4-bit BCD code groups for each decimal digit position using ordinary binary addition.

2. For those positions where the sum is 9 or less, the sum is in proper BCD form and no correction is needed.

3. When the sum of two digits is greater than 9, a correction of 0110 should be added to that sum, to produce the proper BCD result. This will produce a carry to be added to the next decimal position.

A BCD adder circuit must be able to operate in accordance with the above steps. In other words, the circuit must be able to do the following:

1. Add two 4-bit BCD code groups, using straight binaryaddition.

2. Determine, if the sum of this addition is greater than 1101 (decimal 9); if it is , add 0110 (decimal 6) to this sum and generate a carry to the next decimalposition.

The first requirement is easily met by using a 4- bit binary parallel adder such as the 74LS83 IC .For example , if the two BCD code groups $A_3A_2A_1A_0$and $B_3B_2B_1B_0$ are applied to a 4-bit parallel adder, the adder will output $S_4S_3S_2S_1S_0$, where S_4 is actually C_4 , the carry –out of the MSB bits.

The sum outputs $S_4S_3S_2S_1S_0$ can range anywhere from 00000 to 100109when both the BCD code groups are 1001=9). The circuitry for a BCD adder must include the logic needed to detect whenever the sum is greater than 01001, so that the correction can be added in. Those cases , where the sum is greater than 1001 are listed as:

S_4	S_3	S_2	S_1	S_0	Decimal number
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18

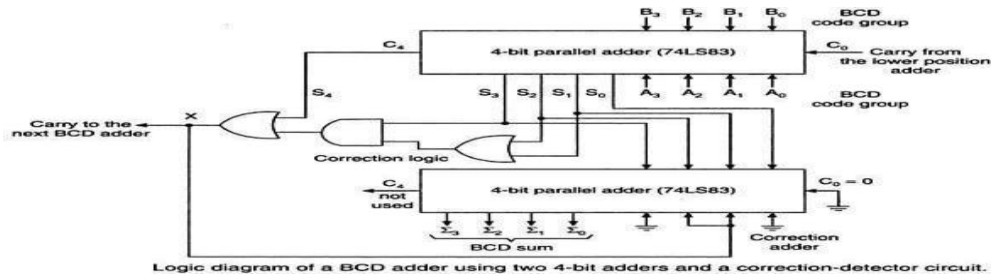
Let us define a logic output X that will go HIGH only when the sum is greater than 01001 (i.e, for the cases in table). If examine these cases ,see that X will be HIGH for either of the following conditions:

1. Whenever S_4 =1(sum greater than15)

2. Whenever S_3 =1 and either S_2 or S_1 or both are 1 (sum 10 to 15) This condition can be expressed as

$X=S_4+S_3(S_2+S_1)$

Whenever X=1, it is necessary to add the correction factor 0110 to the sum bits, and to generate a carry. The circuit consists of three basic parts. The two BCD code groups $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ are added together in the upper 4-bit adder, to produce the sum $S_4S_3S_2S_1S_0$. The logic gates shown implement the expression for X. The lower 4-bit adder will add the correction 0110 to the sum bits, only when X=1, producing the final BCD sum output represented by
$\sum_3\sum_2\sum_1\sum_0$. The X is also the carry-out that is produced when the sum is greater than 01001. When X=0, there is no carry and no addition of 0110. In such cases, $\sum_3\sum_2\sum_1\sum_0= S_3S_2S_1S_0$.
Two or more BCD adders can be connected in cascade when two or more digit decimal numbers are to be added. The carry-out of the first BCD adder is connected as the carry-in of the second BCD adder, the carry-out of the second BCD adder is connected as the carry-in of the third BCD adder and so on.



Logic diagram of a BCD adder using two 4-bit adders and a correction-detector circuit.

EXCESS-3(XS-3) ADDER:

To perform Excess-3 additions,

1. Add two xs-3 code groups
2. If carry=1, add 0011(3) to the sum of those two codegroups

If carry =0, subtract 0011(3) i.e., add 1101 (13 in decimal) to the sum of those two code groups.

Ex: Add 9 and 5

1100		9 in Xs-3
	+1000	5 in xs-3
1	0100	there is a carry
+0011	0011	add 3 to each group
---	---	
0100	0111	14 in xs-3
(1)	(4)	

EX:

(b)	0 1 1 1	4 in XS-3
	+ 0 1 1 0	3 in XS-3
	1 1 0 1	no carry
	+ 1 1 0 1	Subtract 3 (i.e. add 13)
Ignore carry	1 1 0 1 0	7 in XS-3
	(7)	

Implementation of xs-3 adder using 4-bit binary adders is shown. The augend (A_3 $A_2A_1A_0$) and addend ($B_3B_2B_1B_0$) in xs-3 are added using the 4-bit parallel adder. If the carry is a 1, then 0011(3) is added to the sum bits $S_3S_2S_1S_0$ of the upper adder in the lower 4-bit parallel adder. If the carry is a 0, then 1101(3) is added to the sum bits (This is equivalent to subtracting 0011(3) from the sum bits. The correct sum in xs-3 is obtained

Excess-3 (XS-3) Subtractor:

To perform Excess-3 subtraction,

1. Complement the subtrahend
2. Add the complemented subtrahend to theminuend.
3. If carry =1, result is positive. Add 3 and end around carry to the result . If carry=0, the result is negative. Subtract 3, i.e, and take the 1_s complement of the result.

Ex:	Perform 9-4	
1100		9 in xs-3
+1000		Complement of 4 n Xs-3
---		
(1)	0100	There is a carry
+0011		Add 0011(3)
----------	0111	
1		End around carry

1000		5 in xs-3

The minuend and the 1_s complement of the subtrahend in xs-3 are added in the upper 4- bit parallel adder. If the carry-out from the upper adder is a 0, then 1101 is added to the sum bits of the upper adder in the lower adder and the sum bits of the lower adder are complemented to get the result. If the carry-out from the upper adder is a 1, then 3=0011 is added to the sum bits of the lower adder and the sum bits of the lower adder give the result.

Binary Multipliers:

In binary multiplication by the paper and pencil method, is modified somewhat in digital machines because a binary adder can add only two binary numbers at a time.
In a binary multiplier, instead of adding all the partial products at the end, they are added two at a time and their sum accumulated in a register (the accumulator register). In addition, when the multiplier bit is a 0,0s are not written down and added because it does not affect the final result. Instead, the multiplicand is shifted left by one bit.

The multiplication of 1110 by 1001 using this processis Multiplicand 1110
Multiplier 1001
1110 The LSB of the multiplier is a 1; write down the multiplicand; shift the multiplicand one position to the left (1 1 1 0 0)
1110 The second multiplier bit is a 0; write down the previous result 1110; shift the multiplicand to the left again (1 1 1 00 0)
+1110000 The fourth multiplier bit is a 1 write down the new multiplicand add it to the first partial product to obtain the final product.
1111110
This multiplication process can be performed by the serial multiplier circuit , which multiplies two 4-bit numbers to produce an 8-bit product. The circuit consists of following elements
X register: A 4-bit shift register that stores the multiplier --- it will shift right on the falling edge of the clock. Note that 0s are shifted in from the left.
B register: An 8-bit register that stores the multiplicand; it will shift left on the falling edge of the clock. Note that 0s are shifted in from the right.
A register: An 8-bit register, i.e, the accumulator that accumulates the partial products. **Adder:**An 8-bit parallel adder that produces the sum of A and B registers. The adder outputs S_7 through S_0 are connected to the D inputs of the accumulator so that the sum can be transferred to the accumulator only when a clock pulse gets through the AND gate.
The circuit operation can be described by going through each step in the multiplication of 1110 by 1001. The complete process requires 4 clock cycles.

1. **Before the first clock pulse***:* Prior to the occurrence of the first clock pulse, the register A is loaded with 00000000, the register B with the multiplicand 00001110, and the register X with the multiplier 1001. Assume that each of these registers is loaded using its asynchronous inputs(i.e., PRESET and CLEAR). The output of the adder will be the sum of A and B,i.e., 00001110.
2. **First Clock pulse***:*Since the LSB of the multiplier (X_0) is a 1, the first clock pulse gets through the AND gate and its positive going transition transfers the sum outputs into the accumulator. The subsequent negative going transition causes the X and B registers to shift right and left, respectively. This produces a new sum of A andB.
3. **Second Clock Pulse:** The second bit of the original multiplier is now in X_0 . Since this bit is a 0, the second clock pulse is inhibited from reaching the accumulator. Thus, the sum outputs are not transferred into the accumulator and the number in the accumulator does not change. The negative going transition of the clock pulse will again shift the X and B registers. Again a new sum is produced.
4. **Third Clock Pulse**:The third bit of the original multiplier is now in X_0;since this bit is a 0, the third clock pulse is inhibited from reaching the accumulator. Thus, the sum outputs are not transferred into the accumulator and the number in the accumulator does not change. The negative going transition of the clock pulse will again shift the X and B registers. Again a new sum is produced.

5. **Fourth Clock Pulse:** The last bit of the original multiplier is now in X_0 , and since it is a 1, the positive going transition of the fourth pulse transfers the sum into the accumulator. The accumulator now holds the final product. The negative going transition of the clock pulse shifts X and B again. Note that, X is now 0000, since all the multiplier bits have been shifted out.

Code converters:

The availability of a large variety of codes for the same discrete elements of information results in the use of different codes by different digital systems. It is sometimes necessary to use the output of one system as the input to another. A conversion circuit must be inserted between the two systems if each uses different codes for the same information. Thus a code converter is a logic circuit whose inputs are bit patterns representing numbers (or character) in one cod and whose outputs are the corresponding representation in a different code. Code converters are usually multiple output circuits.

To convert from binary code A to binary code B, the input lines must supply the bit combination of elements as specified by code A and the output lines must generate the corresponding bit combination of code B. A combinational circuit performs this transformation by means of logic gates.

For example, a binary –to-gray code converter has four binary input lines B_4, B_3,B_2,B_1 and four gray code output lines G_4,G_3,G_2,G_1. When the input is 0010, for instance, the output should be 0011 and so forth. To design a code converter, we use a code table treating it as a truth table to express each output as a Boolean algebraic function of all the inputs.

In this example, of binary –to-gray code conversion, we can treat the binary to the gray code table as four truth tables to derive expressions for G_4, G3, G2, and G1. Each of these four expressions would, in general, contain all the four input variables B_4, B3,B_2,and B1. Thus,this code converter is actually equivalent to four logic circuits, one for each of the truth tables.

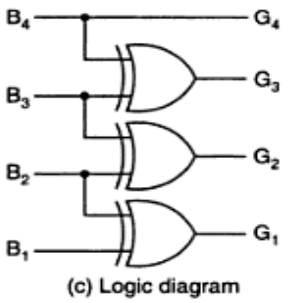
The logic expression derived for the code converter can be simplified using the usual techniques, including _don_t cares_ if present. Even if the input is an unweighted code, the same cell numbering method which we used earlier can be used, but the cell numbers --must correspond to the input combinations as if they were an 8-4-2-1 weighted code. s

Design of a 4-bit binary to gray code converter:

$$G_4 = \Sigma m(8, 9, 10, 11, 12, 13, 14, 15) \qquad G_4 = B_4$$
$$G_3 = \Sigma m(4, 5, 6, 7, 8, 9, 10, 11) \qquad G_3 = \bar{B}_4 B_3 + B_4 \bar{B}_3 = B_4 \oplus B_3$$
$$G_2 = \Sigma m(2, 3, 4, 5, 10, 11, 12, 13) \qquad G_2 = \bar{B}_3 B_2 + B_3 \bar{B}_2 = B_3 \oplus B_2$$
$$G_1 = \Sigma m(1, 2, 5, 6, 9, 10, 13, 14) \qquad G_1 = \bar{B}_2 B_1 + B_2 \bar{B}_1 = B_2 \oplus B_1$$

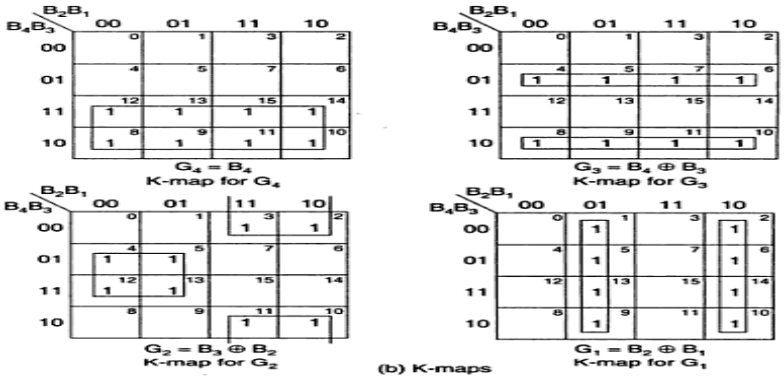
4-bit binary				4-bit Gray			
B_4	B_3	B_2	B_1	G_4	G_3	G_2	G_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

(a) Conversion table



(c) Logic diagram

4-bit binary-to-Gray code converter



(b) K-maps

4-bit binary-to-Gray code converter.

Design of a 4-bit gray to Binary code converter:

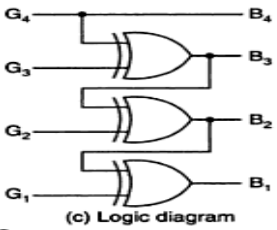
$$B_4 = \Sigma\, m(12, 13, 15, 14, 10, 11, 9, 8) = \Sigma\, m(8, 9, 10, 11, 12, 13, 14, 15)$$
$$B_3 = \Sigma\, m(6, 7, 5, 4, 10, 11, 9, 8) = \Sigma\, m(4, 5, 6, 7, 8, 9, 10, 11)$$
$$B_2 = \Sigma\, m(3, 2, 5, 4, 15, 14, 9, 8) = \Sigma\, m(2, 3, 4, 5, 8, 9, 14, 15)$$
$$B_1 = \Sigma\, m(1, 2, 7, 4, 13, 14, 11, 8) = \Sigma\, m(1, 2, 4, 7, 8, 11, 13, 14)$$

$$B_4 = G_4$$
$$B_3 = \bar{G}_4 G_3 + G_4 \bar{G}_3 = G_4 \oplus G_3$$
$$B_2 = \bar{G}_4 G_3 \bar{G}_2 + \bar{G}_4 \bar{G}_3 G_2 + G_4 \bar{G}_3 \bar{G}_2 + G_4 G_3 G_2$$
$$= \bar{G}_4 (G_3 \oplus G_2) + G_4 (\overline{G_3 \oplus G_2}) = G_4 \oplus G_3 \oplus G_2 = B_3 \oplus G_2$$
$$B_1 = \bar{G}_4 \bar{G}_3 \bar{G}_2 G_1 + \bar{G}_4 \bar{G}_3 G_2 \bar{G}_1 + \bar{G}_4 G_3 G_2 G_1 + \bar{G}_4 G_3 \bar{G}_2 \bar{G}_1 + G_4 G_3 \bar{G}_2 G_1 + G_4 G_3 G_2 \bar{G}_1 + G_4 \bar{G}_3 G_2 G_1 + G_4 \bar{G}_3 \bar{G}_2 \bar{G}_1$$

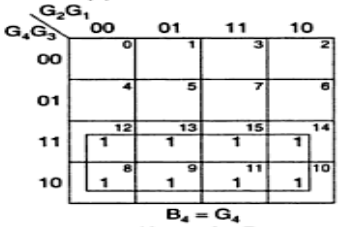
$$= \bar{G}_4 \bar{G}_3 (G_2 \oplus G_1) + G_4 G_3 (G_2 \oplus G_1) + \bar{G}_4 G_3 (\overline{G_2 \oplus G_1}) + G_4 \bar{G}_3 (\overline{G_2 \oplus G_1})$$
$$= (G_2 \oplus G_1)(\overline{G_4 \oplus G_3}) + (\overline{G_2 \oplus G_1})(G_4 \oplus G_3)$$
$$= G_4 \oplus G_3 \oplus G_2 \oplus G_1$$

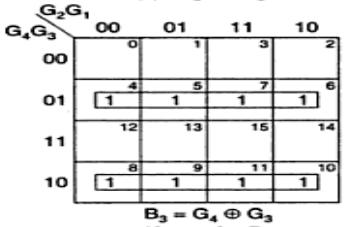
4-bit Gray				4-bit binary			
G_4	G_3	G_2	G_1	B_4	B_3	B_2	B_1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

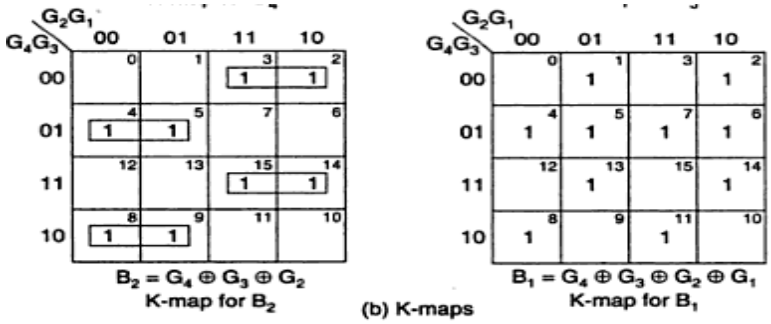
(a) Conversion table



(c) Logic diagram







(b) K-maps

4-bit Gray-to-binary code converter.

Design of a 4-bit BCD to XS-3 code converter:

8421 code				XS-3 code			
B_4	B_3	B_2	B_1	X_4	X_3	X_2	X_1
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

(a) Conversion table

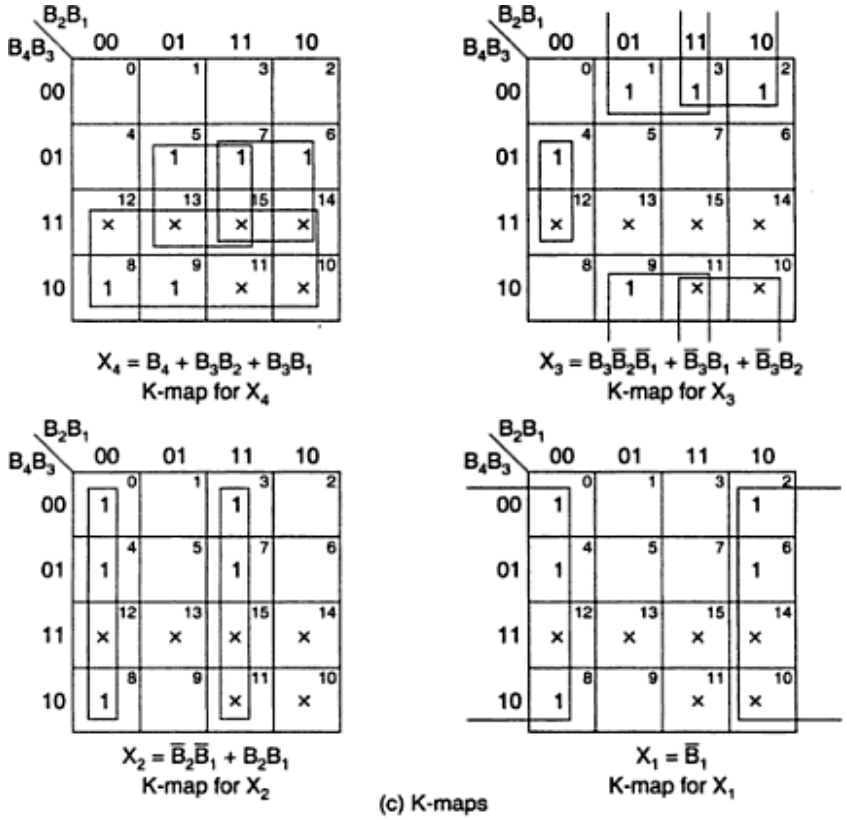
$X_4 = \Sigma\, m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$
$X_3 = \Sigma\, m(1, 2, 3, 4, 9) + d(10, 11, 12, 13, 14, 15)$
$X_2 = \Sigma\, m(0, 3, 4, 7, 8) + d(10, 11, 12, 13, 14, 15)$
$X_1 = \Sigma\, m(0, 2, 4, 6, 8) + d(10, 11, 12, 13, 14, 15)$

The minimal expressions are

$X_4 = B_4 + B_3B_2 + B_3B_1$
$X_3 = B_3\overline{B}_2\overline{B}_1 + \overline{B}_3B_1 + \overline{B}_3B_2$
$X_2 = \overline{B}_2\overline{B}_1 + B_2B_1$
$X_1 = \overline{B}_1$

(b) Minimal expressions

4-bit BCD-to-XS-3 code converter



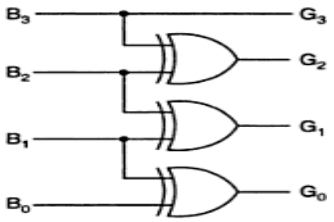
(c) K-maps

4-bit BCD-to-XS-3 code converter.

Design of a BCD to gray code converter:

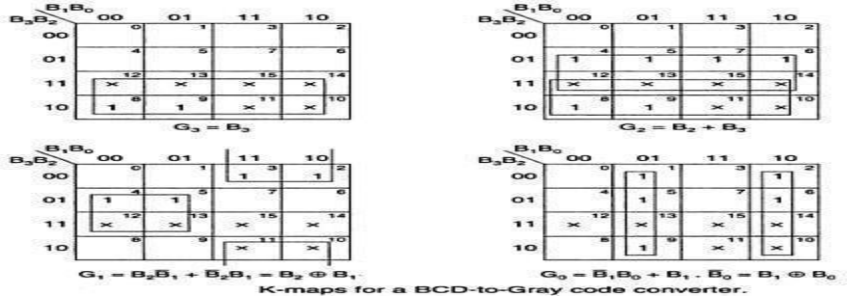
BCD code				Gray code			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1

(a) BCD-to-Gray code conversion table



(b) Logic diagram

BCD-to-Gray code converter.

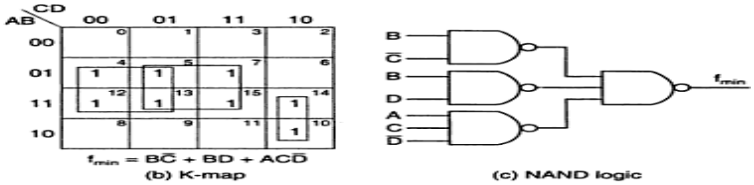


K-maps for a BCD-to-Gray code converter.

Design of a SOP circuit to Detect the Decimal numbers 5 through 12 in a 4-bit gray code Input:

Decimal number	4-bit Gray code A	B	C	D	Output f
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	1	0
3	0	0	1	0	0
4	0	1	1	0	0
5	0	1	1	1	1
6	0	1	0	1	1
7	0	1	0	0	1
8	1	1	0	0	1
9	1	1	0	1	1
10	1	1	1	1	1
11	1	1	1	0	1
12	1	0	1	0	1
13	1	0	1	1	0
14	1	0	0	1	0
15	1	0	0	0	0

(a) Truth table



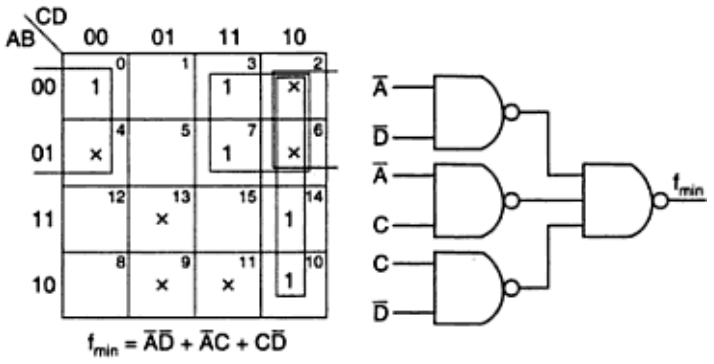
(b) K-map (c) NAND logic

Truth table, K-map and logic diagram for the SOP circuit.

Design of a SOP circuit to detect the decimal numbers 0,2,4,6,8 in a 4-bit 5211 BCD code input:

Decimal number	5211 code A	B	C	D	Output f
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	1	1
3	0	1	0	1	0
4	0	1	1	1	1
5	1	0	0	0	0
6	1	0	1	0	1
7	1	1	0	0	0
8	1	1	1	0	1
9	1	1	1	1	0

(a) Truth table



(b) K-map (c) Logic diagram

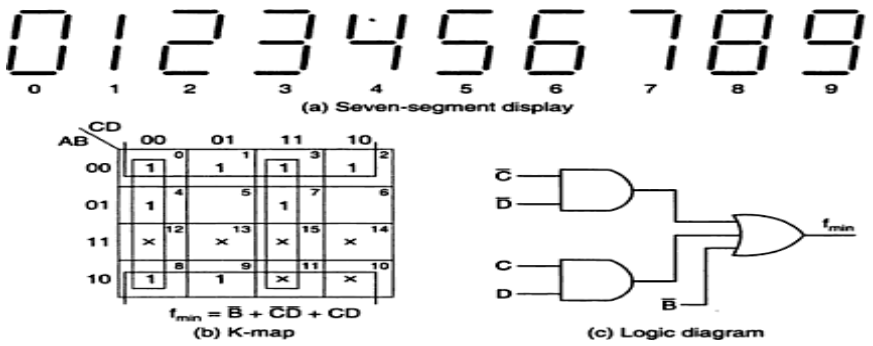
Truth table, K-map and logic diagram for the SOP circuit.

Design of a Combinational circuit to produce the *2's* complement of a 4-bit binary number:

Input				Output			
A	B	C	D	E	F	G	H
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

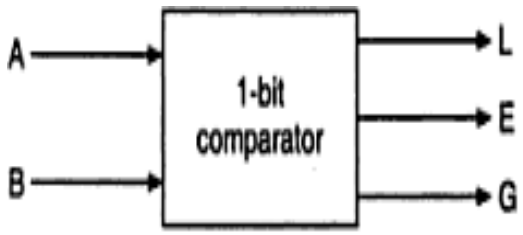
(a) Conversion table

Conversion table and K-maps for the circuit



Comparators:

$$\text{EQUALITY} = (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)$$



Block diagram of a 1-bit comparator.

The logic for a 1-bit magnitude comparator: Let the 1-bit numbers be $A = A_0$ and $B = B_0$.
If $A_0 = 1$ and $B_0 = 0$, then $A > B$.
Therefore,

$$A > B: G = A_0\overline{B}_0$$

If $A_0 = 0$ and $B_0 = 1$, then $A < B$.
Therefore,

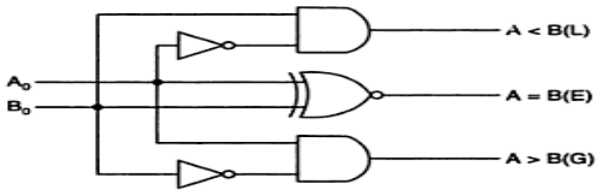
$$A < B: L = \overline{A}_0 B_0$$

If A_0 and B_0 coincide, i.e. $A_0 = B_0 = 0$ or if $A_0 = B_0 = 1$, then $A = B$.
Therefore,

$$A = B : E = A_0 \odot B_0$$

A_0	B_0	L	E	G
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

(a) Truth table



(b) Logic diagram

1-bit comparator.

1. **Magnitude Comparator:**

1- bit Magnitude Comparator:

The logic for a 2-bit magnitude comparator: Let the two 2-bit numbers be $A = A_1 A_0$ and $B = B_1 B_0$.

1. If $A_1 = 1$ and $B_1 = 0$, then $A > B$ or
2. If A_1 and B_1 coincide and $A_0 = 1$ and $B_0 = 0$, then $A > B$. So the logic expression for $A > B$ is

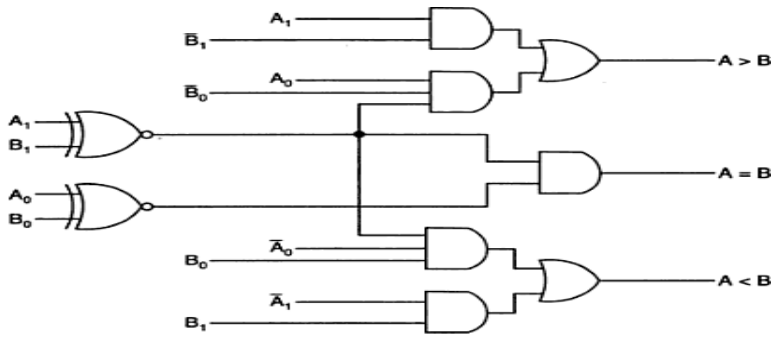
$$A > B : G = A_1\overline{B}_1 + (A_1 \odot B_1)A_0\overline{B}_0$$

1. If $A_1 = 0$ and $B_1 = 1$, then $A < B$ or
2. If A_1 and B_1 coincide and $A_0 = 0$ and $B_0 = 1$, then $A < B$. So the expression for $A < B$ is

$$A < B : L = \overline{A}_1 B_1 + (A_1 \odot B_1)\overline{A}_0 B_0$$

If A_1 and B_1 coincide and if A_0 and B_0 coincide then $A = B$. So the expression for $A = B$ is

$$A = B : E = (A_1 \odot B_1)(A_0 \odot B_0)$$



Logic diagram of a 2-bit magnitude comparator.

4- Bit Magnitude Comparator:

The logic for a 4-bit magnitude comparator: Let the two 4-bit numbers be $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$.

1. If $A_3 = 1$ and $B_3 = 0$, then $A > B$. Or
2. If A_3 and B_3 coincide, and if $A_2 = 1$ and $B_2 = 0$, then $A > B$. Or
3. If A_3 and B_3 coincide, and if A_2 and B_2 coincide, and if $A_1 = 1$ and $B_1 = 0$, then $A > B$. Or
4. If A_3 and B_3 coincide, and if A_2 and B_2 coincide, and if A_1 and B_1 coincide, and if $A_0 = 1$ and $B_0 = 0$, then $A > B$.

From these statements, we see that the logic expression for $A > B$ can be written as

$$(A > B) = A_3\overline{B}_3 + (A_3 \odot B_3)A_2\overline{B}_2 + (A_3 \odot B_3)(A_2 \odot B_2)A_1\overline{B}_1 + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)A_0\overline{B}_0$$

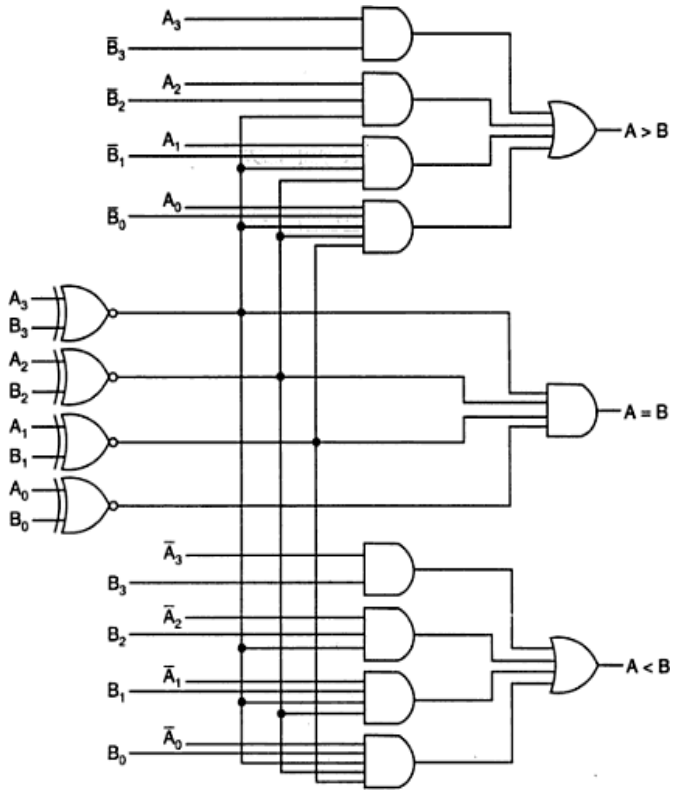
Similarly, the logic expression for $A < B$ can be written as

$$A < B = \overline{A}_3B_3 + (A_3 \odot B_3)\overline{A}_2B_2 + (A_3 \odot B_3)(A_2 \odot B_2)\overline{A}_1B_1 + (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)\overline{A}_0B_0$$

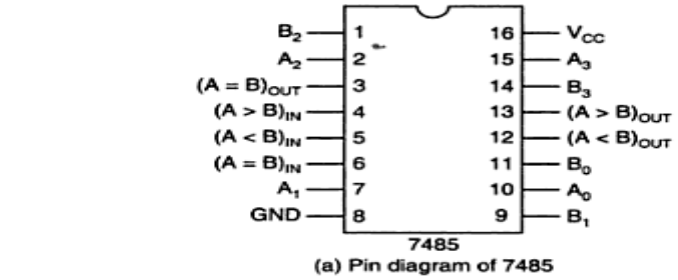
If A_3 and B_3 coincide and if A_2 and B_2 coincide and if A_1 and B_1 coincide and if A_0 and B_0 coincide, then $A = B$.

So the expression for $A = B$ can be written as

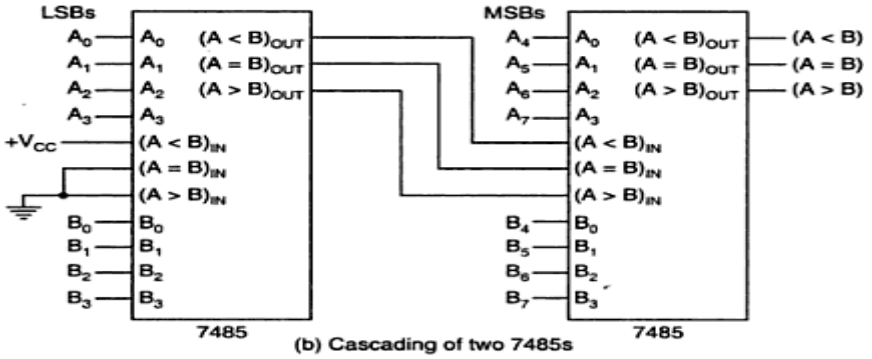
$$(A = B) = (A_3 \odot B_3)(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)$$



IC Comparator:



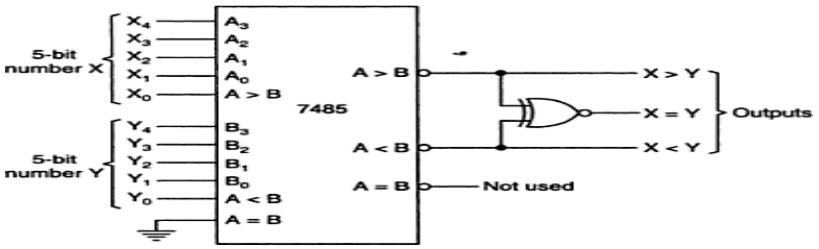
(a) Pin diagram of 7485



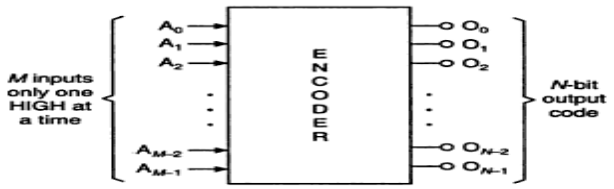
(b) Cascading of two 7485s

Pin diagram and cascading of 7485 4-bit comparators.

ENCODERS:



Use of 7485 as a 5-bit comparator.

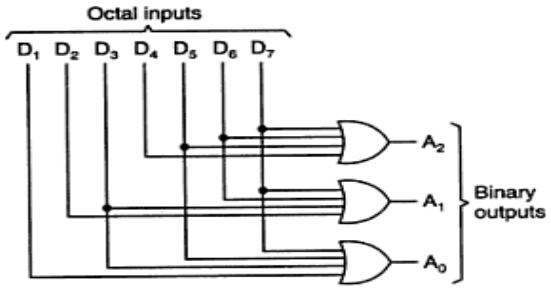


Block diagram of encoder.

Octal to Binary Encoder:

Octal digits		Binary		
		A_2	A_1	A_0
D_0	0	0	0	0
D_1	1	0	0	1
D_2	2	0	1	0
D_3	3	0	1	1
D_4	4	1	0	0
D_5	5	1	0	1
D_6	6	1	1	0
D_7	7	1	1	1

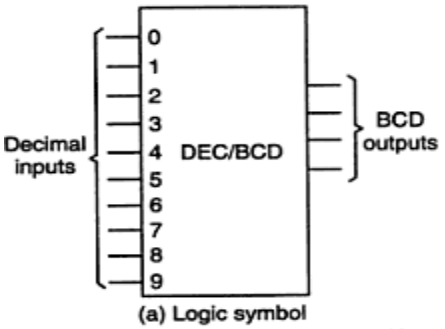
(a) Truth table



(b) Logic diagram

Octal-to-binary encoder.

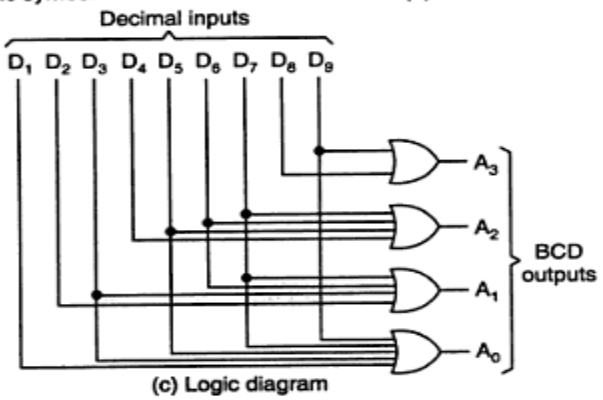
Decimal to BCD Encoder:



(a) Logic symbol

Decimal inputs		Binary			
		A_3	A_2	A_1	A_0
D_0	0	0	0	0	0
D_1	1	0	0	0	1
D_2	2	0	0	1	0
D_3	3	0	0	1	1
D_4	4	0	1	0	0
D_5	5	0	1	0	1
D_6	6	0	1	1	0
D_7	7	0	1	1	1
D_8	8	1	0	0	0
D_9	9	1	0	0	1

(b) Truth table



(c) Logic diagram

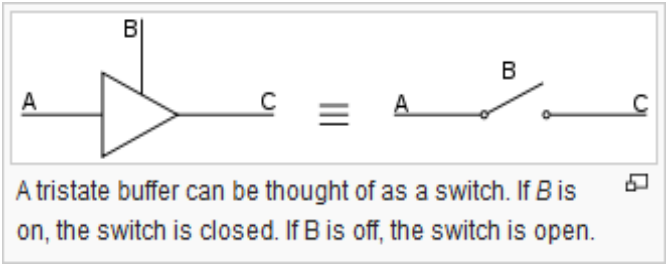
Decimal-to-BCD encoder.

Tristate bus system:

In digital electronics **three-state**, **tri-state**, or **3-state**logic allows an output port to assume a high impedance state in addition to the 0 and 1 logic levels, effectively removing the output from the circuit.

This allows multiple circuits to share the same output line or lines (such as a bus which cannot listen to more than one device at a time).

Three-state outputs are implemented in many registers, bus drivers, and flip-flops in the 7400 and 4000 series as well as in other types, but also internally in many integrated circuits. Other typical uses are internal and external buses in microprocessors, computer memory, and peripherals. Many devices are controlled by an active-low input called OE (Output Enable) which dictates whether the outputs should be held in a high-impedance state or drive their respective loads (to either 0- or 1-level).



A tristate buffer can be thought of as a switch. If *B* is on, the switch is closed. If B is off, the switch is open.

INPUT		OUTPUT
A	B	C
0	1	0
1		1
X	0	Z (high impedance)

UNIT-IV
FEEDBACK AMPLIFIERS AND OSCILLATORS

Introduction

An electronic amplifier circuit is one, which modifies the characteristics of the input signal, when delivered the output side. The modification in the characteristics of the input signal can be with respect to voltage, current, power or phase. Anyone or all these characteristics power, or phase may be changed by the amplifier circuit.

Classification of Amplifiers

There are many forms of electronic circuits classed as amplifiers, from Operational Amplifiers and Small Signal Amplifiers up to Large Signal and Power Amplifiers. The classification of an amplifier depends upon the size of the signal, large or small, its physical configuration and how it processes the input signal that is the relationship between input signal and current flowing in the load.

The type or classification of an amplifier is given in the following table.

Type of Signal	Type of Configuration	Classification	Frequency of Operation	Type of coupling	Based on the output	Number of stages
Small Signal	Common Emitter	Class A Amplifier	Direct Current (DC)	a. RC coupled amplifiers	a. Voltage amplifiers	a. Single stage amplifiers
Large Signal	Common Base	Class B Amplifier	Audio Frequencies (AF)	b. Inductive coupled amplifiers	b. Power amplifiers	b. Two stage amplifiers
	Common Collector	Class AB Amplifier	Radio Frequencies (RF)	c. Transformer coupled amplifiers and		c. Multistage amplifiers.
		Class C Amplifier	VHF, UHF and SHF Frequencies	d. Direct coupled amplifiers.		the number of stages,

Characteristics of amplifiers:

Amplifiers can be thought of as a simple box or block containing the amplifying device, such as a **Transistor**, **Field Effect Transistor** or **Op-amp**, which has two input terminals and two output terminals (ground being common) with the output signal being much greater than that of the input signal as it has been –Amplified‖.

Generally, an ideal signal amplifier has three main properties, Input Resistance or (Rin), Output Resistance or (Rout) and of course amplification known commonly as Gain or (A). No matter how complicated an amplifier circuit is, a general amplifier model can still be used to show the relationship of these three properties.

To choose a right kind of amplifier for a purpose it is necessary to know the general characteristics of amplifiers. They are: Current gain, Voltage gain, Power gain, Input impedance, Output impedance, Bandwidth.

1. Voltage gain:

Voltage gain of an amplifier is the ratio of the change in output voltage to the corresponding change in the input voltage.

$A_V = \Delta V_0 / \Delta V_I$

2. Current gain: Current gain of an amplifier is the ratio of the change in output current to thecorresponding change in the input current

$A_I = \Delta I_0 / \Delta I_I$

3. Power gain: Power gain of an amplifier is the ratio of the change in output power to the corresponding change in the input power. where po and pi are the output power and input power respectively. Since power p = v × i, The power gain

$$A_P = P_O / P_I$$

$$A_P = A_V \times A_I$$

(Power amplification of the input signal takes place at the expense of the d.c. energy.)

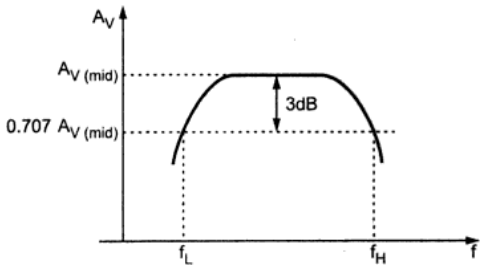
4. Input impedance (Zi): Input impedance of an amplifier is the impedance offered by the amplifier circuit as seen through the input terminals and is given by the ratio of the input voltage to the input current

$$Z_I = \Delta V_I / \Delta I_I$$

5. Output impedance (Z0): Output impedance of an amplifier is the impedance offered by the amplifier circuit as seen through the output terminals and is given by the ratio of the output

$$Z_O = \Delta V_O / \Delta I_O \text{ (At } V_s = 0)$$

6. Band width (BW): The range of frequencies over which the gain (voltage gain or current gain) of an amplifier is equal to and greater than 0.707 times the maximum gain is called the bandwidth.



In figure shown, f_L and f_H are the lower and upper cutoff frequencies where the voltage or the current gain falls to 70.7% of the maximum gain.

Bandwidth BW=(f_H- f_L).

Bandwidth is also defined as the range of frequencies over which the power gain of amplifier is equal to and greater than 50% of the maximum power gain.
The cutoff frequencies are also defined as the frequencies where the power gain falls to 50% of the maximum gain. Therefore, the cutoff frequencies are also called as Half power frequencies.

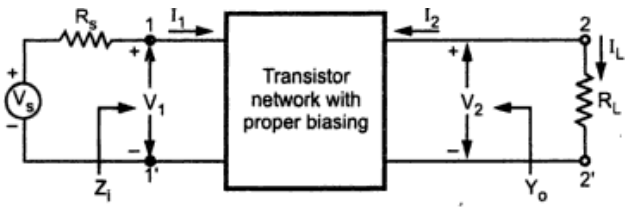
Comparison of CB, CE and CC amplifiers:

Parameters	CB	CE	CC
1. Current gain	Less than 1($\alpha \approx 1$)	High ($\beta > 1$)	Highest ($\gamma > 1$) ($\gamma = \beta + 1$)
2. Voltage gain	High	Very high	Less than 1
3. Power gain	High	Highest	>1 (low when compared to CB & CE amplifiers)
4.Input impedance	Lowest	Moderate	Highest
5.Output impedance	Highest	Moderate	Lowest
6.Phase difference	0^0 or 2π	180^0or (2n+1) π	0^0 or 2π
7. Applica-tions	Used mainly as HF amplifier	Used as a (voltage amplifier)	Used as a Buffer amplifier, impedance matching unit

HIGH FREQUENCY RESPONSE OF AMPLIFIER

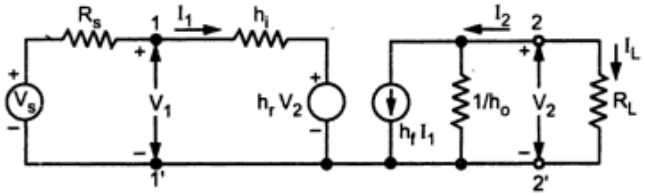
Small signal analysis of transistor amplifier

Fig shows a basic amplifier circuit. It can be noticed that to form a transistor amplifier it is necessary to connect an external load and signal source, along with proper biasing. Fig represents a transistor in any one of the three possible configurations



Basic transistor amplifier

Replacing transistor circuit with its small signal model as shown then analyzing hybrid model to find the current gain, i/p resistance, the voltage gain and the o/p resistance.



Transistor amplifier in its h-parameter model

The tabular column for parameters shown in the tabular column:

$A_i = -\frac{h_f}{1+h_o R_L}$
$A_{is} = \frac{A_i R_s}{Z_i + R_s}$
$Z_i = h_i + h_r A_i R_L = h_i - \frac{h_f h_r}{h_o + Y_L}$
$A_v = \frac{A_i R_L}{Z_i}$
$A_{vs} = \frac{A_v R_i}{Z_i + R_s} = \frac{A_i R_L}{Z_i + R_s} = \frac{A_{is} R_L}{R_s}$
$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} = \frac{1}{Z_o}$
$A_P = A_V A_i = A_i^2 \frac{R_L}{Z_i}$

The above formulae is applicable to all the configurations. An appropriate subscript to h-parameters corresponding to configuration must be added for the expressions.

Table below shows the typical values of h-parameters for 3 configurations at room temperature

Parameter	CE	CC	CB
$h_{11} = h_i$	1100 Ω	1100 Ω	21.6 Ω
$h_{12} = h_r$	2.5×10^{-4}	~ 1	2.9×10^{-4}
$h_{21} = h_f$	50	– 51	– 0.98
$h_{22} = h_o$	25 μA/V	25 μA/V	0.49 μA/V

Procedure for the analysis of transistor amplifier circuit

1. Draw the actual circuit diagram.
2. Replace coupling capacitors and emitter bypass capacitor by short circuit.
3. Replace dc source by a short circuit. In other words, short V_{CC} and ground lines.
4. Mark the points B(base), C(collector), E(emitter) on the circuit diagram and locate these points as the start of the equivalent circuit.
5. Replace the transistor by its h-parameter model.

Converting from one configuration to another configuration

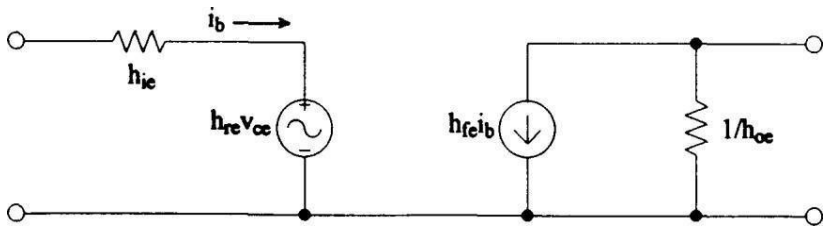
Most of the times h-parameters are specified in CE configuration, therefore for analyzing of CC & CB configurations it is require to first convert the given h-parameters for CE configuration into the required configuration by using conversion formulae as given the table below.

Symbol	Common emitter	Common collector	Common base	T equivalent circuit
h_{ie}	1,100 Ω	h_{ic} *	$\frac{h_{ib}}{1+h_{fb}}$	$r_b + \frac{r_e}{1-a}$
h_{re}	25×10^{-4}	$1 - h_{rc}$ *	$\frac{h_{rb} h_{ob}}{1+h_{fb}} - h_{rb}$	$\frac{r_b}{(1-a) r_c}$
h_{fe}	50	$-(1+h_{fc})$ *	$-\frac{h_{fb}}{1+h_{fb}}$	$\frac{a}{1-a}$
h_{oe}	25 μA/V	h_{oc} *	$\frac{h_{ob}}{1+h_{fb}}$	$\frac{1}{(1-a) r_c}$
h_{ib}	$\frac{h_{ie}}{1+h_{fe}}$	$-\frac{h_{ic}}{h_{fc}}$	21.6 Ω	$r_e + (1-a) r_b$
h_{rb}	$\frac{h_{ie} h_{oe}}{1+h_{fe}} - h_{re}$	$h_{fc} - \frac{h_{ic} h_{oc}}{h_{fc}} - 1$	29×10^{-4}	$\frac{r_b}{r_c}$
h_{fb}	$-\frac{h_{fe}}{1+h_{fe}}$	$-\frac{1+h_{fc}}{h_{fc}}$	− 0.98	− a
h_{ob}	$\frac{h_{oe}}{1+h_{fe}}$	$-\frac{h_{oc}}{h_{fc}}$	0.49 μA/V	$\frac{1}{r_c}$
h_{ic}	h_{ie} *	1,100 Ω	$\frac{h_{ib}}{1+h_{fb}}$	$r_b + \frac{r_e}{1-a}$
h_{rc}	$1 - h_{re} \approx 1$ *	1	1	$1 - \frac{r_e}{(1-a) r_c}$
h_{fc}	$-(1+h_{fe})$ *	− 51	$-\frac{1}{1+h_{fb}}$	$-\frac{1}{1-a}$
h_{oc}	h_{oe} *	25 μA/V	$\frac{h_{ob}}{1+h_{fb}}$	$\frac{1}{(1-a) r_c}$
a	$\frac{h_{fe}}{1+h_{fe}}$	$\frac{1+h_{fc}}{h_{fc}}$	$-h_{fb}$	0.980
r_c	$\frac{1+h_{fe}}{h_{oe}}$ *	$-\frac{h_{fc}}{h_{oc}}$ *	$\frac{1}{h_{ob}}$	2.04 M
r_e	$\frac{h_{re}}{h_{oe}}$ *	$\frac{1-h_{rc}}{h_{oc}}$ *	$h_{ib} + \frac{h_{rb}}{h_{ob}}(1+h_{fb})$ *	10 Ω
r_b	$h_{ic} + \frac{h_{re}}{h_{oe}}(1+h_{fe})$ *	$h_{ic} + \frac{h_{fc}}{h_{oc}}(1+h_{rc})$ *	$\frac{h_{rb}}{h_{ob}}$ *	590 Ω

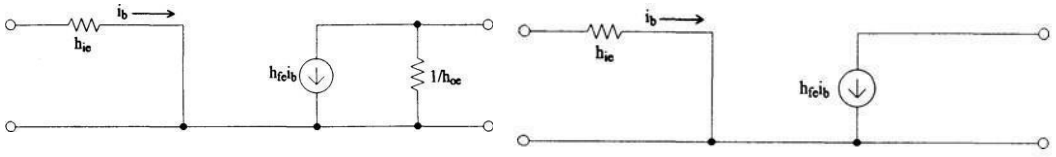
h-parameter conversion table

Simplified analysis of CE Configuration

The hybrid parameter equivalent circuit of a common-emitter transistor is shown in Fig.



The approximation $h_{re} \approx 0$ is sometimes utilized which yields a 3-parameter model shown in Figure The two approximations of $h_{re} \approx 0$ and $h_{oe} \approx 0$ are frequently utilized and result in the common 2-parameter model shown in Fig.

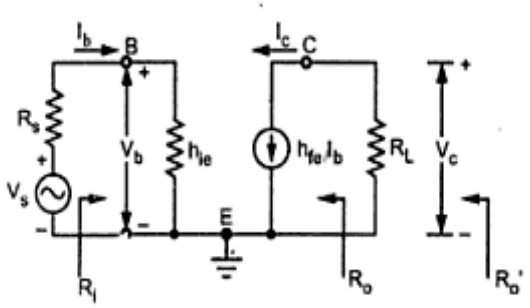


The values of h_{ie} , h_{fe}. h_{re} h_{oe} for a specifci bipolar junction transistor are typically found in the manufacturer‘s small- signal specifications. The values can also be determined from the **common-emitter** output characteristic curves.

Utilizing a single transistor model it is possible to analyze common-emitter, common-base, or common- collector amplifier circuits.

Approximate Hybrid Analysis for CE Transistor Amplifier

The *h*-parameter formulas (*CE* configuration) can be approximated to a form that is easier to handle. While these approximate formulas will not give results that are as accurate as the original formulas, they can be used for many applications. The CE approximate model is as shown in fig.



Approximate CE model

(i) Input impedance

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

In actual practice, the second termin this expression is very small as compared to the first term.

$$Z_{in} = h_{ie}$$

… approximate formula

(ii) Current gain:

$$\text{Current gain, } A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

In actual practice, $h_{oe}\, r_L$ is very small as compared to 1.

$$A_i = h_{fe}$$

… approximate formula

(iii) Voltage gain:

$$\text{Voltage gain, } A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

$$= \frac{-h_{fe}\, r_L}{Z_{in}\,(h_{oe}\, r_L + 1)}$$

Now approximate formula for Z_{in} is h_{ie}. Also $h_{oe}\, r_L$ is very small as compared to 1.

$$A_v = -\frac{h_{fe}\, r_L}{h_{ie}}$$

... approximate formula

(iv) Output impedance:

Output impedance of transistor

$$Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}\, h_{re}}{h_{ie}}}$$

The second term in the denominator is very small as compared to h_{oe}. $Z_{out} = \frac{1}{h_{oe}}$ ...approximate formula

The output impedance of transistor amplifier

$$= Z_{out} \| r_L \qquad \text{where } {}^{*}r_L = R_C \| R_L$$

If the amplifier is unloaded (*i.e.* $RL = \infty$), $rL = RC$.

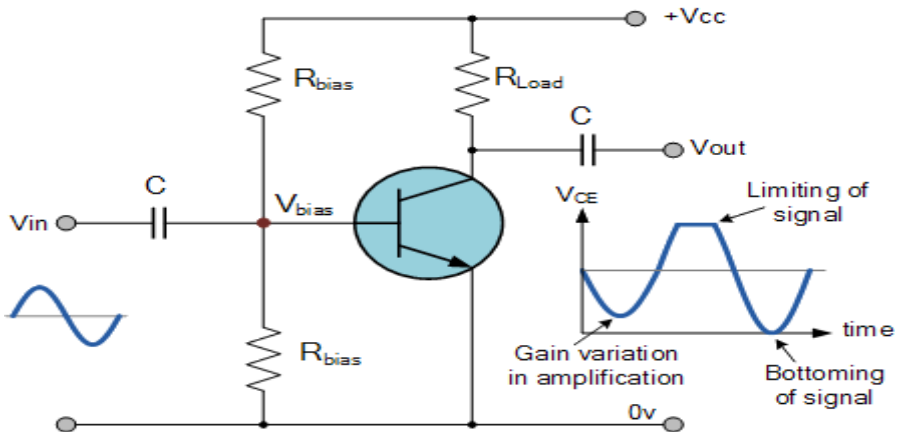
Approximate Hybrid Analysis for CC Transistor Amplifier

Amplifier Distortion

From the previous tutorials we that for a signal amplifier to operate correctly without any distortion to the output signal, it requires some form of DC Bias on its Base or Gate terminal so that it can amplify the input signal over its entire cycle with the bias -Q-point| set as near to the middle of the load line as possible. This then gave us a -Class- A| type amplification configuration with the most common arrangement being the -Common Emitter| for Bipolar transistors and the -Common Source| for unipolar FET transistors.

We also learnt that the Power, Voltage or Current Gain, (amplification) provided by the amplifier is the ratio of the peak output value to its peak input value (Output ÷ Input). However, if we incorrectly design our amplifier circuit and set the biasing Q-point at the wrong position on the load line or apply too large an input signal to the amplifier, the resultant output signal may not be an exact reproduction of the original input signal waveform. In other words the amplifier will suffer from what is commonly called **Amplifier Distortion**. Consider the Common Emitter Amplifiercircuit below.

Common Emitter Amplifier



Distortion of the output signal waveform may occur because:

- **1.** Amplification may not be taking place over the whole signal cycle due to incorrect biasing levels.
- **2.** The input signal may be too large, causing the amplifiers transistors to be limited by the supply voltage.
- **3.** The amplification may not be a linear signal over the entire frequency range of inputs.

This means then that during the amplification process of the signal waveform, some form of**Amplifier Distortion** has occurred.

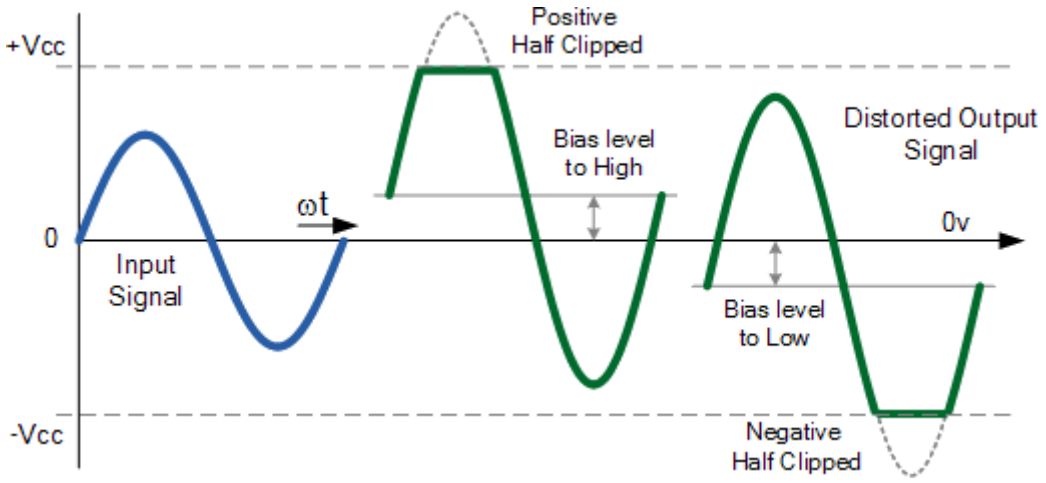
Amplifiers are basically designed to amplify small voltage input signals into much larger output signals and this means that the output signal is constantly changing by some factor or value, called gain, multiplied by the input signal for all input frequencies. We saw previously that this multiplication factor is called the Beta, β value of the transistor.

Common emitter or even common source type transistor circuits work fine for small AC input signals but suffer from one major disadvantage, the calculated position of the bias Q-point of a bipolar amplifier depends on the same Beta value for all transistors. However, this Beta value will vary from transistors of the same type, in other words, the Q-point for one transistor is not necessarily the same as the Q-point for another transistor of the same type due to the inherent manufacturing tolerances.

Then amplifier distortion occurs because the amplifier is not linear and a type of amplifier distortion called **Amplitude Distortion** will result. Careful choice of the transistor and biasing components can help minimise the effect of amplifier distortion.

Amplitude Distortion Amplitude distortion occurs when the peak values of the frequency waveform are attenuated causing distortion due to a shift in the Q-point and amplification may not take place over the whole signal cycle. This non-linearity of the output waveform is shown below.

Amplitude Distortion due to Incorrect Biasing



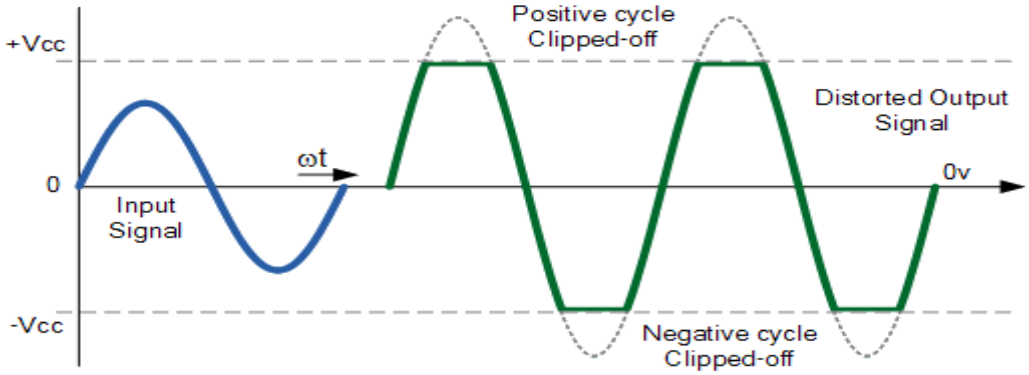
If the transistors biasing point is correct, the output waveform should have the same shape as that of the input waveform only bigger, (amplified). If there is insufficient bias and the Q-point lies in the lower half of the load line, then the output waveform will look like the one on the right with the negative half of the output waveform "cut-off" or clipped. Likewise, if there is too much bias and the Q-point lies in the upper half of the load line, then the output waveform will look like the one on the left with the positive half "cut-off" or clipped.

Also, when the bias voltage is set too small, during the negative half of the cycle the transistor does not fully conduct so the output is set by the supply voltage. When the bias is too great the positive half of the cycle saturates the transistor and the output drops almost to zero.

Even with the correct biasing voltage level set, it is still possible for the output waveform to become distorted due to a large input signal being amplified by the circuits gain. The output voltage signal becomes clipped in both the positive and negative parts of the waveform an no longer resembles a sine wave, even when the bias is correct. This type of amplitude distortion is called **Clipping** and is the result of "over-driving" the input of the amplifier.

When the input amplitude becomes too large, the clipping becomes substantial and forces the output waveform signal to exceed the power supply voltage rails with the peak (+ve half) and the trough (-ve half) parts of the waveform signal becoming flattened or "Clipped-off". To avoid this the maximum value of the input signal must be limited to a level that will prevent this clipping effect as shown above.

Amplitude Distortion due to Clipping



Amplitude Distortion greatly reduces the efficiency of an amplifier circuit. These "flat tops" of the distorted output waveform either due to incorrect biasing or over driving the input do not contribute anything to the strength of the output signal at the desired frequency.

Having said all that, some well known guitarist and rock bands actually prefer that their distinctive sound is highly distorted or "overdriven" by heavily clipping the output waveform to both the +ve and -ve power supply rails. Also, increasing the amounts of clipping on a sinusoid will produce so much amplifier distortion that it will eventually produce an output waveform which resembles that of a "square wave" shape which can then be used in electronic or digital synthesizer circuits.

We have seen that with a DC signal the level of gain of the amplifier can vary with signal amplitude, but as well as Amplitude

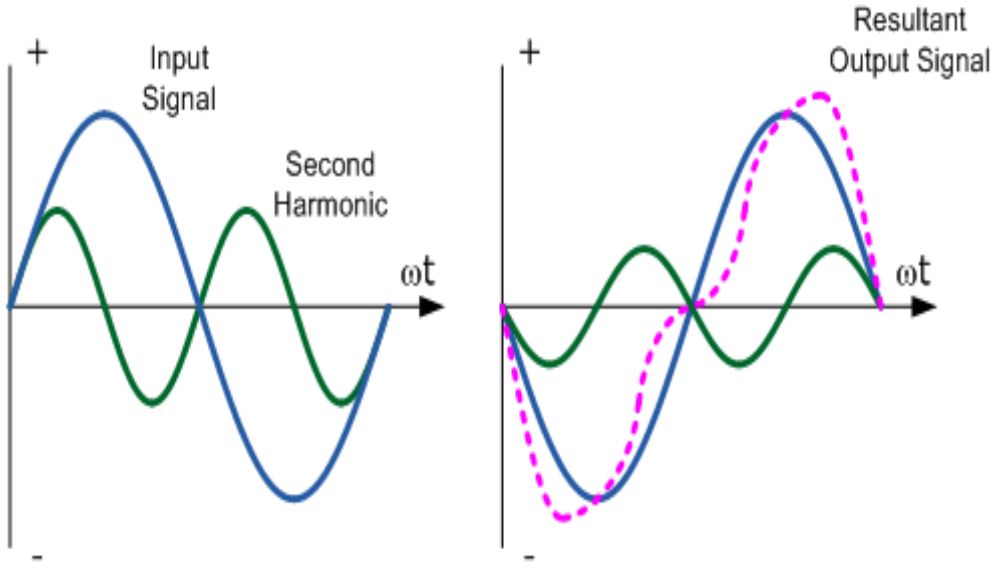
Distortion, other types of amplifier distortion can occur with AC signals in amplifier circuits, such as **Frequency Distortion** and **Phase Distortion**.

Frequency Distortion

Frequency Distortion is another type of amplifier distortion which occurs in a transistor amplifier when the level of amplification varies with frequency. Many of the input signals that a practical amplifier will amplify consist of the required signal waveform called the -Fundamental Frequency plus a number of different frequencies called -Harmonics superimposed onto it.

Normally, the amplitude of these harmonics are a fraction of the fundamental amplitude and therefore have very little or no effect on the output waveform. However, the output waveform can become distorted if these harmonic frequencies increase in amplitude with regards to the fundamental frequency. For example, consider the waveform below:

Frequency Distortiondueto Harmonics



In the example above, the input waveform consists a the fundamental frequency plus a second harmonic signal. The resultant output waveform is shown on the right hand side. The frequency distortion occurs when the fundamental frequency combines with the second harmonic to distort the output signal. Harmonics are therefore multiples of the fundamental frequency and in our simple example a second harmonic was used.

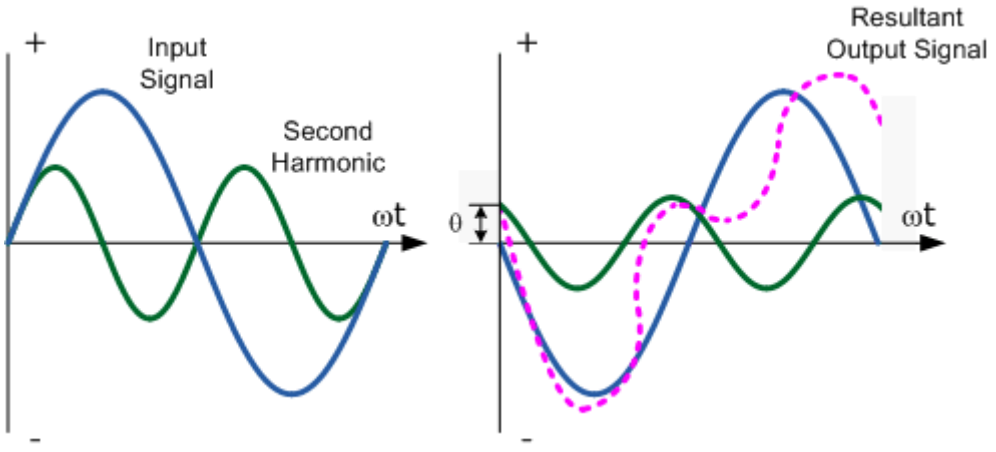
Therefore, the frequency of the harmonic is twice the fundamental, 2 x f or $2f$. Then a third harmonic would be $3f$, a fourth, $4f$, and so on. Frequency distortion due to harmonics is always a possibility in amplifier circuits containing reactive elements such as capacitance or inductance.

Phase Distortion

Phase Distortion or **Delay Distortion** is a type of amplifier distortion which occurs in a non-linear transistor amplifier when there is a time delay between the input signal and its appearance at the output.

If we say that the phase change between the input and the output is zero at the fundamental frequency, the resultant phase angle delay will be the difference between the harmonic and the fundamental. This time delay will depend on the construction of the amplifier and will increase progressively with frequency within the bandwidth of the amplifier. For example, consider the waveform below:

Phase Distortion due to Delay



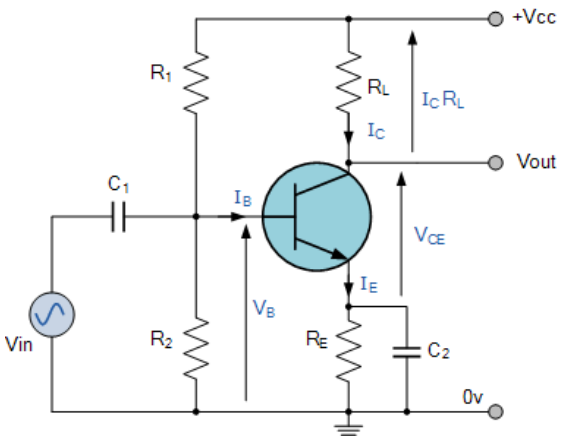
Other than high end audio amplifiers, most Practical Amplifiers will have some form of **Amplifier Distortion** being a combination of both "Frequency Distortion" and "Phase Distortion", together with amplitude distortion. In most applications such as in audio amplifiers or power amplifiers, unless the amplifiers distortion is excessive or severe it will not generally affect the operation or output sound of the amplifier.

In the next tutorial about Amplifiers we will look at the **Class A Amplifier**. Class A amplifiers are the most common type of amplifier output stage making them ideal for use in audio power amplifiers.

Amplifiers Tutorial Summary

Amplifiers are used extensively in electronic circuits to make an electronic signal bigger without affecting it in any other way. Generally we think of *Amplifiers* as audio amplifiers in the radios, CD players and stereo's we use around the home. In this amplifier tutorial section we looked at the amplifier which is based on a single bipolar transistor as shown below, but there are several different kinds of transistor amplifier circuits that we could use.

Typical Single Stage Amplifier Circuit



Small Signal Amplifiers

- Small Signal Amplifiers are also known as **Voltage Amplifiers**.
- Voltage Amplifiers have 3 main properties, **Input Resistance**, **Output Resistance** and **Gain**.

- The Gain of a small signal amplifier is the amount by which the amplifier "Amplifies" the input signal.

- Gain is a ratio of input divided by output, therefore it has no units but is given the symbol (A) with the most common types of transistor gain being, **Voltage Gain (Av), Current Gain (Ai)**and **Power Gain(Ap)**
- The power Gain of the amplifier can also be expressed in **Decibels** or simply **dB**.
- In order to amplify all of the input signal distortion free in a Class A type amplifier, DC Base Biasing is required.
- DC Bias sets the Q-point of the amplifier half way along the loadline.
- This DC Base biasing means that the amplifier consumes power even if there is no input signalpresent.
- The transistor amplifier is non-linear and an incorrect bias setting will produce large amounts of distortion to the output waveform.
- Too large an input signal will produce large amounts of distortion due to clipping, which is also a form of amplitude distortion.
- Incorrect positioning of the Q-point on the load line will produce either **Saturation Clipping**or **Cut-off Clipping**.

- The **Common Emitter Amplifier** configuration is the most common form of all the general purpose voltage amplifier circuit using a Bipolar Junction Transistor.
- The **Common Source Amplifier** configuration is the most common form of all the general purpose voltage amplifier circuit using a Junction Field Effect Transistor.

Simplified common emitter hybrid model:

1.3 Common Emitter Amplifier
Common Emitter Circuit is as shown in the Fig. 1.2. The DC supply, biasing resistors and coupling capacitors are not shown since we are performing an *AC analysis*.

$$h_{ie} = \left.\frac{V_{be}}{I_b}\right|_{V_{ce}=0} \qquad h_{re} = \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0}$$

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b=0} \qquad h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0}$$

The typical values of the *h-parameter* for a transistor in Common Emitter Configuration are,

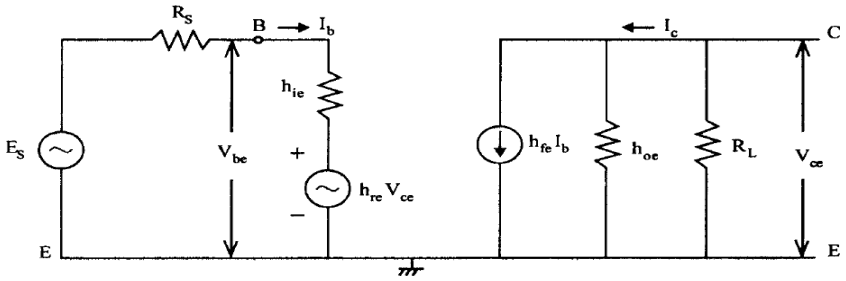


Fig. 1.3 h-parameter Equivalent Circuit Since,
V be is a fraction of volt O.2V, Ib in ~A, 1 00 ~A and so on. 0.2V
h· = =4KO
Ie 50xlO-6

hfe == Ic/Ib :: 100.
Ie is in rnA and Is in 1lA. hfe » 1:: P

hre == 0.2 x 10-3. Because, it is the *Reverse* Voltage Gain. and
Vbe
hre = Vee Vee> Vbe;
Input
h = -'"---
re Output
Output is » input, because amplification takes place. Therefore hre « 1. ho e= 8 Il 7v0;: and ho e == ~ .
Vee

1.3.1 Input Resistance of the Amplifier Circuit (Ri)

Common Base	Common Emitter	Common Collector	Definitions
		$h_{ic} = \frac{v_{bc}}{i_b}$	Input Impedance with Output Short Circuit
		$h_{rc} = \frac{v_{bc}}{v_{ec}}$	Reverse Voltage Ratio Input Open Circuit
$h_{fb} = \frac{i_c}{i_e}$	$h_{fe} = \frac{i_c}{i_b}$	$h_{fc} = \frac{i_e}{i_b}$	Forward Current Gain Output Short Circuit
$h_{ob} = \frac{i_c}{v_{cb}}$	v_{ce}		Output Admittance Input Open Circuit

In most practical cases it is appropriate to obtain approximate values of A_V, A_i etc rather than calculating exact values. How the circuit can be modified without greatly reducing the accuracy. **Fig. 4** shows the CE amplifier equivalent circuit in terms of h-parameters Since 1 / h_{oe} in parallel with R_L is approximately equal to R_L if 1 / h_{oe} >> R_L then h_{oe} may be neglected. Under these conditions.

$I_c = h_{fe} I_B$.

$h_{re} v_c = h_{re} I_c R_L = h_{re} h_{fe} I_b R_L$.

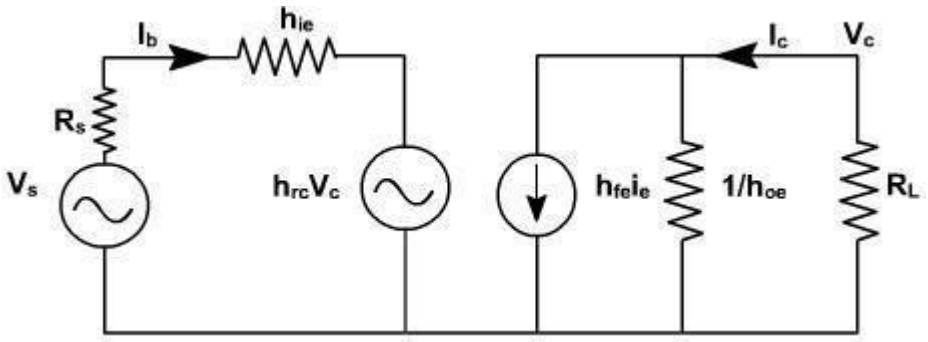


Fig. 4

Since $h_{fe}.h_{re}$ □ 0.01, this voltage may be neglected in comparison with h_{ic} I_b drop across h_{ie} provided R_L is not very large. If load resistance R_L is small than hoe and h_{re} can beneglected.

$$A_I = -\frac{h_{fe}}{1+h_{oe}\,R_L} \approx -h_{fe}$$

$$R_i = h_{ie}$$

$$A_V = \frac{A_I\,R_L}{R_i} = -\frac{h_{fe}\,R_L}{h_{ie}}$$

Output impedence seems to be infinite. When $V_s = 0$, and an external voltage is applied at the output we fined $I_b = 0$, $I_C = 0$. True value depends upon R_S and lies between 40 K and 80K.
On the same lines, the calculations for CC and CB can be done.

CE amplifier with an emitter resistor:

The voltage gain of a CE stage depends upon h_{fe}. This transistor parameter depends upon temperature, aging and the operating point. Moreover, h_{fe} may vary widely from device to device, even for same type of transistor. To stabilize voltage gain A_V of each stage, it should be independent of h_{fe}. A simple and effective way is to connect an emitter resistor R_e as shown in **fig. 5**. The resistor provides negative feedback and provide stabilization.

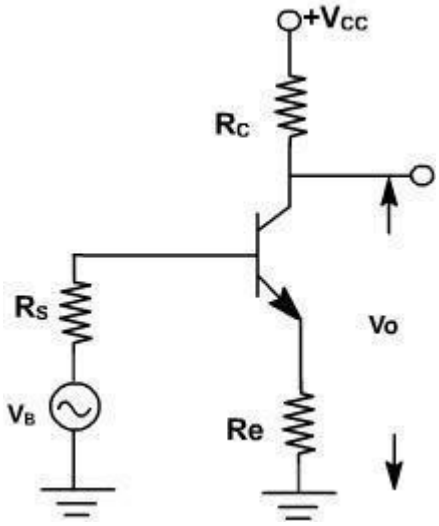


Fig. 5

An approximate analysis of the circuit can be made using the simplified model.

Current gain $A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b} = -\frac{h_{fe}\, I_b}{I_b}$

$= -h_{fe}$

It is unaffected by the addition of R_C.

Input resistance is given by

$$R_i = \frac{V_i}{I_b}$$

$$= \frac{h_{ie}\, I_b + (1+h_{fe})\, I_b\, R_e}{I_b}$$

$$= h_{ie} = (1+h_{fe})\, R_e$$

The input resistance increases by $(1+h_{fe})R_e$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe}\, R_L}{h_{ie} + (1+h_{fe})R_e}$$

Clearly, the addition of R_e reduces the voltage gain.

If $(1+h_{fe})R_e >> h_{ie}$ and $h_{fe} >> 1$

then

$$A_v = \frac{-h_{fe}\, R_L}{(1+h_{fe})R_e} \approx -\frac{R_L}{R_e}$$

Subject to above approximation A_V is completely stable. The output resistance is infinite for the approximate model.

Common Emitter Amplifier Example No1

A common emitter amplifier circuit has a load resistance, R_L of 1.2kΩs and a supply voltage of 12v. Calculate the maximum Collector current (Ic) flowing through the load resistor when the transistor is switched fully -ON| (saturation), assume Vce = 0. Also find the value of the Emitter resistor, R_E with a voltage drop of 1v across it. Calculate the values of all the other circuit resistors assuming an NPN silicon transistor.

$$I_{C(MAX)} = \frac{V_{CC} - V_{RE}}{R_L} = \frac{12-1}{1200} = 9.2\text{mA}$$

$$V_{CE} = 0 \text{ (Saturation)}$$

This then establishes point -A| on the Collector current vertical axis of the characteristics curves and occurs when Vce = 0. When the transistor is switched fully -OFF|, their is no voltage drop across either resistor R_E or R_L as no current is flowing through them. Then the voltage drop across the transistor, Vce is equal to the supply voltage, Vcc. This establishes point -B| on the horizontal axis of the characteristics curves.

Generally, the quiescent Q-point of the amplifier is with zero input signal applied to the Base, so the Collector sits half-way along the load line between zero volts and the supply voltage, (Vcc/2). Therefore, the Collector current at the Q-point of the amplifier will be given as:

$$Ic_{(Q)} = \frac{\frac{12-1}{2}}{1200} = \frac{5.5}{1200} = 4.58\text{mA}$$

This static DC load line produces a straight line equation whose slope is given as: $-1/(R_L + R_E)$ and that it crosses the vertical Ic axis at a point equal to $Vcc/(R_L + R_E)$. The actual position of the Q-point on the DC load line is determined by the mean value of Ib.

As the Collector current, Ic of the transistor is also equal to the DC gain of the transistor (Beta), times the Base current (β x Ib), if we assume a Beta (β) value for the transistor of say 100, (one hundred is a reasonable average value for low power signal transistors) the Base current Ib flowing into the transistor will be given as:

$$\beta = \frac{I_C}{I_B}$$

$$\therefore I_B = \frac{I_C}{\beta} = \frac{4.58mA}{100} = 45.8\mu A$$

Instead of using a separate Base bias supply, it is usual to provide the Base Bias Voltage from the main supply rail (Vcc) through a dropping resistor, R1. Resistors, R1 and R2 can now be chosen to give a suitable quiescent Base current of 45.8µA or 46µA rounded off. The current flowing through the potential divider circuit has to be large compared to the actual Base current, Ib, so that the voltage divider network is not loaded by the Base current flow.

A general rule of thumb is a value of at least 10 times Ib flowing through the resistor R2. Transistor Base/Emitter voltage, Vbe is fixed at 0.7V (silicon transistor) then this gives the value of R2 as:

$$R_2 = \frac{V_{(RE)} + V_{(BE)}}{10 \times I_B} = \frac{1 + 0.7}{458 \times 10^{-6}} = 3.71k\Omega$$

If the current flowing through resistor R2 is 10 times the value of the Base current, then the current flowing through resistor R1 in the divider network must be 11 times the value of the Base current. The voltage across resistor R1 is equal to Vcc – 1.7v (V_{RE} + 0.7 for silicon transistor) which is equal to 10.3V, therefore R1 can be calculated as:

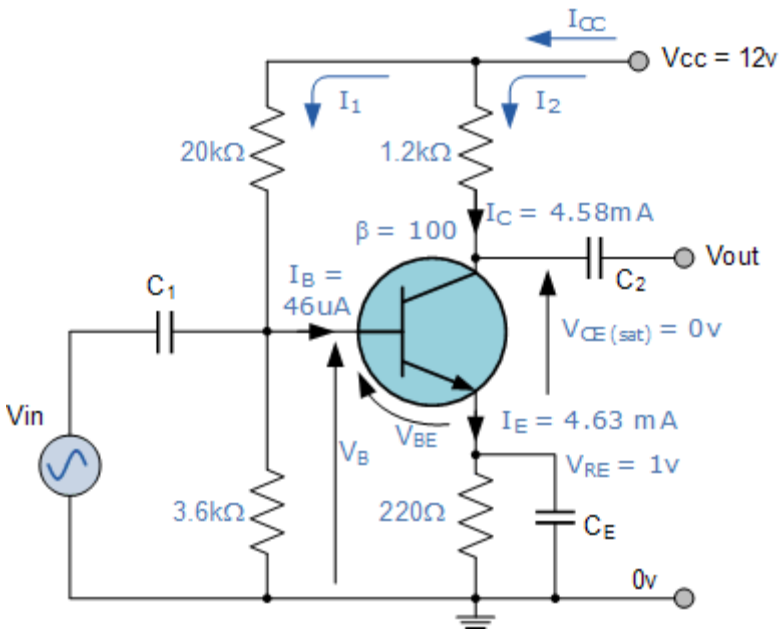
$$R_1 = \frac{V_{CC} - \left(V_{(RE)} + V_{(BE)}\right)}{11 \times I_B} = \frac{12 - 1.7}{504 \times 10^{-6}} = 20.45k\Omega$$

The value of the Emitter resistor, R_E can be easily calculated using **Ohm's Law**. The current flowing through R_E is a combination of the Base current, Ib and the Collector current Ic and is given as:

$$I_E = I_C + I_B = 4.58mA + 45.8\mu A = 4.63mA$$

Resistor, R_E is connected between the Emitter and ground and we said previously that it has a voltage of 1 volt across it. Then the value of R_E is given as:

$$R_E = \frac{V_{RE}}{I_E} = \frac{1v}{4.63mA} = 216\Omega$$



Coupling Capacitors

In **Common Emitter Amplifier** circuits, capacitors C1 and C2 are used as **Coupling Capacitors** to separate the AC signals from the DC biasing voltage. This ensures that the bias condition set up for the circuit to operate correctly is not effected by any additional amplifier stages, as the capacitors will only pass AC signals and block any DC component. The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, C_E is included in the Emitter leg circuit.

This capacitor is an open circuit component for DC bias meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor short circuits the Emitter resistor at high frequency signals and only R_L plus a very small internal resistance acts as the transistors load increasing the voltage gain to its maximum. Generally, the value of the bypass capacitor, C_E is chosen to provide a reactance of at most, 1/10th the value of R_E at the lowest operating signal frequency.

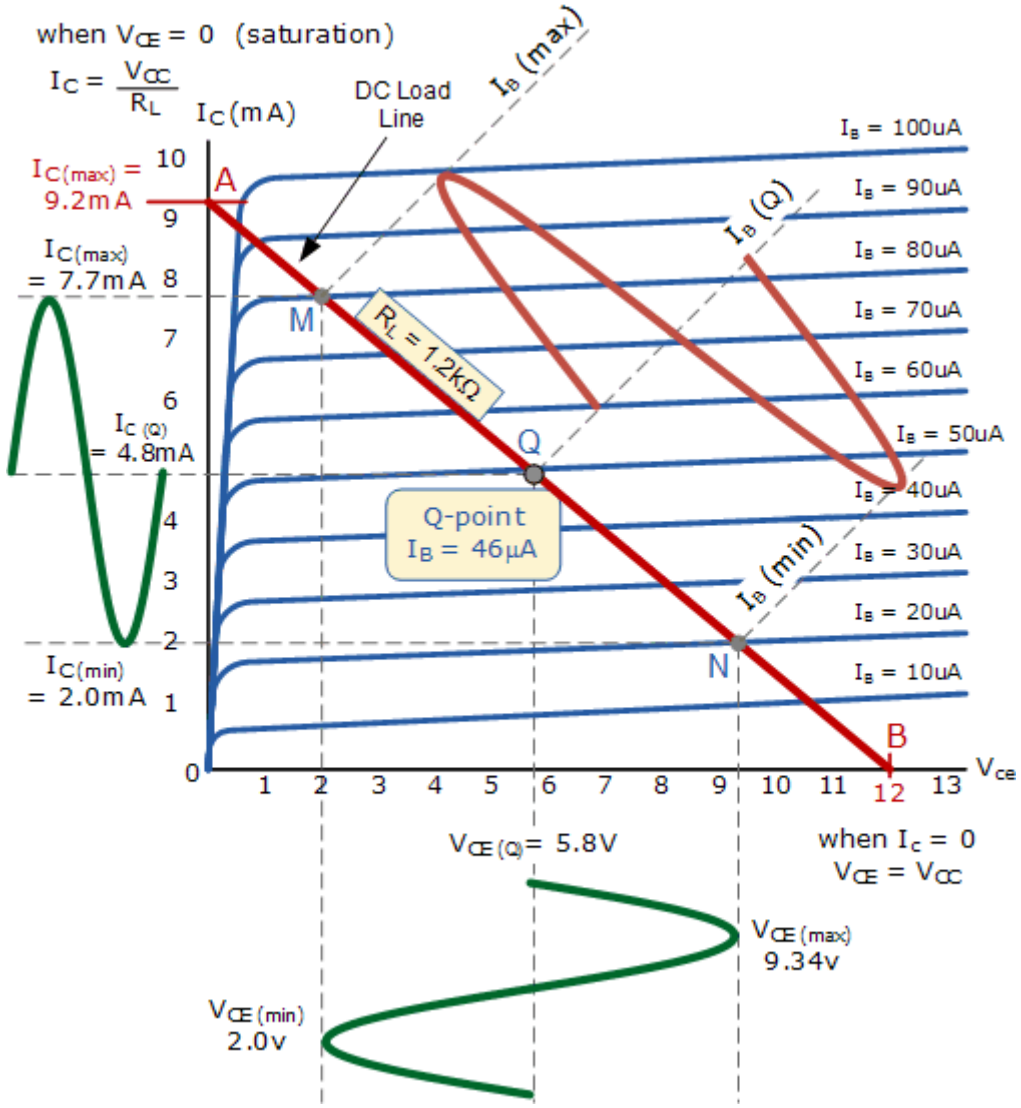
Output Characteristics Curves

Ok, so far so good. We can now construct a series of curves that show the Collector current, Icagainst the Collector/Emitter voltage, Vce with different values of Base current, Ib for our simple common emitter amplifier circuit. These curves are known as the -Output Characteristic Curves| and are used to show how the transistor will operate over its dynamic range. A static or DC load line is drawn onto the curves for the load resistor RL of 1.2kΩ to show all the transistors possible operating points.

When the transistor is switched -OFF|, Vce equals the supply voltage Vcc and this is point B on the line. Likewise when the transistor is fully -ON| and saturated the Collector current is determined by the load resistor, RL and this is point A on the line.

We calculated before from the DC gain of the transistor that the Base current required for the mean position of the transistor was 45.8µA and this is marked as point Q on the load line which represents the **Quiescent point** or **Q- point** of the amplifier. We could quite easily make life easy for ourselves and round off this value to 50µA exactly, without any effect to the operating point.

Output Characteristics Curves



Point Q on the load line gives us the Base current Q-point of Ib = 45.8µA or 46µA. We need to find the maximum and minimum peak swings of Base current that will result in a proportional change to the Collector current, Ic without any distortion to the output signal.

As the load line cuts through the different Base current values on the DC characteristics curves we can find the peak swings of Base current that are equally spaced along the load line. These values are marked as points N and M on the line, giving a minimum and a maximum Base current of 20µAand 80µA respectively.

These points, N and M can be anywhere along the load line that we choose as long as they are equally spaced from Q. This then gives us a theoretical maximum input signal to the Base terminal of 60µA peak-to-peak, (30µA peak) without producing any distortion to the output signal.

Any input signal giving a Base current greater than this value will drive the transistor to go beyond point N and into its "cut-off" region or beyond point M and into its Saturation region thereby resulting in distortion to the output signal in the form of "clipping".

Using points N and M as an example, the instantaneous values of Collector current and corresponding values of Collector-emitter voltage can be projected from the load line. It can be seen that the Collector-emitter voltage is in anti-phase (-180°) with the collector current.

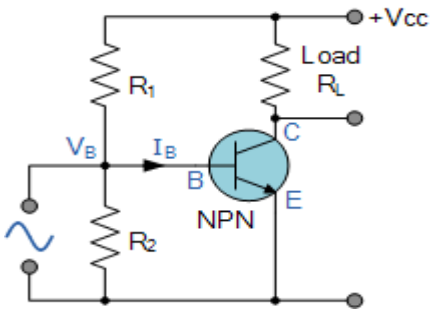
As the Base current Ib changes in a positive direction from 50µA to80µA, the Collector-emitter voltage, which is also the output voltage decreases from its steady state value of 5.8v to 2.0v.

Then a single stage **Common Emitter Amplifier** is also an "Inverting Amplifier" as an increase in Base voltage causes a decrease in Vout and a decrease in Base voltage produces an increase in Vout. In other words the output signal is 180° out-of-phase with the input signal.

Emitter Resistance in a Transistor Amplifier

The aim of an AC signal amplifier circuit is to stabilise the DC biased input voltage to the amplifier and thus only amplify the required AC signal. This stabilisation is achieved by the use of an Emitter Resistance which provides the required amount of automatic biasing needed for a common emitter amplifier.

To explain this a little further, consider the following Basic Amplifier circuit below. Basic Common Emitter Amplifier Circuit



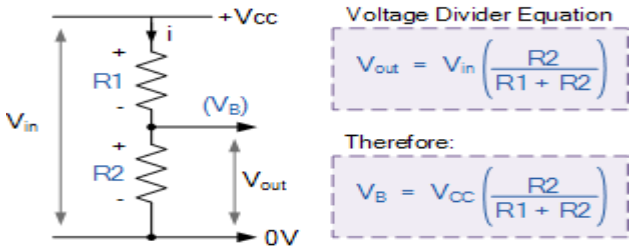
The common emitter amplifier circuit shown uses a voltage divider network to bias the transistors base and the common emitter configuration is a very popular way of designing bipolar transistor amplifier circuits. An important feature of this circuit is that an appreciable amount of current flows into the base of the transistor.

The voltage at the junction of the two biasing resistors, R1and R2, holds the transistors base voltage, V_B at a constant voltage and proportional to the supply voltage, Vcc. Note that V_B is the voltage measured from base to ground, which is the actual voltage drop across R2.

This "class-A" type amplifier circuit is always designed so that the base current (Ib) is less than 10% of the current flowing through the biasing resistor R2. So for example, if we require a quiescent collector current of 1mA, the base current, I_B will be about one hundredth of this, or 10µA. Therefore the current flowing through resistor R2 of the potential divider network must be at least 10 times this amount, or **100µA**.

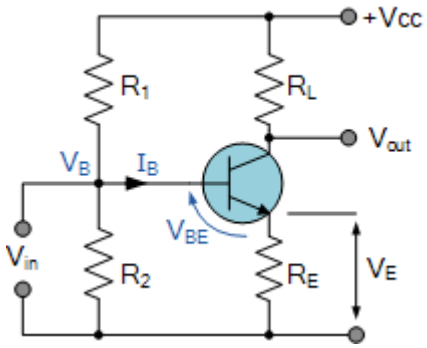
The advantage of using a voltage divider lies in its stability. Since the voltage divider formed by R1and R2 is lightly loaded, the base voltage, Vb can be easily calculated by using the simple voltage divider formula as shown.

Voltage Divider Equation



However, with this type of biasing arrangement the voltage divider network is not loaded by the base current as it is too small, so if there are any changes in the supply voltage Vcc, then the voltage level on the base will also change by a proportional amount. Then some form of voltage stabilisation of the transistors base bias or Q-point is required.

Emitter Resistance Stabilisation



The amplifiers bias voltage can be stabilised by placing a single resistor in the transistors emitter circuit as shown. This resistance is known as the **Emitter Resistance**, R_E. The addition of this *emitter resistor* means that the transistors emitter terminal is no longer grounded or at zero volt potential but sits at a small potential above it given by the Ohms Law equation of: $V_E = I_E \times R_E$. Where: I_E is the actual emitter current.

Now if the supply voltage Vcc increases, the transistors collector current Ic also increases for a given load resistance. If the collector current increases, the corresponding emitter current must also increase causing the voltage drop across R_E to increase, causing an increase in base voltage because $V_B = V_E + V_{BE}$.
Since the base is held constant by the divider resistors R1 and R2, the DC voltage on the base relative to the emitter Vbe is lowered thus reducing the base current and keeping the collector current from increasing. A similar action occurs if the supply voltage and collector current try to decrease.

In other words, the addition of this emitter resistance helps control the transistors base bias using negative feedback, which negates any attempted change in collector current with an opposing change in the base bias voltage and so the circuit tends to be stabilised at a fixed level.

Also, since part of the supply is dropped across R_E, its value should be as small as possible so that the largest possible voltage can be developed across the load resistance, R_L and therefore the output. However, its value cannot be too small or once again the instability of the circuit will suffer.

Then the current flowing through the emitter resistor is calculated as: Emitter Resistor Current

$$I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}$$

As a general rule of thumb, the voltage drop across this emitter resistance is generally taken to be:V_B - V_{BE}, or one-tenth (1/10th) of the value of the supply voltage, Vcc. A common figure for the emitter resistor voltage is between 1 to 2 volts, whichever is the lower. The value of the emitter resistance, R_E can also be found from the gain as now the AC voltage gain is equal to: R_L / R_E

Emitter Resistance Example No1

A common emitter amplifier has the following characteristics, $\beta = 100$, Vcc = 30V and $R_L = 1k\Omega$. If the amplifier circuit uses an emitter resistance to improve its stability, calculate its resistance.

The amplifiers quiescent current, I_{CQ} is given as:

$$I_{CQ} = \frac{½Vcc}{R_L} = \frac{15V}{1k\Omega} = 15mA$$

$$I_B = \frac{I_{CQ}}{\beta} = \frac{15mA}{100} = 150\mu A$$

The voltage drop across the emitter resistance is generally between 1 and 2 volts, so lets assume a voltage drop, V_E of 1.5 volts.

$$V_B = V_E + V_{BE} = 1.5V + 0.7V = 2.2\,Volts$$

$$R_2 = \frac{V_B}{10 \times I_B} = \frac{2.2}{10 \times 150\mu A} = 1.47k\Omega$$

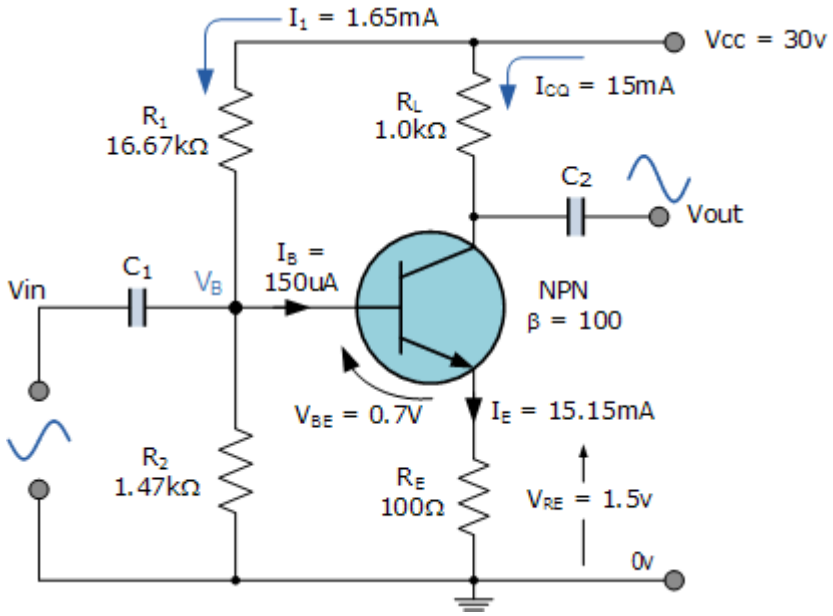
$$R_1 = \frac{Vcc - V_B}{11 \times I_B} = \frac{30 - 2.2}{11 \times 150\mu A} = 16.67k\Omega$$

$$I_E = I_{CQ} + I_B = 15mA + 150\mu A = 15.15mA$$

$$R_E = \frac{V_E}{I_E} = \frac{1.5V}{15.15mA} = 100\Omega$$

Then the value of the **Emitter Resistance** required for the amplifier circuit is given as: 100Ω's, and the final common emitter circuit is given as:

Final Common Emitter Amplifier

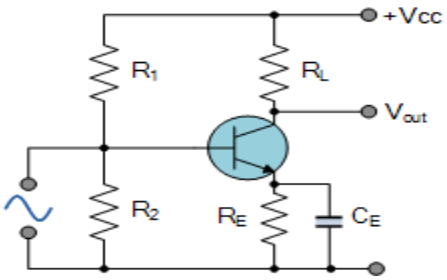


The gain of the amplifier stage can also be found if so required and is given as:

$$\text{Gain, } (A) = \frac{R_L}{R_E} = \frac{1k\Omega}{100\Omega} = 10$$

Emitter By-pass Capacitor

In the basic series feedback circuit above, the emitter resistor, R_E performs two functions: DC negative feedback for stable biasing and AC negative feedback for signal transconductance and voltage gain specification. But as the emitter resistance is a feedback resistor, it will also reduce the amplifiers gain due to fluctuations in the emitter current I_E owing to the AC input signal.



To overcome this problem a capacitor, called an -Emitter Bypass Capacitor|, C_E is connected across the emitter resistance as shown. This bypass capacitor causes the frequency response of the amplifier to break at a designated cut-off frequency, fc, by-passing (hence its name) signal currents to ground.

Being a capacitor it appears as an open circuit for the for DC bias and therefore, the biased currents and voltages are unaffected by the addition of the bypass capacitor. Over the amplifiers operating range of frequencies, the capacitors reactance, X_C will be extremely high at low frequencies producing a negative feedback effect, reducing the amplifiers gain.

The value of this bypass capacitor C_E is generally chosen to provide a capacitive reactance of, at most one-tenth (1/10th) of the value of the emitter resistor R_E at the lowest cut-off frequency point. Then assuming that the lowest signal frequency to be amplified is 100 Hz. The value of the bypass capacitor C_E is calculated as:

Emitter Bypass Capacitor

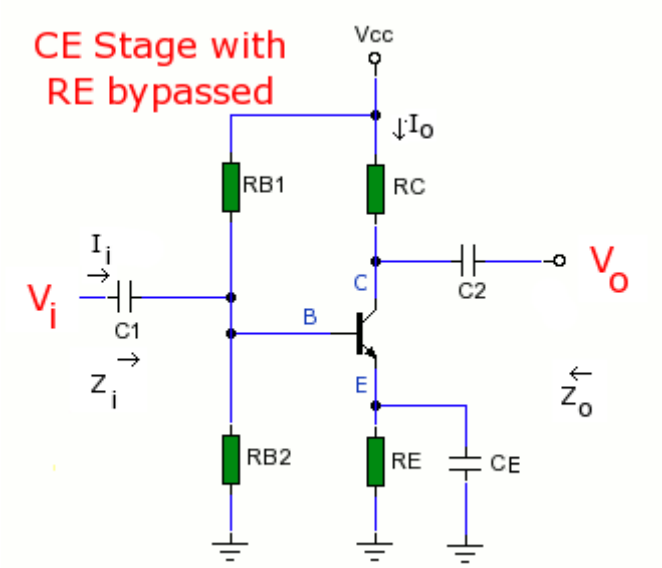
$$X_C = 1/10^{th} R_E \text{ at } f_{3dB} = 0.1 \times 100\Omega = 10\Omega$$

$$C_E = \frac{1}{2\pi f_{3dB} X_C} = \frac{1}{2\pi \times 100 \times 10} = 160\mu F$$

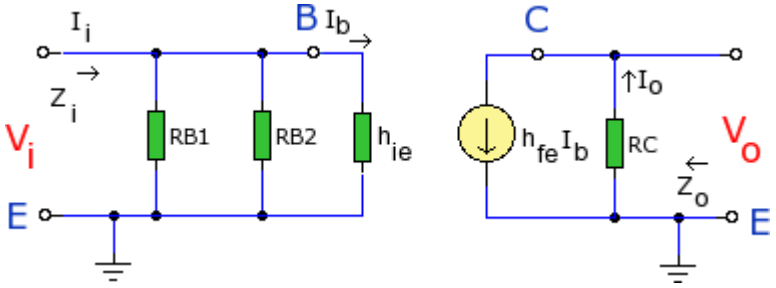
Then for our simple common emitter amplifier above the value of the emitter bypass capacitor connected in parallel with the emitter resistance is: 160uF

Examples

CE Stage with RE Bypassed The h-parameter model will be applied to a single common emitter (CE) stage with the emitter resistor (RE) bypassed. The model will be used to build equations for voltage gain, current gain, input and output impedance. The circuit is shown below:



The small signal parameter $h_{re}V_{ce}$ is often too small to be considered so the input resistance is just h_{ie}. Often the output resistance h_{oe} is often large compared wi the the collector resistor RC and its effects can be ignored. The h- parameter equivalent model is now simplified and drawn below:



Input Impedance Z_i The input impedance is the parallel combination of bias resistors RB1 and RB2. As the power supply is considered short circuit at small signal levels then RB1 and RB2 are in parallel. RBB will represent the parallel combination:

$$R_{BB} = RB1 \parallel RB2 = RB1\ RB2$$

B1 + RB2

As R_{BB} is in parallel with h_{ie} then: Z_i = $R_{BB} \parallel h_{ie}$

Output ImpedanceZ_o As $h_{fe}I_b$ is an ideal current generator with infinite output impedance, then output impedance looking into the circuit is:

$Z_o = RC$

Voltage GainA_v Note the − sign in the equation, this indicates phase inversion of the output waveform.

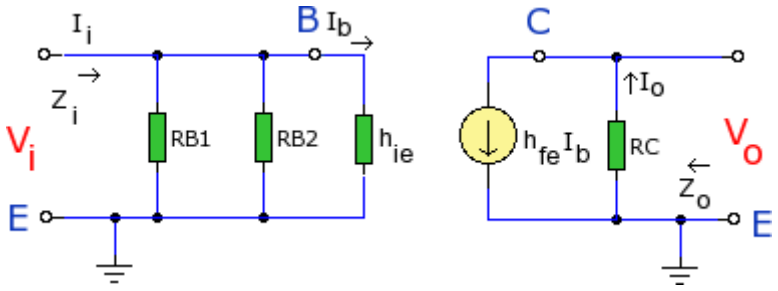
$V_o = -I_o\ RC = -h_{fe}\ I_b\ RC$ as $I_b = V_i / h_{ie}$ then:= $-h_{fe}$ h_{fe}

$$V_i$$
$$RC$$
$$h_{ie}$$

$$= -RC\ V_i$$
$$h_{ie}$$

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fe}\ RC}{h_{ie}}$$

Current GainA_i The current gain is the ratio Io / Ii. At the input the current is split between the parallel branch R_{BB} and h_{ie}. So looking at the equivalent h-parameter model again (shown below):



The current divider rule can be used for I_b:

$$I_b = \frac{R_{BB}\ I_i}{R_{BB} + h_{ie}}$$

$$I_b = R_{BB}$$

$I_i \qquad R_{BB} + h_{ie}$

At the output side, $I_o = h_{fe}\, I_b$ re-

arranging $I_o / I_b = h_{fe}$

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b}\cdot\frac{I_b}{I_i} = \frac{R_{BB}}{R_{BB} + h_{ie}} = h_{fe}$$

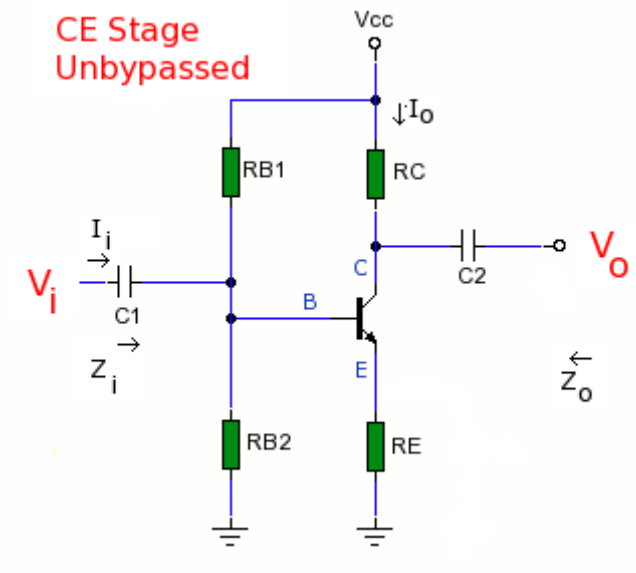
$$A_i = \frac{R_{BB}\, h_{fe}}{R_{BB} + h_{ie}}$$

If RBB >> hie then,

$$A_i \approx \frac{R_{BB}\, h_{fe}}{R_{BB}} = h_{fe}$$

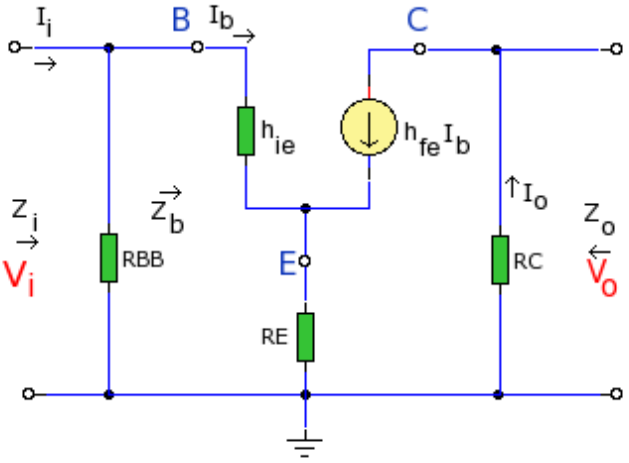
CE Stage with RE Unbypassed

The h-parameter model of a common emitter stage with the emitter resistor unbypassed is now shown. The model will be used to build equations for voltage gain, current gain, input and output impedance. The circuit is shown below:



As in the previous example, RB1 and RB2 are in parallel, the bias resistors are replaced by resistance R_{BB}, but as RE is now unbypassed this resistor appears in series with the emitter terminal. The hybrid small signal model is shown below, once again effects of small signal parameters $h_{re} V_{ce}$ and h_{oe} have been omitted.

CE Stage RE Unbypassed



Input Impedance Z_i

The input impedance Z_i is the bias resistors R_{BB} in parallel with the impedance of the base, Z_b. $Z_b = h_{ie} + (1 + h_{fe})\, RE$

Since hfe is normally much larger than 1, the equation can be reduced to: $Z_b = h_{ie} + h_{fe}\, RE$

$Z_i = R_{BB} \,||\, (h_{ie} + h_{fe}\, RE)$

Output Impedance Z_o With Vi set to zero, then Ib = 0 and $h_{fe} I_b$ can be replaced by an open-circuit. The output impedance is: $Z_o = RC$

Voltage Gain A_v Note the−sign in the equation, this indicates phase inversion of the output waveform.

$$I_b = \frac{V_i}{Z_b}$$

$V_o = -I_o\, RC = -h_{fe}\, I_b\, RC$

$$\frac{V_i}{} = -h_{fe} \quad RC\ Z_b$$

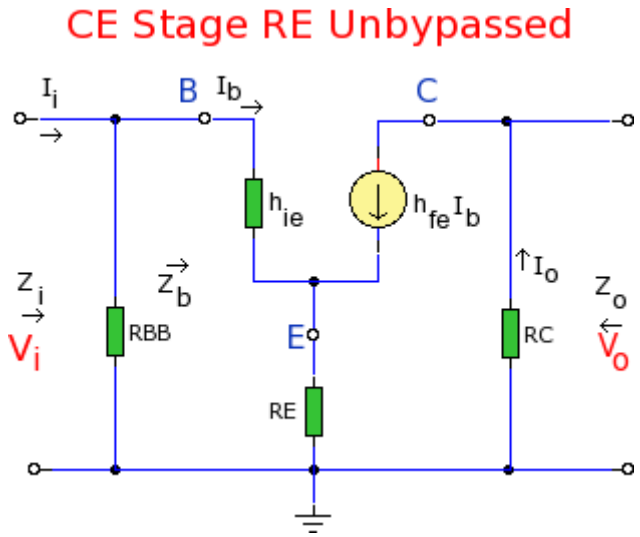
$$A_v = \frac{V_o}{} = \frac{-h_{fe}\, RC}{}$$

V_i Z_bAs $Z_b = h_{ie} + h_{fe}$ RE often the product h_{fe}RE is much larger than hie, so Z_b can reduced to the approximation: $Z_b \approx h_{fe}$RE

$$\therefore A_v = \frac{-h_{fe}RC\ h_{fe}RE}{V_i}$$

$$A_v = \frac{V_o}{V_i} = -\frac{RC}{RE}$$

Current Gain A_i The current gain is the ratio Io / Ii. At the input the current is split between the parallel branch R_{BB} and Z_b. So looking at the equivalent h-parameter model again (shown below):



The current divider rule can be used for I_b:

$$I_b = I_b \frac{R_{BB}}{I_i} = \frac{I_i R_{BB} + Z_b R_{BB}}{R_{BB} + Z_b}$$

At the output side, $I_o = h_{fe} I_b$ re-

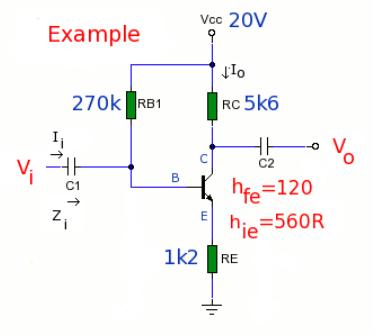
arranging $I_o / I_b = h_{fe}$

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b} \frac{I_b}{I_i} = h_{fe} \frac{R_{BB}}{R_{BB} + Z_b}$$

$$A_i = R_{BB} h_{fe}$$

$R_{BB} + Z_b$

E Stage



The hybrid parameters must be known to use the hybrid model, either from the datasheet or measured. In the above circuit, Zi, Zo, Av, and Ai will now be calculated. Note that this CE stage uses a single bias resistor RB1 which is the value RBB.

Z_i

$Z_b = h_{ie} + (1 + h_{fe})\ RE$

$= 0.56k + (1 + 120)\ 1.2k = 145.76k$

$Z_i = RB \parallel Z_b$

$Z_i = 270k \parallel 145.76k = 94.66k$

Z_o

$Z_o \approx 5.6k\ A_v$

$$A_v = - \frac{h_{fe}\ RC\ Z_b}{}$$

$A_v = -\ 4.61$

$$A_i$$

$$= - \frac{120 \times 5.6k}{145.76k}$$

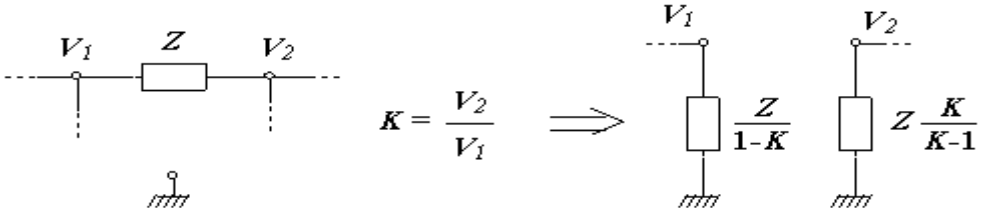
$$R_{BB}\ h_{fe}\ A_i = \frac{}{R_{BB} + Z_b}$$

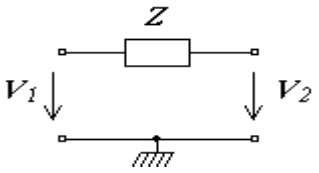
$A_i =$

77.93

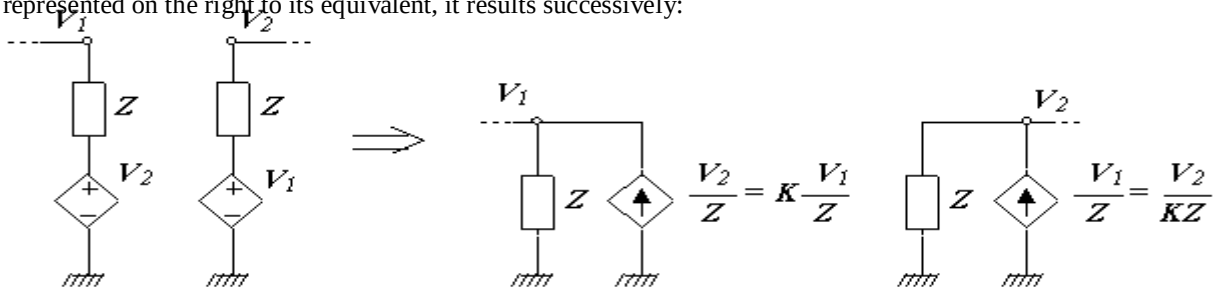
Miller's theorem

The Miller‘s theorem establishes that in a linear circuit, if there exists a branch with impedance *Z*, connecting two nodes with nodal voltages $V_1$and V_2, we can replace this branch by two branches connecting the corresponding nodes to ground by impedances respectively $Z / (1-K)$ and $KZ / (K-1)$, where $K = V_2 / V_1$.

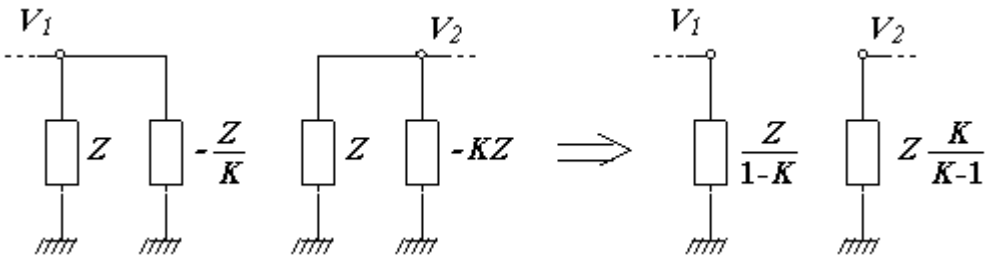




In fact, if we use the equivalent two-port network technique to replace the two-port represented on the right to its equivalent, it results successively:



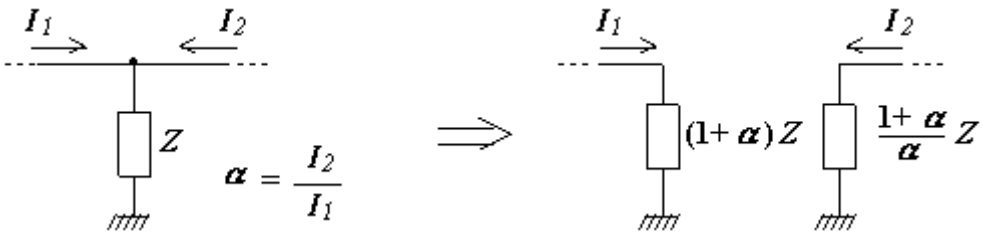
and, according to the source absorption theorem, we get the following:



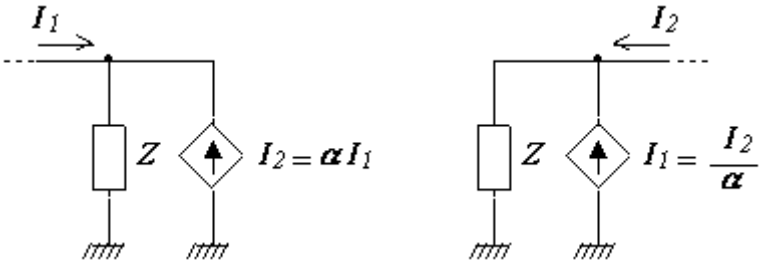
As all the linear circuit theorems, the Miller‘s theorem also has a dual form:

Miller's dual theorem

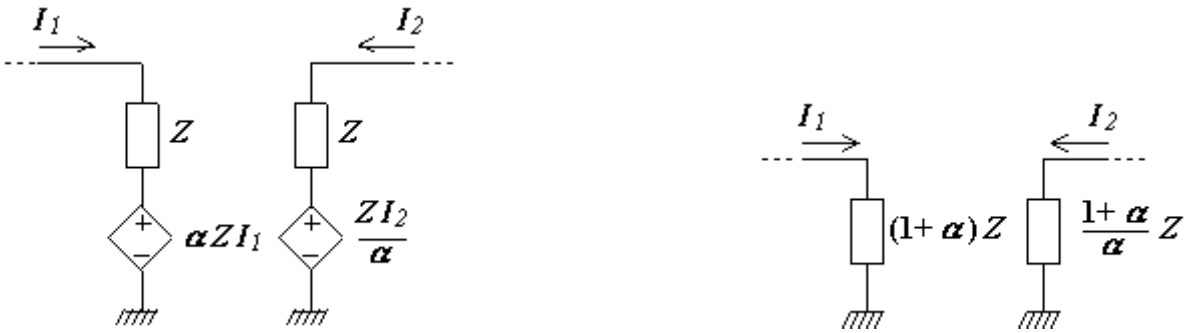
If there is a branch in a circuit with impedance *Z* connecting a node, where two currents I_1 and I_2converge, to ground, we can replace this branch by two conducting the referred currents, with impedances respectively equal to (1+ □)*Z* and (1+
)*Z* / □ □ , where□ I_2 / I_1.



In fact, replacing the two-port network by its equivalent, as in the figure,



it results the circuit on the left in the next figure and then, applying the source absorption theorem, the circuit on the right.

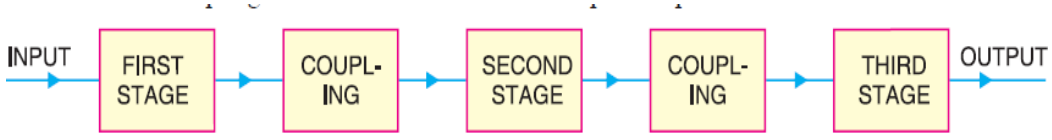


Multistage Transistor Amplifiers

T he output from a single stage amplifier is usually insufficient to drive an output device.
Inther words, the gain of a single amplifier is inadequate for practical purposes. Consequently, additional amplification over two or three stages is necessary. To achieve this, the output of each amplifier stage is *coupled* in some way to the input of the next stage. The resulting
system is referred to as multistage amplifier. It may be emphasised here that a practical amplifier is always a multistage amplifier. For example, in a transistor radio receiver, the number of amplification stages may be six or more. In this chapter, we shall focus our attention on the various multistage transistor amplifiers and their practical applications.

11.1 Multistage Transistor Amplifier

A transistor circuit containing more than one stage of amplification is known as **multistage transistor amplifier.**
In a multistage amplifier, a number of single amplifiers are connected in **cascade arrangement*
i.e. output of first stage is connected to the input of the second stage through a suitable *coupling device* and so on. The purpose of coupling device (*e.g.* a capacitor, transformer etc.) is (*i*) to transfer
a.c. output of one stage to the input of the next stage and (*ii*) to isolate the d.c. conditions of one stage from the next stage.
Fig. 11.1 shows the block diagram of a 3-stage amplifier. Each stage consists of
one transistor and associated circuitry and is coupled to the next stage through a coupling device. The name of the amplifier is usually given after the type of coupling used. *e.g.*



Hence, it almost remains constant.

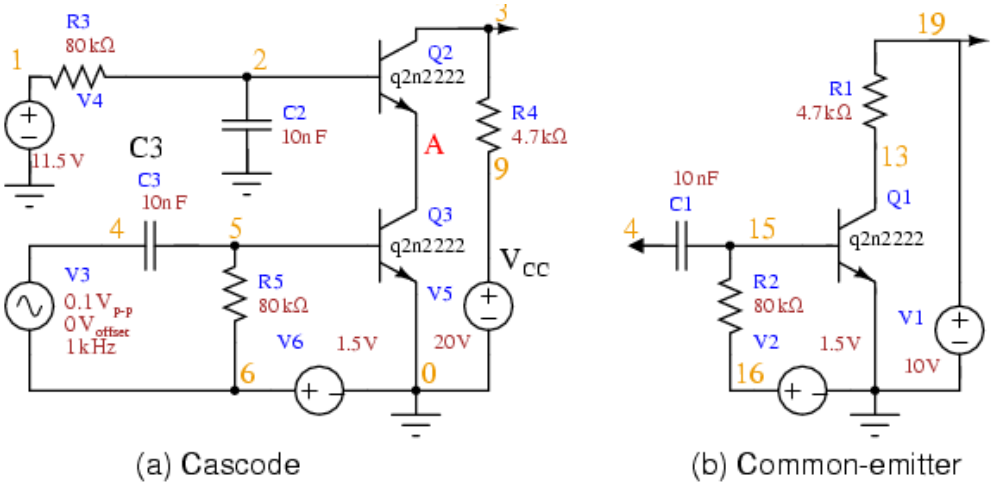
The cascode amplifier is combined common-emitter and common-base. This is an AC circuit equivalent with batteries and capacitors replaced by short circuits.

The key to understanding the wide bandwidth of the cascode configuration is the *Miller effect*. The Miller effect is the multiplication of the bandwidth robbing collector-base capacitance by voltage gain A_v. This C-B capacitance is smaller than the E-B capacitance. Thus, one would think that the C-B capacitance would have little effect. However, in the C-E configuration, the collector output signal is out of phase with the input at the base. The collector signal capacitively coupled back opposes the base signal. Moreover, the collector feedback is $(1-A_v)$ times larger than the base signal. Keep in mind that A_v is a negative number for the inverting C-E amplifier. Thus, the small C-B capacitance appears $(1+A|_v|)$ times larger than its actual value. This capacitive gain reducing feedback increases with frequency, reducing the high frequency response of a C-E amplifier.

The approximate voltage gain of the C-E amplifier in Figure below is $-R_L/r_{EE}$. The emitter current is set to 1.0 mA by biasing. $R_{EE}= 26mV/I_E = 26mV/1.0ma = 26\ \Omega$. Thus, $A_v = -R_L/R_{EE} = -4700/26 = -181$. The pn2222 datasheet list $C_{cbo} = 8$ pF.[FAR] The miller capacitance is $C_{cbo}(1-A_v)$. Gain $A_v = -181$, negative since it is inverting gain. $C_{miller} = C_{cbo}(1-A_v) = 8pF(1-(-181)=1456pF$

A common-base configuration is not subject to the Miller effect because the grounded base shields the collector signal from being fed back to the emitter input. Thus, a C-B amplifier has better high frequency response. To have a moderately high input impedance, the C-E stage is still desirable. The key is to reduce the gain (to about 1) of the C- E stage which reduces the Miller effect C-B feedback to $1\cdot C_{CBO}$. The total C-B feedback is the feedback capacitance $1\cdot C_{CB}$ plus the actual capacitance C_{CB} for a total of $2\cdot C_{CBO}$. This is a considerable reduction from $181\cdot C_{CBO}$. The miller capacitance for a gain of -2 C-E stage is $C_{miller} = C_{cbo}(1-A_v)= C_{miller} = C_{cbo}(1-(-1)) = C_{cbo}\cdot 2$.

The way to reduce the common-emitter gain is to reduce the load resistance. The gain of a C-E amplifier is approximately R_C/R_E. The internal emitter resistance r_{EE} at 1mA emitter current is 26Ω. For details on the 26Ω, see -Derivation of R_{EE}|, see REE. The collector load R_C is the resistance of the emitter of the C-B stage loading the C-E stage, 26Ω again. CE gain amplifier gain is approximately $A_v = R_C/R_E=26/26=1$. This Miller capacitance is $C_{miller} = C_{cbo}(1-A_v) = 8pF(1-(-1)=16pF$. We now have a moderately high input impedance C-E stage without suffering the Miller effect, but no C-E dB voltage gain. The C-B stage provides a high voltage gain, $A_V = -181$. Current gain of cascode is β of the C-E stage, 1 for the C-B, β overall. Thus, the cascode has moderately high input impedance of the C-E, good gain, and good bandwidth of the C-B.



SPICE: Cascode and common-emitter for comparison.

The SPICE version of both a cascode amplifier, and for comparison, a common-emitter amplifier is shown in Figure above. The netlist is in Table below. The AC source V3 drives both amplifiers via node 4. The bias resistors for this circuit are calculated in an example problem cascode.

Frequency response of RC coupled amplifier: The frequency response of a typical RC coupled amplifiers is shown in the fig. It is clear from the graph that the voltage gain drops off at low frequencies and high frequencies.
While it remains constant in the mid frequency range. This behavior of the amplifier is explained as follows;
At low frequencies: The coupling capacitors CC offer a high reactance. Hence it will allow only a part of the signal to pass from one stage to the next stage. In addition to this, the emitter bypass capacitor CE cannot shunt the emitter resistor RE effectively, because of its large reactance at low frequencies. Due to these reasons, the gain of the amplifier drops at low frequencies.
At high frequencies: The coupling capacitor CC offers a low reactance and it acts as a short circuit. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. Moreover, at high frequencies, capacitive reactance of base emitter junction is low which increases the base current. This in turn reduces the current amplification factor β. As a result of these two factors, gain drops at high frequencies.
At mid frequency: In the mid frequency range, the effect of coupling capacitor is such that it maintains a constant gain. Thus, as the frequency increases, the reactance of capacitor CC decreases, which tends to increase the gain. However, at the same time, lower capacitive reactance increases the loading effect of first stage to which the gain reduces. These two factors cancel each other. Thus the constant gain is maintained.
Advantages of RC coupled amplifiers:
it requires components like resistors and capacitors. Hence, it is small, light and inexpensive. **Amax** 2max*A* **f1 f2 f (Hz) Band Width Gain 3dB LF HFMF** Transistor Amplifiers Page 19 of 23
It has a wide frequency response. The gain is constant over audio frequency range which is the region of most importance for speech and music.
It provides less frequency distortion.
Its overall amplification is higher than that of other coupling combinations.
Disadvantages of RC coupled amplifiers:
The overall gain of the amplifier is comparatively small because of the loading effect.
RC coupled amplifiers have tendency to become noisy with age, especially in moist climate.
The impedance matching is poor as the output impedance is several hundred ohms, where as that of a speaker is only few ohms. Hence, small amount of power will be transferred to the speaker.
Applications:
RC coupled amplifiers have excellent audio frequency fidelity over a wide range of frequency i.e, they are widely used as voltage amplifiers. This property makes it very useful in the initial stages of public address system. However, it may be noted that a coupled amplifier cannot be used as a final stage of the amplifier because of its poor impedance matching.

Direct coupled amplifier :

The circuit diagram of direct coupling using two identical transistors is shown in the fig. In this method, the ac output signal is fed directly to the next stage. This type of coupling is used where low frequency signals are to be amplified. The coupling devices such as capacitors, inductors and transformers cannot be used at low frequencies because there size becomes very large. The amplifiers using this coupling are called direct coupled amplifiers or dc amplifiers.

Advantages Fig . Two stage Direct coupled amplifier R1 RC *v*s is iB ic +VCCR1RC*v*o2 ic *v*o1

The circuit arrangement is simple because of minimum number of components.

The circuit can amplify even very low frequency signals as well as direct current signals. No bypass and coupling capacitors are required.

Disadvantages

1. It cannot be used for amplifying high frequencies.
2. The operating point is shifted due to temperature variations.

Applications : Direct coupled amplifiers find applications in regulator circuits of electronic power supplies, differential amplifiers,pulseamplifiers,electronic instrument.

INTRODUCTION

Feedback Amplifiers

A practical amplifier has a gain of nearly one million *i.e.* its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output. There is a strong tendency in amplifiers to introduce *hum* due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output. The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level in amplifiers can be reduced considerably by the use of *negative feedback i.e.* by injecting a fraction of output in phase opposition to the input signal. The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

Ideally an amplifier should reproduce the input signal, with change in magnitude and with or without change in phase. But some of the short comings of the amplifier circuit are

I. Change in the value of the gain due to variation in supplying voltage, temperature or due to components.

2. Distortion in wave-form due to non linearities in the operating characters of the Amplifying device.

3. The amplifier may introduce noise (undesired signals)

The above drawbacks can be minimizing if we introduce feedback CLASSIFICATION OF

AMPLIFIERS

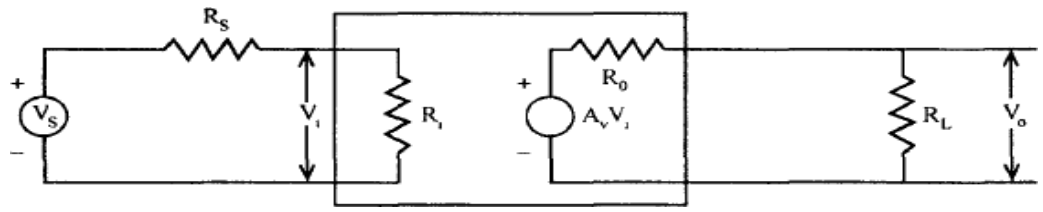
Amplifiers can be classified broadly as,

I. Voltage amplifiers.
2. Current amplifiers.
3. Transconductance amplifiers.
4. Transresistance amplifiers.

This classification is with respect to the input and output impedances relative to the load and source impedances.

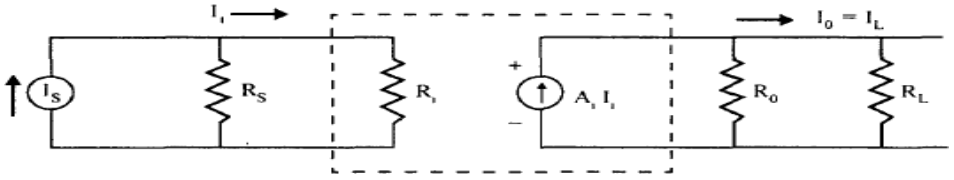
VOLTAGE AMPLIFIER

This circuit is a 2-port network and it represents an amplifier (see in Fig 7.1). Suppose R,» Rs, drop across Rs is very small.



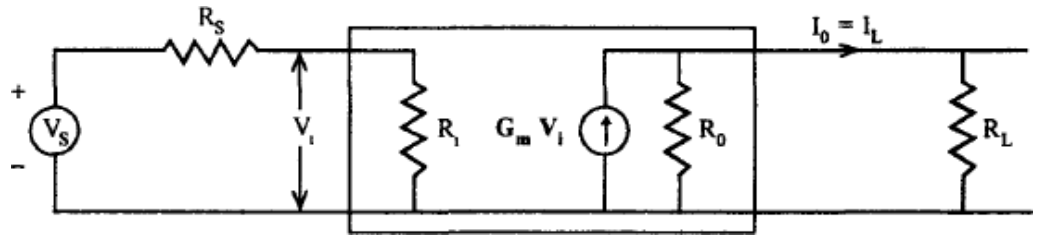
CURRENT AMPLIFIER

An ideal current amplifier is one which gives output current proportional to input current and the proportionality factor is independent ofRs and RL.



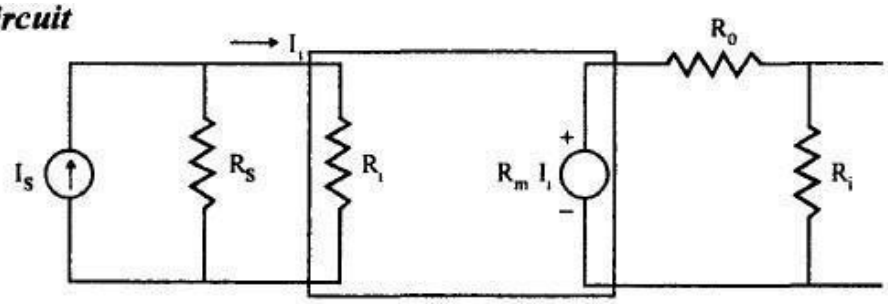
TRANSCONDUCTANCE AMPLIFIER

Ideal Transconductance amplifier supplies output current which is proportional to input voitage independently ofthe magnitude ofRs and RL.



TRANS RESISTANCE AMPLIFIER
It gives output voltage Vo proportional to Is, independent of Rs a. RL. For *ideal amplifiers* Rj =0, Ro=O

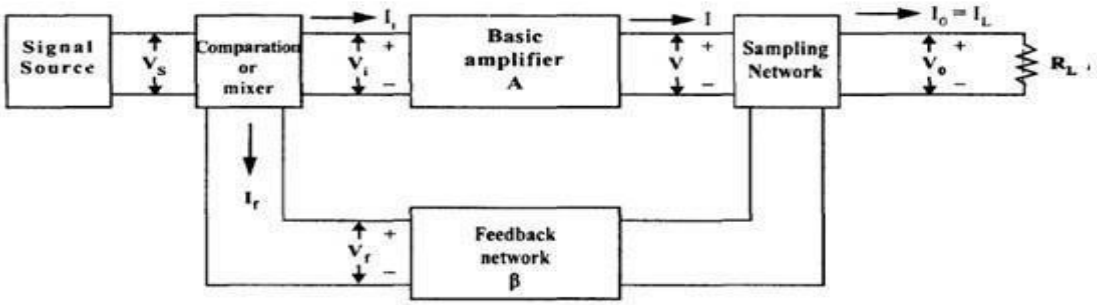
Equivalent circuit



Concepts of feedback

The process of injecting a fraction of output energy of some device back to the input is known as **feedback**. The principle of feedback is probably as old as the invention of first machine but it is only some 50 years ago that feedback has come into use in connection with electronic circuits. It has been found very useful in reducing noise in amplifiers and making amplifier operation stable. Depending upon whether the feedback energy aids or opposes the input signal, there are two basic types of feedback in amplifiers *viz positive feedback* and *negative feedback*.

GENERALIZED BLOCK SCHEMATIC



Signal Source
It can be a voltage source V s or a current source Is FEEDBACK NETWORK
It is a passive two port network. It may contain resistors, capacitors or inductors. But usually a resistance is used as the feedback element. Here the output current is sampled and feedback. The feedback network is connected in series with the output. This is called as *Current Sampling or* Loop Sampling.

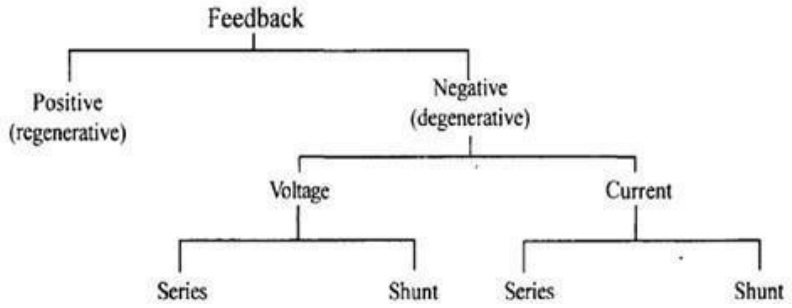
A voltage feedback is distinguished in this way from current feedback. For voltage feedback,

the feedback element (resistor) will be in parallel with the output. For current feedback the element will be in series.

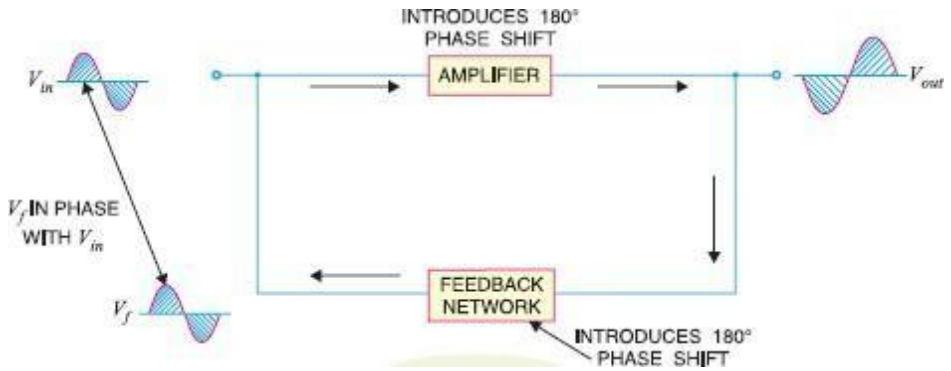
COMPARATOR OR MIXER NETWORK

This is usually a differential amplifier. It has two inputs and gives a single output which is the difference of the two inputs.

basic types of feedback in amplifiers



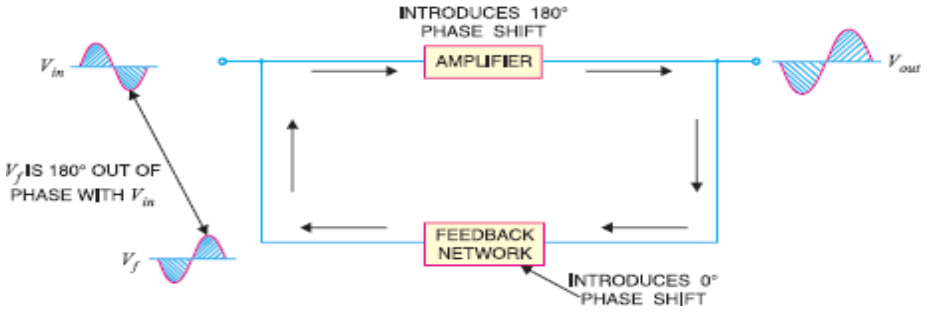
(i) Positive feedback. When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called *positive feedback*. This is illustrated in Fig.. Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the *feedback voltage Vf* to be in phase with the input signal *Vin*.



The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is seldom employed in amplifiers. One important use of positive feedback is in oscillators. As we shall see in the next chapter, if positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

(ii) Negative feedback. When the feedback energy (voltage or current) is out of phase with the

input signal and thus opposes it, it is called *negative feedback*. This is illustrated in Fig.. As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (*i.e.*, 0° phase shift). The result is that the *feedback voltage Vf* is 180° out of phase with the input signal *Vin*.



General characteristics of negative feedback amplifiers

Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances. It is due to these advantages that negative feedback is frequently employed in amplifiers.

Advantages of Negative Voltage Feedback

The following are the advantages of negative voltage feedback in amplifiers :

(i) Gain stability. An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product *Av mv* much greater than unity. Therefore, in the above relation, 1 can be neglected as compared to *Av mv* and the expression becomes : It may be seen that the gain now depends only

$$A_{vf} = \frac{A_v}{A_v\, m_v} = \frac{1}{m_v}$$

upon feedback fraction *mv i.e.*, on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

(ii) Reduces non-linear distortion. A large signal stage has non-linear distortion because its voltage gain changes at various points in the cycle. The negative voltage feedback reduces the nonlinear distortion in large signal amplifiers. It can be proved mathematically that :

$$D_{vf} = \frac{D}{1 + A_v\, m_v}$$

where *D* = distortion in amplifier without feedback
Dvf = distortion in amplifier with negative feedback
It is clear that by applying negative voltage feedback to an amplifier, distortion is reduced by a factor 1 + *Av mv*.

(iii) Improves frequency response. As feedback is usually obtained through a resistive network, therefore, voltage gain of the amplifier is *independent of signal frequency. The result is that voltage gain of the amplifier will be substantially constant over a wide range of signal frequency. The negative voltage feedback, therefore, improves the frequency response of the amplifier.

(iv) Increases circuit stability. The output of an ordinary amplifier is easily changed due to variations in ambient temperature, frequency and signal amplitude. This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilized or accurately fixed in value. This can be easily explained. Suppose the output of a negative voltage feedback amplifier has increased because of temperature change or due

to some other reason. This means more negative feedback since feedback is being given from the output. This tends to oppose the increase in amplification and maintains it stable. The same is true should the output voltage decrease. Consequently, the circuit stability is considerably increased.

(v) Increases input impedance and decreases output impedance. The negative voltage feedback increases the input impedance and decreases the output impedance of amplifier. Such a change is profitable in practice as the amplifier can then serve the purpose of impedance matching.

(a) Input impedance. The increase in input impedance with negative voltage feedback can be explained by referring to Fig.. Suppose the input impedance of the amplifier is *Zin* without feedback and *Z 'in* with negative feedback. Let us further assume that input current is *i*1.

$$Z'_{in} = Z_{in}(1 + A_v m_v)$$

(b) Output impedance. Following similar line, we can show that output impedance with negative voltage feedback is given by :

$$Z'_{out} = \frac{Z_{out}}{1 + A_v\ m_v}$$

It is clear that by applying negative feedback, the output impedance of the amplifier is decreased by a factor 1 + *A*v *m*v. This is an added benefit of using negative voltage feedback. With lower value of output impedance, the amplifier is much better suited to drive low impedance loads.

Effect of feedback on amplifier characteristics

CLASSIFACTION OF FEEDBACK AMPLIFIERS

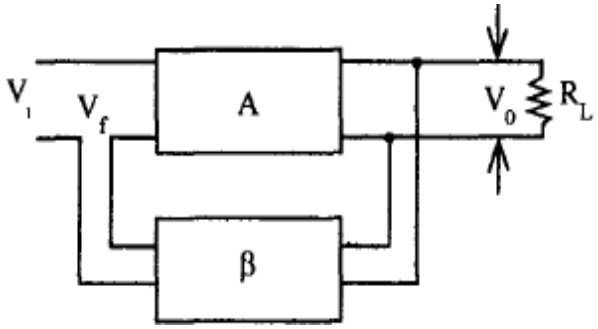
There are four types of feedback,

1. Voltage series feedback.
2. Voltage shunt feedback.
3. Current shunt feedback.
4. Current series feedback.

If the feedback signal is taken across RL, it is a Vo or so it is *Voltage feedback.*
If the feedback signal is taken in series with the output terminals, feedback signal is proportional to I0 , So it is *current feedback.*
If the feedback signal is in series with the input, it is *seriesfeedback.*
If the feedback signal is in shunt with the input, it is *shuntfeedback.*

Voltage Series Configuration

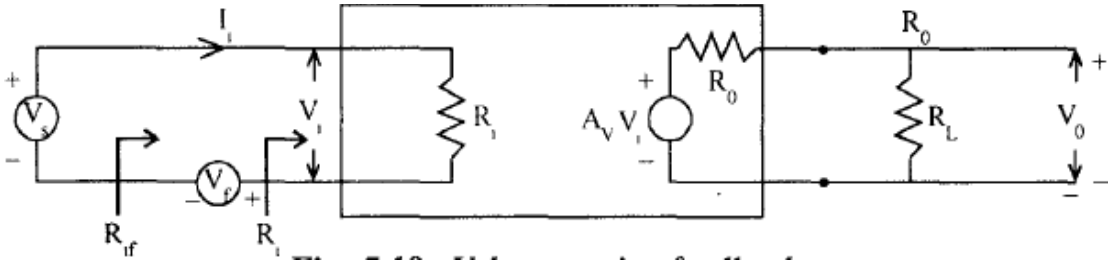
Feedback signal is taken across RL.proportional to Vo. So it is voltage feedback. Vf is coming in series with VI So it is Voltage series feedback.



Voltage series feedback.

EXPRESSION FOR INPUT RESISTANCE R_I WITH VOLTAGE SERIES FEEDBACK

In this circuit Av represents the open circuit voltage gain taking Rs into account



Voltage series feedback

$$A_V = \frac{V_o}{V_i} = \frac{A_v R_L}{R_o + R_L}$$

$$V_S = I_i R_i + \beta \cdot V_0$$

$$\boxed{\frac{V_s}{I_i} = R_i + \frac{\beta . V_o}{I_i} = R_i \left(1 + \frac{\beta . V_o}{I_i \times R_i}\right)}$$

$$R_{if} = R_i \left(1 + \beta . \frac{V_o}{V_i}\right) = R_i (1 + \beta . A_V)$$

A_V = voltage gain, without feedback.

EXPRESSION FOR OUTPUT RESISTANCE R_o WITH VOLTAGE SERIES FEEDBACK

$$V_i = V_S - V_f$$

$$V_s = V_i + V_f$$

$$R_0' = R_{if} = V_S / I_i .$$

$$V_f = I_i R_i + V_f = I_i R_i + \beta V_0$$

$$V_0 = \frac{A_v V_i R_L}{R_o + R_L} = (A_V I_i R_i)$$

$$\frac{A_v . R_L}{R_o + R_L} = A_V, \; V_i = I_i . R_i .$$

R_O is determined by impressing voltage 'V' at the output terminals or messing 'I', with input R_{of} terminals.-shorted.

$$I = \frac{V_0 - A_V V_i}{R_0} = \frac{V_0 + \beta A_v V}{R_o}$$

$\because$ V_0 = output voltage.

$V_i = -\beta_V$

Because with $V_S = 0. \; V_i = -V_f = -\beta_V$

Hence, $R_{of} = \frac{V_0}{I} = \frac{R_o}{1 + \beta A_v}$

This expression is excluding R_L. If we consider R_L also R_{of} is in parallel with R_L.

$$R_{of}' = \frac{R_{of} . R_L}{R_{of} + R_L}$$ Substitute the1 value of R_{of}

$$R_{of}' = \frac{\frac{R_o}{1 + \beta A_V} \times R_L}{\frac{R_0}{1 + \beta A_V} + R_L} = \frac{R_o R_L}{R_o + R_L + \beta . A_v R_L}$$

Disconnect R_{oL} To find R_{of}' remove external signal (set Vs = 0, or Is = 0) Let $R_L = \infty$
Impress a voltage V across the output terminals and calculate the current I delivered by V.

Then, R_{Of} = V/I.

Oscillators

Condition Classification of oscillators for oscillations

RC Phase shift Oscillators

Generalized analysis of LC Oscillators- Hartley Oscillators

Colpitts Oscillators,

Wien Bridge Oscillators

Crystal Oscillators,

Stability of Oscillators

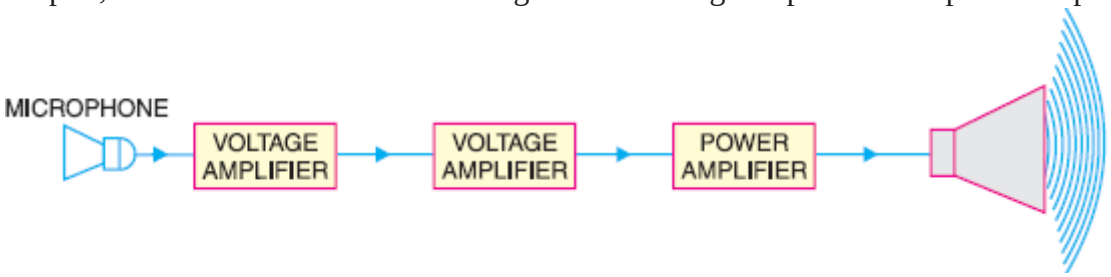
UNIT – IV

LARGE SIGNAL AMPLIFIERS

INTRODUCTION

A practical amplifier always consists of a number of stages that amplify a weak signal until sufficient power is available to operate a loudspeaker or other output device. The first few stages in this multistage amplifier have the function of only voltage amplification. However, the last stage is designed to provide maximum power. This final stage is known as *power stage*.

The term audio means the range of frequencies which our ears can hear. The range of human hearing extends from 20 Hz to 20 kHz. Therefore, audio amplifiers amplify electrical signals that have a frequency range corresponding to the range of human hearing *i.e.* 20 Hz to 20 kHz. Fig. 12.1 shows the block diagram of an audio amplifier. The early stages build up the voltage level of the signal while the last stage builds up power to a level sufficient to operate the loudspeaker. In this chapter, we shall talk about the final stage in a multistage amplifier—the power amplifier.



Transistor Audio Power Amplifier

A transistor amplifier which raises the power level of the signals that have audio frequency range is known as **transistor audio power amplifier.** In general, the last stage of a multistage amplifier is the *power stage*. The power amplifier differs from all the previous stages in that here a concentrated effort is made to obtain maximum output power. A transistor that is suitable for power amplification is generally called a *power transistor*. It differs from other transistors mostly in size ; it is considerably larger to provide for handling the great amount of power.

Audio power amplifiers are used to deliver a large amount of power to a low resistance load. Typical load values range from 300Ω (for transmission antennas) to 8Ω (for loudspeakers). Although these load values do not cover every possibility, they do illustrate the fact that audio power amplifiers usually drive low-resistance loads. The typical power output rating of a power amplifier is 1W or more.

Small-Signal and Large-Signal Amplifiers: **The input signal to a multistage amplifier is generally small (a few mV from a cassette or CD or a few μV from an antenna). Therefore, the first few stages of a multistage amplifier handle small signals and have the function of only voltage amplification. However, the last stage handles a large signal and its job is to produce a large amount of power in order to operate the output device (*e.g.* speaker).**

(i) Small-signal amplifiers. Those amplifiers which handle small input a.c. signals (a few μV or a few mV) are called *small-signal amplifiers.* Voltage amplifiers generally fall in this class.

The small-signal amplifiers are designed to operate over the linear portion of the output characteristics. Therefore, the transistor parameters such as current gain, input impedance, output impedance etc. do not change as the amplitude of the signal changes. Such amplifiers amplify the signal with little or no distortion.

(ii) Large-signal amplifiers. Those amplifiers which handle large input a.c. signals (a few volts)

are called *large-signal amplifiers.* Power amplifiers fall in this class. The large-signal amplifiers are designed to provide a large amount of a.c. power output so that they can operate the output device *e.g.* a speaker. The main features of a large-signal amplifier or power amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling and the impedance matching to the output device. It may be noted that all large-signal amplifiers are not necessarily power amplifiers but it is safe to say that most are. In general, where amount of power involved is 1W or more, the amplifier is termed as *power amplifier.*

Output Power of Amplifier

An amplifier converts d.c. power drawn from d.c. supply *VCC* into a.c. output power. The output power is always less than the input power because losses occur in the various resistors present in the circuit. For example, consider the R-C coupled amplifier circuit shown in Fig. 12.2. The currents are flowing through various resistors causing *I*2*R* loss. Thus power loss in *R*1 is *I*1
2 *R*1, power loss in *RC* is *IC* 2 *RC*, power loss in *RE* is *IE* 2 *RE* and so on. All these losses appear as heat. Therefore, losses occurring in an amplifier not only decrease the efficiency but they also increase the temperature of the circuit.

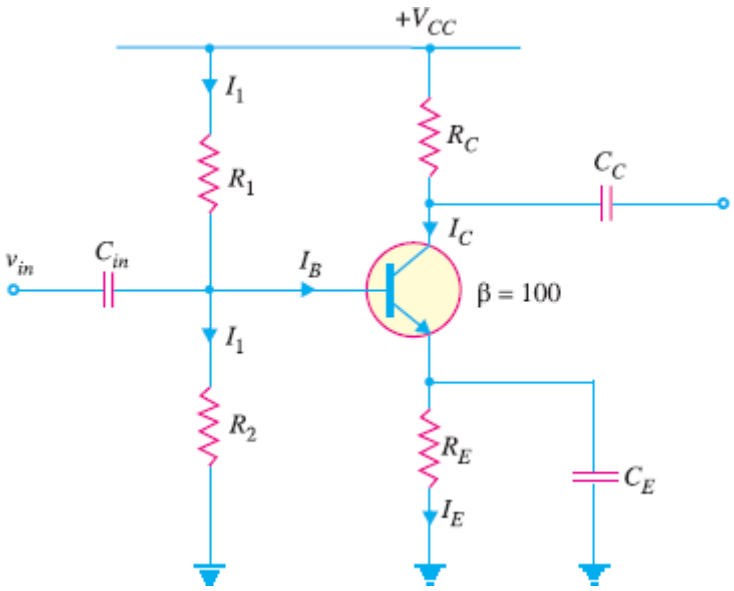


Fig. 4.2

When load *RL* is connected to the amplifier, A.C. output power,

$$P_o = \frac{V_L^2}{R_L}$$

Example 4.1. If in Fig. 4.2; R1 = 10 k ; R2 = 2.2 k ; RC = 3.6 k ; RE = 1.1. k and VCC = + 10 V, find the d.c. power drawn from the supply by the amplifier.

Solution. The current *I*1 flowing through *R*1 also flows through *R*2 (a reasonable assumption because *IB* is small).

$$I_1 = \frac{V_{CC}}{R_1 + R_2} = \frac{10\text{V}}{10\ \text{k}\Omega + 2.2\ \text{k}\Omega} = \frac{10\text{V}}{12.2\ \text{k}\Omega} = 0.82\ \text{mA}$$

D.C. voltage across R_2, $V_2 = I_1 R_2 = 0.82\ \text{mA} \times 2.2\ \text{k}\Omega = 1.8\text{V}$

D.C. voltage across R_E, $V_E = V_2 - V_{BE} = 1.8\text{V} - 0.7\text{V} = 1.1\text{V}$

D.C. emitter current, $I_E = V_E/R_E = 1.1\text{V}/1.1\ \text{k}\Omega = 1\ \text{mA}$

$\therefore \quad I_C \simeq I_E = 1\ \text{mA}$

Total d.c current I_T drawn from the supply is

$$I_T = I_C + I_1 = 1\ \text{mA} + 0.82\ \text{mA} = 1.82\ \text{mA}$$

$\therefore$ D.C. power drawn from the supply is

$$P_{dc} = V_{CC} I_T = 10\text{V} \times 1.82\ \text{mA} = \mathbf{18.2\ mW}$$

Example 4.2. Determine the a.c. load power for the circuit shown in Fig. 4.3.

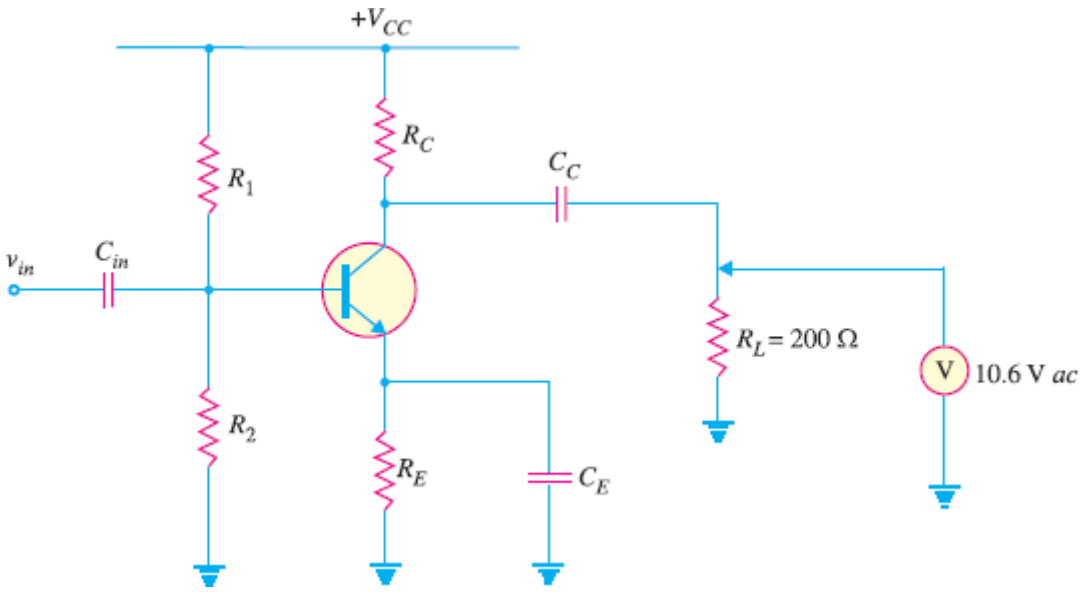


Fig. 4.3.

Solution. The reading of a.c. voltmeter is 10.6V. Since a.c. voltmeters read r.m.s. voltage, we have,

$$\text{A.C. output power, } P_O = \frac{V_L^2}{R_L} = \frac{(10.6)^2}{200\ \Omega} = \mathbf{561.8\ mW}$$

Example 4.3. In an RC coupled power amplifier, the a.c. voltage across load RL (= 100) has a peak- to-peak value of 18V. Find the maximum possible a.c. load power.

Solution. The peak-to-peak voltage, VPP = 18V. Therefore, peak voltage (or maximum voltage) =

$V_{PP}/2$ and the r.m.s value, $V_L = V_{PP}/2\sqrt{2}$.

$$\therefore \quad P_{O\,(max)} = \frac{V_L^2}{R_L} = \frac{(V_{PP}/2\sqrt{2})^2}{R_L} = \frac{V_{PP}^2}{8\ R_L}$$

Here $V_{PP} = 18\text{V}$ and $R_L = 100\Omega$

$$\therefore \quad P_{O\,(max)} = \frac{(18V)^2}{(8 \times 100)\ \Omega} = 405 \times 10^{-3}\ \text{W} = \mathbf{405\ mW}$$

Difference Between Voltage and Power Amplifiers

The distinction between voltage and power amplifiers is somewhat artificial since useful power (*i.e.* product of voltage and current) is always developed in the load resistance through which current flows. The difference between the two types is really one of degree; it is a question of how much voltage and how much power. A voltage amplifier is designed to achieve maximum voltage amplification. It is, however, not important to raise the power level. On the other hand, a power amplifier is designed to obtain maximum output power.

1. Voltage amplifier. The voltage gain of an amplifier is given by :

$$A_v = \beta \times \frac{R_C}{R_{in}}$$

In order to achieve high voltage amplification, the following features are incorporated in such amplifiers :

(i) The transistor with high β □ (>100) is used in the circuit. In other words, those transistors are employed which have thin base.

(ii) The input resistance *Rin* of the transistor is sought to be quite low as compared to the collector load *RC*.

(iii) A relatively high load *RC* is used in the collector. To permit this condition, voltage amplifiers are always operated at low collector currents (j 1 mA). If the collector current is small, we can use large *RC* in the collector circuit.

2. Power amplifier. A power amplifier is required to deliver a large amount of power and as such it has to handle large current. In order to achieve high power amplification, the following features are incorporated in such amplifiers :

(i) The size of power transistor is made considerably larger in order to dissipate the heat produced in the transistor during operation.

(ii) The base is made thicker to handle large currents. In other words, transistors with comparatively smaller □ □ are used.

(iii) Transformer coupling is used for impedance matching.

The comparison between voltage and power amplifiers is given below in the tabular form :

S. No.	Particular	Voltage amplifier	Power amplifier
1.	β	High (> 100)	low (5 to 20)
2.	R_C	High (4 – 10 kΩ)	low (5 to 20 Ω)
3.	*Coupling*	usually *R – C* coupling	Invariably transformer coupling
4.	*Input voltage*	low (a few mV)	High (2 – 4 V)
5.	*Collector current*	low (≃ 1 mA)	High (> 100 mA)
6.	*Power output*	low	high
7.	*Output impedance*	High (≃ 12 kΩ)	low (200 Ω)

Example 4.4. A power amplifier operated from 12V battery gives an output of 2W. Find the maximum collector current in the circuit.

Solution.

Let IC be the maximum collector current.

Power = battery voltage □□ collector current

$$2 = 12 \times I_C$$

$$I_C = \frac{2}{12} = \frac{1}{6}\text{A} = \mathbf{166.7\ mA}$$

This example shows that a power amplifier handles large power as well as large current. **Example**

4.5. A voltage amplifier operated from a 12 V battery has a collector load of 4 k . Find the maximum collector current in the circuit.

Solution.

The maximum collector current will flow when the whole battery voltage is dropped across RC.

$$\text{Max. collector current} = \frac{\text{battery voltage}}{\text{collector load}} = \frac{12\text{ V}}{4\text{ k}\Omega} = 3\text{ mA}$$

This example shows that a voltage amplifier handles small current.

Example 4.6. A power amplifier supplies 50 W to an 8-ohm speaker. Find (i) a.c. output voltage (ii) a.c. output current.

Solution.

(i) $P = V^2/R$

$\therefore$ a.c. output voltage, $V = \sqrt{PR} = \sqrt{50 \times 8} = 20\text{ V}$

(ii) a.c. output current, $I = V/R = 20/8 = 2.5\text{ A}$

Performance Quantities of Power Amplifiers

As mentioned previously, the prime objective for a power amplifier is to obtain maximum output power. Since a transistor, like any other electronic device has voltage, current and power dissipation limits, therefore, the criteria for a power amplifier are : ***collector efficiency, distortion*** and ***power dissipation capability.***

(i) Collector efficiency. The main criterion for a power amplifier is not the power gain rather it is the maximum a.c. power output. Now, an amplifier converts d.c. power from supply into a.c. power output. Therefore, the ability of a power amplifier to convert d.c. power from supply into a.c. output power is a measure of its effectiveness. This is known as collector efficiency and may be defined as under :

The ratio of a.c. output power to the zero signal power (i.e. d.c. power) supplied by the battery of a power amplifier is known as **collector efficiency.**

Collector efficiency means as to how well an amplifier converts d.c. power from the battery into a.c. output power. For instance, if the d.c. power supplied by the battery is 10W and a.c. output power is 2W, then collector efficiency is 20%. The greater the collector efficiency, the larger is the a.c. power output. It is obvious that for power amplifiers, maximum collector efficiency is the desired goal.

(ii) Distortion. *The change of output wave shape from the input wave shape of an amplifier is known as* **distortion.** A transistor like other electronic devices, is essentially a non-linear device. Therefore, whenever a signal is applied to the input of the transistor, the output signal is not exactly like the input signal *i.e.* distortion occurs. Distortion is not a problem for small signals (*i.e.* voltage amplifiers) since transistor is a linear device for small variations about the operating point. However, a power amplifier handles large signals and, therefore, the problem of distortion immediately arises. For the comparison of two power amplifiers, the one which has the less distortion is the better. We shall discuss the method of reducing distortion in amplifiers in the chapter of negative feedback in amplifiers.

(iii) Power dissipation capability. *The ability of a power transistor to dissipate heat is known as* **power dissipation capability.** As stated before, a power transistor handles large currents and heats up during operation. As any temperature change influences the operation of transistor, therefore, the transistor must dissipate this heat to its surroundings. To achieve this, generally a *heat sink* (a metal case) is attached to a power transistor case. The increased surface area allows heat to escape easily and keeps the case temperature of the transistor within permissible limits. Classification of Power

Amplifiers

Transistor power amplifiers handle large signals. Many of them are driven so hard by the input large signal that collector current is either cut-off or is in the saturation region during a large portion of the input cycle. Therefore, such amplifiers are generally classified according to their mode of operation *i.e.* the portion of the input cycle during which the collector current is expected to flow. On this basis, they are classified as :

Amplifier circuits may be classified in terms of the portion of the cycle for which the active device conducts.

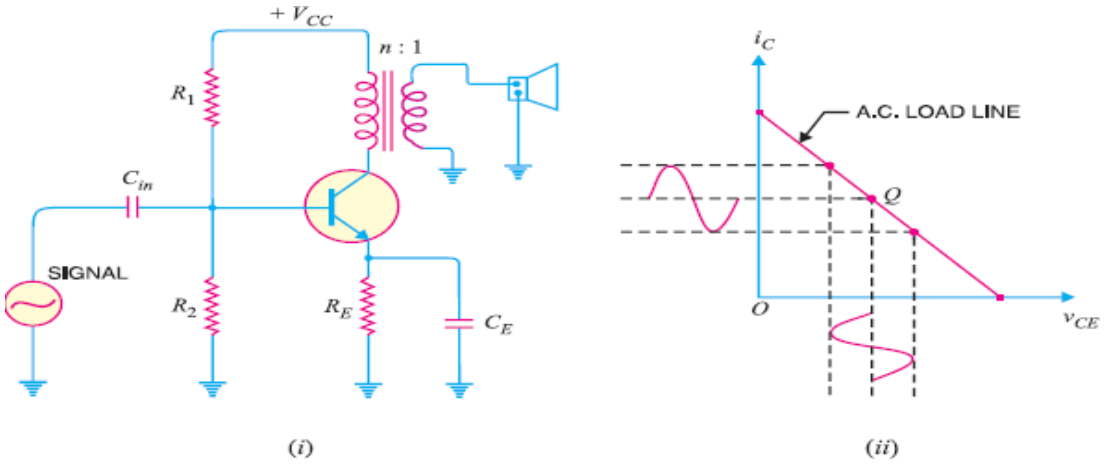
Class A: It is one, in which the active device conducts for the full 360°. Class B: Conduction for 1800

Class C: Conduction for < 1800

Class AB :Conduction angle is between 1800 and 3600

(*i*) class *A* power amplifier **(*ii*)** class *B* power amplifier **(*iii*)** class *C* power amplifier

(i) Class A power amplifier. *If the collector current flows at all times during the full cycle of the*



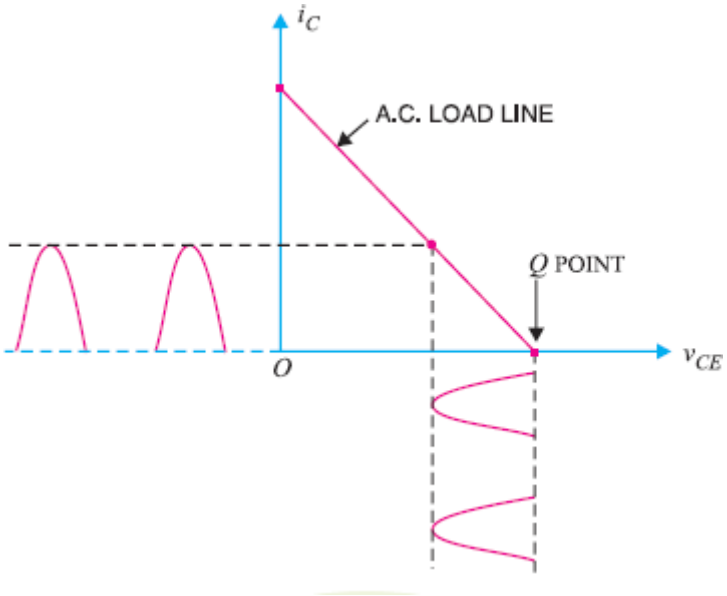
(ii) *signal, the power amplifier is known as* **class A power amplifier.**

Fig. 4.4

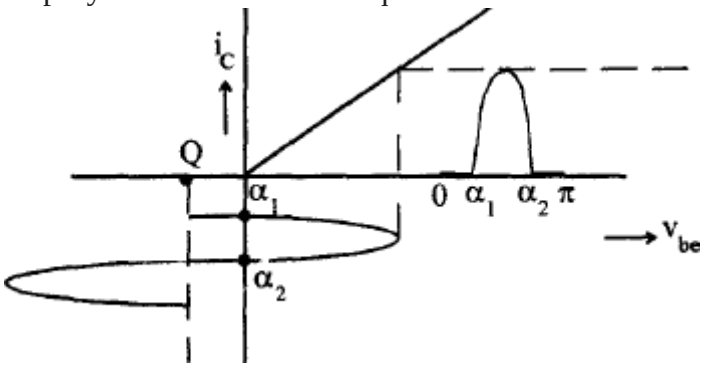
Obviously, for this to happen, the power amplifier must be biased in such a way that no part of the signal is cut off. Fig. 4.4 (*i*) shows circuit of class *A* power amplifier. Note that collector has a transformer as the load which is most common for all classes of power amplifiers. The use of transformer permits impedance matching, resulting in the transference of maximum power to the load *e.g.* loudspeaker. Fig. 4.4 (*ii*) shows the class *A* operation in terms of *a.c.* load line. The operating point *Q* is so selected that collector current flows at all times throughout the full cycle of the applied signal. As the output wave shape is exactly similar to the input wave shape, therefore, such amplifiers have least distortion. However, they have the disadvantage of low power output and low collector efficiency (about 35%).

(iii) **Class B power amplifier.** *If the collector current flows only during the positive half-cycle of the input signal, it is called a* **class B power amplifier.** In class *B* operation, the transistor bias is so adjusted that zero signal collector current is zero *i.e.* no biasing circuit is needed at all. During the positive half-cycle of the signal, the input circuit is forward biased and hence collector current flows. However, during the negative half-cycle of the signal, the input circuit is reverse biased and no collector current flows. Fig. 12.5 shows the class *B* operation in terms of

a.c. load line. Obviously, the operating point *Q* shall be located at collector cut off voltage. It is easy to see that output from a class *B* amplifier is amplified half-wave rectification. In a class *B* amplifier, the negative half-cycle of the signal is cut off and hence a severe distortion occurs. However, class *B* amplifiers provide higher power output and collector efficiency (50 −60%). Such amplifiers are mostly used for power amplification in push-pull arrangement. In such an Arrangement, 2 transistors are used in class *B* operation. One transistor amplifies the positive half cycle of the signal while the other amplifies the negative half-cycle.



(iv) **Class C power amplifier.** *If the collector current flows for less than half-cycle of the input signal, it is called* **class C power amplifier.** In class *C* amplifier, the base is given some negative bias so that collector current does not flow just when the positive half-cycle of the signal starts. Such amplifiers are never used for power amplification. However, they are used as tuned amplifiers *i.e*. to amplify a narrow band of frequencies near the resonant frequency.



Expression for Collector Efficiency

For comparing power amplifiers, collector efficiency is the main criterion. The greater the collector efficiency, the better is the power amplifier.

Now, Collector efficiency

$$* P_o = [(0.5\times0.707)\, v_{ce\,(p-p)}]\,[(0.5\times0.707)\, i_{c\,(p-p)}]$$

$$= \frac{v_{ce(p-p)} \times i_{c(p-p)}}{8}$$

$$\text{Collector } \eta = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8\, V_{CC}\, I_C}$$

where *Vce* is the *r.m.s.* value of signal output voltage and *Ic* is the *r.m.s.* value of output signal current. In terms of peak-to-peak values (which are often convenient values in load-line work), the a.c. power output can be expressed as :

$$\text{Collector efficiency, } \eta = \frac{\text{a.c. power output}}{\text{d.c. power input}}$$

$$= \frac{P_o}{P_{dc}}$$

$$* P_{dc} = V_{CC} I_C$$

$$P_o = V_{ce} I_c$$

Series-Fed Class A Amplifier

Fig. 4.6 (*i*) shows a series – fed class *A* amplifier. This circuit is seldom used for power amplification due to its poor collector efficiency. Nevertheless, it will help the reader to understand the class *A* operation. The d.c. load line of the circuit is shown in Fig. 12.6 (*ii*). When an *ac* signal is applied to the amplifier, the output current and voltage will vary about the operating point *Q*. In order to achieve the maximum symmetrical swing of current and voltage (to achieve maximum output power), the *Q* point should be located at the centre of the *dc* load line. In that case, operating point is *IC* =*VCC*/2*RC* and *VCE* = *VCC*/2 .

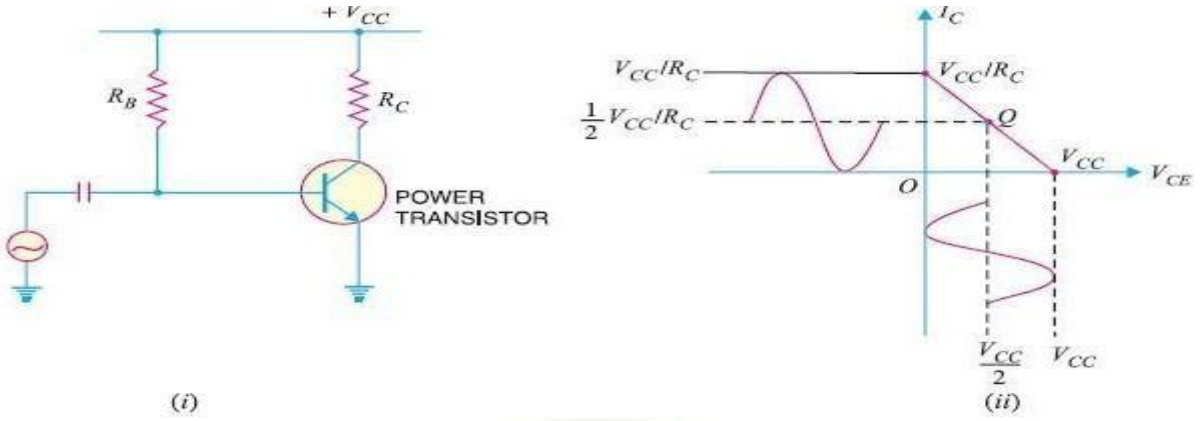


Fig. 4.6

$$\text{Maximum } v_{ce\,(p-p)} = V_{CC}$$

$$\text{Maximum } i_{c\,(p-p)} = V_{CC}/R_C$$

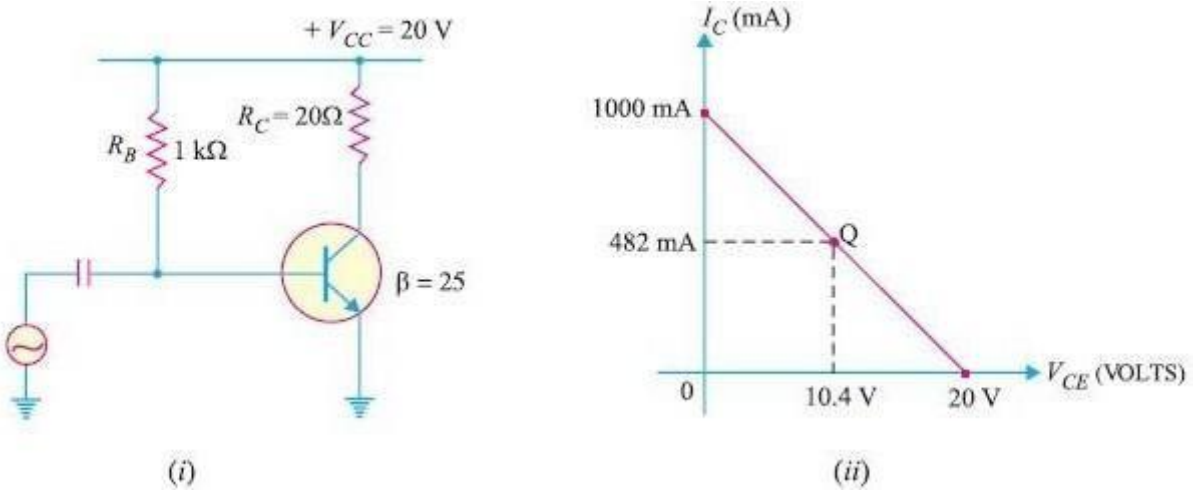
$$\text{Max. } ac \text{ output power, } P_{o\,(max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8} = \frac{V_{CC} \times V_{CC}/R_C}{8} = \frac{V_{CC}^2}{8R_C}$$

$$\text{D.C. power supplied, } P_{dc} = V_{CC}\, I_C = V_{CC}\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{2R_C}$$

$$\therefore \quad \text{Maximum collector } \eta = \frac{P_{o(max)}}{P_{dc}} \times 100 = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100 = 25\%$$

Thus the maximum collector efficiency of a class *A* series-fed amplifier is 25%. In actual practice, the collector efficiency is far less than this value.

Example 4.7. *Calculate the* (*i*) *output power* (*ii*) *input power and* (*iii*) *collector efficiency of the amplifier circuit shown in Fig. 12.7* (*i*). *It is given that input voltage results in a base current of 10 mA peak.*



(*i*) (*ii*)

Solution. First draw the *d.c.* load line by locating the two end points *viz.*, $I_{C\,(sat)} = V_{CC}/R_C = 20\text{ V}/20\ \Omega = 1\text{ A} = 1000\text{ mA}$ and $V_{CE} = V_{CC} = 20\text{ V}$ as shown in Fig. 12.7 (*ii*). The operating point *Q* of the circuit can be located as under :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{1\,\text{k}\Omega} = 19.3\text{ mA}$$

$$\therefore \quad I_C = \beta I_B = 25\,(19.3\text{ mA}) = 482\text{ mA}$$

$$\text{Also} \quad V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - (482\text{ mA})\,(20\ \Omega) = 10.4\text{ V}$$

The operating point *Q* (10.4 V, 482 mA) is shown on the d.c. load line.

(*i*) $i_c\text{-}(peak) = \beta\, i_b\,(peak) = 25 \times (10\text{ mA}) = 250\text{ mA}$

$$\therefore \quad P_{o\,(ac)} = \frac{i_c^2(peak)}{2} R_C = \frac{(250 \times 10^{-3})^2}{2} \times 20 = \mathbf{0.625\text{ W}}$$

(*ii*) $P_{dc} = V_{CC} I_C = (20\text{ V})\,(482 \times 10^{-3}) = \mathbf{9.6\text{ W}}$

(*iii*) $\text{Collector } \eta = \frac{P_o(ac)}{P_{dc}} \times 100 = \frac{0.625}{9.6} \times 100 = \mathbf{6.5\ \%}$

Maximum Collector Efficiency of Transformer Coupled Class A Power Amplifier

In class *A* power amplifier, the load can be either connected directly in the collector or it can be transformer coupled. The latter method is often preferred for two main reasons. First, transformer coupling permits impedance matching and secondly it keeps the d.c. power loss small because of the small resistance of the transformer primary winding.

Fig. 12.8 (*i*) shows the transformer coupled class *A* power amplifier. In order to determine maximum collector efficiency, refer to the output characteristics shown in Fig. 4.8 (*ii*). Under zero signal conditions, the effective resistance in the collector circuit is that of the primary winding of the transformer. The primary resistance has a v line is a vertical line rising from *VCC* as shown in Fig. 12.8 (*ii*). When signal is applied, the collector current will vary about the operating point *Q*.

In order to get maximum a.c. power output (and hence maximum collector □), the peak value of collector current due to signal alone should be equal to the zero signal collector current *IC*. In terms of a.c. load line, the operating point *Q* should be located at the centre of a.c. load line.ery small value and is

assumed zero. Therefore, d.c. load

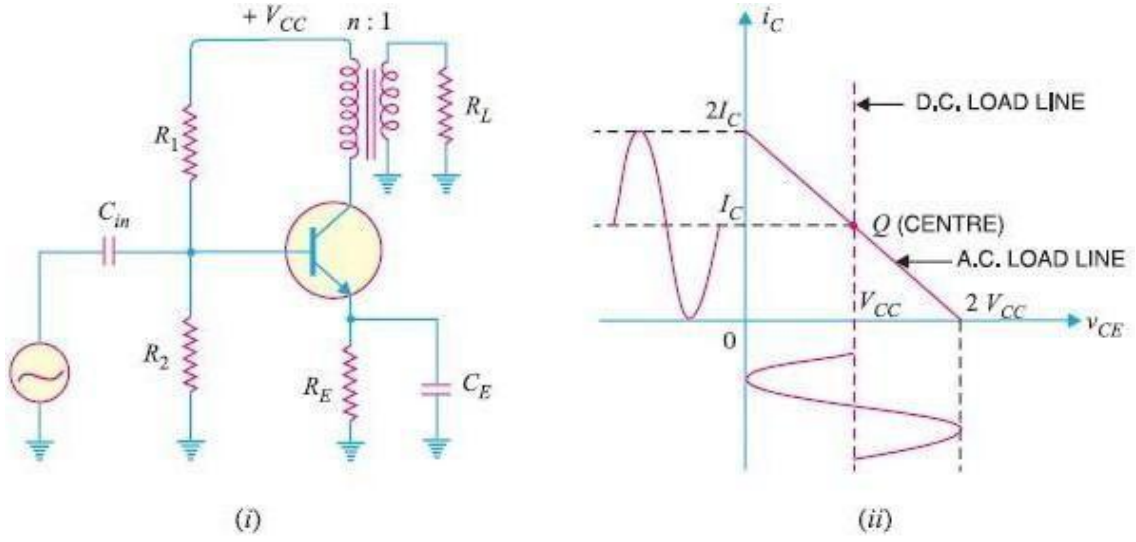


Fig. 4.8

During the peak of the positive half-cycle of the signal, the total collector current is 2 IC and vce = 0. During the negative peak of the signal, the collector current is zero and vce = 2VCC.

 Peak-to-peak collector-emitter voltage is

vce (p - p) = 2VCC Peak-to-peak collector current, ic (p - p) = 2 IC

$$= \frac{v_{ce(p-p)}}{R_L'} = \frac{2V_{CC}}{R_L'}$$

where RL' is the reflected value of load RL and appears in the primary of the transformer. If n (= Np/Ns) is the turn ratio of the transformer, then, RL' = n^2 RL.

d.c. power input, P_{dc} = VCC IC

$$= I_C^2 R_L'$$

Max.a.c. output power, P_O (max)=

$$P_{o\,(max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8}$$

$$= \frac{2V_{CC} \times 2I_C}{8}$$

$$= \frac{1}{2} V_{CC} I_C$$

$$= \frac{1}{2} I_C^2 R_L'$$

$$\therefore \quad \text{Max. collector } \eta = \frac{P_{o\,(max)}}{P_{dc}} \times 100$$

$$= \frac{(1/2)\, I_C^2\, R_L'}{I_C^2\, R_L'} \times 100 = 50\%$$

Important Points About Class A Power Amplifier

(i) A *transformer coupled class A power amplifier has a maximum collector efficiency of50% *i.e.*, maximum of 50% d.c. supply power is converted into a.c. power output. In practice, the efficiency of such an amplifier is less than 50% (about 35%) due to power losses in the output transformer, power dissipation in the transistor etc.

(ii) The power dissipated by a transistor is given by :

Pdis = *Pdc* - *Pac* where *Pdc* = available d.c. power *Pac* = available a.c. power
Clearly, in class *A* operation, the transistor must dissipate less heat when signal is applied and therefore runs cooler.

(iii) When no signal is applied to a class *A* power amplifier, *Pac* = 0.
Pdis = *Pdc*
Thus in class *A* operation, maximum power dissipation in the transistor occurs under zero signal conditions. Therefore, the power dissipation capability of a power transistor (for class *A* operation) must be atleast equal to the zero signal rating. For example, if the zero signal power dissipation of a transistor is 1 W, then transistor needs a rating of atleast 1W. If the power rating of the transistor is less than 1 W, it is likely to be damaged.

(iv) When a class *A* power amplifier is used in the final stage, it is called **single ended class A power amplifier.**

Example 4.8. *A power transistor working in class A operation has zero signal power dissipation of 10 watts. If the a.c. output power is 4 watts, find :*
(*i*) *collector efficiency* (*ii*) *power rating of transistor*

Solution.
Zero signal power dissipation, *Pdc* = 10 W
a.c. power output, *Po* = 4 W

(i) Collector efficiency =

$$\frac{P_o}{P_{dc}} \times 100 = \frac{4}{10} \times 100 = 40\%$$

(ii) The zero signal power represents the worst case *i.e.* maximum power dissipation in a transistor occurs under zero signal conditions.
∴ Power rating of transistor = **10 W**
It means to avoid damage, the transistor must have a power rating of atleast 10 W.

Example 4.9. *A class A power amplifier has a transformer as the load. If the transformer has a turn ratio of 10 and the secondary load is 100 Ω, find the maximum a.c. power output. Given that zero signal collector current is 100 mA.*

Solution.
Secondary load, *RL* = 100 Ω

Transformer turn ratio, $n = 10$
Zero signal collector current, $I_C = 100\,\text{mA}$
Load as seen by the primary of the transformer is

$$R'_L = n^2 R_L = (10)^2 \times 100 = 10{,}000\,\Omega$$

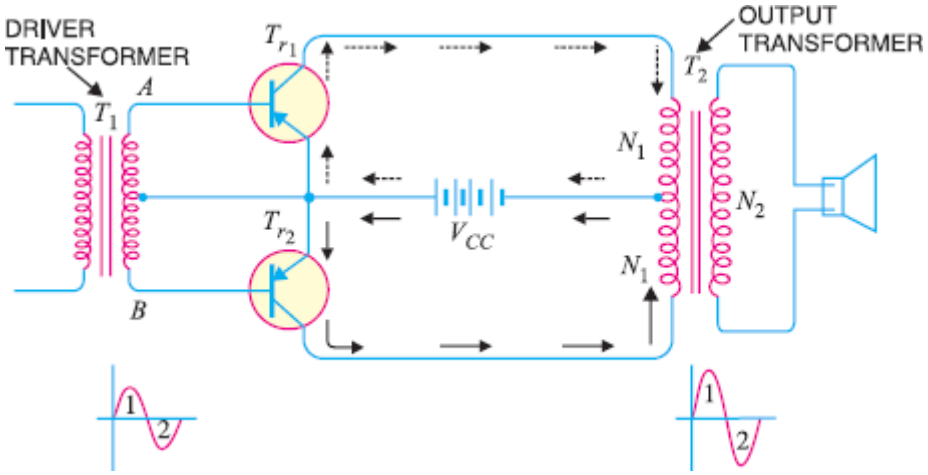
$$\therefore \quad \text{Max. a.c. power output} = \frac{1}{2} I_C^2 R'_L = \frac{1}{2}\left(\frac{100}{1000}\right)^2 \times 10{,}000$$

$$= 50\ \text{W}$$

Class B Push-Pull Power Amplifier

The push-pull amplifier is a power amplifier and is frequently employed in the output stages of electronic circuits. It is used whenever high output power at high efficiency is required. Fig. 4.14 shows the circuit of a push-pull amplifier. Two transistors *Tr*1 and *Tr*2 placed back to back are employed. Both transistors are operated in class *B* operation *i.e.* collector current is nearly zero in the absence of the signal. The centre-tapped secondary of driver transformer *T*1 supplies equal and opposite voltages to the base circuits of two transistors. The output transformer *T*2 has the centre-tapped primary winding. The supply voltage *VCC* is connected between the bases and this centre tap. The loudspeaker is connected across the secondary of this transformer.

Circuit operation. The input signal appears across the secondary *AB* of driver transformer. Suppose during the first half-cycle (marked 1) of the signal, end *A* becomes positive and end *B* negative. This will make the base-emitter junction of *Tr*1 reverse biased and that of *Tr*2 forward biased. The circuit will conduct current due to *Tr*2 only and is shown by solid arrows. Therefore, this half-cycle of the signal is amplified by *Tr*2 and appears in the lower half of the primary of output transformer. In the next halfcycle of the signal, *Tr*1 is forward biased whereas *Tr*2 is reverse biased. Therefore, *Tr*1 conducts and is shown by dotted arrows. Consequently, this half- cycle of the signal is amplified by *Tr*1 and appears in the upper half of the output transformer primary. The centre-tapped primary of the output transformer combines two collector currents to form a sine wave output in the secondary.



. Fig. 4.14

It may be noted here that push-pull arrangement also permits a maximum transfer of power to the load through impedance matching. If *RL* is the resistance appearing across secondary of output transformer,
then resistance *R'L* of primary shall become :

$$R'_L = \left(\frac{2N_1}{N_2}\right)^2 R_L$$

where N_1 = Number of turns between either end of primary winding and centre-tap

N_2 = Number of secondary turns

Advantages

(i) The efficiency of the circuit is quite high (i.e 75%) due to class *B* operation.
(ii) A high a.c. output power is obtained.

Disadvantages

(i) Two transistors have to be used.
(ii) It requires two equal and opposite voltages at the input. Therefore, push-pull circuit requires the use of driver stage to furnish these signals.
(iii) If the parameters of the two transistors are not the same, there will be unequal amplification of the two halves of the signal.
(iv) The circuit gives more distortion.
(v) Transformers used are bulky and expensive.

Maximum Efficiency for Class B Power Amplifier

We have already seen that a push-pull circuit uses two transistors working in class *B* operation. For class *B* operation, the Q-point is located at cut-off on both d.c. and a.c. load lines. For maximum signal operation, the two transistors in class B amplifier are alternately driven from cut-off to saturation. This is shown in Fig. 4.15 (*i*). It is clear that a.c. output voltage has a peak value of *VCE* and a.c. output current has a peak value of *IC* (*sat*). The same information is also conveyed through the a.c. load line for the circuit [See Fig. 4.15 (*ii*)].

$\therefore$ Peak a.c. output voltage $= V_{CE}$

Peak a.c. output current $= I_{C\,(sat)} = \dfrac{V_{CE}}{R_L} = \dfrac{V_{CC}}{2\,R_L}$ $\left(\because V_{CE} = \dfrac{V_{CC}}{2}\right)$

Maximum average a.c. output power $P_{o\,(max)}$ is

$P_{o\,(max)}$ = Product of r.m.s. values of a.c. output voltage and a.c. output current

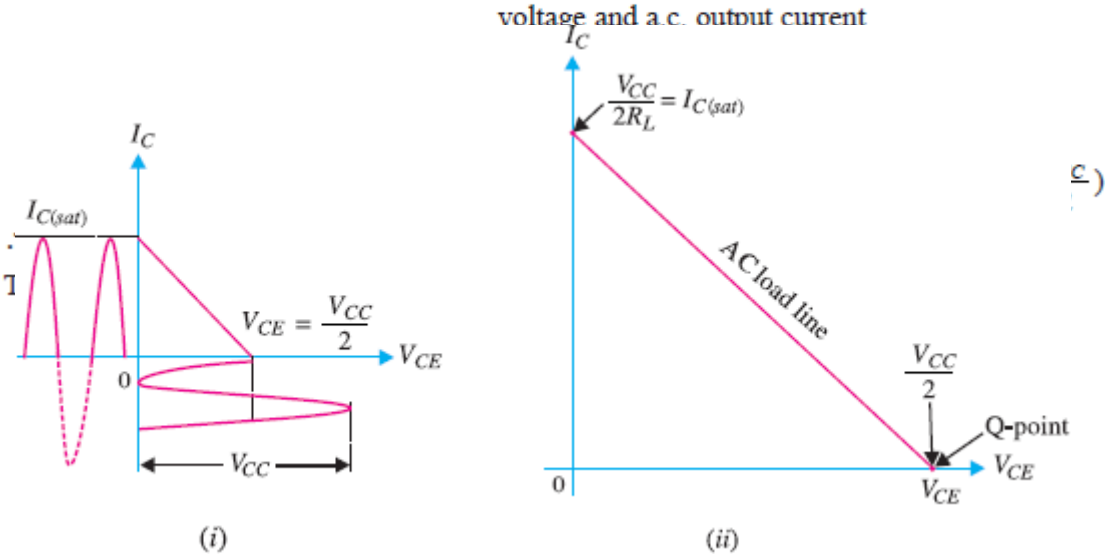


Fig. 4.15

where *Idc* is the average current drawn from the supply *VCC*. Since the transistor is on for alternating half-cycles, it effectively acts as a half-wave rectifier.

$\therefore \quad I_{dc} = \dfrac{I_{C\,(sat)}}{\pi}$

$\therefore \quad P_{dc} = \dfrac{V_{CC}\, I_{C\,(sat)}}{\pi}$

$\therefore$ Max. collector $\eta = \dfrac{P_{o\,(max)}}{P_{dc}} = \dfrac{0.25\, V_{CC}\ I_{C\,(sat)}}{\left(V_{CC}\, I_{C\,(sat)}\right)/\pi} \times 100 = 0.25\pi \times 100 = 78.5\%$

Thus the maximum collector efficiency of class *B* power amplifier is 78.5%. Recall that maximum collector efficiency for class A transformer coupled amplifier is 50%.

Power dissipated by transistors. The power dissipated (as heat) by the transistors in class *B* amplifier is the difference between the input power delivered by *VCC* and the output power

$P_{2T} = P_{dc} - P_{ac}$

where P_{2T} = power dissipated by the two transistors

$\therefore$ Power dissipated by each transistor is

$P_T = \dfrac{P_{2T}}{2} = \dfrac{P_{dc} - P_{ac}}{2}$

delivered to the load *i.e.*

Example 4.18. *For a class B amplifier using a supply of VCC = 12V and driving a load of 8Ω, determine (i) maximum load power (ii) d.c. input power (iii) collector efficiency.*

Solution. $V_{CC} = 12\text{ V}\ ;\ R_L = 8\Omega$

(i) Maximum load power, $P_{o\,(max)} = 0.25\ V_{CC}\ I_{C\,(sat)}$

$$= 0.25\ V_{CC} \times \frac{V_{CC}}{2\,R_L} \qquad \left(\because I_{C\,(sat)} = \frac{V_{CC}}{2\,R_L}\right)$$

$$= 0.25 \times 12 \times \frac{12}{2 \times 8} = \mathbf{2.25\ W}$$

(ii) D.C. input power, $P_{dc} = \dfrac{V_{CC}\ I_{C\,(sat)}}{\pi} = \dfrac{V_{CC}}{\pi} \times \dfrac{V_{CC}}{2\,R_L}$

$$= \frac{12}{\pi} \times \frac{12}{2 \times 8} = \mathbf{2.87\ W}$$

(iii) Collector $\eta = \dfrac{P_{o\,(max)}}{P_{dc}} \times 100 = \dfrac{2.25}{2.87} \times 100 = \mathbf{78.4\%}$

Example 4.19. *A class B push-pull amplifier with transformer coupled load uses two transistors rated 10 W each. What is the maximum power output one can obtain at the load from thecircuit?*

Solution. The power dissipation by each transistor is $P_T = 10\text{W}$. Therefore, power dissipated by two transistors is $P_{2T} = 2 \times 10 = 20\text{W}$.

Now $P_{dc} = P_{o\,(max)} + P_{2T}\ ;$ Max. $\eta = 0.785$

$$\therefore \quad \text{Max } \eta = \frac{P_{o\,(max)}}{P_{dc}} = \frac{P_{o\,(max)}}{P_{o\,(max)} + P_{2T}} = \frac{P_{o\,(max)}}{P_{o\,(max)} + 20}$$

$$\text{or} \quad 0.785 = \frac{P_{o\,(max)}}{P_{o\,(max)} + 20}$$

$$\text{or} \quad 0.785\ P_{o\,(max)} + 15.7 = P_{o\,(max)}$$

$$\text{or} \quad P_{o\,(max)}\,(1 - 0.785) = 15.7$$

$$\therefore \quad P_{o\,(max)} = \frac{15.7}{1 - 0.785} = \frac{15.7}{0.215} = \mathbf{73.02\ W}$$

Example 4.20. *A class B amplifier has an efficiency of 60% and each transistor has a rating of 2.5W. Find the a.c. output power and d.c. input power*

Solution. The power dissipated by each transistor is $P_T = 2.5\text{W}$.

Therefore, power dissipated by the two transistors is $P_{2T} = 2 \times 2.5 = 5\text{W}$.

Now $P_{dc} = P_{ac} + P_{2T}$; $\eta = 0.6$

$\therefore$ $\eta = \dfrac{P_{ac}}{P_{dc}} = \dfrac{P_{ac}}{P_{ac} + P_{2T}}$

or $0.6 = \dfrac{P_{ac}}{P_{ac} + 5}$ or $0.6\ P_{ac} + 3 = P_{ac}$

$\therefore$ $P_{ac} = \dfrac{3}{1 - 0.6} = \dfrac{3}{0.4} = \mathbf{7.5\ W}$

and $P_{dc} = P_{ac} + P_{2T} = 7.5 + 5 = \mathbf{12.5\ W}$

Example 4.21. *A class B amplifier uses VCC = 10V and drives a load of 10Ω. Determine the end point values of the a.c. load line.*

Solution.

$$I_{C\,(sat)} = \frac{V_{CC}}{2R_L} = \frac{10\text{V}}{2(10\ \Omega)} = \mathbf{500\ mA}$$

This locates one end-point of the a.c. load line on the collector current axis.

$$V_{CE\,(off)} = \frac{V_{CC}}{2} = \frac{10\text{V}}{2} = \mathbf{5V}$$

Complementary-Symmetry Amplifier

By complementary symmetry is meant a principle of assembling push-pull class *B* amplifier without requiring centre-tapped transformers at the input and output stages. Fig. 4.16 shows the transistor push-pull amplifier using complementary symmetry. It employs one *npn* and one *pnp* transistor and requires no centre-tapped transformers. The circuit action is as follows. During the positive-half of the input signal, transistor *T*1 (the *npn* transistor) conducts current while *T*2 (the *pnp* transistor) is cut off. During the negative half-cycle of the signal, *T*2 conducts while *T*1 is cut off. In this way, *npn* transistor amplifies the positive half-cycles of the signal while the *pnp* transistor amplifies the negative half-cycles of the signal. Note that we generally use an output transformer (not centre-tapped) for impedance matching.

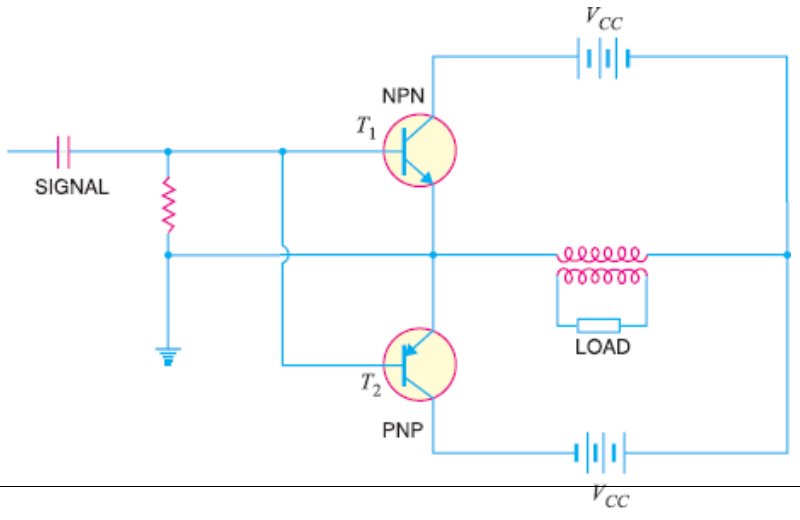


Fig. 4.16

Advantages

(i) This circuit does not require transformer. This saves on weight and cost.

(ii) Equal and opposite input signal voltages are not required.

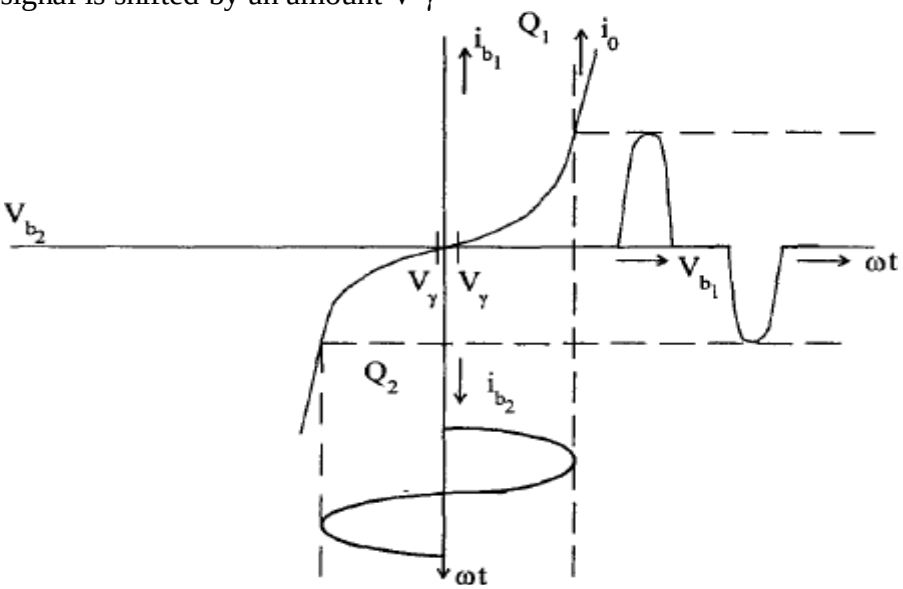
Disadvantages

(i) It is difficult to get a pair of transistors (*npn* and *pnp*) that have similar characteristics.

(ii) We require both positive and negative supply voltages.

DISTORTION

Let ib1 V c, Vb1 be the input characteristic of the first transistor and ib2, V s, Vb2 is the input characteristic of th6 second transistor. V y is the cut)n voltage. These are t6e two tiansistors of the class B pushpull amplifier. Now the base input voltage being given to the transistor is sinusoidal, i.e., base drive is sinusoidal. So because of the *cut in voltage*, eventhough input voltage is present, output will not be transmitted or there is distortion in the output current of the transistor. This is known as *crossover distortion*. But this will not occur if the base current drive is sinusoidal. Since in the graphical analysis the input current is taken in the I quadrant. No distortion if the operating point is in the active region. Cross-over distortion can also be laminated in class AB operation. A small stand by current flows at zero excitation. The input signal is shifted by constant DC bias so that the input signal is shifted by an amount V γ



Thermal Runaway

All semiconductor devices are very sensitive to temperature variations. If the temperature of a transistor exceeds the permissible limit, the transistor may be *permanently damaged. Silicon transistors can withstand temperatures upto 250ºC while the germanium transistors can withstand temperatures upto 100ºC.

There are two factors which determine the operating temperature of a transistor *viz*.

(i) surrounding temperature and

(ii) power dissipated by the transistor.

When the transistor is in operation, almost the entire heat is produced at the collector-base junction. This power dissipation causes the junction temperature to rise. This in turn increases the collector current since more electron-hole pairs are generated due to the rise in temperature. This produces an increased power dissipation in the transistor and consequently a further rise in temperature. Unless adequate cooling is provided or the transistor has built-in temperature compensation circuits to prevent excessive collector current rise, the junction temperature will continue to increase until the maximum permissible temperature is exceeded. If this situation occurs, the transistor will be permanently damaged.

The unstable condition where, owing to rise in temperature, the collector current rises and continues to increase is known as **thermal runaway.**

Thermal runaway must always be avoided. If it occurs, permanent damage is caused and the transistor must be replaced.

Heat Sink

As power transistors handle large currents, they always heat up during operation. Since transistor is a temperature dependent device, the heat generated must be dissipated to the surroundings in order to keep the temperature within permissible limits. Generally, the transistor is fixed on a metal sheet (usually aluminium) so that additional heat is transferred to the *Al* sheet.

The metal sheet that serves to dissipate the additional heat from the power transistor is known as **heat sink.**

Most of the heat within the transistor is produced at the collector junction. The heat sink increases the surface area and allows heat to escape from the collector junction easily. The result is that temperature of the transistor is sufficiently lowered. Thus heat sink is a direct practical means of combating the undesirable thermal effects *e.g.* thermal runaway. material, volume, area, shape, contact between case and sink and movement of air around the sink. Finned aluminium heat sinks yield the best heat transfer per unit cost. It should be realised that the use of heat sink alone may not be sufficient to prevent thermal runaway under all conditions. In designing a transistor circuit, consideration should also be given to the choice of

(i) operating point
(ii) ambient temperatures which are likely to be encountered and
(iii) the type of transistor *e.g.* metal case transistors are more readily cooled by conduction than plastic ones.

Circuits may also be designed to compensate automatically for temperature changes and thus stabilise the operation of the transistor components.

Classification of heat Sinks

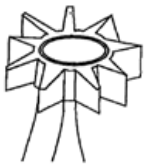
(i) Low Power Transistor Type.
(ii) High Power Transistor Type.

Low Power Transistor Type

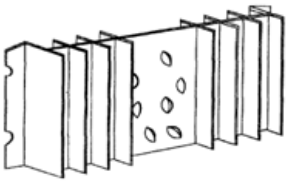
- Low Power Transistors can be mounted directly on the metal chassis to increase the heat dissipation capability. The casing of the transistor must be insulated from the metal chassis to prevent shorting.
- Beryllium oxide insulating washers are used for insulating casing from the chassis. They have good thermal conductivity.
- Zinc oxide film silicon compound between washer and chassis, improves the heat transfer from the semiconductor device to case to the chassis.

High Power Transistor Type.

- re TO-3 and TO-66 types. These are diamond shaped. For power transistors, usually, the ease itself in the collector convention and radiation
- Finned aluminium heat sinks yield the best heat transfer per unit cost.



Fin-type heat sink



Power transistor heat sink

Mathematical Analysis

The permissible power dissipation of the transistor is very important item for power transistors. The permissible power rating of a transistor is calculated from the following relation :

$$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta}$$

where
P_{total} = total power dissipated within the transistor
$T_{J\,max}$ = maximum junction temperature. It is 90°C for *germanium* transistors and 150°C for *silicon* transistors.
T_{amb} = ambient temperature *i.e.* temperature of surrounding air
θ = *thermal resistance *i.e.* resistance to heat flow from the junction to the surrounding air

The unit of Ə is °C/ watt and its value is always given in the transistor manual. A low thermal resistance means that it is easy for heat to flow from the junction to the surrounding air. The larger the transistor case, the lower is the thermal resistance and *vice-versa*. It is then clear that by using heat sink, the value of θ can be decreased considerably, resulting in increased power dissipation.

Example 4.15. *A power transistor dissipates 4 W. If TJmax = 90°C, find the maximum ambient temperature at which it can be operated. Given Ə = 10°C/W.*

Solution.

$$P_{total} = 4\ \text{W}$$
$$T_{J\,max} = 90°\text{C}$$
$$\theta = 10°\text{C/W}$$

Now $$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta}$$

or $$4 = \frac{90 - T_{amb}}{10}$$

∴ Ambient temperature, $T_{amb} = 90 - 40 = 50°\text{C}$

The above example shows the effect of ambient temperature on the permissible power dissipation in a transistor. The lower the ambient temperature, the greater is the permissible power dissipation. Thus, a transistor can pass a higher collector current in winter than insummer.

Example 4.16. (*i*) *A power transistor has thermal resistance* $\theta = 300^oC/W$. *If the maximum junction temperature is* 90^oC *and the ambient temperature is* 30^oC, *find the maximum permissible power dissipation.*

(*ii*) *If a heat sink is used with the above transistor, the value of* θ *is reduced to* $60^oC/W$. *Find the maximum permissible power dissipation.*

Solution.

(i) Without heat sink

$$T_{J\,max} = 90°C$$
$$T_{amb} = 30°C$$
$$\theta = 300°C/W$$

$$\therefore \quad P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{90-30}{300} = 0.2\ W = \mathbf{200\ mW}$$

(ii) With heat sink

$$T_{J\,max} = 90°C$$
$$T_{amb} = 30°C$$
$$\theta = 60°C/W$$

$$\therefore \quad P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{90-30}{60} = 1\ W = \mathbf{1000\ mW}$$

It is clear from the above example that permissible power dissipation with heat sink is 5 times as compared to the case when no heat sink is used.

Example 4.17. *The total thermal resistance of a power transistor and heat sink is* $20°C/W$. *The ambient temperature is* $25°C$ *and* T_J *max* $= 200°C$. *If* $V_{CE} = 4$ *V, find the maximum collector current that the transistor can carry without destruction. What will be the allowed value of collector current if ambient temperature rises to* $75°C$ *?*

Solution.

$$P_{total} = \frac{T_{Jmax} - T_{amb}}{\theta} = \frac{200-25}{20} = 8.75\ W$$

This means that maximum permissible power dissipation of the transistor at ambient temperature of 25°C is 8.75 W *i.e.*

$$V_{CE} I_C = 8.75$$
$$\therefore \quad I_C = 8.75/4 = \mathbf{2.19\ A}$$

Again $$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta} = \frac{200-75}{20} = 6.25\ W$$

$$\therefore \quad I_C = 6.25/4 = \mathbf{1.56\ A}$$

This example clearly shows the effect of ambient temperature.

Transistor Tuned Amplifiers

INTRODUCTION

An audio amplifier amplifies a wide band of frequencies equally well and does not permit the selection of a particular desired frequency while rejecting all other frequencies. However, sometimes it is desired that an amplifier should be selective *i.e.* it should select a desired frequency or narrow band of frequencies for amplification. For instance, radio and television transmission are carried on a specific radio frequency assigned to the broadcasting station. The radio receiver is required to pick up and amplify the radio frequency desired while discriminating all others. To achieve this, the simple resistive load is replaced by a parallel tuned circuit whose impedance strongly depends upon frequency. Such a tuned circuit becomes very selective and amplifies very strongly signals of resonant frequency and narrow band on either side. Therefore, the use of tuned circuits in conjunction with a transistor makes possible the selection and efficient amplification of a particular desired radio frequency. Such an amplifier is called a *tuned amplifier*. In this chapter, we shall focus our attention on transistor tuned amplifiers and their increasing applications in high frequency electronic circuits.

Advantages of Tuned Amplifiers

In high frequency applications, it is generally required to amplify a single frequency, rejecting all other frequencies present. For such purposes, tuned amplifiers are used. These amplifiers use tuned parallel circuit as the collector load and offer the following advantages :

(i) Small power loss. A tuned parallel circuit employs reactive components *L* and *C*. Consequently, the power loss in such a circuit is quite low. On the other hand, if a resistive load is used in the collector circuit, there will be considerable loss of power. Therefore, tuned amplifiers are highly efficient.

(ii) High selectivity. A tuned circuit has the property of selectivity *i.e.* it can select the desired frequency for amplification out of a large number of frequencies simultaneously impressed upon it. For instance, if a mixture of frequencies including *fr* is fed to the input of a tuned amplifier, then maximum amplification occurs for *fr*. For all other frequencies, the tuned circuit offers very low impedance and hence these are amplified to a little extent and may be thought as rejected by the circuit. On the other hand, if we use resistive load in the collector, all the frequencies will be amplified equally well *i.e.* the circuit will not have the ability to select the desired frequency.

(iii) Smaller collector supply voltage. Because of little resistance in the parallel tuned circuit,

it requires small collector supply voltage *VCC*. On the other hand, if a high load resistance is used in the collector for amplifying even one frequency, it would mean large voltage drop across it due to zero signal collector current. Consequently, a higher collector supply will be needed.

Why not Tuned Circuits for Low Frequency Amplification?

The tuned amplifiers are used to select and amplify a specific high frequency or narrow band of frequencies. The reader may be inclined to think as to why tuned circuits are not used to amplify low frequencies. This is due to the following reasons :

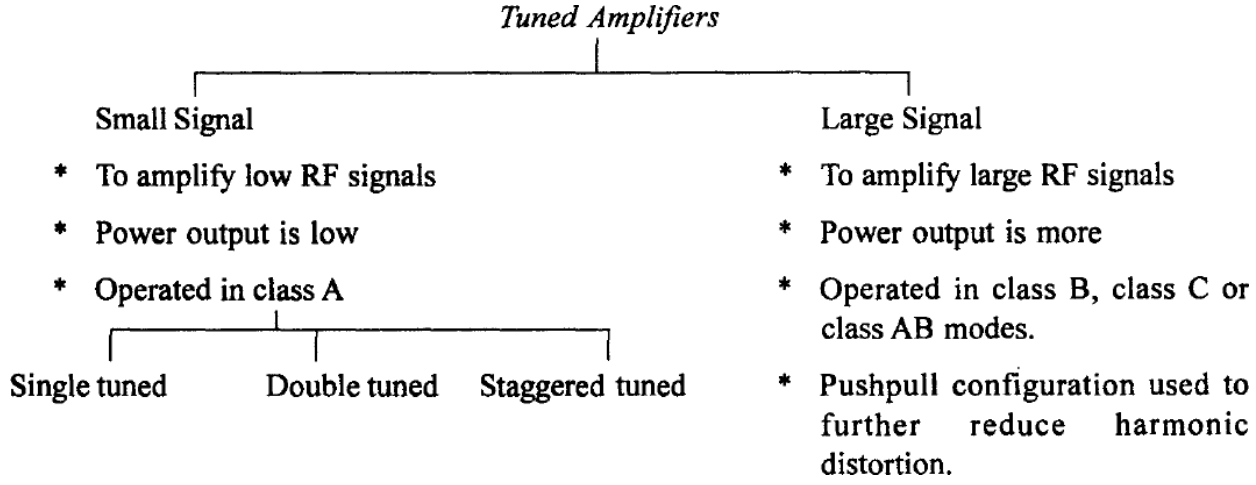
(i) *Low frequencies are never single.* A tuned amplifier selects and amplifies a single frequency. However, the low frequencies found in practice are the audio frequencies which are a mixture of frequencies from 20 Hz to 20 kHz and are not single. It is desired that all these frequencies should be equally amplified for proper reproduction of the signal. Consequently, tuned amplifiers cannot be used for the purpose.

(ii) *High values of L and C.* The resonant frequency of a parallel tuned circuit is given by;

$fr = 1/2\pi\ LC$

For low frequency amplification, we require large values of *L* and *C*. This will make the tuned Circuit bulky and expensive. It is worthwhile to mention here that *R-C* and transformer coupled Amplifiers, which are comparatively cheap, can be conveniently used for low frequency applications.

Classification



Tuned Amplifiers

Amplifiers which amplify a specific frequency or narrow band of frequencies are called **tuned amplifiers.** Tuned amplifiers are mostly used for the amplification of high or radio frequencies.

It is because radio frequencies are generally single and the tuned circuit permits their selection and efficient amplification. However, such amplifiers are not suitable for the amplification of audio frequencies as they are mixture of frequencies from 20 Hz to 20 kHz and not single.

Tuned amplifiers are widely used in radio and television circuits where they are called upon to handle radio frequencies. Fig. 5.1 shows the circuit of a simple transistor tuned amplifier. Here, instead of load resistor, we have a parallel tuned circuit in the collector. The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance

at *resonant frequency* and very small impedance at all other frequencies. If the signal has the same frequency as the resonant frequency of *LC* circuit, large amplification will result due to high impedance of *LC* circuit at this frequency. When signals of many frequencies are present at the input of tuned amplifier, it will select and strongly amplify the signals of resonant frequency while *rejecting all others. Therefore, such amplifiers are very useful in radio receivers to select the signal from one particular broadcasting station when signals of many other frequencies are present at the receiving aerial.

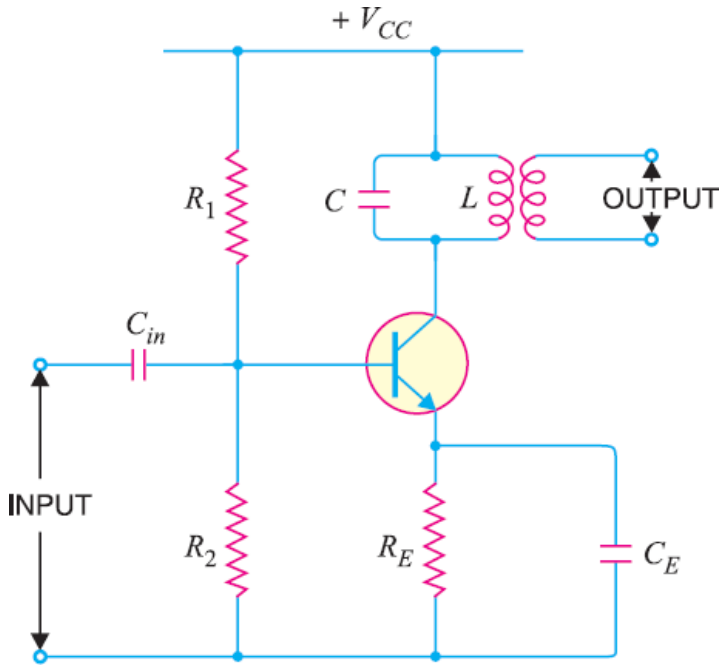


Fig.5.1

Distinction between Tuned Amplifiers and other Amplifiers

We have seen that amplifiers (*e.g.*, voltage amplifier, power amplifier *etc.*) provide the constant gain over a limited band of frequencies *i.e.*, from lower cut-off frequency *f*1 to upper cut-off frequency *f*2. Now bandwidth of the amplifier, $BW = f2 - f1$. The reader may wonder, then, what distinguishes atuned amplifier from other amplifiers? The difference is that tuned amplifiers are designed to have specific, usually narrow bandwidth. This point is illustrated in in Fig.5.2. Note that *BWS* is the bandwidth of standard frequency response while *BWT* is the bandwidth of the tuned amplifier. In many applications, the narrower the bandwidth of a tuned amplifier, the better it is.

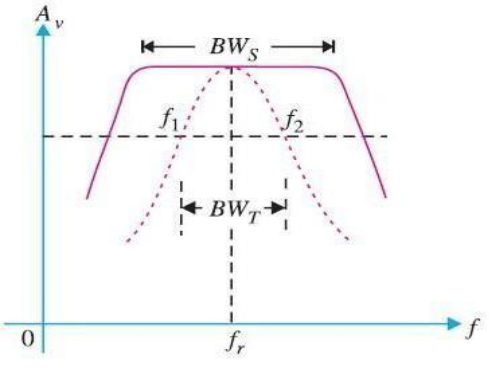


Fig.5.2

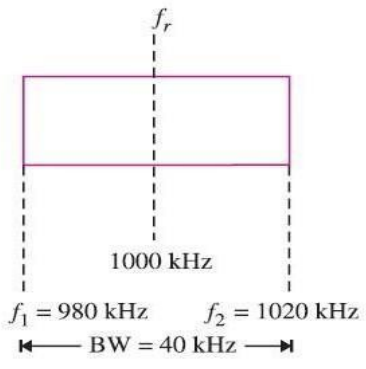


Fig.5.3

Illustration. Consider a tuned amplifier that is designed to amplify only those frequencies that are within ± 20 kHz of the central frequency of 1000 kHz (*i.e.*, *fr* = 1000 kHz). Here [See Fig. 5.3], *f*1 = 980 kHz, *fr* = 1000 kHz, *f*2 = 1020 kHz, *BW* = 40 kHz
This means that so long as the input signal is within the range of 980 – 1020 kHz, it will be amplified. If the frequency of input signal goes out of this range, amplification will be drastically reduced.

Analysis of Parallel Tuned Circuit

A parallel tuned circuit consists of a capacitor *C* and inductor *L* in parallel as shown in Fig. 15.4 (*i*).In practice, some resistance *R* is always present with the coil. If an alternating voltage is applied across this parallel circuit, the frequency of oscillations will be that of the applied voltage. However, if the frequency of applied voltage is equal to the natural or resonant frequency of *LC* circuit, then *electrical resonance* will occur. Under such conditions, the impedance of the tuned circuit becomes maximum and the line current is minimum. The circuit then draws just enough energy from a.c. supply necessary to overcome the losses in the resistance *R*.
Parallel resonance. A parallel circuit containing reactive elements (*L* and *C*) is *resonant when the circuit power factor is unity *i.e*. applied voltage and the supply current are in phase. The phasor diagram of the parallel circuit is shown in Fig. 15. 4 (*ii*). The coil current *IL* has two rectangular components *viz* active component *IL* cos □*L* and reactive component *IL* sin w*L*. This parallel circuit will resonate when the circuit power factor is unity. This is possible only when the net reactive component of the circuit current is zero *i.e*.

$$I_C - I_L \sin \phi_L = 0$$
$$I_C = I_L \sin \phi_L$$

Resonance in parallel circuit can be obtained by changing the supply frequency. At some frequency *fr* (called resonant frequency), *IC* = *IL* sin w*L* and resonance occurs.
Resonant frequency. The frequency at which parallel resonance occurs (*i.e*. reactive component of circuit current becomes zero) is called the *resonant frequency fr*.

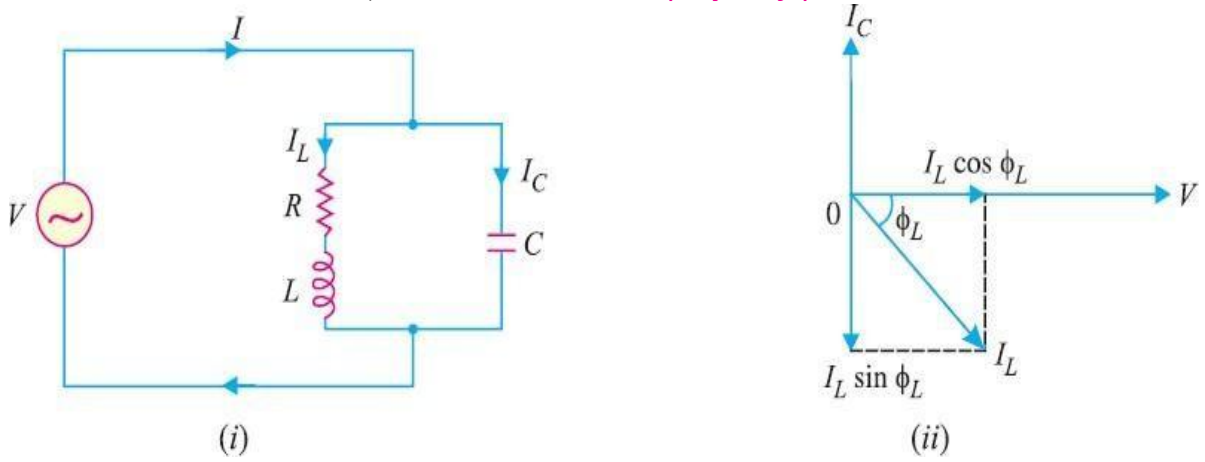


Fig. 5.4

At parallel resonance, we have, $I_C = I_L \sin \phi_L$

Now $I_L = V/Z_L$; $\sin \phi_L = X_L/Z_L$ and $I_C = V/X_C$

$$\therefore \quad \frac{V}{X_C} = \frac{V}{Z_L} \times \frac{X_L}{Z_L}$$

$$\text{or} \quad X_L X_C = Z_L^2$$

$$\text{or} \quad \frac{\omega L}{\omega C} = Z_L^2 = R^2 + X_L^2 \qquad ...(i)$$

$$\text{or} \quad \frac{L}{C} = R^2 + (2\pi f_r L)^2$$

$$\text{or} \quad (2\pi f_r L)^2 = \frac{L}{C} - R^2$$

$$\text{or} \quad 2\pi f_r L = \sqrt{\frac{L}{C} - R^2}$$

$$\text{or} \quad f_r = \frac{1}{2\pi L}\sqrt{\frac{L}{C} - R^2}$$

$$\therefore \quad \text{Resonant frequency, } f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}} \qquad ...(ii)$$

If coil resistance R is small (as is generally the case), then,

$$f_r = \frac{1}{2\pi\sqrt{L\,C}} \qquad ...(iii)$$

The resonant frequency will be in Hz if R, L and C are in ohms, henry and farad respectively.

Note. If in the problem, the value of R is given, then eq. (*ii*) should be used to find *fr*. However, if R is not given, then eq. (*iii*) may be used to find *fr*.

15.4 Characteristics of Parallel Resonant Circuit

It is now desirable to discuss some important characteristics of parallel resonant circuit.

(i) Impedance of tuned circuit. The impedance offered by the parallel *LC* circuit is given by the supply voltage divided by the line current *i.e.*, *V*/*I*. Since at resonance, line current is minimum, therefore, impedance is maximum at resonant frequency. This fact is shown by the impedance-frequency curve of Fig 5.5. It is clear from impedance-frequency curve that impedance rises to a steep peak at resonant frequency *fr*. However, the impedance of the circuit decreases rapidly when the frequency is changed above or below the resonant frequency. This characteristic of parallel tuned circuit provides it the selective properties *i.e.* to select the resonant frequency and reject all others.

Line current, $I = I_L \cos \phi_L$

$$\text{or} \quad \frac{V}{Z_r} = \frac{V}{Z_L} \times \frac{R}{Z_L}$$

$$\text{or} \quad \frac{1}{Z_r} = \frac{R}{Z_L^2}$$

$$\text{or} \quad \frac{1}{Z_r} = \frac{R}{L/C} = \frac{C\,R}{L}$$

$$\left[\because \; Z_L^2 = \frac{L}{C} \text{ from eq. } (i)\right]$$

$$\therefore \quad \text{Circuit impedance, } Z_r = \frac{L}{C\,R}$$

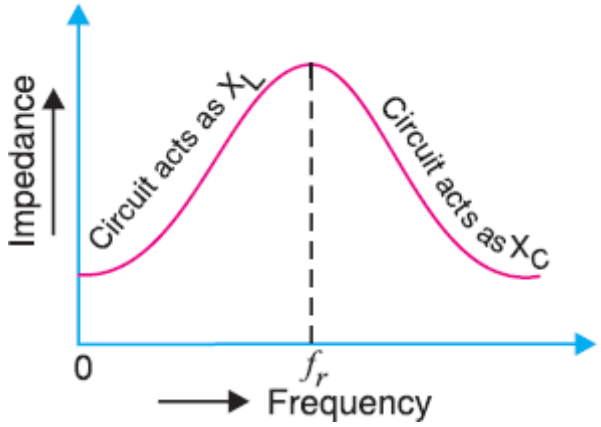


Fig. 5.5

Thus at parallel resonance, the circuit impedance is equal to *L/CR. It may be noted that Zr will be in ohms if R, L and C are measured in ohms, henry and farad respectively.

(ii) Circuit Current. At parallel resonance, the circuit or line current I is given by the applied voltage divided by the circuit impedance Zr *i.e.*,

$$\text{Line current, } I = \frac{V}{Z_r} \qquad \text{where } Z_r = \frac{L}{C\,R}$$

Because Zr is very high, the line current I will be very small.

Quality factor Q. It is desired that resonance curve of a parallel tuned circuit should be as sharp as possible in order to provide selectivity. The sharp resonance curve means that impedance falls rapidly as the frequency is varied from the resonant frequency. The smaller the resistance of coil, the more sharp is the resonance curve. This is due to the fact that a small resistance consumes less power and draws a relatively small line current. The ratio of inductive reactance and resistance of the coil at resonance, therefore, becomes a measure of the quality of the tuned circuit. This is called *quality factor* and may be defined as under :

The ratio of inductive reactance of the coil at resonance to its resistance is known as ****quality factor Q** *i.e.*,

$$Q = \frac{X_L}{R} = \frac{2\pi f_r L}{R}$$

The quality factor Q of a parallel tuned circuit is very important because the sharpness of resonance curve and hence selectivity of the circuit depends upon it. The higher the value of Q, the more selective is the tuned circuit. Fig. 5.6 shows the effect of resistance R of the coil on the sharpness of the resonance curve. It is clear that when the resistance is small, the resonance curve is very sharp. However, if the coil has large resistance, the resonance curve is less sharp. It may be emphasised that where high selectivity is desired, the value of Q should be very large.

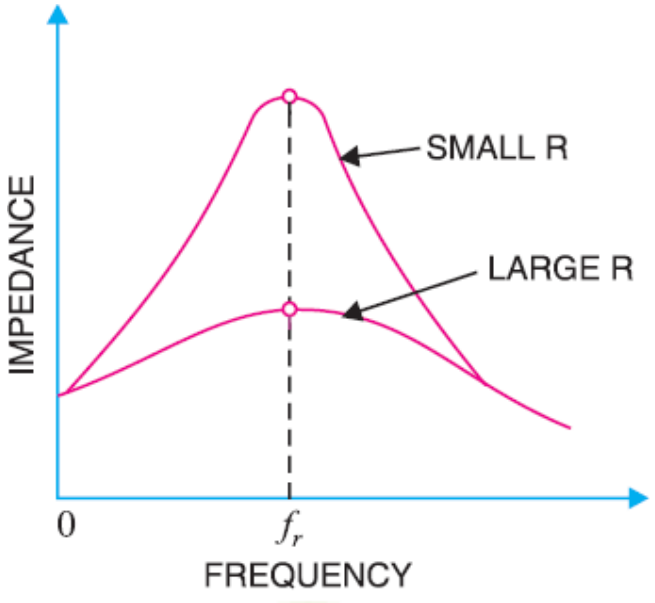


Fig. 5.6

Two things are worth noting. First, *Zr* (= *L*/*CR*) is a pure resistance because there is no frequency term present. Secondly, the value of *Zr* is very high because the ratio *L*/*C* is very large at parallel resonance.

** Strictly speaking, the *Q* of a tank circuit is defined as the ratio of the energy stored in the circuit to the energy lost in the circuit *i.e.*,

$$Q = \frac{\text{Energy stored}}{\text{Energy lost}} = \frac{\text{Reactive Power}}{\text{Resistive Power}} = \frac{I_L^2 X_L}{I_L^2 R} \quad \text{or} \quad Q = \frac{X_L}{R}$$

Example 5.1. A parallel resonant circuit has a capacitor of 250pF in one branch and inductance of 1.25mH plus a resistance of 10ohm in the parallel branch. Find (i) resonant frequency (ii) impedance of the circuit at resonance (iii) Q-factor of the circuit.

Solution.

$R = 10\Omega\,; L = 1.25 \times 10^{-3}$H; $C = 250 \times 10^{-12}$ F **Fig. 15.6**

(*i*) Resonant frequency of the circuit is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{1.25 \times 10^{-3} \times 250} - \frac{10^2}{(1.25 \times 10^{-3})^2}} \text{ Hz}$$

$$= 284.7 \times 10^3 \text{ Hz} = \mathbf{284.7\ kHz}$$

(*ii*) Impedance of the circuit at resonance is

$$Z_r = \frac{L}{C\,R} = \frac{1.25 \times 10^{-3}}{250 \times 10^{-12} \times 10} = 500 \times 10^3\ \Omega$$

$$= \mathbf{500\ k\Omega}$$

(*iii*) Quality factor of the circuit is

$$Q = \frac{2\pi f_r L}{R} = \frac{2\pi (284.7 \times 10^3) \times 1.25 \times 10^{-3}}{10} = \mathbf{223.6}$$

Example 5.2. A parallel resonant circuit has a capacitor of 100 pF in one branch and inductance of 100 μH plus a resistance of 10 ohm in parallel branch. If the supply voltage is 10 V, calculate (i) resonant frequency (ii) impedance of the circuit and line current at resonance.

Solution.

$R = 10\ \Omega, L = 100 \times 10^{-6}$ H ; $C = 100 \times 10^{-12}$ F

(i) Resonant frequency of the circuit is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{100 \times 10^{-6} \times 100} - \frac{10^2}{(100 \times 10^{-6})^2}}\ \text{Hz}$$

$$= 1592.28 \times 10^3\ \text{Hz} = \mathbf{1592.28\ kHz}$$

(ii) Impedance of the circuit at resonance is

$$Z_r = \frac{L}{C\,R} = \frac{L}{C} \times \frac{1}{R} = \frac{100 \times 10^{-6}}{100 \times 10^{-12}} \times \frac{1}{R}$$

$$= 10^6 \times \frac{1}{R} = 10^6 \times \frac{1}{10} = 10^5\ \Omega = \mathbf{0.1\ M\Omega}$$

Note that the circuit impedance *Zr* is very high at resonance. It is because the ratio *L*/*C* is very large at resonance.Line current at resonance is

$$I = \frac{V}{Z_r} = \frac{10\ \text{V}}{10^5\ \Omega} = \mathbf{100\ \mu A}$$

Example 5.3. The *dynamic impedance of a parallel resonant circuit is 500 k□ The circuit consists of a 250 pF capacitor in parallel with a coil of resistance 10ohm. Calculate (i) the coil inductance (ii) the resonant frequency and (iii) Q-factor of the circuit.

Solution.

(i) Dynamic impedance, $Z_r = \frac{L}{CR}$

$\therefore$ Inductance of coil, $L = Z_r CR = (500 \times 10^3) \times (250 \times 10^{-12}) \times 10$

$= 1.25 \times 10^{-3}$ H $= \mathbf{1.25\ mH}$

(ii) Resonant frequency, $f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$

$$= \frac{1}{2\pi}\sqrt{\frac{10^{12}}{1.25 \times 10^{-3} \times 250} - \frac{10^2}{(1.25 \times 10^{-3})^2}}$$

$= 284.7 \times 10^3$ Hz $= \mathbf{284.7\ kHz}$

(iii) Q-factor of the circuit $= \frac{2\pi f_r L}{R} = \frac{2\pi \times (284.7 \times 10^3) \times (1.25 \times 10^{-3})}{10} = \mathbf{223.6}$

Frequency Response of Tuned Amplifier

The voltage gain of an amplifier depends upon □ , input impedance and effective collector load. In a tuned amplifier, tuned circuit is used in the collector. Therefore, voltage gain of such an amplifier is given by :

$$\text{Voltage gain} = \frac{\beta Z_C}{Z_{in}}$$

where *ZC* = effective collector load
Zin = input impedance of the amplifier
The value of *ZC* and hence gain strongly depends upon frequency in the tuned amplifier. As *ZC* is maximum at resonant frequency, therefore, voltage gain will be maximum at this frequency. The value of *ZC* and gain decrease as the frequency is varied above and below the resonant frequency. Fig. 5.7 shows the frequency response of a tuned amplifier. It is clear that voltage gain is maximum at resonant frequency and falls off as the frequency is varied in either direction from resonance.

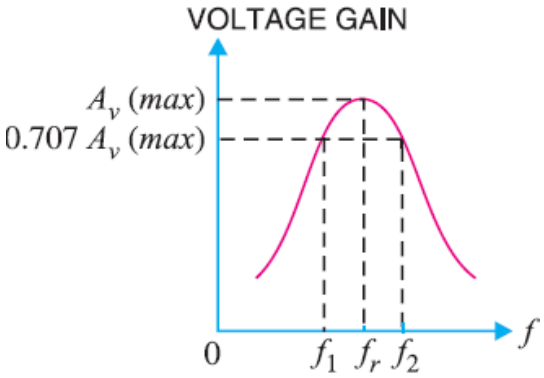


Fig.5.7

Bandwidth. The range of frequencies at which the voltage gain of the tuned amplifier falls to 70.7 % of the maximum gain is called its *bandwidth*. Referring to Fig. 15.7, the bandwidth of tuned amplifier is $f1 - f2$. The amplifier will amplify nicely any signal in this frequency range. The bandwidth of tuned amplifier depends upon the value of *Q* of *LC* circuit *i.e.* upon the sharpness of the frequency response. The greater the value of *Q* of tuned circuit, the lesser is the bandwidth of the amplifier and *vice-versa*. In practice, the value of *Q* of *LC* circuit is made such so as to permit the amplification of desired narrow band of high frequencies. The practical importance of bandwidth of tuned amplifiers is found in communication system. In radio and TV transmission, a very high frequency wave, called *carrier wave* is used to carry the audio or picture signal. In radio transmission, the audio signal has a frequency range of 10 kHz. If the carrier wave frequency is 710 kHz, then the resultant radio wave has a frequency range *between (710 –5) kHz and (710 +5) kHz. Consequently, the tuned amplifier must have a bandwidth of 705 kHz to 715 kHz (*i.e.* 10 kHz). The *Q* of the tuned circuit should be such that bandwidth of the amplifier lies in this range.

Relation between Q and Bandwidth

The quality factor *Q* of a tuned amplifier is equal to the ratio of resonant frequency (*fr*) to bandwidth (*BW*) *i.e.*,

$$Q = \frac{f_r}{BW}$$

The *Q* of an amplifier is determined by the circuit component values. It may be noted here that *Q* of a tuned amplifier is generally greater than 10. When this condition is met, the resonant frequency at parallel resonance is approximately given by:

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Example 5.4. The Q of a tuned amplifier is 60. If the resonant frequency for the amplifier is 1200 kHz, find (i) bandwidth and (ii) cut-off frequencies.

Solution.

$$(i) \qquad BW = \frac{f_r}{Q} = \frac{1200 \text{ kHz}}{60} = \mathbf{20 \text{ kHz}}$$

$$(ii) \qquad \text{Lower cut-off frequency, } f_1 = 1200 - 10 = \mathbf{1190 \text{ kHz}}$$

$$\text{Upper cut-off frequency, } f_2 = 1200 + 10 = \mathbf{1210 \text{ kHz}}$$

Example 5.5. A tuned amplifier has maximum voltage gain at a frequency of 2 MHz and the bandwidth is 50 kHz. Find the Q factor.

Solution. The maximum voltage gain occurs at the resonant frequency. Therefore, fr = 2 MHz = 2×10^6 Hz and BW = 50 kHz = 50×10^3 Hz.

Now

$$BW = \frac{f_r}{Q}$$

$$Q = \frac{f_r}{BW} = \frac{2 \times 10^6}{50 \times 10^3} = \mathbf{40}$$

Example 5.6. Draw the frequency response of an ideal tuned amplifier and discuss its characteristics.

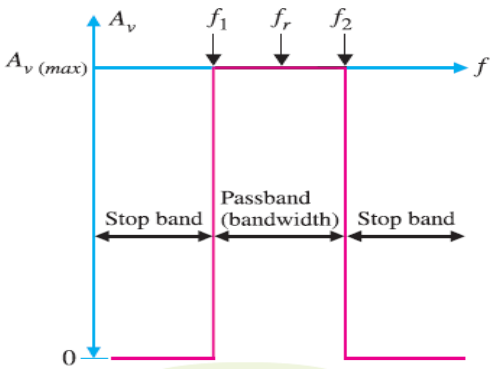


Fig.5.8

Solution. Fig. 5.8 shows the frequency response of an ideal tuned amplifier. The ideal tuned amplifier has zero gain for all frequencies from 0 Hz up to the lower cut-off frequency *f1*. At this point, the gain *instantly* jumps to the maximum value [*Av* (*max*)]. The gain stays at the maximum value until *f*2 is reached. At this time, the gain *instantly* drops back to zero. Thus all the frequencies within the bandwidth (*f*1 to *f*2) of the amplifier would be *passed* by the circuit while all others would be effectively stopped. This is where the terms *pass band* and *stop band* come from. The pass band is the range of frequencies that is passed (amplified) by a tuned amplifier.

On the other hand, the stop band is the range of frequencies that is outside the amplifier‘s pass band. In practice, the ideal characteristics of the tuned amplifier cannot be achieved. In a practical frequency response (refer back to Fig. 5.7), the gain falls gradually from maximum value as the frequency goes outside the *f*1 or *f*2 limits. However, the closer the frequency response of a tuned amplifier to that of the ideal, the better.

Single Tuned Amplifier

A single tuned amplifier consists of a transistor amplifier containing a parallel tuned circuit as the collector load. The values of capacitance and inductance of the tuned circuit are so selected that its resonant frequency is equal to the frequency to be amplified. The output from a single tuned amplifier can be obtained either (*a*) by a coupling capacitor *CC* or (*b*) by a secondary coil

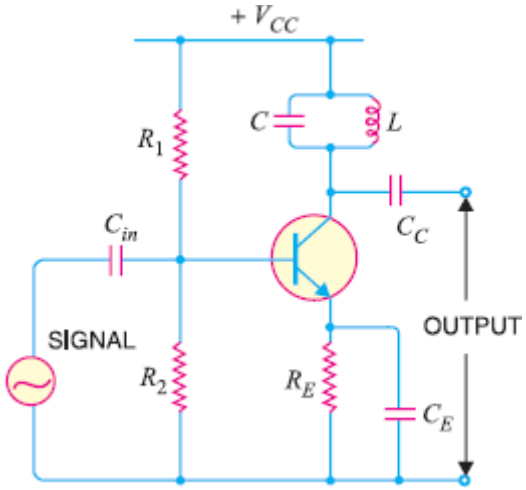


Fig.5.9 Capacitive coupled single tuned amplifier

Operation. The high frequency signal to be amplified is given to the input of the amplifier. The resonant frequency of parallel tuned circuit is made equal to the frequency of the signal by changing the value of *C*. Under such conditions, the tuned circuit will offer very high impedance to the signal frequency. Hence a large output appears across the tuned circuit. In case the input signal is complex containing many frequencies, only that frequency which corresponds to the resonant frequency of the tuned circuit will be amplified. All other frequencies will be rejected by the tuned circuit. In this way, a tuned amplifier selects and amplifies the desired frequency.

. The fundamental difference between *AF* and tuned (*RF*) amplifiers is the bandwidth they are expected to amplify. The *AF* amplifiers amplify a major portion of *AF* specturm (20 Hz to 20 kHz) equally well throughout. The tuned amplifiers amplify a relatively narrow portion of *RF* spectrum, rejecting all other frequencies L, C tuned circuit is not connected between collector and ground because, the transistor will be short circuited at some frequency other than resonant frequency. The output of the tuned circuit is coupled to the next stage or output device, through capacitor Cb. So this circuit is called single tuned capacitbe coupled amplifier. RI, R2, RE, CE are biasing resistors and capacitors. The tuned circuit formed by Inductance (L) and capacitor (C) resonates at the frequency of operation. Transistor hybrid equivalent circuit must be used since the transistor is operated at high frequencies. Tuned circuits are high frequency circuits. Rj = input resistance of the next stage.

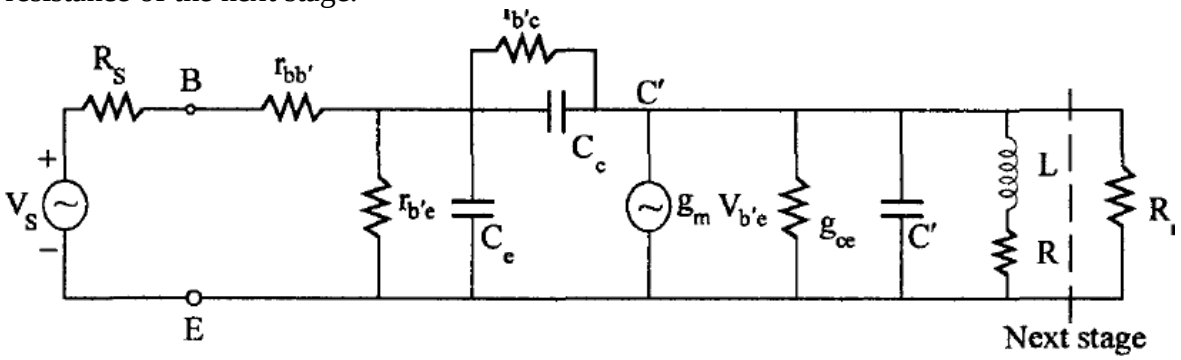


Fig. 5.10 Equivalent circuit

Modified equivalent circuit using Miller's Theorem.

According to Miller's theorem, the feedback capacitance Cc is Cc (1 - A) on the input side and $C_C\left(\frac{A-1}{A}\right)$ on the output side. But where as resistance is $\frac{r_{b'c}}{(1-A)}$ on the input side $\frac{r_{b'c}}{\left(\frac{A-1}{A}\right)}$ on the output side.

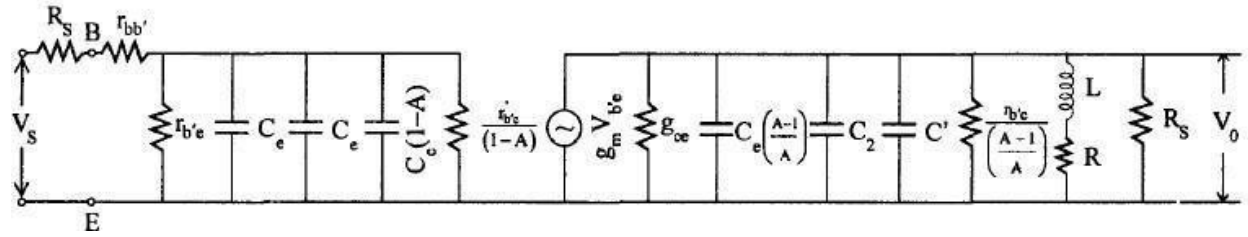


Fig. 5.11 Equivalent circuit (applying Miller's Theorem)

The equivalent circuit after simplification, neglecting $\frac{r_{b'c}}{\left(\frac{A-1}{A}\right)}$ is shown in Fig. 5.12.

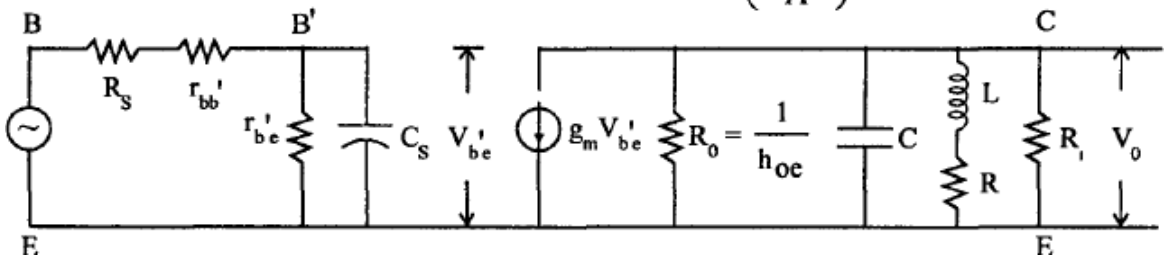


Fig. 5.12 Simplified equivalent circuit

$$Y_i = \frac{1}{R + j\omega L} = \frac{R - j\omega L}{R^2 + \omega^2 L^2} = \frac{R}{R^2 + \omega^2 L^2} - j\frac{\omega L}{R^2 + \omega^2 L^2}$$

Input admittance as seen by II stage.

Instead of L and R being in series, they are being represented as equivalent shunt element~ Rp and Lp for parallel

$$= \frac{1}{R_P} + \frac{1}{j\omega L_P}$$

$$R_P = \frac{R^2 + \omega^2 L^2}{R}$$

$$L_P = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$$

Inductor is represented by Rp in series with inductance Lp.

Q at resonance,

$$Q_0 = \frac{\omega_0 L}{R}$$

$$\omega L >> R$$

$$R_P = \frac{\omega^2 L^2}{R}$$

$$L_P = L$$

.: Resistance of the inductor R is small, neglecting R^2 compared to $^2L^2$.

Therefore output circuit is simplified to,

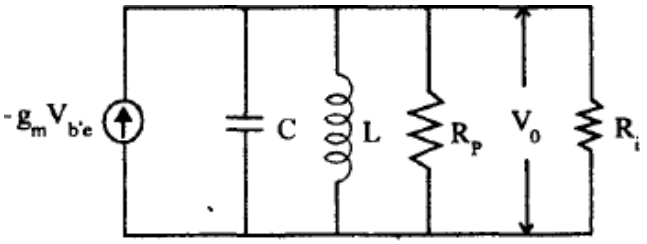


Fig. 5.13 Simplified circuit

$$\frac{1}{R_t} = \frac{1}{R} + \frac{1}{R_P} + \frac{1}{R_i}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

R_i is the input Fesistance of the next stage

$$Q_e = \frac{\text{Suspectance of L or capacitance of C}}{\text{Conductance of shunt resistance } R_t}$$

R_t = resistance of tuned circuit

$$Q_e = \omega_0 C R_t$$

$$= \frac{R_t}{\omega_0 L} \frac{(1/\omega_0 L)}{1/R_t} = \left(\frac{\omega_0 C}{1/R_t}\right)$$

□ □□□ be the resonant angular frequency in rad/sec.

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Output voltage Vo = -gm Vb'e·Z (-gm Vb'e is the current source). where Z is the impedance of C, Land Rt in parallel.

Admittance

$$Y = \frac{1}{Z} = \frac{1}{R_t} + \frac{1}{j\omega L} + j\omega C$$

$$Y = \frac{1}{R_t}\left[1 + \frac{R_t}{j\omega L} + j\omega C R_t\right]$$

$$= \frac{1}{R_t}\left[1 + j\frac{\omega_0 \omega C R_t}{\omega_0} + \frac{R_t \omega_0}{j\omega_0 \omega L}\right] \text{ (Multiplying and dividing by } \omega_0)$$

$$Y = \frac{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}{R_t} \qquad (\because \quad Q_e = \frac{R_t}{w_0 L} = \omega_0 C R_t)$$

$$Q_e = \omega_0 C R_t$$

$$= \frac{R_t}{\omega_0 L} \qquad \because \quad \omega_0 L = \frac{1}{\omega_0 C}$$

$$Z = \frac{R_t}{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}$$

Qe is defined as

$$\frac{\text{Susceptance of L or C}}{\text{Conductance of shunt resistance } R_t}$$

$$\delta = \frac{\omega - \omega_0}{\omega_0} = \frac{\omega}{\omega_0} - 1$$

$$\frac{\omega}{\omega_0} = 1 + \delta$$

Rewriting the expression for Z, as

$$Z = \frac{R_t}{1 + jQ_e\left[(1+\delta) - \frac{1}{(1+\delta)}\right]}$$

$$= \frac{X + \delta^2 + 2\delta - X}{1+\delta} = \frac{2\delta\left(1 + \frac{\delta}{2}\right)}{1+\delta}$$

$$Z = \frac{R_t}{1 + j2Q_e\delta\left[\frac{1+\delta/2}{1+\delta}\right]}$$

If the frequency □ is close to resonant frequency □0,□ « 1.

Therefore Simplified expression for Z is

$$Z = \frac{R_t}{1 + j2Q_e\delta}$$

$$R_p = Q_0^2 R = Q_0 = \sqrt{\frac{L}{C}} = \omega_0 L Q_0$$

$$V_{b'e} = V_i \cdot \frac{r_{b'e}}{r_{bb'} + r_{b'e}}$$

$$V_0 = -g_m V_{be} \cdot Z$$

$$V_0 = -g_m V_i \cdot \frac{r_{b'e}}{r_{b'e} + r_{b'e}} Z$$

$$A = \frac{V_0}{V_i} = -g_m \cdot \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \cdot Z$$

$$A = -g_m \cdot \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \cdot \frac{R_t}{1 + j2\delta Q_e}$$

voltage gain at resonance. Since at resonance w0 = 0

$$A_{reso} = \frac{-g_m \cdot r_{b'e}}{r_{b'e} + r_{bb'}} \cdot R_t$$

$$\frac{A}{A_{reso}} = \frac{1}{1 + j2\delta Q_e}$$

Magnitude

$$\left|\frac{A}{A_{reso}}\right| = \frac{1}{\sqrt{1 + (2\delta Q_e)^2}}$$

Phase angle

$$\left|\frac{A}{A_{reso}}\right| = -\tan^{-1}(2\,\delta\,Q_e)$$

At a frequency □ 1 below the resonant frequency □ has the value

$$= -\frac{1}{2Q_e};$$

$$\frac{A}{A_{reso}} = \frac{1}{\sqrt{2}} = 0.707$$

□ 1 is the lower 3db frequency. Similarly □ 2, the upper 3db frequency is

$$\delta = +\frac{1}{2Q_e};\ \frac{A}{A_{reso}} = \frac{1}{\sqrt{2}} = 0.707$$

The 3 db band width □ = (□ 2- □ 1l)

$$= \frac{[(\omega_2 - \omega_0) + (\omega_0 - \omega_1)] \cdot \omega_0}{\omega_0}$$

$$= [\delta + \delta]\,\omega_0 \quad = 2\,\delta\,\omega_0$$

$$\delta = \frac{1}{2Q_e}$$

$$\Delta\omega = \frac{\omega_0}{Q_e} = \frac{\omega_0}{R_t \omega_0 C} = \frac{1}{R_t C} \quad \text{rad/sec.}$$

Tapped Single Tuned Capacitance Coupled Amplifier:

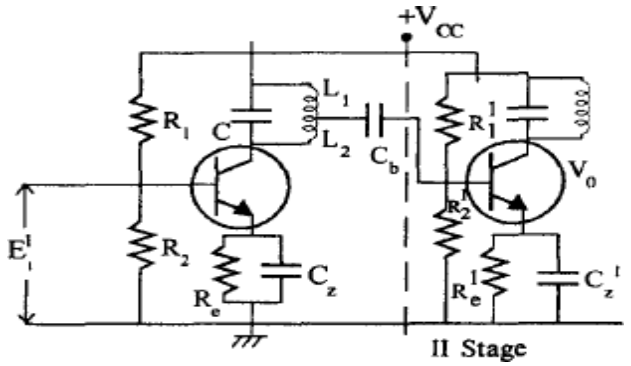
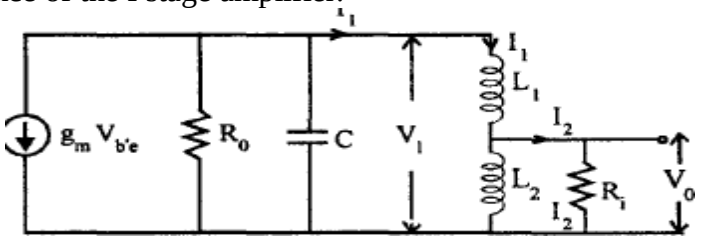


Fig. 5.7 Tapped single tuned capacitive coupled amplifier circuit

5.3.1 Equivalent Circuit on the Output Side of the I Stage

RI is the input resistance of the II stage.

Ro is the output resistance of the I stage amplifier.



The input IZI of the common emitter amplifier circuits will be less. So the output impedance of the circuit being coupled to one common emitter amplifier, should also have low IZI for impedance matching and to get maximum power transfer. So in order to reduce the impedance of the LC resonant circuit, to match the low IZI of the common emitter circuit, tapping is made in the LC tuned circuit. Tapped single tuned circuits are used in such applications. 5.3.2 Expression for 'Inductance' for Maximum Power Transfer Let the tapping point divide the impedance into two parts LI and L2.

Let LI = nL so that L2 = (1 - n) Writing Kirchoff's Voltage Law (KVL)

Where M is the mutual inductance between LI and L2. Solving equations 1 and 2,

$$V_1 = j\omega L \cdot I_1 - j\omega (L_2 + M) I_2 \qquad \text{.....(1)}$$

$$0 = -j\omega (L_1 + M) I_1 + (R_i + j\omega L_2) I_2 \qquad \text{.....(2)}$$

$$I_1 = \frac{V_1 (R_i + j\omega L_2)}{j\omega L (R_i + j\omega L_2) + \omega^2 (L_2 + M)^2}$$

Hence the IZI offered by the coil along with input resistance ~i of the next stage is

$$Z_1 = \frac{V_1}{I_1} = \frac{j\omega L\left(R_i + j\omega L_2\right) + \omega^2\left(L_2 + M\right)^2}{\left(R_i + j\omega L_2\right)}$$

$$= j\omega L + \frac{\omega^2\left(L_2 + M\right)^2}{R_i + j\omega L_2}$$

But wL2 much less than Ri.
As Ri, the input resistance of transistor circuit II stage is KQ and much greater than roL2

$$Z_1 = j\omega L + \frac{\omega^2\left(L_2 + M\right)^2}{R_i}$$

$M = K\sqrt{L_1 L_2}$ M = Mutual Inductance

Where K is the coefficient of coupling. Since Ll = nL, L2 = (l-n)L

$$= K\sqrt{nL(1-n)L} = KL\sqrt{\left(n - n^2\right)}$$

Putting K = I, we get

$$M \simeq L\sqrt{n - n^2}$$

$$Z_1 \simeq j\omega L \pm \frac{\omega^2\left[(1-n)L + L\sqrt{n - n^2}\right]^2}{R_i}$$

The resistance effectively reflected in series with the coil due to the resistance R, is given by,

$$R_{is} \simeq \frac{\omega^2 L^2\left[(1-n) + \sqrt{n - n^2}\right]^2}{R_i}$$

This is the resistance component; $: series, i : input
This resistance R is in series with the coil L may be equated to a resistance Rip in shunt with the coil where Rip is given by, ~

$$R_{ip} = (\omega L)^2 / R_{is}$$

So the equivalent circuit is

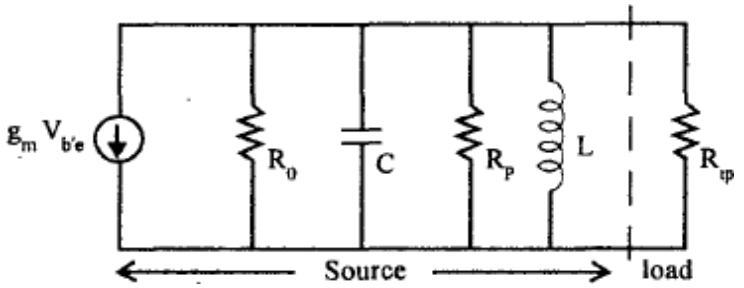


Fig. 5.9 Equivalent circuit

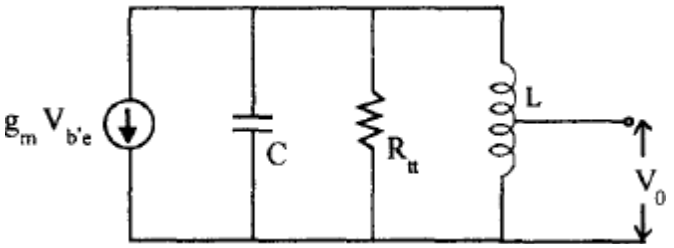


Fig. 5.10 Equivalent circuit after simplification

$$\frac{1}{R_{tt}} = \frac{1}{R_0} + \frac{1}{R_p} + \frac{1}{R_{ip}}$$

$$Q_e = \frac{R_{tt}}{\omega_0 L}$$

Rtt : tuned tapped circuit.

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Under the conditions of maximum power transfer theorem, the total resistance appearing in shunt with the coil is = Rop

Since it is a resonant circuit, at resonance, the IZI in purely resistive. For maximum power transfer IZI = R/2.

$$Q_e = \frac{R_{op}/2}{\omega_0 L}; \quad R_{tt} = R_{op}/2$$

$$R_{op} = 2\, Q_e .\, \omega_0\, L$$

$$R_{op} = \frac{R_0 R_p}{R_0 + R_p}$$

$$2\, Q_e\, \omega_0\, L = \frac{R_0\, \omega_0\, Q_0\, L}{R_0 + \omega_0\, Q_0\, L}$$

$$L = \frac{R_0 (Q_0 - 2Q_e)}{2\omega_0 Q_0 Q_e}$$

$$L = \frac{R_0}{\omega_0}\left[\frac{1}{2Q_e} - \frac{1}{Q_0}\right]$$

This is the value of L for maximum power transfer.

Expression for voltage gain and Bandwidth are determined in the same way as done for a single tuned circuit. In this circuit we have,

1. R_{tt} instead of ~ (as in single tuned) tapped tuned circuit.

2. Output voltage equals (l - n) times the voltage developed across the complete coil. IZI at any frequency close to Wo is given by,

$$Z = \frac{R_{tt}}{1 + j\,2\delta\,Q_e}$$

$$V_0 = \frac{-g_m V_i\, r_{b'e}}{r_{b'e} + r_{bb'}} \cdot Z\,(1 - n)$$

$$A = \frac{V_0}{V_i} = -g_m (1-n) \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \cdot Z$$

$$= -g_m\,(1 - n).\frac{r_{b'e}}{r_{b'e} + r_{bb'}} \cdot \frac{R_{tt}}{1 + j\,2\delta Q_e}$$

At resonance, voltage gain is

$$A_{reso} = -\,g_m\,(1 - n)\,.\,\frac{r_{b'e}}{r_{b'e} + r_{bb'}}\,.\,R_{tt}$$

$$\frac{A}{A_{reso}} = \frac{1}{1 - j\,2\delta Q_e}$$

Inductive coupled single tuned amplifier

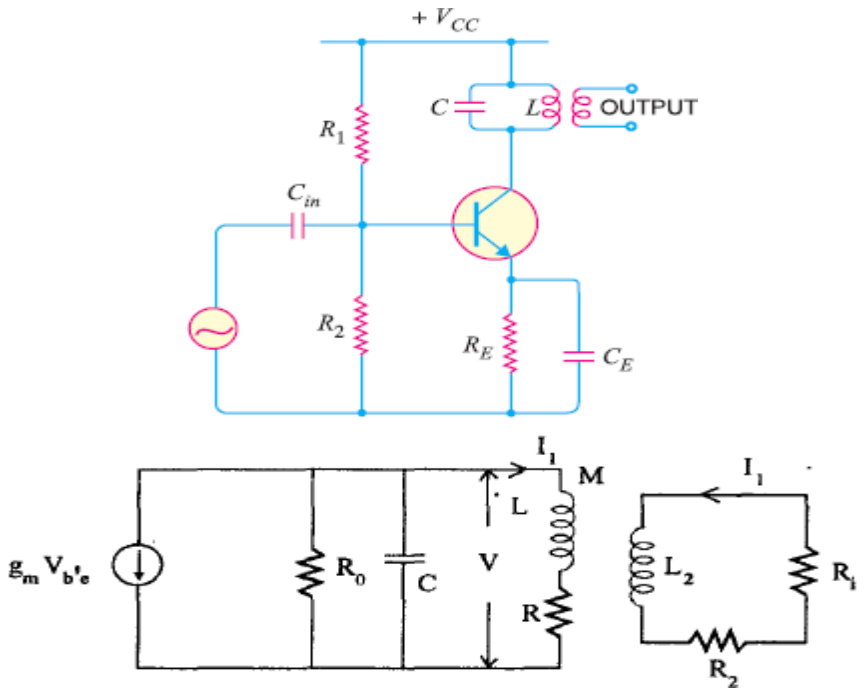


Fig. 5.11 Inductive coupled amplifier circuit (a) and its equivalent (b)

in this circuit, the voltage developed across the tuned circuit is inductively coupled to the next stage. Coil L, of the tuned circuit, and the inductor coupling the voltage to the II stage, L2 form' a transformer with mutual coupling M. This type of circuit is also used, where the input IZI of the II stage is smaller or different from the tuned circuit. SO IZI matching is done by the transformer depending on its tum ratio. In such requirements, this type of circuit is used.

The resistors RI, R2 and R; and R2 are the biasing resistors. The parallel tuned circuit,

Land C resonates at the frequency of operation. Fig. (b) shows output equivalent circuit. Input equivalent circuit will be the same as that of the capacitive coupled circuit. In the output equivalent circuit, C is the total capacitance, including the stray capacitance, Miller equivalent capacitance C (A-1)/A. L2 and R2 are the inductance and resistance of the secondary winding.

5.4.1 Expression for Ll for Maximum Power Transformer Writing KVL to the primary and secondary windings,

$V = I_1 Z_{11} + I_2 Z_{12}$ o $= I_1 Z_{21} + I_2 Z_{22}$

where $Z_{11} = R + jwL$ $Z_{12} = Z_{21} = jwM$

$Z_{22} = R2 + Rj + jwL2$

$$I_1 = \frac{V.Z_{22}}{Z_{11}Z_{22} - Z_{12}^2}$$

The impedance seen looking into the primary is,

$$Z_{in} = \frac{V}{I_1} \frac{Z_{11}Z_{22} - Z_{12}^2}{Z_{22}}$$

$$= Z_{11} - \frac{Z_{12}^2}{Z_{22}}$$

Substituting the values of Zll' Z22 and ZI2 in equation (7) we get,

$$Z_{in} = (R + j\omega L) + \frac{\omega^2 M^2}{R_2 + R_i + j\omega L_2}$$

Rj generally much greater than R2 and wL2.

$$Z_{in} \simeq (R + j\omega L) + \frac{\omega^2 M^2}{R_i}$$

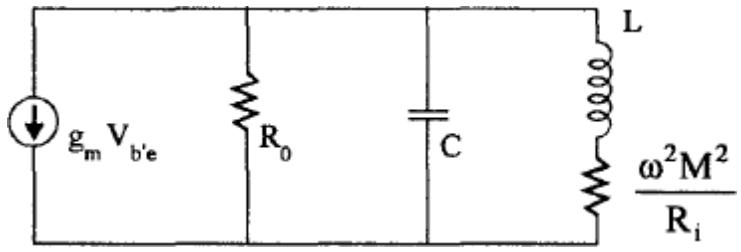


Fig. 5.12 Equivalent circuit

$$\frac{\omega^2 M^2}{R_i}$$

is the impedance of the secondary side reflected to the primary.
If M is reasonably large, then I

$$R << \frac{\omega^2 M^2}{R_i}$$

$$Z_{in} \simeq j\omega L + \frac{\omega^2 M^2}{R_i}$$

The equivalent circuit may be written as,
Inductance L with series resistance may be represented as L in shunt with Rio as R.
shown below, where

$$R_{ip} = \frac{(\omega L)^2}{\left(\frac{\omega^2 M^2}{R_i}\right)} = \left(\frac{L}{M}\right)^2 . R_i$$

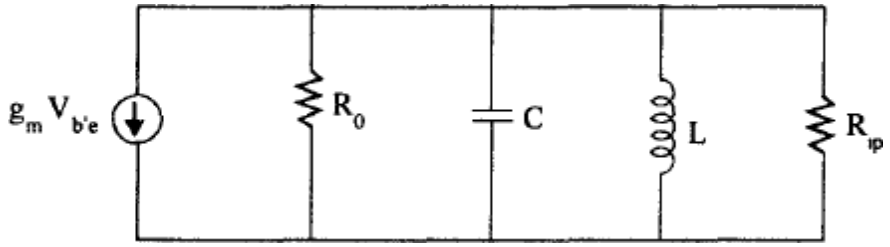


Fig. 5.13 Simplified circuit

$R_{ip} = R_0$

$$R_0 = \left(\frac{L}{M}\right)^2 . R_i$$

gives the value of M for maximum power transfer.

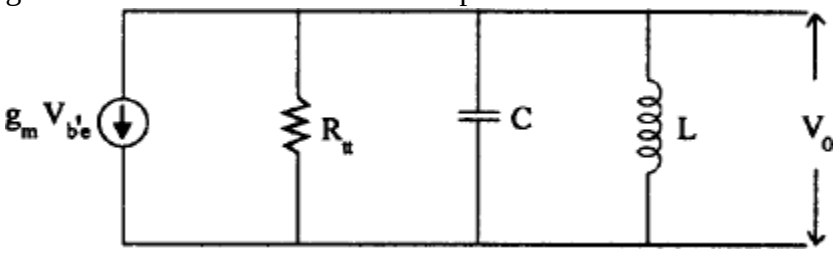


Fig. 5.14 Equivalent circuit
L and L2 are the primary and secondary windings of inductances.

$$M = K\sqrt{LL_2}$$

$$R_0 = \left(\frac{L}{K^2 L_2}\right) R_i$$

Therefore from equation 14, for a given value of Ro and coefficient of coupling K and ~, we can determine L2 for maximum transformer of power.
Shunt resistance Ro and Rip may be combined to yield the total shunt resistance Ru.

$$\frac{1}{R_{tt}} = \frac{1}{R_0} + \frac{1}{R_{ip}}$$

Rtt = Resistance of tapped tuned circuit Effective Q of the entire circuit is,

$$Q_e = \frac{R_{tt}}{\omega_0 L}$$

where Wo is the resonaqt frequency of Land C.

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Under conditions of maximum transfer of power, total resistance appearing in shunt with the coil equals *Ro/2.* Since it is respnant circuit, at resonance, IZI = resistance only.
maximum power, R = Rl2.

$$Q_e = \frac{R_0/2}{\omega_0 L}$$

$$R_0 = 2\, Q_e\, \omega_0\, L$$

$$I_2 = \frac{V.Z_{21}}{Z_{21}.Z_{12} - Z_{11}\, Z_{22}}$$

$$V_0 = -I_2 \,.\, R_i$$

$$= V \,.\, \frac{R_i.Z_{21}}{Z_{11}.Z_{22} - Z_{12}^2}$$

IZI of the output circuit at any frequency 'w' close to _w0' is given by, Impedance of output circuit is

$$Z = \frac{R_{tt}}{1 + j2\delta Q_e}$$

$$V_0 = -\, g_m \,.\, \frac{V_0\, r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, Z \,.\, \frac{R_i\, Z_{21}}{Z_{11}\, Z_{22} - Z_{12}^2}$$

$$= -\, g_m\, V_i \,.\, \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, \frac{R_i.Z_{21}}{Z_{11}\, Z_{22} - Z_{12}^2} \,.\, \frac{R_{tt}}{1 + j2\delta Q_e}$$

Voltage gain A at any frequency wo is,

$$A = \frac{V_0}{V_i} = -\, g_m\, \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, \frac{R_i\, Z_{21}}{Z_{11}\, Z_{22} - Z_{12}^2} \,.\, \frac{R_{tt}}{1 + j2\delta Q_e}$$

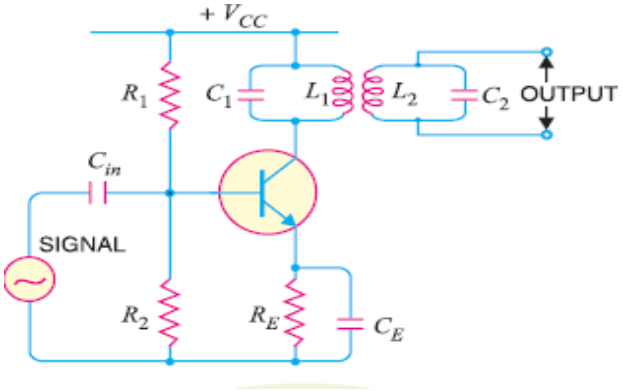
Voltage at resonance,

$$A_{reso} = -g_m \cdot \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \cdot \frac{R_i Z_{22}}{Z_{11} Z_{22} - Z_{12}^2}$$

$$\boxed{\frac{A}{A_{reso}} = \frac{1}{1 + j2\delta Q_e}}$$

Double Tuned Amplifier

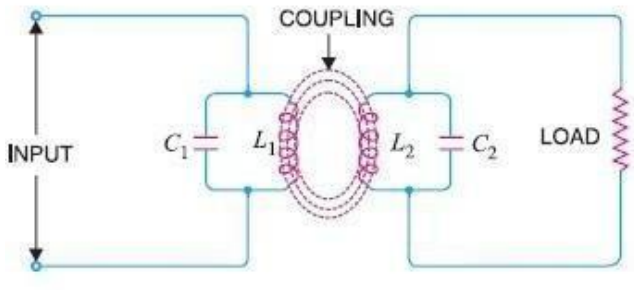
Fig. 15.13 shows the circuit of a double tuned amplifier. It consists of a transistor amplifier containing two tuned circuits ; one ($L1C1$) in the collector and the other ($L2C2$) in the output as



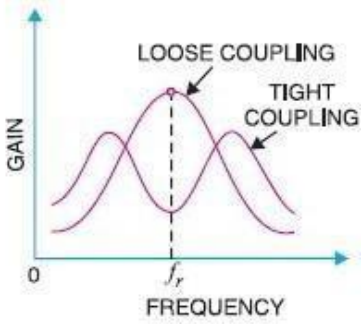
shown. The high frequency signal to be amplified is applied to the input terminals of the amplifier. The resonant frequency of tuned circuit $L1C1$ is made equal to the signal frequency. Under such conditions, the the signal frequency. Consequently, large output appears across the tuned circuit $L1C1$. The output from this tuned circuit is transferred to the second tuned circuit $L2C2$ through mutual induction. Double tuned circuits are extensively used for coupling the various circuits of radio and television receivers.

Frequency response. The frequency response of a double tuned circuit depends upon the degree of coupling *i.e.* upon the amount of mutual inductance between the two tuned circuits. When coil $L2$ is coupled to coil $L1$ [See Fig. 15.14 (*i*)], a portion of load resistance is coupled into the primary tank circuit $L1C1$ and affects the primary circuit in exactly the same manner as though a resistor had been added in series with the primary coil $L1$. When the coils are spaced apart, all the primary coil $L1$ flux will not link the secondary coil $L2$. The coils are said to have *loose coupling*. Under such conditions, the resistance reflected from the load (*i.e.* secondary circuit) is small. The resonance curve will be sharp and the circuit Q is high as shown in Fig. 15.14 (*ii*).

When the primary and secondary coils are very close together, they are said to have *tight coupling*. Under such conditions, the reflected resistance will be large and the circuit Q is lower. Two positions of gain maxima, one above and the other below the resonant frequency, are obtained.



(*i*)



(*ii*)

Bandwidth of Double–Tuned Circuit

If you refer to the frequency response of double-tuned circuit shown in Fig. 15.14 (*ii*), it is clear that bandwidth increases with the degree of coupling. Obviously, the determining factor in a doubletuned circuit is not *Q* but the coupling. For a given frequency, the tighter the coupling, the greater is the bandwidth.

BWdt = k fr

The subscript *dt* is used to indicate double-tuned circuit. Here *k* is coefficient of coupling.

Example 15.8. It is desired to obtain a bandwidth of 200 kHz at an operating frequency of 10 MHz using a double tuned circuit. What value of co-efficient of coupling should be used ?

Solution.

BWdt = k fr

$$\therefore \quad \text{Co-efficient of coupling, } k = \frac{BW_{dt}}{f_r} = \frac{200 \text{ kHz}}{10 \times 10^3 \text{ kHz}} = 0.02$$

Stagger Tuning

Tuned amplifiers have large gain, since at resonance, Z is maximum. So Av is maximum. To get this large Av over a wide range of frequencies, stagger tuned amplifiers are employed. This is done by taking two single tuned circuits of a certain Bandwidth, and displacing or staggering their resonance peaks by an amount equal to their Bandwidth. The resultant staggered pair will have a Bandwidth, $\sqrt{2}$ times as great as that of each of individual pairs.