17333

21718

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Answer ***each*** *next main question on a* ***new*** *page.*
(3) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(4) Figures to the ***right*** *indicate* ***full*** *marks.*
(5) Assume suitable data, if ***necessary****.*

Marks

1. A) Attempt **any six**: **12**

a) State any two advantages and disadvantages of digital circuits.

b) Define Fan-out and Power Dissipation.

c) Draw symbol and truth table of 3-i/p EX-OR gate.

d) Convert $(10110)_2 = (?)_6, (?)_8$.

e) State any four Boolean Laws.

f) Explain the rules to simplify Boolean equation using K-map (any two).

g) Compare RAM and ROM memories (any two point).

h) State two specification of DAC.

B) Attempt **any two**: **8**

a) State and prove DeMorgan's theorem.

b) Perform the following BCD subtraction using 9's complement

i) $(47)_{10} - (31)_{10}$ ii) $(52)_{10} - (67)_{10}$

c) Implement OR and AND gets using NOR gate only.

2. Attempt **any four** of the following: **16**

a) Simplify the following Boolean expression

i) $Y = AB + ABC + \bar{A}B + A\bar{B}C$

ii) $Y = (A + B)(A + \bar{B})(\bar{A} + B)$

b) Subtract the given number using 2's complement

i) $(11011)_2 - (11100)$ ii) $(1010)_2 - (101)_2$

c) Design Half subtracter using K-map.

P.T.O.

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d) Simplify the following equation using K-map and realize it using logic gates
$Y = \sum m\ (1, 5, 7, 9, 11, 13, 15)$.

e) Draw X-OR gate using NAND gate only.

f) Design 1 : 4 demultiplexer using 1 : 2 demultiplexer.

3. Attempt **any four** of the following : **16**

a) Simplify the following expressions using Boolean Laws and De-morgan's theorems.

b) Design 16 : 1 multiplexer using 8 : 1 multiplexer.

c) Describe different types of triggering methods for a flip-flop.

d) Draw and explain 3-bit asynchronous up counter with timing diagram.

e) Minimize the following equation using K-map

i) $F\ (A, B, C, D) = \pi\ M\ (4, 6, 11, 14, 15)$

ii) $F\ (A, B, C, D) = \sum m\ (1, 3, 7, 11, 15) + d\ (0, 2, 5)$

f) Draw block diagram of ALU and describe any four function performed by ALU.

4. Attempt **any four** of the following : **16**

a) Describe working of JK Flip-Flop and write its truth table.

b) Simplify the following equation using K-map and realize it using basic gates only

$F\ (A, B, C, D) = \sum m\ (1, 3, 7, 8, 10, 12, 13, 15)$.

c) Explain the working of EPROM.

d) Draw the circuit diagram of 3-bit R-2R ladder type DAC obtain its only output voltage expression.

e) Define following terms with reference to A/D converters and list any four application of A/D converters.

i) Resolution

ii) Quantization error

f) Design a mod-6 asynchronous counter with truth table and logic diagram.

5. Attempt **any four** of the following : **16**

a) How many flip-flops are required to construct following modulus counters ?

i) 27 ii) 83

iii) 95 iv) 9

b) Draw logic diagram of S-R Flip-Flop with negative edge triggering and write its truth table.

c) Draw BCD to seven segment decoder using IC 7447 and give functions of each pin.

Marks

d) Implement using NOR gates only $Y = (A + B) \cdot (\bar{A} + C)$.

e) Convert the following :

i) $(429)_{10} = (?)_{BCD}$ ii) $(2.45)_{10} = (?)_2$

iii) $(AF)_{16} = (?)_8$ iv) $(1011010)_2 = (?)_{16}$

f) Draw the circuit of Johnsons counter and describe with timing diagram.

6. Attempt **any four** of the following : **16**

a) Explain successive approximation method of ADC with neat diagram.

b) List four application flip-flops.

c) Give classification of memory and compare RAM and ROM (any 2 point).

d) Compare combination circuit and sequential logic circuit (any 4 pts.)

e) With suitable diagram explain the working of ramp type ADC.

f) In Fig. 1, if the 4-bit serial in parallel out right shift resister has the initial contents 0110. After 3 clock pulses are applied what will be the contents of the shift resister ?

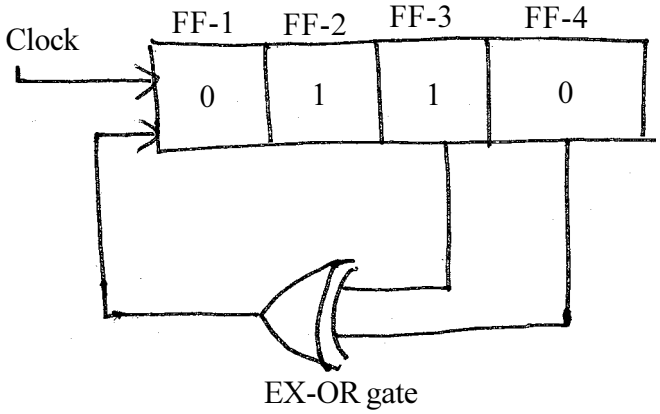

Fig. 1