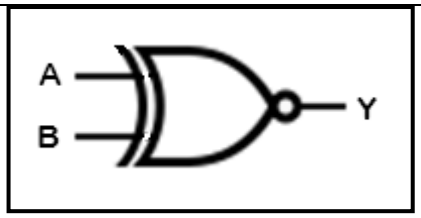
WINTER– 17 EXAMINATION

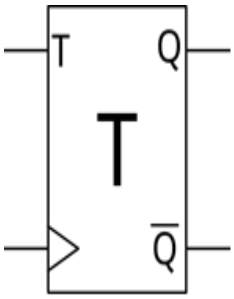
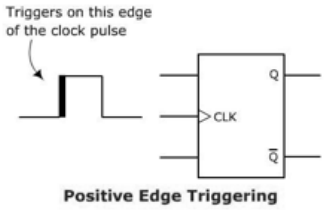
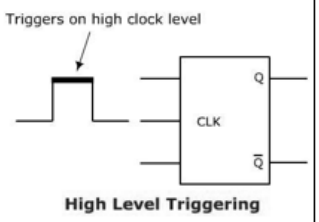
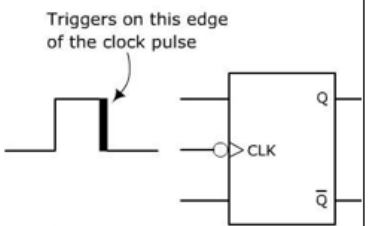
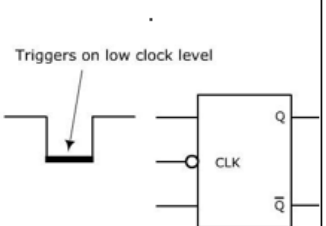
Subject Name: Digital Techniques **Model Answer** **Subject Code:** 17333

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answer	Marking Scheme
1.	(a)	**Attempt any six of the following:**	**12 Marks**
	i)	**List any two advantage and disadvantage of digital circuits.**	**2M**
	Ans:	**Advantages:** • Digital circuits are highly reliable and accurate. • They are small in size and the speed of operation is very high. • Digital ICs can be programmable. • The effect of fluctuations in the characteristics of the components, ageing of components, temperature, and noise etc. is very small in digital circuits. • Digital circuits have capability of memory which makes these circuits highly suitable for computers, calculators, watches, telephones etc. **Disadvantages:** • If there is a loss of digital data in a transmission, there will be error and misinterpretation of data. • All real world signals are analog in nature. So it is necessary to convert these signals into digital to process digitally. This requires additional circuitry	**(Any two Advantages: ½ mark each, Any two disadvantages : ½ mark each)**
	ii)	**Define fan in and noise margin.**	**2M**
	Ans:	**Fan in:** The number of inputs that a logic gate can handle. **Noise margin:** The difference between the tolerable output and input voltage ranges is called the **noise margin** of the **gate**.	**(Definitions: 1 mark each)**

	iii)	**Simplify using Boolean algebra (A+B) (A+C).**	**2M**
	Ans:	(A+B)(A+C) = AA + AC+ AB + BC = A + AB + AC + BC (Since A.A =A) = A (1+ B + C) + BC (Since 1+B+C = 1) = A +BC	**(2 marks)**
	iv)	**Draw symbol, truth table and logic equation of EX-NOR gate.**	**2M**
	Ans:	**Symbol:**  **Truth Table:** **Inputs** / **Output** $Y = \overline{A \oplus B}$ A B Y 0 0 1 0 1 0 1 0 0 1 1 1 **Logic Equation:** $Y = A.B + \overline{A}.\overline{B}$ $Y = \overline{A \oplus B}$	**(Symbol: (1/2 mark, Truth Table: 1 mark, Logic Equation: ½ mark)**
	v)	**Define minterm and maxterm.**	**2M**
	Ans:	**Minterm:** A minterm, denoted as mi, where $0 \leq i < 2^n$, is a product (AND) of the n variables in which each variable is complemented if the value assigned to it is 0, and uncomplemented if it is 1. **Maxterm:** A maxterm, denoted as Mi, where $0 \leq i < 2^n$, is a sum (OR) of the n variables (literals) in which each variable is complemented if the value assigned to it is 1, and uncomplemented if it is 0.	**(minterm and maxterm :1mark each)**

	vi)	**Draw symbol and truth table of T-flip-flop.**	**2M**
	Ans:	Symbol:  Truth Table: Inputs | Outputs | Comments E T Q_{n+1} $\overline{Q}_{n+1}$ 1 0 Q_n $\overline{Q}_n$ No change 1 1 $\overline{Q}_n$ Q_n Toggle	**(Symbol: 1 mark, Truth table: 1 mark)**
	vii)	**What is the difference between edge Triggering and level Triggering (any 2)?**	**2M**
	Ans:	**Edge Triggering** | **Level Triggering** A logical circuit whose output changes during the positive or negative transition of the clock is called edge triggering | A logical circuit whose output changes during 0 level or 1 level of the clock is called level triggering It is instantaneous in nature | The output changes during a certain definite pulse duration of the clock  **Positive Edge Triggering**  **High Level Triggering**  **Negative Edge Triggering**  **Low Level Triggering**	**(1 mark each)**

	viii)	**State two specification of DAC.**	**2M**
	Ans:	**Specifications of DAC:** Resolution Settling time Linearity Accuracy	**(Any 2 specification: 1 mark each)**
	(b)	**Attempt any two of the following:**	**8 Marks**
	i)	**Perform the following operation** **a) 10110 – 1010 using 1's complement method.** **b) 11010 – 11110 using 2nd complement method.**	**4M**
	Ans:	**{**Note: Steps marking should be given marks**}** **a) 10110 – 1010 using 1's complement method:** Step 1: Make the number of bits in the minuend and subtrahend equal 1010 =01010 Step 2: Obtain 1's complement of subtrahend (01010) 1's complement of (01010) 01010 10101 Step 3: Adding 10110 to 0101 Step 4: Since final carry is generated, adding it to final answer and the result is positive **10110-1010 = 1100** **b) 11010 – 11110 using 2nd complement method:** The number of bits in minuend and subtrahend are equal Step I: Obtain 2's complement of (11110) 1's complement of (11110) 11110 00001	**(2 marks each)**

		1	0	1	1	0
+		1	0	1	0	1
Carry	1		1			
=	1	0	1	0	1	1

	0	1	0	1	1
+					1
Carry			1	1	
=		1	1	0	0

Adding 1to 00001

	0	0	0	0	1
+					1
Carry				1	
=	0	0	0	1	0

Step II: Adding 11010 to 00001

	1	1	0	1	0
+	0	0	0	1	0
Carry			1		
=	1	1	1	0	0

Step III: Since no carry is generated, the answer is negative and in 2's compliment form

Finding 2's compliment of 11100

	1	1	1	0	0
1's compliment	0	0	0	1	1
+					1
Carry			1	1	
	0	0	1	0	0

11010-11110 = (-00100)

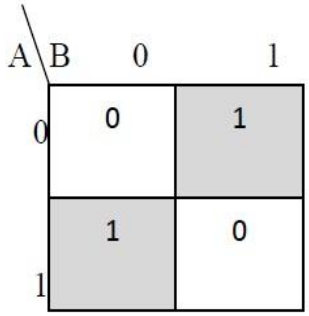
	ii)	**State and verify De-Morgan's first theorem using truth table.**	**4M**
	Ans:	It states that the, complement of a sum is equal to product of their complements	**(Statement : 1 mark, Verification: 3 marks)**

A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0
		LHS			RHS

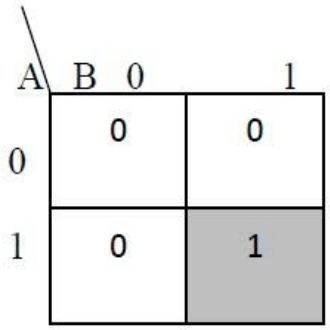
	iii)	**Compare R-2R and weighted resistor DAC any four points.**	**4M**
	Ans:		**(1 mark each)**

Weighted resistor DAC	R-2R ladder DAC
It requires more than two resistor values.	It requires resistors of only two values.
To get precise high value resistor is difficult	Since same 2 value resistors are used, the precision of resistors is not a problem
It requires one resistor per bit	It requires two resistor per bit
It is not possible to expand	It can be easily expanded to handle more number of bits by adding resistors

2.		**Attempt any four of the following:**	**16 Marks**
	a)	**Reduce the following logic expression using Boolean laws and De- Morgan's theorems.** $Y = \overline{A.\overline{(A.B)}} \ . \ \overline{B.\overline{(A.B)}}$	**4M**
	Ans:	$Y = \overline{A.\overline{(A.B)}} \ . \ \overline{B.\overline{(A.B)}}$ $Y = (\overline{A} + \overline{\overline{AB}})\ (\overline{B} + \overline{\overline{AB}})$ (Applying De Morgan's Theorems) $Y = (\overline{A} + AB)(\overline{B} + AB)$` (By applying the Boolean law $A + \overline{A}B = A + B$) $Y = (\overline{A} + B)(A + \overline{B})$ $Y = A\overline{A} + \overline{A}\,\overline{B} + AB + B\overline{B}$ $Y = \overline{A}\,\overline{B} + AB$	**(1 marks for each step)**

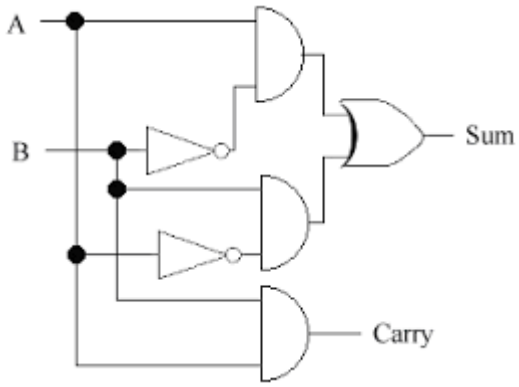
	b)	**Convert the following:** **i) $(6AC)_{16} = (?)_{10}$ ii) $(372)_8 = (?)_2$**	**4M**
	Ans:	**{**Note: Step marking should be given marks**}** i) $(6AC)_{16} = 6x\ 16^2 + 10x\ 16^1 + 12x\ 16^0$ $= 6\ x256 + 160 + 12$ $= 1536 + 160 + 12$ $= 1708$ **$(6AC)_{16} = (1708)_{10}$** **ii)$(372)_8 = (?)$** Binary equivalent of 3 is 011 Binary equivalent of 7 is 111 Binary equivalent of 2 is 010 **$(372)_8 = (011\ 111\ 010)_2$**	**(2 marks for each correct Conversion)**
	c)	**Design Half adder using K-map and basic gates.**	**4M**
	Ans:	Truth Table: <table><tr><th colspan="2">INPUTS</th><th colspan="2">OUTPUTS</th></tr><tr><th>A</th><th>B</th><th>SUM</th><th>CARRY</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr></table> K map **K-map for Sum:**  Sum = $\overline{A}\,B + A\,\overline{B}$	**(Truth table: 1mark, 1 mark each k map, 1mark circuit)**

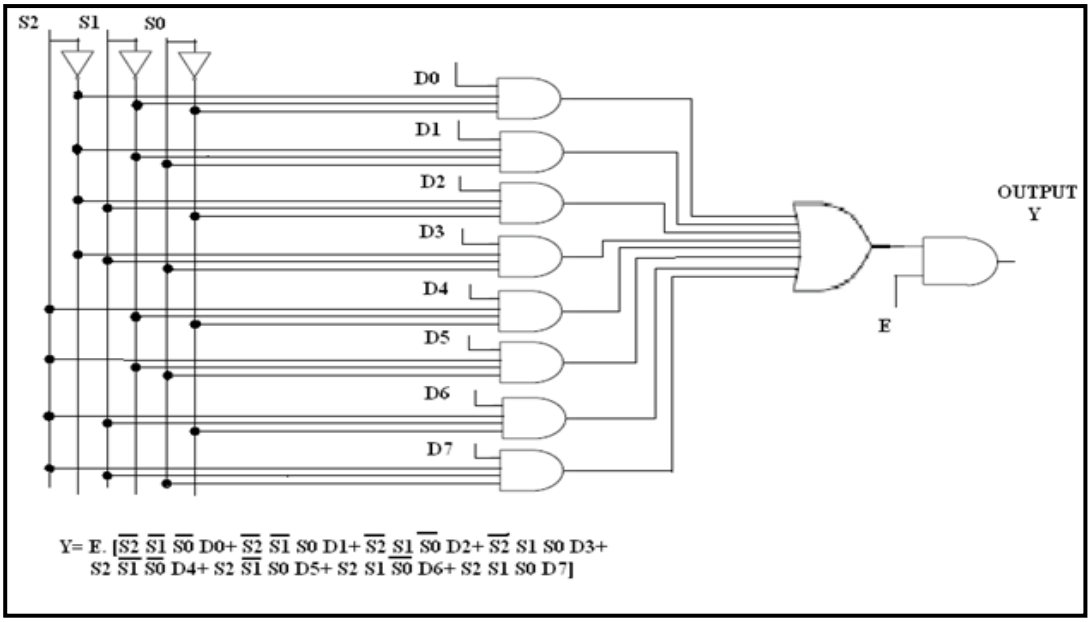
K-map for Carry:



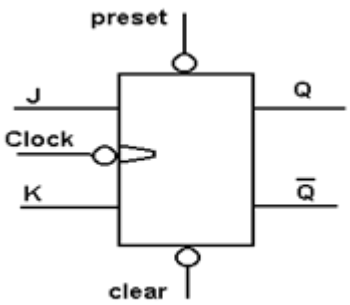
Carry = AB

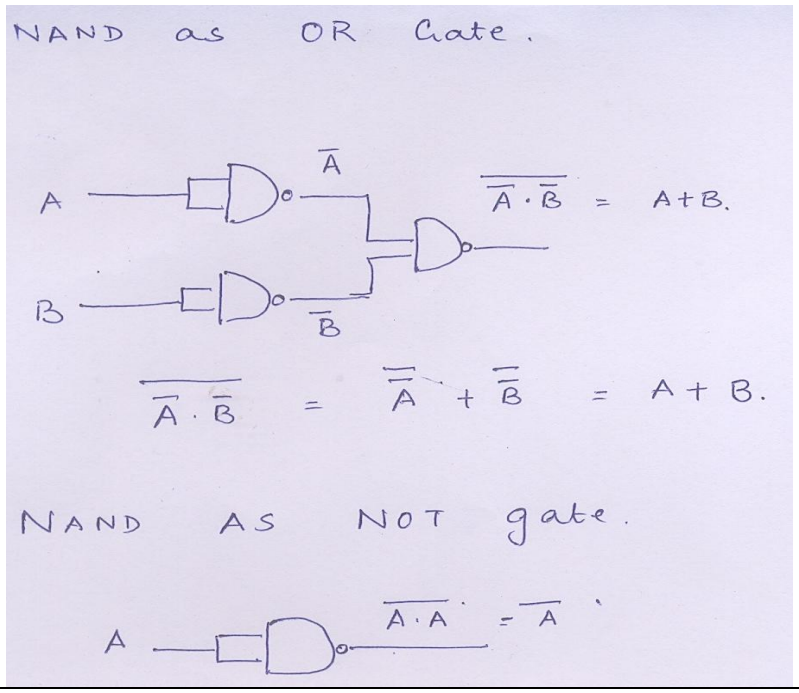
Half adder using Basic gates



	d)	**Draw 8: 1 multiplexer using basic logic gates.**	**4M**
	Ans:	**{**Note: Equation optional**}**  $Y = E.[\overline{S2}\ \overline{S1}\ \overline{S0}\ D0 + \overline{S2}\ \overline{S1}\ S0\ D1 + \overline{S2}\ S1\ \overline{S0}\ D2 + \overline{S2}\ S1\ S0\ D3 + S2\ \overline{S1}\ \overline{S0}\ D4 + S2\ \overline{S1}\ S0\ D5 + S2\ S1\ \overline{S0}\ D6 + S2\ S1\ S0\ D7]$	**(Diagram: 4 marks)**
	e)	**Compare RAM and ROM any four point.**	**4M**
	Ans:		**(Four points:1 mark each)**

RAM	ROM
Random Access Memory or RAM is a form of data storage that can be accessed randomly at any time, in any order and from any physical location, allowing quick access and manipulation	Read-only memory or ROM is also a form of data storage that cannot be easily altered or reprogrammed. Stores instructions that are not necessary for re-booting to make the computer operate when it is switched off. They are hardwired
RAM allows the computer to read data quickly to run applications. It allows reading and writing.	ROM stores the program required to initially boot the computer. It only allows reading
RAM is volatile i.e. its contents are lost when the device is powered off.	It is non-volatile i.e. its contents are retained even when the device is powered off.
The two main types of RAM are static RAM and dynamic RAM	The types of ROM include PROM, EPROM and EEPROM.

	f)	**Draw logic diagram of JK-flop-flop and write its truth table.**	**4M**
	Ans:	**Logic Diagram:**  **Truth Table:** Inputs: J_n, K_n — Output: Q_{n+1} 0 0 — Q_n 1 0 — 1 0 0 — 0 1 1 — $\overline{Qn}$	**(Logic Diagram:2 marks, Truth Table :2 marks)**
3.		**Attempt any four of the following:**	**16 Marks**
	a)	**Perform the following BCD arithmetic operation:** **i) $(637)_{10}$ +$(463)_{10}$ ii) $(63)_{10}$ + $(19)_{10}$**	**4M**
	Ans:	**{**Note: Steps marking should be given marks**}** **i)** $(673)_{10} \Rightarrow$ 0110 0111 0011 $+ (463)_{10} \Rightarrow$ 0100 0110 0011 1010 1101 0110 ← invalid BCD Add BCD of 6 in invalid BCD: + 0110 0110 1 0001 0011 0110 1 1 3 6 $\therefore (673)_{10} + (463)_{10} = (1136)_{10}$	**(Correct answer: 2 marks each)**

		ii) $(63)_{10} \Rightarrow$ 0110 0011 $+ (19)_{10} \Rightarrow$ 0001 1001 0111 1100 ← invalid BCD 0110 1 1000 0010 8 2 $\therefore (63)_{10} + (19)_{10} = (82)_{10}$	
	b)	**What is an Universal gate? Prove NAND as an universal gate.**	**4M**
	Ans:	NAND and NOR gates are called as Universal Gates because it is possible to implement any Boolean expression with the help of only NAND or NOR gates, Hence, a user can build any combinational; circuit with the help of only NAND gates or NOR gates. **Proof:** Using NAND gates, OR, AND and NOT gates may be constructed as shown below  	**(Universal gate: 2 marks, Proof: 2 marks)**

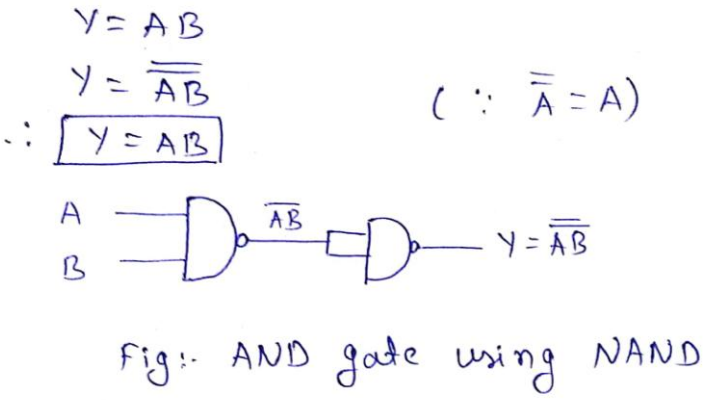
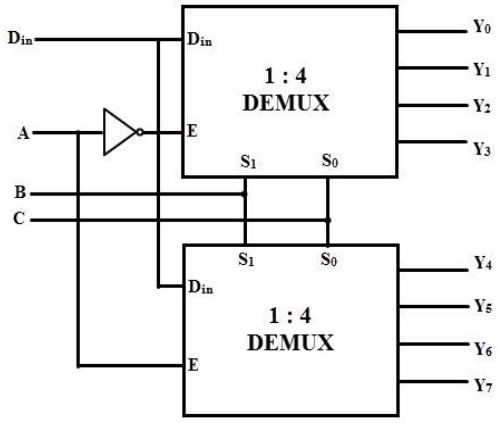
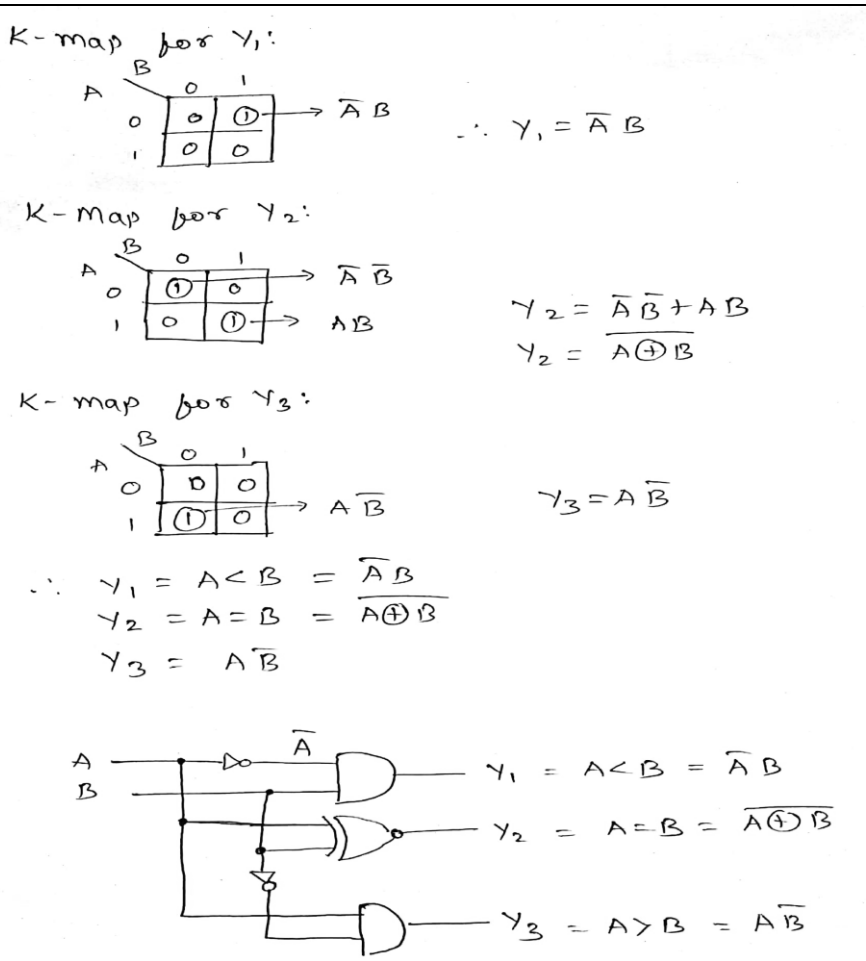
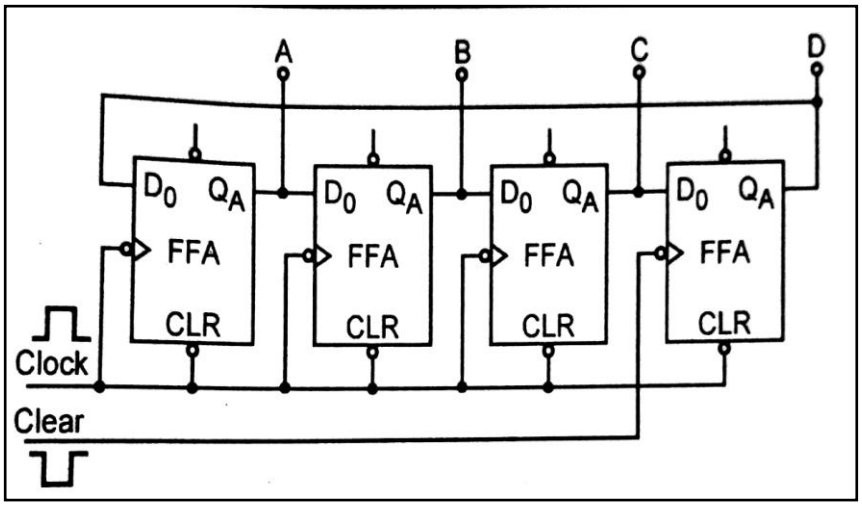


Fig:- AND gate using NAND

	c)	**Design 1:8 De-multiplexer using 1:4 demultiplexer.**	**4M**
	Ans:	 A,B,C are the select line inputs **Fig: 1:8 De-multiplexer using 1:4 De-multiplexer**	**(Designing: 4 marks)**
	d)	**Design 1 bit comparator using K-map and draw its logic diagram.**	**4M**
	Ans:	1. The one-bit comparator is combinational logic circuit with two inputs A and B and three Outputs namely A<B, A+B, A>B. 2. It compares two single bit numbers A and B and produces an output that indicates the result of comparison. Truth Table:	**(Truth table :1 mark, Implementation using K maps :2 marks, Diagram :1 mark)**

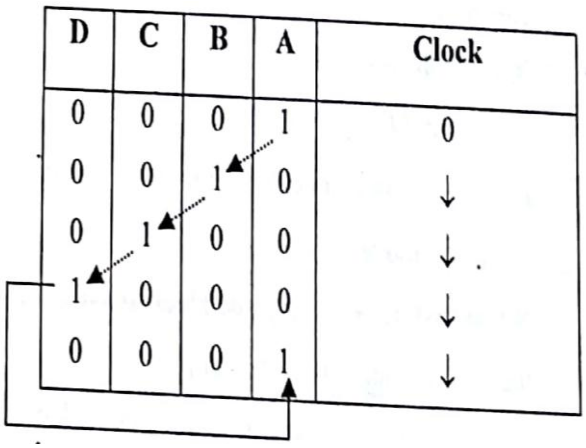
INPUTS		**OUTPUTS**		
A	**B**	**Y1= A<B**	**Y2= A=B**	**Y3 = A>B**
0	**0**	**0**	**1**	**0**
0	**1**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**
1	**1**	**0**	**1**	**0**



	e)	**With the help of block diagram explain the working of a ring counter.**	**4M**
	Ans:	 **Fig: Ring Counter Block diagram** **Working:** 1. Ring Counter is nothing but a SISO (Serial in Serial out) Shift register in which serial out i.e. Q_3 output of the fourth Flip flop is connected to D input of the first	**(Block diagram: 2 marks, working: 2 marks)**

Flip-Flop. Thus there is feedback from output to the input.

2. Clock pulses are given simultaneously to all flip-Flops
3. Initially, count stored is D C B A = 0 0 0 1 Clock pulses are applied. Count 0 0 0 1 is rotated as shown in below table.



D	C	B	A	Clock
0	0	0	1	0
0	0	1	0	↓
0	1	0	0	↓
1	0	0	0	↓
0	0	0	1	↓

f) Give four features of a dynamic RAM. **4M**

Ans:

1. Data is stored in the form of charge on the capacitor. Hence each DRAM unit consists of one MOSFET and a capacitor.
2. Since Capacitors are used on input side, refreshing circuit is required.
3. Access time is more, hence it is slow in speed.
4. Memory cell per unit area are more than Static RAM.
5. Dynamic RAM are cheaper than SRAM.

(Any 4 features: 1 mark each)

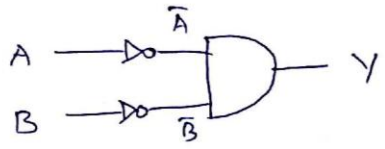
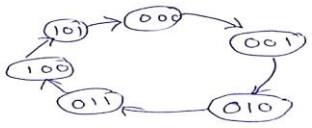
4. Attempt any four of the following: **16 Marks**

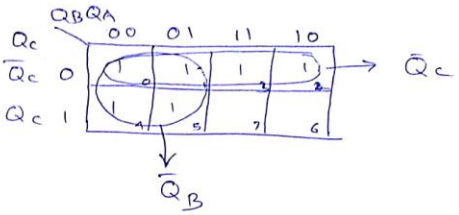
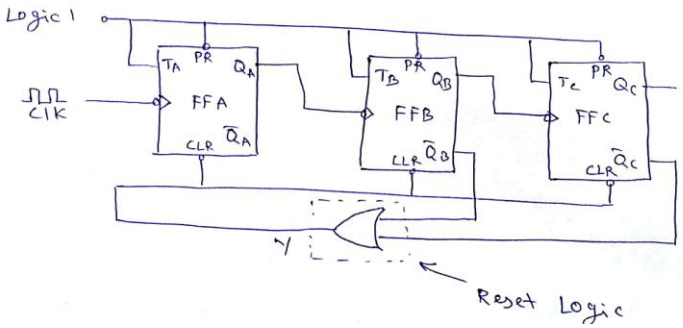
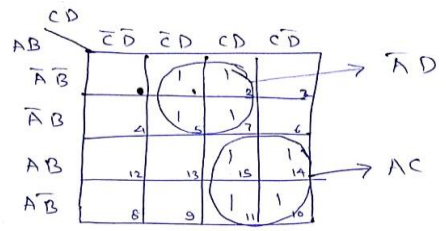
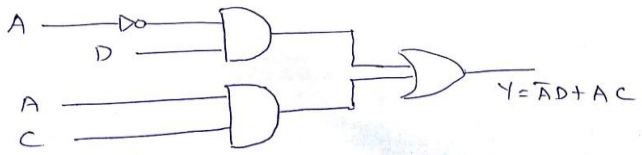
a) Compare between TTL and CMOS logic family (any four). **4M**

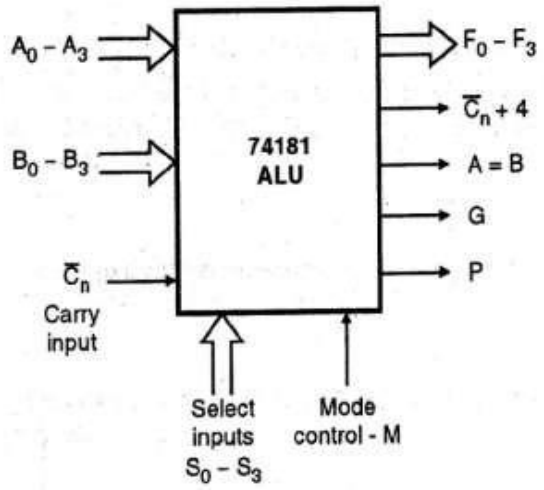
Ans:

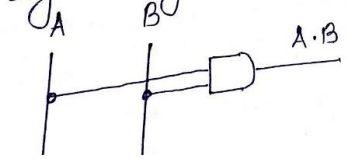
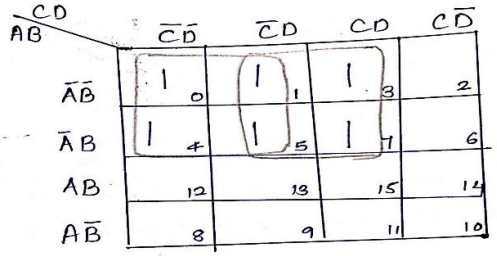
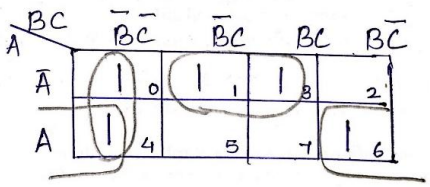
Sr. No.	Parameters	TTL	CMOS
1	Basic gates	NAND	NOR or NAND
2	Fan-in	8	10
3	Fan-out	10	>50
4	Power dissipation per gate	10mW	0.01mW
5	Noise margin (immunity)	0.4V good	5V (excellent)
6	Propagation delay	10 ns	70 ns
7	Speed-power product	100	0.7
8	Clock rate for flip-flop	35 MHz	10 MHz
9	Available function	Very large	Large
10	Packing Density	Lower	Larger
11	Cost	Low	Very low.

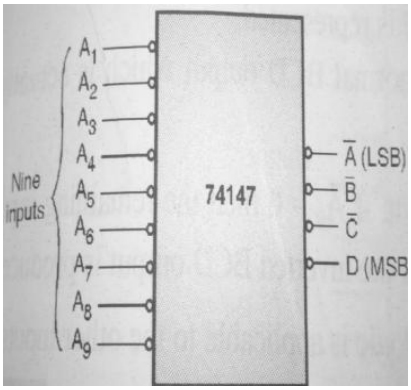
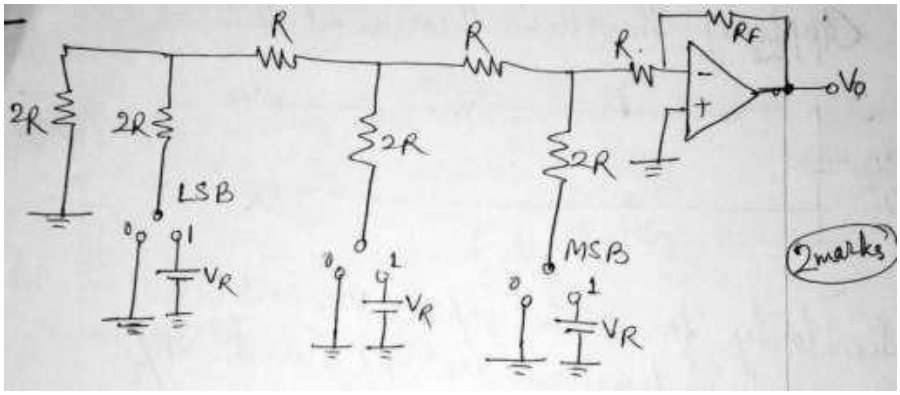
(Any 4 points: 1 mark each)

	b)	**Simplify following equation using Boolean Algebra and draw circuit diagram.** **$Y = \bar{A}(A + \bar{B}) + \bar{B}(\bar{A}+B)$.**	**4M**
	Ans:	$Y = \bar{A}(A+\bar{B}) + \bar{B}(\bar{A}+B)$ $= \bar{A}A + \bar{A}\bar{B} + \bar{B}\bar{A} + B\bar{B}$ $= 0 + \bar{A}\bar{B} + \bar{A}\bar{B} + 0 \quad (\because A\cdot\bar{A} = B\cdot\bar{B} = 0)$ $= \bar{A}\bar{B} + \bar{A}\bar{B} \quad (\because A+A = A)$ $= \bar{A}\bar{B}$  	**(Simplification: 2 marks, Circuit Diagram: 2 marks)**
	c)	**Design asynchronous mod-6 counter with its truth table.**	**4M**
	Ans:	Step 1> State diagram of a counter (Mod-6)  Mod-6 Counter will pass through 6 states i.e. will count from 000 to 101 Thus, 3 bits will be required for counter i.e. $6 < 2^3$ Number of Flip Flops = 3 Step 2> Truth table | State	Flip Flop Output			Output of Reset Logic	
---	---	---	---	---	---
	Q_C	Q_B	Q_A		
0	0	0	0	1	Valid states
1	0	0	1	1	
2	0	1	0	1	
3	0	1	1	1	
4	1	0	0	1	
5	1	0	1	1	
6	1	1	0	0	Invalid states.
7	1	1	1	0		 From truth table state 6,7 are invalid. We develop Reset logic for state 6,7. Thus by using K-Map the reset logic in terms of Q_C, Q_B, Q_A	**(1 mark for each Step)**

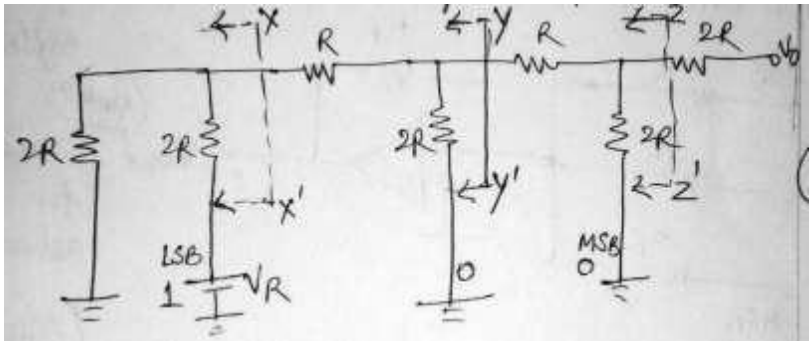
		Step 3) K Map Simplification  $\therefore Y = \bar{Q}_C + \bar{Q}_B$ Step 4) Logic Diagram With Logic Circuit (Reset) Mod-6 Counter can be designed  **{**Note: A reset logic using NAND gate may also be considered**}**	
	d)	**Minimize the following Boolean expression using K-map, Y = $\sum_m$ (1, 3, 5, 7, 10, 11, 14, 15).Draw the logical circuit diagram of minimized expression using basic gates.**	**4M**
	Ans:	$Y = \Sigma m\ (1,3,5,7,10,11,14,15)$  $Y = \bar{A}D + AC$ Realization using Basic gates 	**(Simplification: 2 marks, Logical Circuit diagram : 2 marks)**
	e)	**What is race around condition? How can it be avoided?**	**4M**
	Ans:	**Race around Condition:** The Race Around condition occurs when J=K=1 i.e. when the FF is in the toggle mode. In J-K Flip Flop, when J = 1 & K = 1 then the Output of J-K flip flop is Qn compliments of previous Output. Let Q = 0 & clock pulse is	**(Race around Conditi**

		applied. At a time interval Δt, the Output will change to Qn that means the Output now is Q = 1.Now we have J =1, K = 1 & Q = 1. After another time interval Δt, the Output will again change from 1 to 0 (Qn) due to feedback connection. Thus the output oscillates back and forth between 0 to 1 for the duration of the clock pulse. (C1K = 1) Hence at the end of the clock pulse, when Clock=0, the value of a Q Output is uncertain. This situation is called as race around condition. This race around condition can be avoided by using 1) Master Slave I-K flip flop: Master Slave J-K flip flop is a cascade of two J-K flip flop. 2) Edge Triggered JK Flip Flop.	**on: 2 marks, Avoidance: 2 marks)**
	f)	**Draw block diagram of ALU IC-74181 and explain function of each pin.**	**4M**
	Ans:	 **Block diagram: ALU IC-74181** A_0–A_3 Operand Inputs (Active LOW) B_0–B_3 Operand Inputs (Active LOW) S_0–S_3 Function Select Inputs M Mode Control Input Cn Carry Input F_0–F_3 Function Outputs (Active LOW) A = B Comparator Output G Carry Generate Output (Active LOW) P Carry Propagate Output (Active LOW) C_{n+4} Carry Output	**(Diagram: 2 marks, Functions of Pin: 2 marks)**

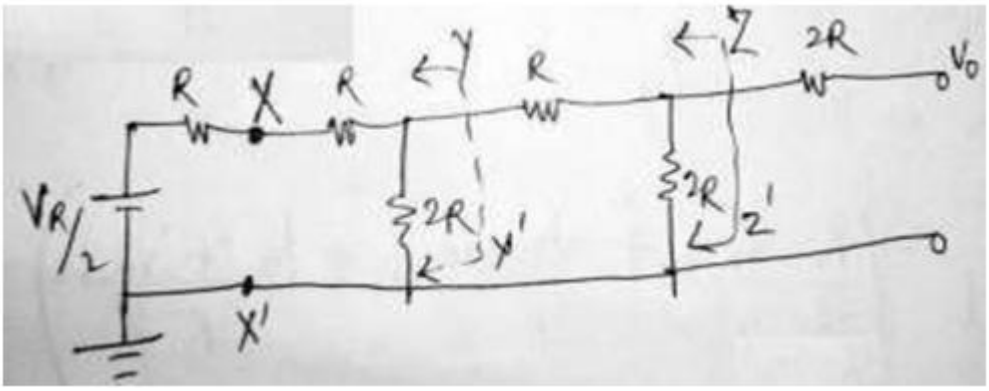
5.		**Attempt any four of the following:**	**16 Marks**
	a)	**Reduce the following expression and implement logic gates** **Y = AB+ ABC +AB (E+F)**	**4M**
	Ans:	a) $Y = AB + ABC + AB(E+F)$ $= AB(1+C) + ABE + ABF$ $\because 1+C=1$ $= AB + ABE + ABF$ $= AB(1+E) + ABF$ $\because 1+E=1$ $= AB(1) + ABF$ $= AB(1+F)$ $\because 1+F=1$ $= AB$ Logic diagram.  	**(Reducing Equation: 2 marks, Logic diagram: 2 marks)**
	b)	**Simplify the following SOP expression with K-Map** **i) F(A , B, C, D) = $\sum_m$ (0,1,3,4,5,7) ii) F (A,B,C) = $\sum_m$ (0,1,3,4,6).**	**4M**
	Ans:	**{**Note: Steps marking shall be considered**}** **i)** $F(A,B,C,D) = \sum m(0,1,3,4,5,7)$  $Y = \bar{A}\bar{C} + \bar{A}D$ **ii)** $F(A,B,C) = \sum m(0,1,3,4,6)$  $Y = \bar{A}C + \bar{B}\bar{C} + A\bar{C}$	**(Simplification: 2 marks each)**

	c)	**Draw and explain the block diagram of IC–74147 decimal to BCD encoder. Write truth table.**	**4M**
	Ans:	**Explanation:** IC 74147 is basically a 10:4 encoder or decimal to BCD encoder. A1 to A9 inputs are the active low inputs and A, B, C and D are the active low outputs.A1 has the lowest priority and A9 has the highest priority. In response to the inputs, chip produces inverted BCD code corresponding to the highest numbered Active input as shown in the truth table. **Diagram:**  **Truth Table:** **Inputs** | **Outputs (Inverted BCD)** | **Normal BCD** $\bar{A}_1$ $\bar{A}_2$ $\bar{A}_3$ $\bar{A}_4$ $\bar{A}_5$ $\bar{A}_6$ $\bar{A}_7$ $\bar{A}_8$ $\bar{A}_9$ | D C B A | D C B A 1 1 1 1 1 1 1 1 1 | 1 1 1 1 | 0 0 0 0 X X X X X X X X 0 | 0 1 1 0 | 1 0 0 1 X X X X X X X 0 1 | 0 1 1 1 | 1 0 0 0 X X X X X X 0 1 1 | 1 0 0 0 | 0 1 1 1 X X X X X 0 1 1 1 | 1 0 0 1 | 0 1 1 0 X X X X 0 1 1 1 1 | 1 0 1 0 | 0 1 0 1 X X X 0 1 1 1 1 1 | 1 0 1 1 | 0 1 0 0 X X 0 1 1 1 1 1 1 | 1 1 0 0 | 0 0 1 1 X 0 1 1 1 1 1 1 1 | 1 1 0 1 | 0 0 1 0 0 1 1 1 1 1 1 1 1 | 1 1 1 0 | 0 0 0 1	**(Diagram: 1 mark, truth table :2 marks, explanation: 1 mark)**
	d)	**Describe working of R-2R ladder type DAC.**	**4M**
	Ans:	R-2R ladder DAC uses two resistors R & 2R. The input is applied through digitally controlled switches.  	**(Explanation: 2 marks , Diagram: 2 marks)**

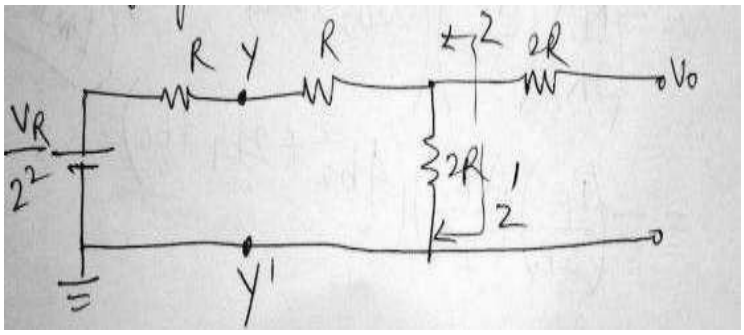
For example if the digital input is 001



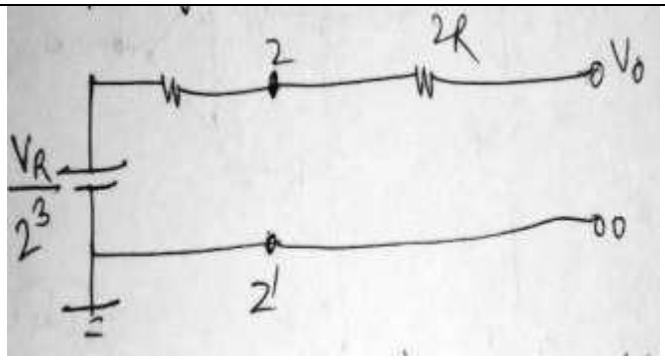
Applying Thevenins theorem at XX´



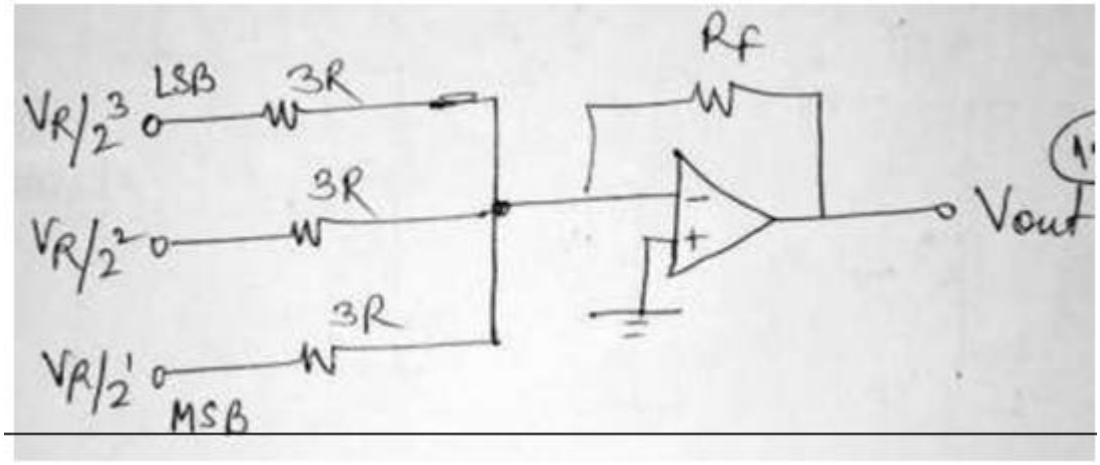
Applying Thevenins theorem at YY´



Applying Thevenins theorem at ZZ´



Similarly for digital input 010 and 100 the equivalent voltages are $VR/2^2$ and $VR/2^1$ respectively. The equivalent resistance is 3R in each case.
So the simplified circuit of 3bit R-2R ladder DAC is :



The analog output voltage for a given digital input is given by

$V_{out} = -((R_F/3R)\, V_R \times b_0/2^3 + R_F/3R\, V_R \times b_1/2^2 + R_F/3R\, V_R \times b_2/2^1)$

$= -(R_F/3R)(V_R/2^3)(2^2 b_2 + 2^1 b_1 + 2^0 b_0)$

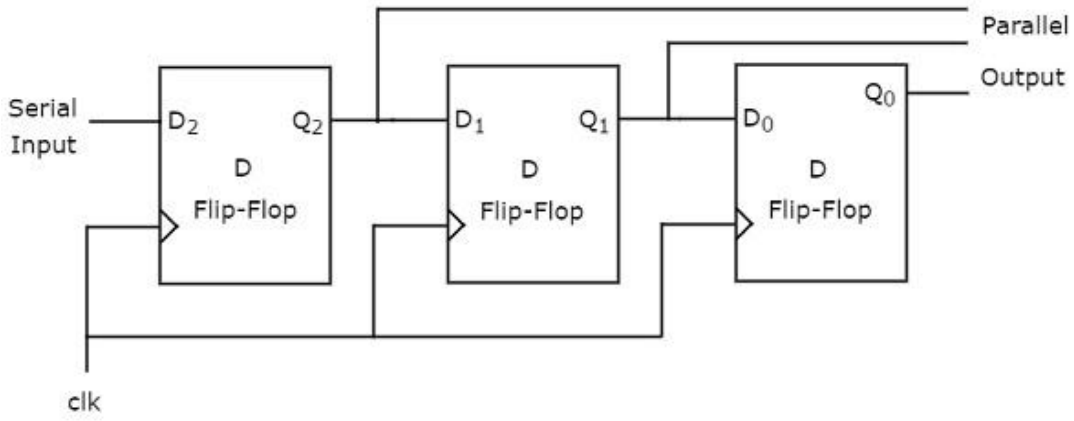
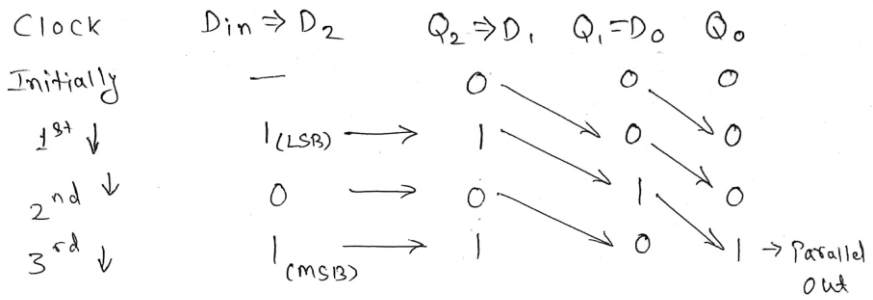
$= -(R_F/3R)(V_R/2^3)(4b_2 + 2b_1 + b_0)$

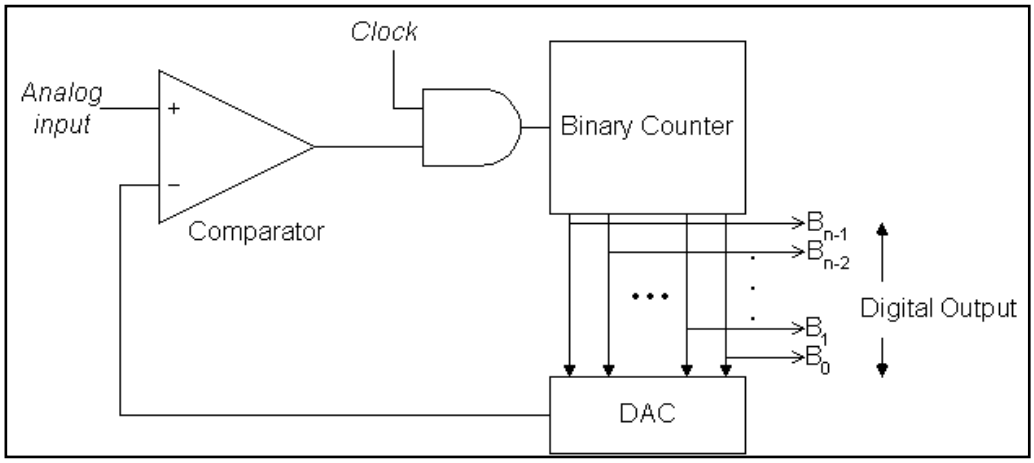
e) **Differentiate between combination logic and sequential logic system.** **4M**

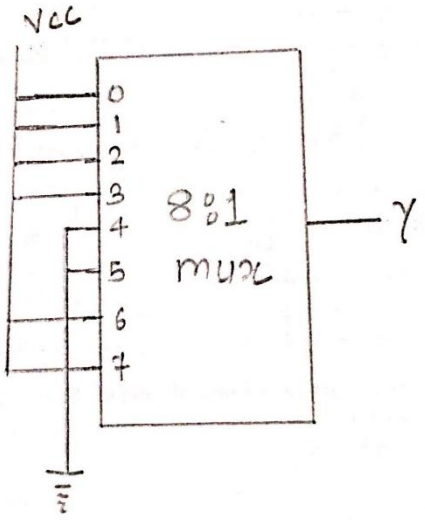
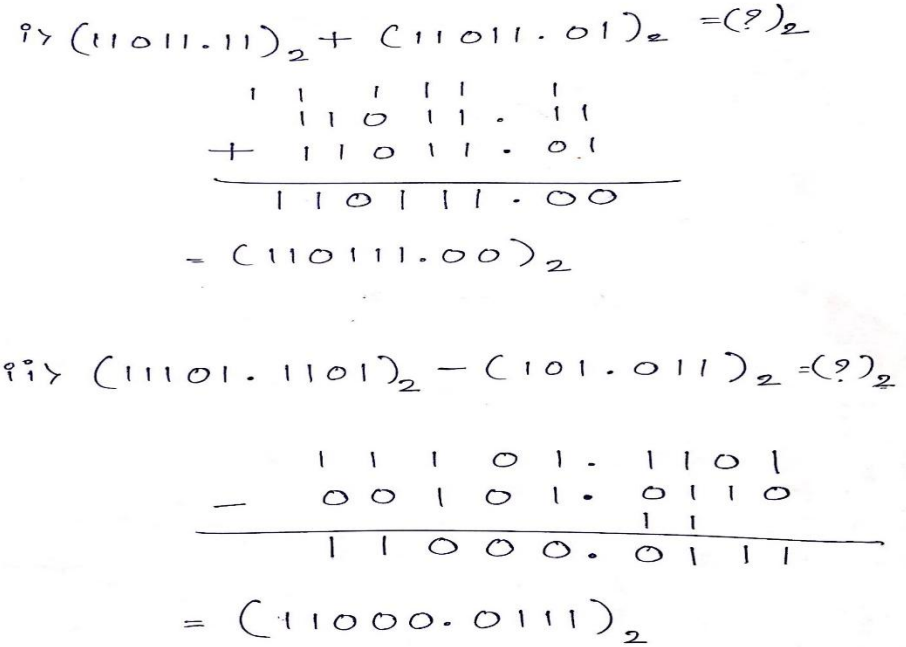
Ans:

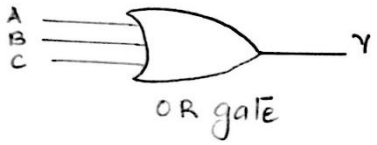
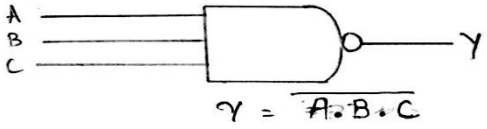
Combinational Logic Circuits	Sequential Logic Circuits
Output is a function of the present inputs (Time Independent Logic)	Output is a function of clock, present inputs and the previous states of the system.
Do not have the ability to store data (state).	Have memory to store the present states that is sent as control input (enable) for the next operation.
Logic gates are the elementary building blocks.	Flip flops (binary storage device) are the elementary building unit.
Independent of clock and hence does not require triggering to operate.	Clocked (Triggered for operation with electronic pulses).

(Each Difference: 1mark (any 4))

			Used mainly for Arithmetic and Boolean operations.	Used for storing data (and hence used in RAM).		
			It does not require any feedback. It simply outputs the input according to the logic designed.	It involves feedback from output to input that is stored in the memory for the next operation.		
	f)	**Draw circuit diagram of 3-bit SIPO shift register, right shift mode with the help of block diagram.**				**4M**
	Ans:	**Diagram:**  **Truth Table:**  **Explanation:-** • The serial input parallel output shift register is shown above (SIPO). • It accepts the input data serially i.e. one bit at a time and outputs the stored data in parallel form. • At the end of each clock pulse (-ve edge) a first data bit of higher significant bit (as LSB is entered first) enters into the Di i/p of FF1 and Q output of every FF gets shifted to the next FF on right side. • Thus once the data bits are stored, each bit appears on its respective output line & all bits are available simultaneously at Q2 Q1 Q0 rather than a bit by bit basis with the serial output. D in=101			**(Diagram: 2 marks, Truth table: 1 mark, Explanation: 1 mark)**

6.		**Attempt any four of the following :**	**16 Marks**
	a)	**Draw neat block diagram of Ramp ADC and explain its working.**	**4M**
	Ans:	 Fig: Ramp ADC Working the counter is reset to zero first by applying a reset pulse. Then after releasing the reset pulse, the clock pulse are applied to the counter through an AND gate Initially the DAC output is zero. Therefore the analog input voltage V_A is greater than the DAC output V_d i.e., $V_A > V_d$ The comparator output is high and the AND gate is enabled .Thus the clock pulses are allowed to pass through the .AND gate to the counter. The counter starts counting these clock pulse. Its output goes on increasing. As the counter output acts as input to DAC, the DAC output which is in staircase waveform also increase. As long as the DAC output $V_d < V_A$ this process will continue, as the comparator output remains high enabling the AND gate. However, when the DAC output is high than the input analog voltage i.e. $V_d > V_A$, the comparator output becomes low so that AND gate is disabled and stop the clock pulse i.e. counting stops. Thus the digital output of the counter represents the analog input voltage v_A. When the analog input change to a new value, a second reset pulse is applied to the counter to clear it again the counting starts.	**(Explanation: 2 marks, Diagram: 2 marks)**
	b)	**State the application of shift register (any four).**	**4M**
	Ans:	**Application of Shift Registers** 1. Delay line 2. Serial to parallel converter 3. Parallel to serial converter 4. Ring counter 5. Twisted Ring counter 6. Sequence generator	**(Any four application :1 mark each)**

	c)	**Implement following logical equation using multiplexer:** **$Y(A, B, C) = \sum_m (0, 1, 2, 3, 6, 7)$.**	**4M**
	Ans:		**(Implementation: 4 marks)**
	d)	**Perform the binary arithmetic** **i)$(11011.11)_2 + (11011.01)_2 = (?)_2$ (ii) $(11101.1101)_2 - (101.011)_2 = (?)_2$**	**4M**
	Ans:	**{**Note: Steps marking should be given marks**}** 	**(Each conversion : 2 marks)**

	e)	**Draw symbol for 3 input OR gate with truth table and 3 input NAND gate with truth table.**	**4M**
	Ans:	OR GATE:  OR gate $Y = A+B+C$ A B C Y 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1 1 NAND GATE:  $Y = \overline{A \cdot B \cdot C}$ A B C Y 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1 0	**(Symbol: 1 mark each, Truth Table: 1 mark each)**
	f)	**Define the following specification of A-D Converter** **i) Conversion time (ii) Resolution.**	**4M**
	Ans:	i) **Conversion time:** It is the total time required to convert the analog input signal into a corresponding digital output. This Conversion rate is also called as speed. This varies with analog voltage. ii) **Resolution:** Resolution is define as the maximum number of digital output codes. This is same as that of a DAC. Resolution is defined as the ratio of change in the value of the input analog voltage VA, required to change the digital output by 1 LSB. $$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$	**(Definition: 2 marks each)**