MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION
(Autonomous)
(ISO/IEC - 27001 - 2013 Certified)

WINTER– 2017 EXAMINATION

Subject Name: Basic Electronics **Model Answer** Subject Code: 17321

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q.1 Attempt any TEN from following **20 Marks**

a) Define Knee voltage (V_{knee}) and give the value of (V_{knee}) for Si and Ge diode.

Ans: (Definition -1M, Values -1M)

Knee voltage (V_{knee}): It is minimum forward voltage at which diode starts conducting rapidly

Knee voltage for for silicon diode is 0.7V and for germanium diode it is 0.3V

b) Draw the symbol of EXOR, EXNOR gate and give the truth table for the same

Ans: (Each gate with symbol and Truth table -1M)

EXOR gate

2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

EXNOR gate

2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

c) Define Depletion region and Barrier voltage of PN junction

Ans: (Each definition -1M)

1. **Depletion region :** The region consisting of immobile positive charge at n-side and immobile negative charge at p-side near the junction acts like a barrier and prevents the further flow of free electrons and holes.
2. **Barrier voltage :** The negative charge formed at the p-side of the p-n junction is called negative barrier voltage while the positive charge formed at the n-side of the p-n junction is called positive barrier voltage. The total charge formed at the p-n junction is called barrier voltage, barrier potential or junction barrier.

d) Define ripple factor and PIV of diode

Ans: (Each definition -1M)

1. **Ripple factor:** It is define as ratio of R.M.S. value of AC component to the DC component in the output.
2. **PIV :** It is maximum reverse voltage that diode can withstand without destroying junction.

e) State any four advantages of LC filter.

Ans: (Any four points-2M)

1. The choke input (LC) filter has a high output D.C voltage.

2. It has no loading effect on the rectifier and power transformer.
3. The diode does not have to carry surge currents.
4. It has a very low ripple factor as compared to series inductor filter and shunt capacitor filter.
5. It has very good load regulation.
6. It has no loading effect on the rectifier and power transformer.
7. It has better voltage regulation than that of π filter.

f) State the applications of digital electronics.

Ans: (Any four applications)

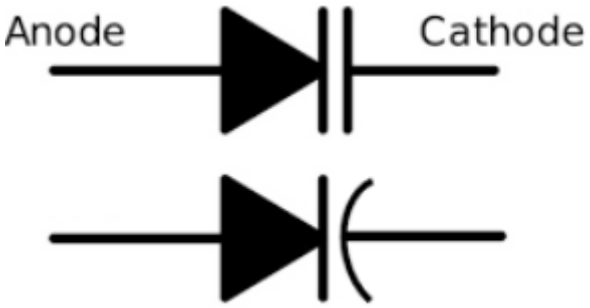
1. The processor, graphics controller are built on principles of digital electronics.
2. In Computers, tablet, displays, LCD/LED TV.
3. mobile/smart phone, , computer ,keyboard, mouse
4. speed/distance meter on bike/car, various control of the car,
5. ATM machines, credit /debit cards
6. Telephone exchange

g) Draw the symbol of Schottky diode and Varactor diode.

Ans: (Each symbol-1M)

1) Schottky diode

2) Varactor diode.



h) Define pinch off voltage and drain resistance of FET.

Ans: (Each definition -1M)

1. Pinch-off Voltage: It is the value of the drain to source voltage V_{DS} at which the drain current I_D reaches its constant saturation value. Any further increase in V_{DS} does not have any effect on the value of I_D. It is denoted by V_P.

2. Drain resistance : It is change in drain to source voltage to the change in drain current. It is also called AC/dynamic drain resistance.

i) What is regulator ? State its need.

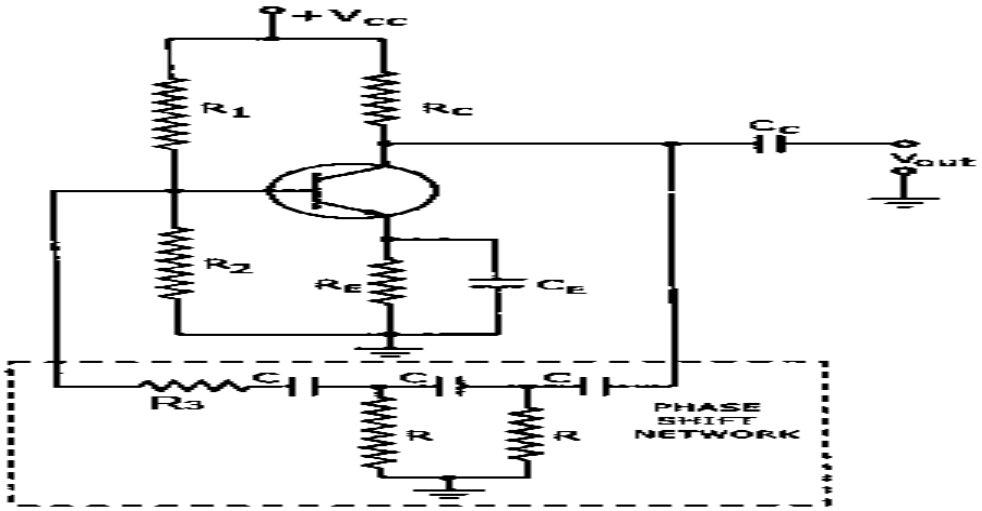
Ans: (Explanation -1M, Need-1M)

A voltage regulator is a circuit or device designed to deliver a constant voltage at its output regardless of changes in ac supply voltage and load current.

Need:- A voltage regulator is one of the most widely used electronic circuitry in any device. A regulated voltage very important for the smooth functioning of many electronic circuits. Without voltage regulator in power supply, it may give unexpected result or damage one of the components in the circuit, hence voltage regulator is needed.

j) Draw circuit diagram of RC phase shift oscillator.

Ans: (Circuit diagram-2M)



RC Phase Shift Oscillator

k) Define load and line regulation

Ans : (Each definition for 1M)

1. Load regulation : The load regulation indicates how much the load voltage changes when the load current changes. The load regulation is defined as:

% Load regulation = (VNL-VFL) / VFL *100

Where VNL = load voltage with no load current

VFL = load voltage with full load current.

The smaller the load regulation, the better the power supply. A well-regulated power supply can have a load regulation of less than 1%

2. Line regulation : Any change in the line voltage out of the nominal value (i.e., 230V ac) will affect the performance of the power supply.

OR

Line regulation is a measure of how well a power supply is able to maintain the dc output voltage for a change in the ac input line voltage.

The smaller the line regulation, the better the power supply. A well-regulated power supply can have a line regulation of less than 0.1%.

l) Enlist names of regulator IC's .

Ans: (Any 2 IC's - 2M)

1. Fixed Voltage Regulators IC - a. Positive voltage regulator IC's - 78XX series eg. 7805, 7812 etc.

b. Negative voltage regulator IC's - 79XX series eg. 7905, 7912 etc.

2. Adjustable Voltage Regulator - LM317 is example of positive adjustable voltage regulator.

m) Define biasing of transistor

Ans: (Definition - 2M)

Biasing of transistor is the process that makes the base emitter junction of transistor always forward biased and collector junction reverse biased for achieving the faithful amplification .

n) Define negative and positive feedback

Ans : (Each definition for 1M)

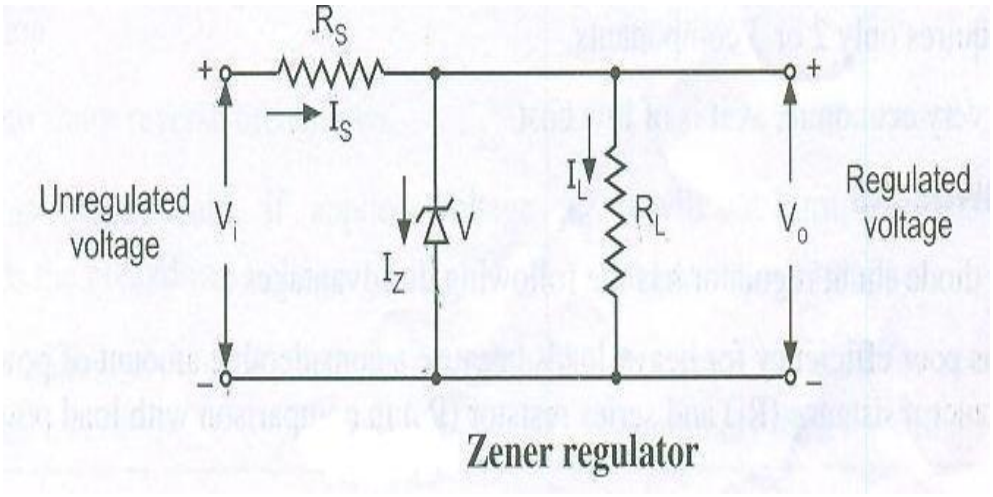
1. **Negative feedback:** Feedback in which feedback signal is out of phase with input signal and it decreases output is called negative feedback.
2. **Positive feedback:** Feedback in which feedback signal is in phase with input signal and it increases output is called positive feedback.

Q. 2: Attempt any four of the following **16 M**

a) Draw circuit diagram and describe the working of Zener diode as voltage regulator.

Ans: (Circuit diagram 2M, Explanation 2M)

Circuit diagram of Zener Diode as Voltage Regulator:



Zener regulator

A Voltage Regulator circuit provides constant O/P voltage inspite of changes in its i/p voltage or load current.
The Series Resistance Rs is connected to limit the total current drawn from the unregulated power supply.

Zener diode is a shunt type voltage regulator because the zener diode is connected in parallel with the load resistance and is connected in reverse biased condition.

If Vin is higher than Vz and if the Iz is between Izmin & Izmax then the voltage across zener will remain constant equal to Vz irrespective of any changes in Vin & IL. As output voltage is constant and equal to Vz, a regulated o/p voltage is obtained.

When Vin varies

Assume R_L constant, Vin is varying

So, I_L is also constant as $I_L = V_Z/R_L$

But Vin changes & supply current also changes

$$I = \frac{Vin - Vz}{R_S} \qquad \text{Also } I = Iz + I_L$$

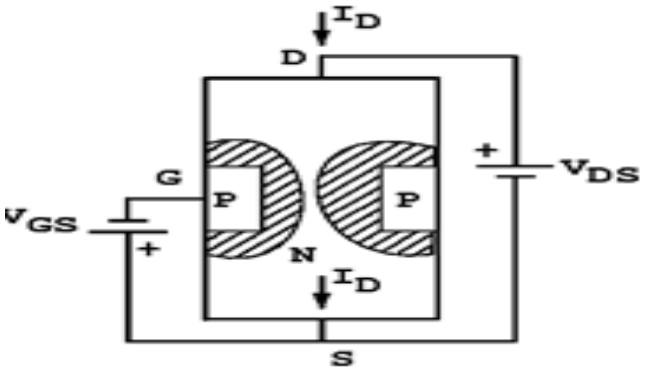
If Vin is increased, then current I will increase. But as Vz is constant & R_L is also constant, the I_L will remain constant.

The increase in current I will increase Iz but Iz is less than Iz (max).
Thus the output voltage will remain constant.

b) Describe operation of N-channel JFET

Ans: (Circuit diagram 2M, Explanation 2M)

Circuit diagram:



Operation of N-channel JFET

1) When V_{GS} = 0 volt:

When a voltage is applied between the drain and source with a DC supply voltage V_{DD} with V_{GS} = 0 V, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes drain current I_D. The value of drain current is maximum when V_{GS} = 0 V. This current is designated by the symbol I_{DSS}.

2) When V_{GS} is negative:

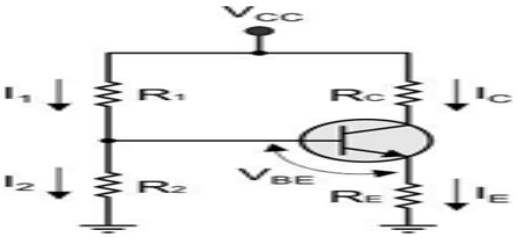
When V_{GS} is increased below zero i.e negative, the reverse voltage across the gate source junction is increased. As a result depletion regions are widened. This reduces effective width of channel and therefore controls the flow of drain current through the channel.

If V_{GS} is increased further, two depletion regions touch each other. The drain current reduces to zero. The gate to source voltage at which current reduces to zero is called as pinch-off voltage.

c) Describe the operation of voltage divider biasing with proper circuit diagram.

Ans: (Circuit diagram 2M, Explanation 2M)

Circuit diagram:



In all the D.C. bias circuits, the value of D.C. bias current and voltage of the collector depends upon the current gain (β) of the transistor. But we know that the value of current gain (β) is temperature sensitive, therefore it would be desirable to provide a D.C. bias circuit which is independent of the transistor current gain (β). It is commonly known as voltage divider bias or self-bias circuit

It is evident from that the voltage at the transistor base (due to the voltage divider network of resistors R_1 and R_2).

$$V_B = V_{CC} x \frac{R_2}{R_1+R_2}$$

Since the voltage drop across the base – emitter junction (V_{BE}) when forward biased is very small, as compared to the voltage at the base (V_B), therefore the voltage at the emitter is almost equal to the voltage at the base i.e. ., Neglecting V_{BE}

Therefore value of emitter current,

$$I_E = \frac{V_E}{R_E}$$

And the value of collector current,

$$I_C = I_E$$

The voltage drop across the collector resistor,

$$V_{RC} = I_C * R_C$$

And the voltage at the collector (measured with respect to the ground)

$$V_C = V_{CC} - V_{RC} = V_{CC} - I_C * R_C$$

The voltage from collector – to – emitter.

$$V_{CE} = V_C - V_E = V_{CC} - I_C * R_E$$

$$V_{CE} = V_{CC} - I_E(R_C + R_E) \quad \ldots\ldots\ldots\ldots\ldots\ldots (I_C = I_E)$$

From above equation it is concluded that operating point is independent on β and hence this method provides very good stabilization of operating point.

d) Draw diagram of class A push-pull amplifier and explain its operation.

Ans: (Circuit diagram -2M, operation- 2M)

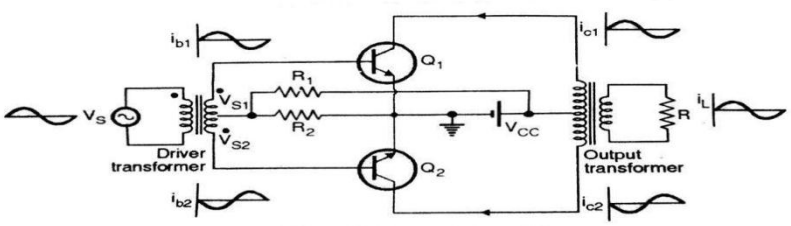
Class A Push-pull Amplifier:

The circuit diagram of class A push-pull amplifier is as shown in the fig.(a).

Operation:

The resistors R1 and R2 along with Vcc provide the dc biasing so as to keep the operating point (Q-point) at the centre of the dc load line, in order to achieve the class A operation. The driver transformer provides the phase splitting function and

produces two voltages Va1 and Va2 which are equal in magnitude but 180 degree out of phase. The Vcc is applied to the collectors of transistors Q1 and Q2 through the centre-tapped output transformer.

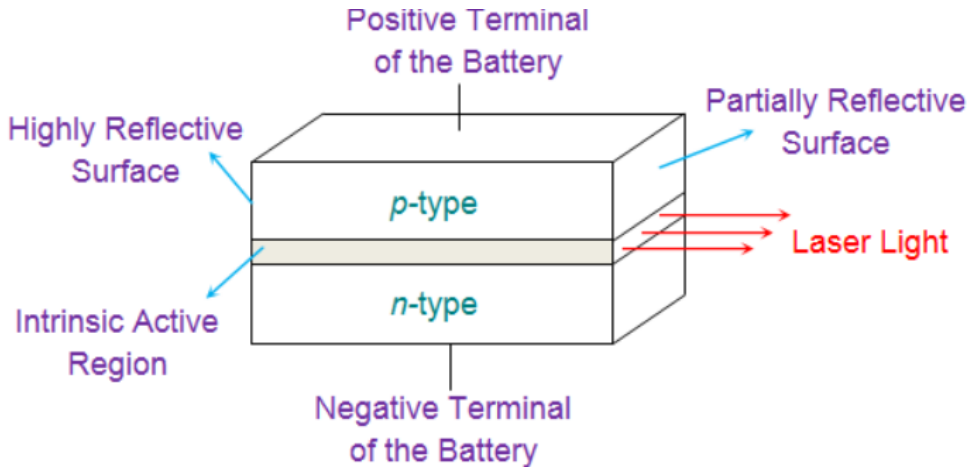


(a) Class A Pushpull Amplifier

e) Describe operating principle of LASER diode.

Ans: (Circuit diagram -2M, operation- 2M)

Circuit diagram :



A basic construction of Laser diode is shown below. A PN junction is formed by two layers of doped gallium arsenide. There is highly reflective surface at one end of PN junction and partially reflective surface at the other end, forming resonant cavity for the photon .

Operating Principle:

The Laser diode is biased by external voltage source. As electron move through the junction, recombination occurs just like a ordinary diode. As electrons fall into holes to recombine, photons are released. A released photon can strike atom, causing another photon to released. As forward current is increased, more electrons enter the depletion region and cause more photons to be emitted. Eventually some of the photons that are randomly drifting within the depletion region strike the reflected surfaces perpendicularly. These reflected photons move along the depletion region, striking atoms and releasing additional photons due to avalanche effect

f) Describe transistor as a switch with neat circuit diagram.

Ans: (Circuit diagram -2M, operation- 2M)

Transistor as Switch:

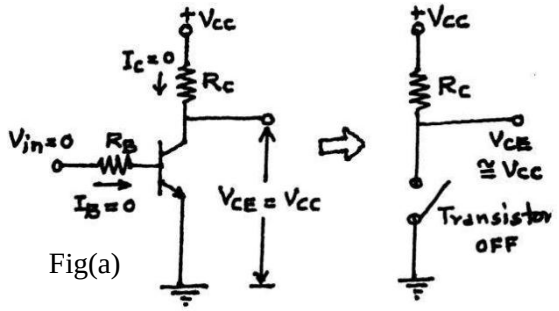
A transistor can be used for two types of applications viz. amplification and

switching. For amplification, the transistor is biased in its active region.

For switching applications, transistor is biased to operate in the saturation (full on)

or cut-off (full off) region.

(i) Transistor in cut-off region (Open switch):



Fig(a)

In the cur-off region, both the junctions of transistor are reverse biased and very small reverse current flows through the transistor.

The voltage drop across the transistor (V_{CE}) is high, nearly equal to supply voltage V_{CC}. Thus, in cut-off region the transistor is equivalent to an open switch as shown in fig.(a).

(ii) Transistor in Saturation region (Closed switch):

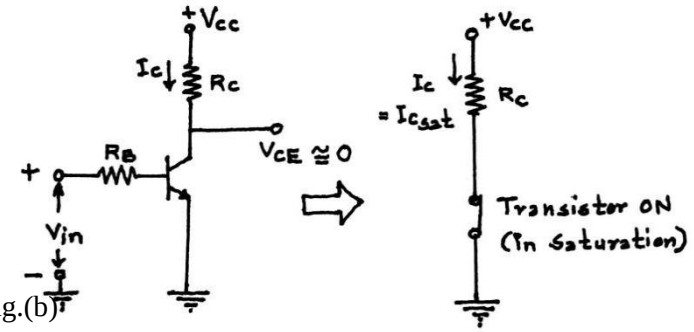


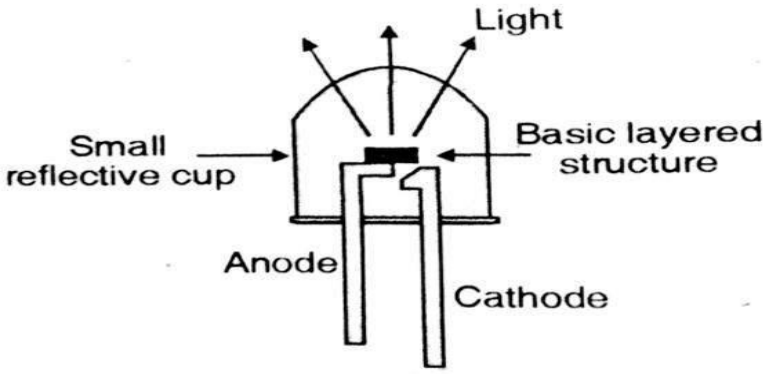
Fig.(b)

When V_{in} is positive, a large base current flows and transistor saturates. In the saturation region, both the junctions of transistor are forward biased. The collector current is very large, the voltage drop across the transistor (V_{CE}) is very small, of the order of 0.2V to 1 V, depending on the type of transistor. Thus in saturation region, the transistor is equivalent to a closed switch.

Q. 3: Attempt any FOUR of the following **16 M**

a) Explain construction and working principle of LED.

Ans: (Construction-2M, Working principle-2M)

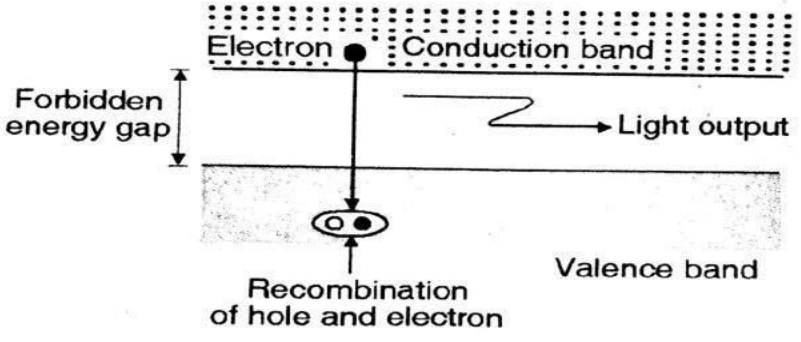


(b) Cup type Construction

Construction of LED:

The basic structure of LED is shown in fig.(a). The active region exists between the p and n regions. The light emerges from the active side in all the directions when electron hole-pairs recombine. The disadvantage of this structure is that the LED emits light in all the directions. This problem is solved by placing the basic structure inside a small reflective cup so as to focus the light in the desired direction. Such a structure is called as a cup type construction and is shown in fig.(b).

Working Principle of LED:



(c) Working Principle of LED

See fig(c) ,when the LED is forward biased, the electrons in the n-region will cross the junction and recombine with the holes in the p-type material. These free electrons reside in the conduction band and hence at a higher energy level than the holes in the valance b a n d . When t h e recombination takes place, these electrons return back to the valance band which is at lower energy level than the conduction band. While returning back, the recombining electrons give away the excess energy in the form of light. This process is called as "electroluminescence", shown in fig.(c). In this way an LED emits light. This is the principle of operation of LED.

b) Define α & β and derive the relation between (α) &) (β) of transistor.

Ans : [Each definition 1M, Derivation 2M]

α : The ratio of output collector current IC to input emitter current IE in the CB configuration is called current gain alpha (α).

β : The ratio of output collector current IC to the input base current IB in the CE configuration is called current gain beta (β) .

Relationship between α and β:

- We know, $I_E = I_B + I_C$
- Dividing the above equation on both sides by I_C, $I_E/I_C = I_B/I_C + 1$
- Since $I_C/I_E = \alpha$ and $I_C/I_B = \beta$

So, $I_E/I_C = 1/\alpha$ and $I_B/I_C = 1/\beta$

Therefore, $1/\alpha = (1/\beta) + 1$

hence $1/\alpha = (1+\beta)/\beta$

Therefore, $\alpha = \beta/(1+\beta)$

c) Compare between BJT and FET on the basis of
(i) Biolar/Unipolar
(ii) Tharmal Runaway
(iii) Noise
(iv) Applications

Ans: [Each point for 1M]

Parameter	BJT	FET
Bipolar/Unipolar	It is bipolar device i.e. current in this device is carried by electrons and holes.	It is unipolar device i.e. current in this device is carried by either electrons or holes.

Thermal Runaway	Can occur	Cannot occur
Noise	More	Less
Applications	Automatically controlled switches, TTL circuits, amplifiers, drivers circuits etc.	FETs are widely used as input amplifiers in oscilloscopes, electronic voltmeters and other measuring and testing equipment because of their high input impedance.

d) In CE configuration if β=99, leakage current I_{CEO}=50μA, if base current is 0.5mA determine I_C and I_E

Ans: (For obtaining I_C -1M, I_E -1M)

Given: β=99, I_{CEO}=50μA

Find: I_C and I_E

Equation of I_C in terms of β and I_{CEO} is

$$I_C = \beta I_B + I_{CEO}$$

$$=99*0.5*10^{-3} +50*10^{-6}$$

$$I_C = 49.55\text{mA}$$

But $I_E = I_B + I_C$

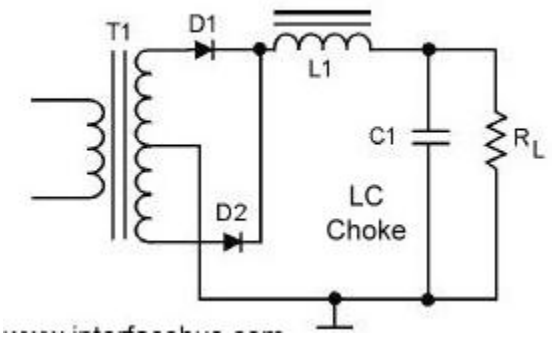
$$= (0.5+49.55)\text{mA}$$

$$IE = 50.05\text{ mA}$$

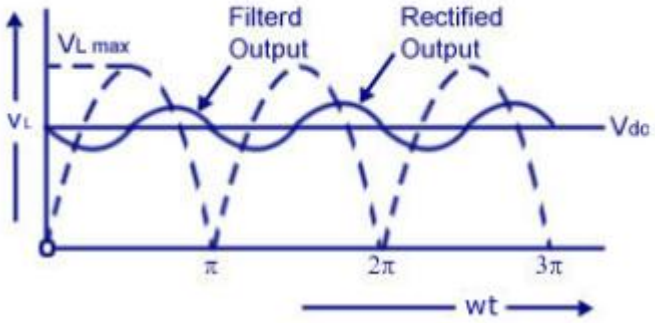
e) Draw full wave rectifier (center tap) with LC filter and draw input and output voltage waveforms.

Ans: (Circuit diagram-2M , Waveforms-2M)

Circuit Diagram:



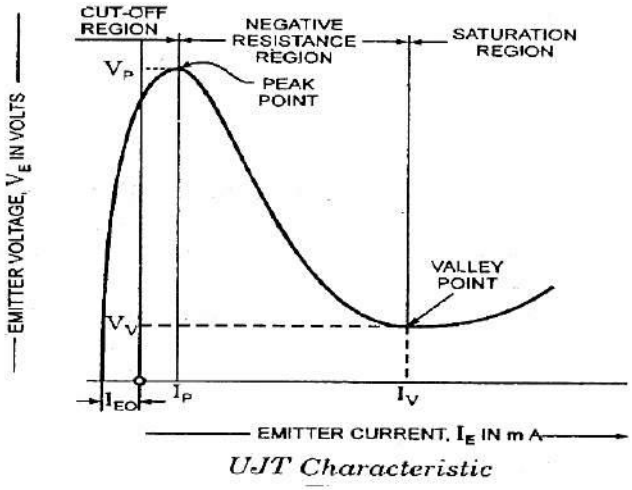
Waveforms:



f) Draw and explain the characteristic of UJT.

Ans: (Graph-2M,Explanation-2M)

UJT Characteristics:



UJT Characteristic

The UJT characteristic is emitter voltage versus emitter current characteristic, as shown in the figure. There three operating regions in UJT

1.Cut off region: For emitter voltages less than V_P (peak point voltage) the UJT is in the off state and magnitude of I_E is not greater than I_{EO}. The emitter current I_{EO} corresponds very closely with the reverse leakage current I_{CO} of a bipolar transistor. This region is known as the cut off region.

2. **Negative Resistance region:** As the emitter voltage increases and reaches $V_P = (\eta V_{BB}+V_D)$, the UJT starts conducting. Then with increase in emitter I_E the emitter voltage decreases as shown. The reduction in voltage across UJT is due to the drop in resistance R_{B1} with increase in the value of I_E. This region of operation is known as a "Negative Resistance" region, which is stable enough to be used in various applications.

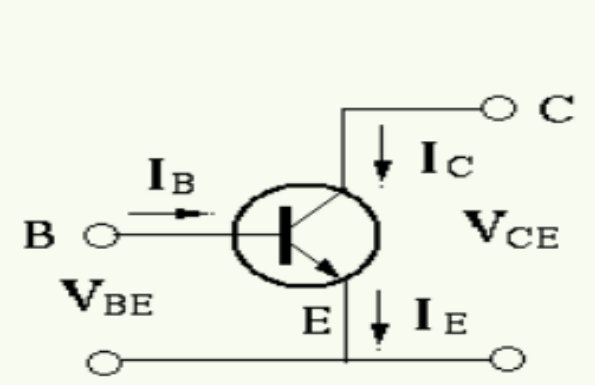
3. **Saturation region**: Eventually the "valley point" will be reached and further increase in I_E will place the device into saturation and hence after valley point there is valley point.

Q. 4: Attempt any FOUR of the following **16 M**

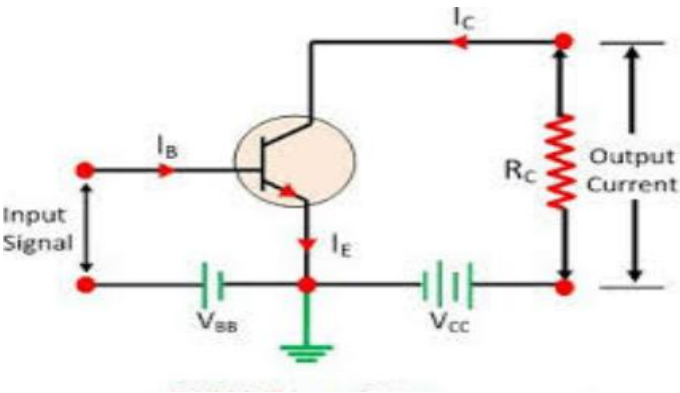
a) Draw CE configuration of NPN transistor and sketch output characteristic.

Ans: (Diagram-1M, Output characteristic-3M)

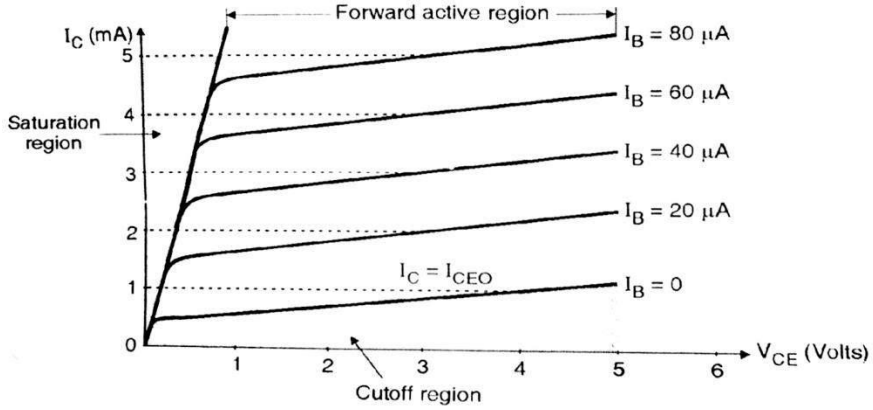
CE configuration of NPN transistor:



OR



Output characteristic of CE configuration:

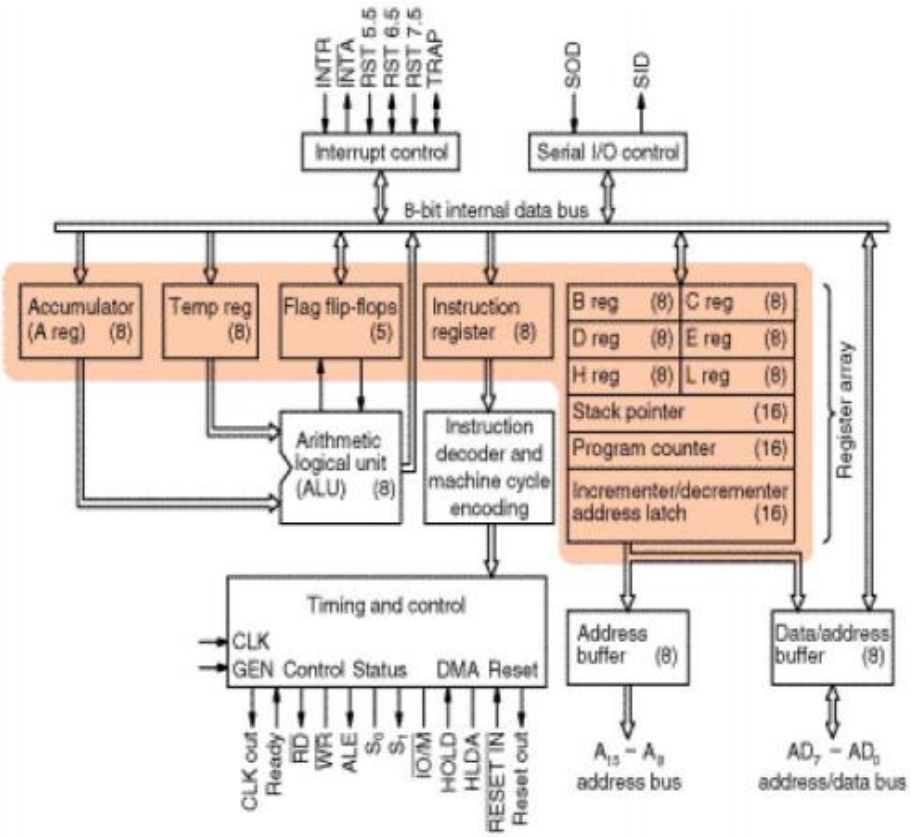


Output characteristics of a n-p-n transistor in CE configuration

b)Draw block diagram of microprocessor and state the function of each block.

Ans: (Block diagram -2M, Function of blocks- 2M)

Any relevant block diagram can be considered



Registers: The 8085 includes six registers, one accumulator, and one flag register, as shown in Figure. In addition, it has two 16-bit registers: the stack pointer and the program counter. The 8085 has six general-purpose registers to store 8-bit data; these are identified as B, C, D, E, H, and L.

Program Counter (PC): This 16-bit register deals with sequencing the execution of instructions. This register is a memory pointer. The microprocessor uses this register to sequence the execution of the instructions. The function of the program counter is to point to the memory address from which the next byte is to be fetched. When a byte is being fetched, the program counter is automatically incremented by one to point to the next memory location.

Stack Pointer (SP): The stack pointer is also a 16-bit register, used as a memory pointer. It points to a memory location in R/W memory, called stack. The beginning of the stack is defined by loading 16-bit address in the stack pointer.

Arithmetic & Logic Unit (ALU) : It performs various arithmetic and logic operations. The data is available in accumulator and temporary/general purpose registers.

Arithmetic Operations: Addition, Subtraction, Increment, Decrement etc.

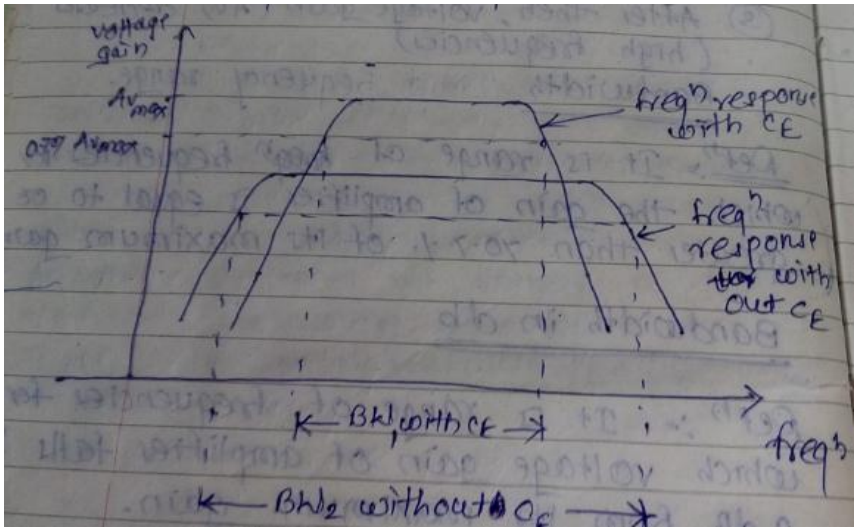
Logic Operations: AND, OR, X-OR, Complement etc.

b) State the effect of coupling capacitor and bypass capacitor on bandwidth

Ans: (Effect of coupling capacitor-2M, Effect of bypass capacitor-2M)

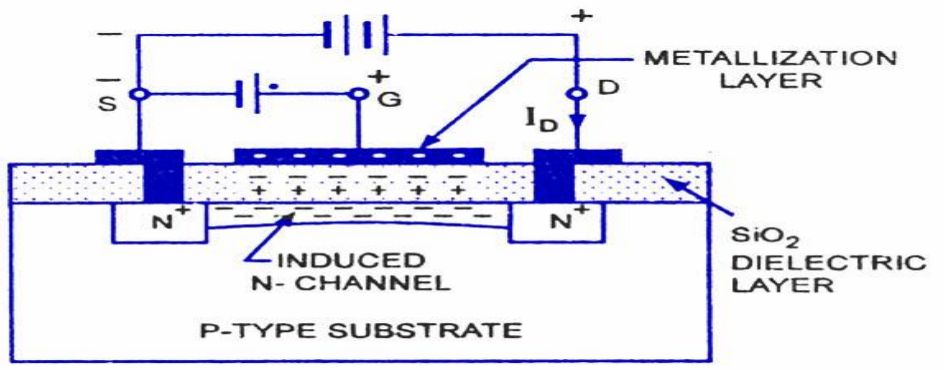
1. Due to coupling capacitors in amplifier voltage gain of amplifier reduces at low frequency because reactance of capacitor ($Xc = \frac{1}{2\pi fc}$). As voltage gain of amplifier decreases, bandwidth increases in amplifier because in amplifier gain bandwidth product is always constant.

2. Due to bypass capacitor C_E connected in amplifier allows an easy path for AC i.e. it bypasses the as current and hence it avoid any voltage drop across RE resistance and hence avoid drop in voltage gain . If bypass capacitor is not used ,Ac current will flow through RE ,which will cause voltage drop across RE producing negative feedback and hence amplifier gain will reduce. So due to bypass capacitor bandwidth increases as voltage gain reduces.



c) Describe the operation of N channel enhancement type MOSFET with diagram

Ans: (Diagram-2M,Operation -2M)



Operation of N-Channel E-MOSFET

As its name indicates, this MOSFET operates only in the enhancement mode and has no depletion mode. It operates with large positive gate voltage only. It does not conduct when the gate-source voltage VGS = 0. This is the reason that it is called normally-off MOSFET. In these MOSFET's drain current ID flows only when VGS exceeds VGST [gate-to-source threshold voltage].

When drain is applied with positive voltage with respect to source and no potential is applied to the gate two N-regions and one P-substrate from two P-N junctions connected back to back with a resistance of the P-substrate. So a very small drain current that is, reverse leakage current flows. If the P-type substrate is now connected to the source terminal, there is zero voltage across the source substrate junction, and the–drain-substrate junction remains reverse biased.

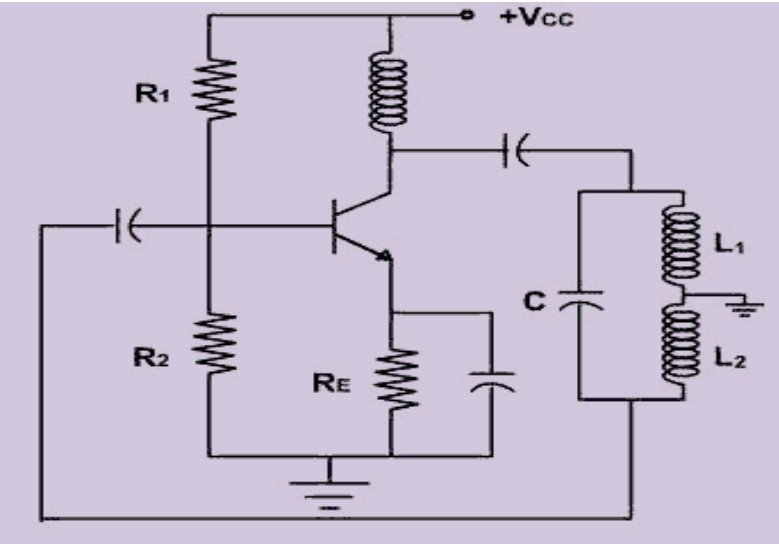
When the gate is made positive with respect to the source and the substrate, negative (i.e. minority) charge carriers within the substrate are attracted to the positive gate and accumulate close to the-surface of the substrate. As the gate voltage is increased, more and more electrons accumulate under the gate.

Since these electrons cannot flow across the insulated layer of silicon dioxide to the gate, so they accumulate at the surface of the substrate just below the gate. These accumulated minority charge carriers N -type channel stretching from drain to source. When this occurs, a channel is induced by forming what is termed an inversion layer (N-type). Now a drain current start flowing. The strength of the drain current depends upon the channel resistance which, in turn, depends upon the number of charge carriers attracted to the positive gate. Thus drain current is controlled by the gate potential.

d) Draw circuit diagram of Hartley oscillator give function of each component.

Ans: (Circuit diagram 2M, Function of each component- 2M)

Circuit diagram:



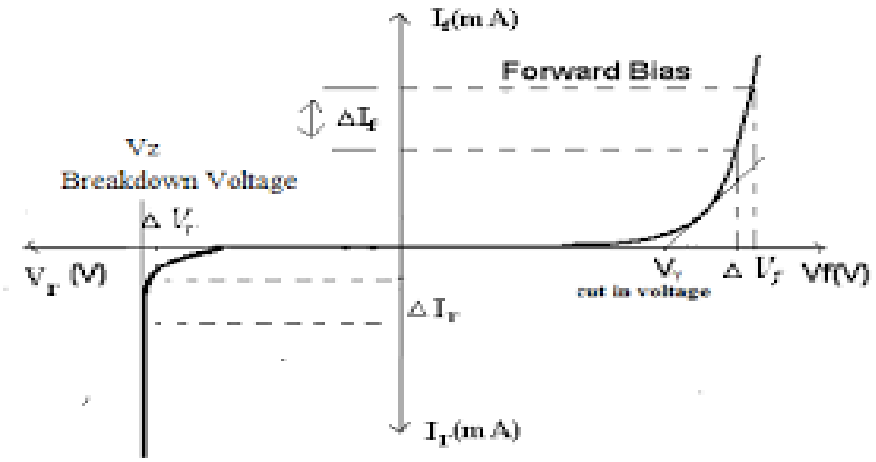
Function of each component:

1. An NPN transistor connected in a common emitter configuration works as the active device in amplifier stage and CE configuration provides 180°phase shift.
2. R1 and R2 are biasing resistors and RE is used for stabilization of operating point against β variations.
3. RFC is the radio frequency choke, which provides the isolation between AC and DC operation.
4. CE is the emitter bypass capacitor andCC1 and CC2 are the coupling capacitors.
5. L1 and L2 forms tank circuit which also The mutual inductance between L1 and L2 provides the feedback of energy from collector-emitter circuit to the base-emitter circuit.

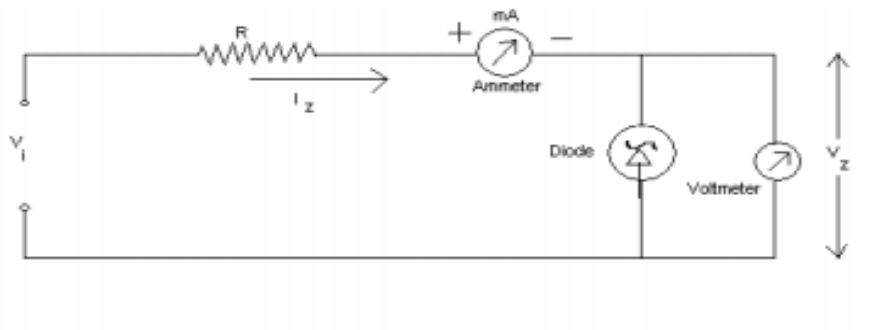
e) Draw forward and reverse characteristics of Zener diode with neat circuit diagram.

Ans: (Labeled each characteristics-2M, Circuit diagram-2M)

Forward Characteristics and Reverse Characteristics:



Circuit diagram:

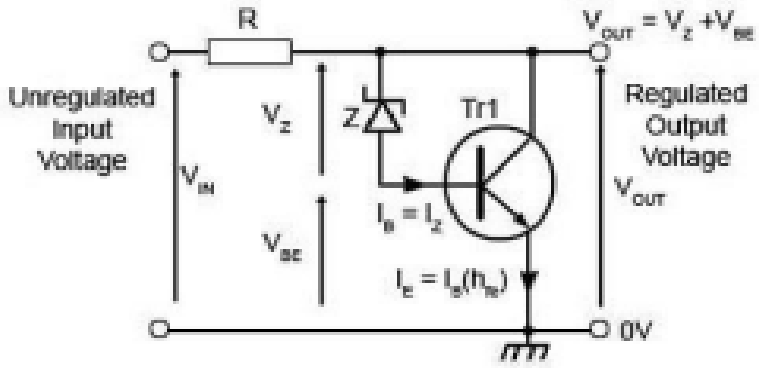


Q. 5: Attempt any FOUR of the following **16 M**

a) Describe the operation of transistorized shunt voltage regulator with neat circuit diagram.

Ans: (Circuit diagram-2M, Operation-2M)

Circuit Diagram:



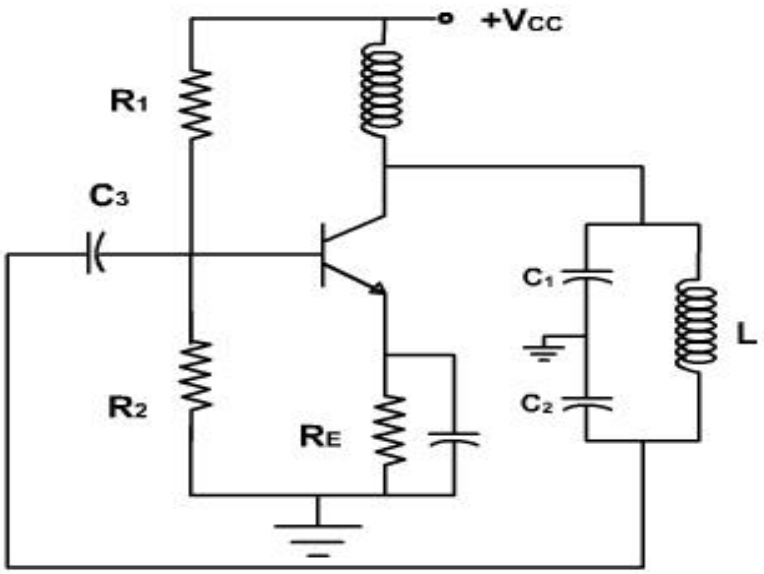
Operation:

- From the above circuit the load voltage is given by
- $V_L = V_Z + V_{BE}$ Or $V_{BE} = V_L - V_Z$ ..... (i)
- Since the load voltage for a given zener diode is fixed, therefore any decrease or increase in load voltage will have a corresponding effect on the base to emitter voltage V_{BE}.
- The unregulated input voltage increases, load voltage also increases. As a result of this from equation (i) above, we find that V_{BE} is also increases. And the base current I_B increases. Due to this the collector current I_C also increases. This causes the input current (I_S) to increase, which in turn increases the voltage drop across series resistance (V_{RS}) . Consequently, the load voltage decreases.
- If the output voltage decreases then V_{BE} will decrease. This will reduce the collector current Ic. So more current will flow through the load and the load voltage will increase. This increase in load voltage will compensate the initial decrease in load voltage. Thus output voltage gets regulated.

b) Draw the circuit diagram of colpitts oscillator , colpitts oscillator has C1=250PF, C2-100PF & L=60µH,Find the value of frequency of oscillation.

Ans: (Circuit diagram-2M, Frequency of oscillation-2M)

Circuit Diagram:



Given :

C1=250PF, C2=100PF, L=60µH

Find f_{osc}

Frequency of oscillation

$$f_{osc} = \frac{1}{2\pi\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

=2.

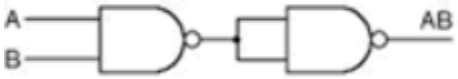
431 *10^6 H_Z

c) Why NAND is called universal gate ? , implement OR, AND, using NAND gate ?

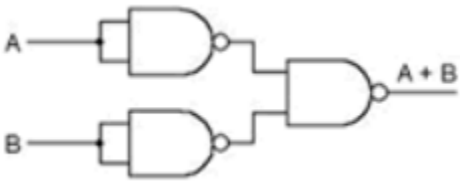
Ans: (Explanation-1M, Gates using NAND-3M)

NAND is called universal gate because using only NAND gate one can implement any Boolean function or equation and any logic gate.

Implementation OR, AND, using NAND gate



AND gate using NAND



OR gate, using NAND

d) Compare CB, CE and CC configurations on the basis of

i) Input impedance

ii) Current gain

iii) Voltage gain

iv) Output impedance

Ans: (Each point-1M)

Comparison between CB, CE and CC configurations

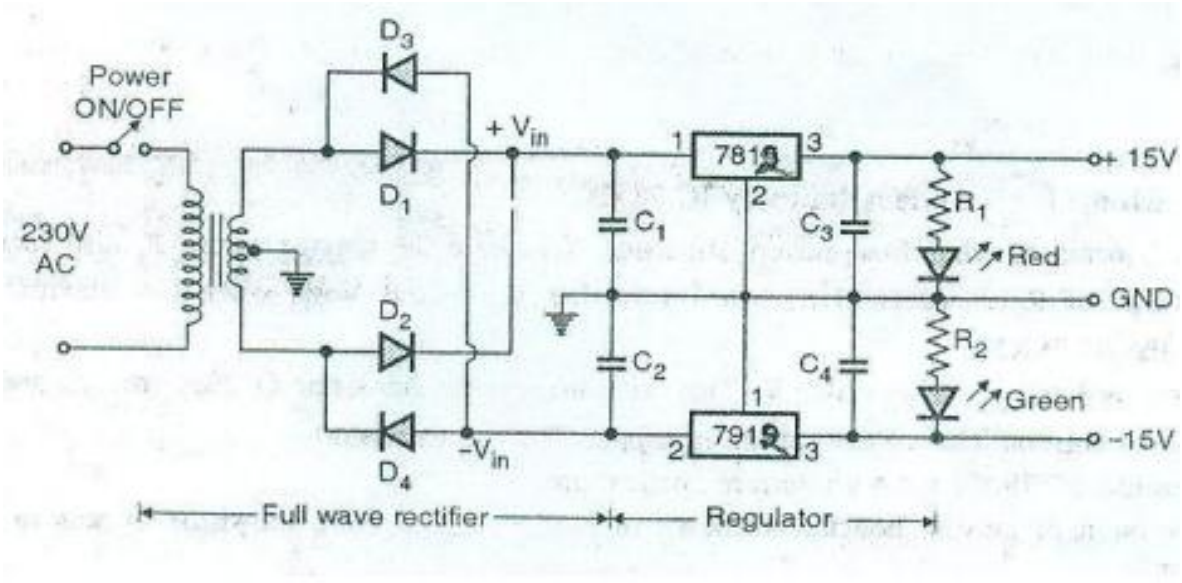
Parameter	CB	CE	CC

I/P impedance	Low Or Typical 50Ω	Medium Or 600 Ωto 4kΩ	High Or 1 MΩ
Current Gain	Less than or equal to 1	High	High
Voltage Gain	Medium	Medium	Less than or equal to 1
Output Impedance	High	Medium	Low

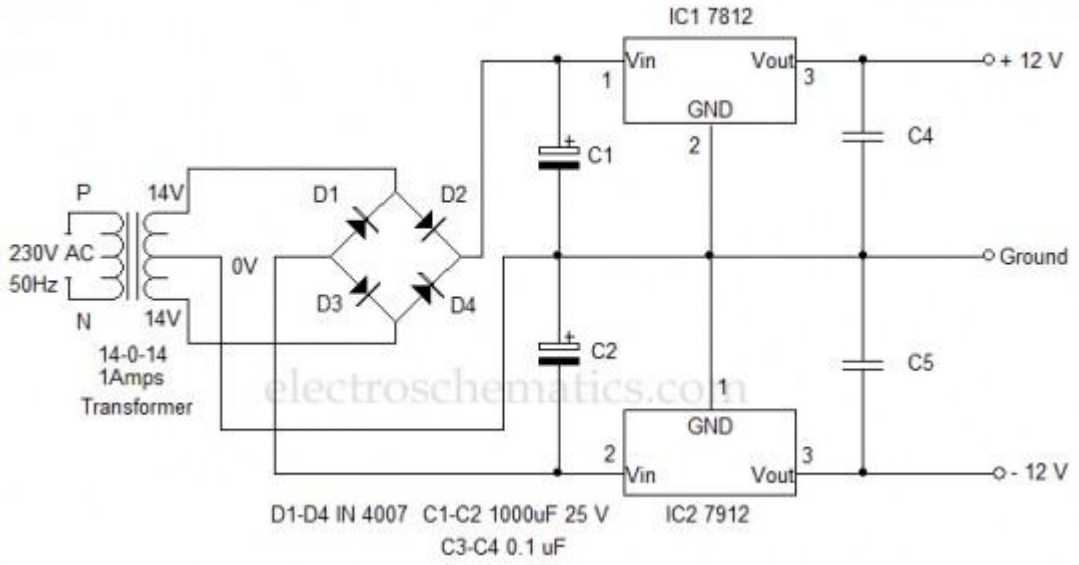
e)Construct a dual power supply capable of supplying ±12 V using 78XX &79XX IC's.

Ans: (Neat labeled diagram -4M)

Note: Any relevant diagram can be consider



OR



1. **Define the terms w.r.t transistor**

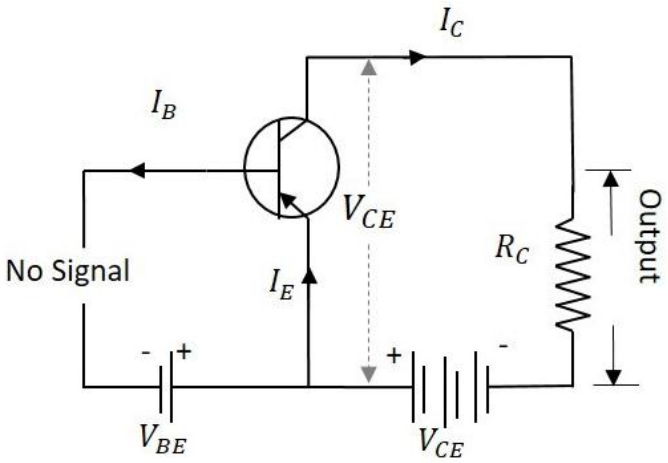
i. **DC load line**

ii. **Operating point**

Ans: (Each term -2M)

i) **DC load line:**

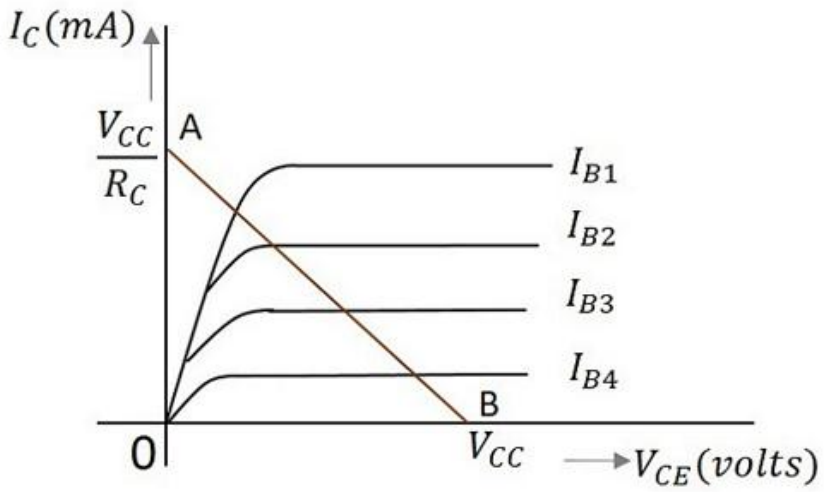
When the transistor is given the bias and no signal is applied at its input, the load line drawn at such condition, can be understood as DC condition. The dc load line is the locus of IC and VCE at which BJT remains in active region i.e. it represents all the possible combinations of IC and VCE for a given amplifier. Here there will be no amplification as the signal is absent. The circuit will be as shown below.



The value of collector emitter voltage at any given time will be

VCE=VCC−ICRCVCE=VCC−ICRC

As VCC and RC are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as D.C. Load line.

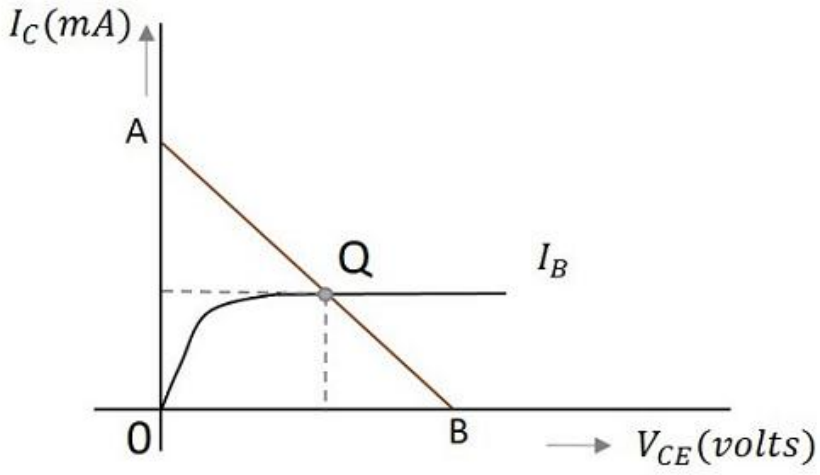


ii. Operating point:

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the saturation point. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the cutoff point.

When a line is drawn joining these two points, such a line can be called as Load line. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as Operating point.

This operating point is also called as quiescent point or simply Q-point. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region. This can be better understood through the figure below.



Q. 6: Attempt any FOUR of the following **16 M**

a) State the concept of feedback and Barkhausen criteria in oscillator.

Ans : (Concept-2M, Criteria-2M)

Concept of feedback: Feedback is process to fed back part of output to the input. Feed back concept is introduced in amplifier to improve the parameters of amplifier like voltage gain, current gain, stability, bandwidth. There are two types of feedback depending upon whether output increases or decreases.

There are four different types of feedback topologies based on type of output signal and feedback signal (voltage or current signal). Voltage feedback is taken in series with the load and current feedback is taken in shunt with the load. They are

a) Voltage-series: Output signal is voltage signal, feedback signal is voltage signal.

b) Current series: Output signal is current signal, feedback signal is voltage signal.

c) Current shunt: Output signal is current signal, feedback signal is current signal

d) Voltage shunt: Output signal is voltage signal, feedback signal is current signal.

Barkhausen's Criterion for Oscillations

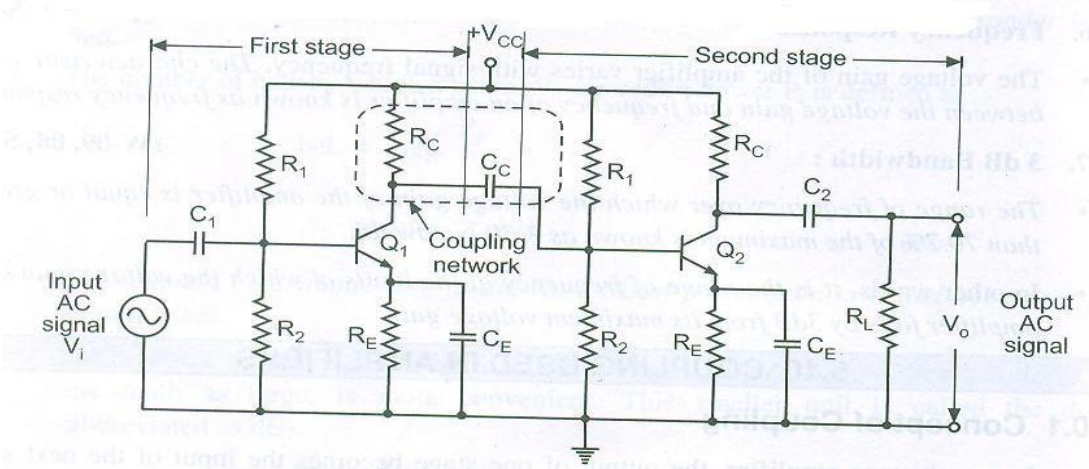
The necessary condition for sustained oscillations are

1. Product of voltage gain and feedback factor should be equal to and greater than Loop gain ($\beta.Av) \geq 1$

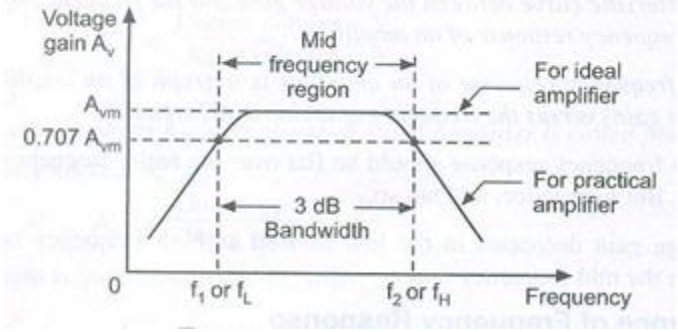
2. Phase shift between the input and output signal or around the loop must be equal to 360^0 or 0^0.

b) Draw two stage RC coupled amplifier and draw its frequency response .

Ans:(Circuit diagram-2M,Frequency response -2M)



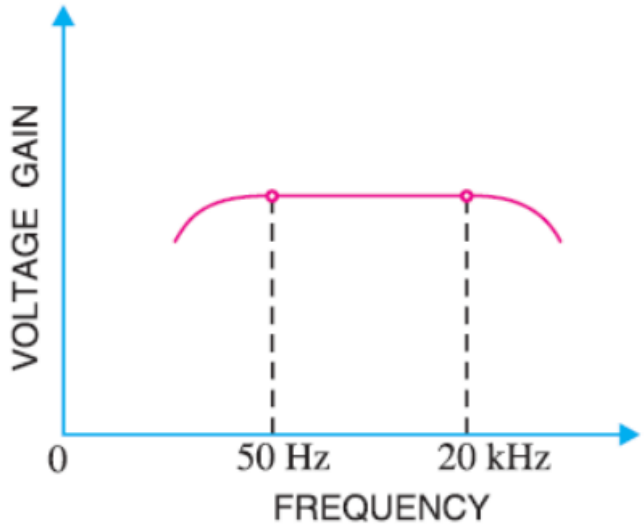
Two-stage RC coupled CE amplifier



Frequency response of RC coupled two stage amplifier

c) Draw frequency response of single stage CE amplifier and explain why the gain of amplifier falls at low and high frequency.

Ans: (Frequency response-2M, Explanation-2M)



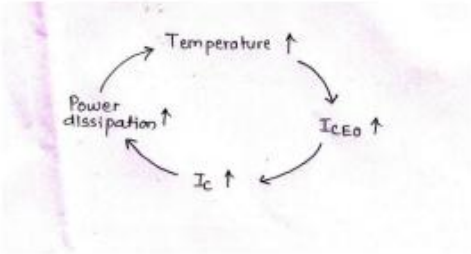
Explanation of why the gain of amplifier falls at low and high frequency:

1. 1. Due to coupling capacitors and bypass capacitor in amplifier voltage gain of amplifier reduces at low frequency because reactance of capacitor ($Xc = \frac{1}{2\pi fc}$).
2. While at higher frequency gain of amplifier reduces due to internal capacitances /parasitic capacitors transistor.

d) What do you mean by thermal runaway? And how it should be avoided?

Ans: (Thermal runaway-2M , To avoid thermal runaway-2M)

Thermal Runaway



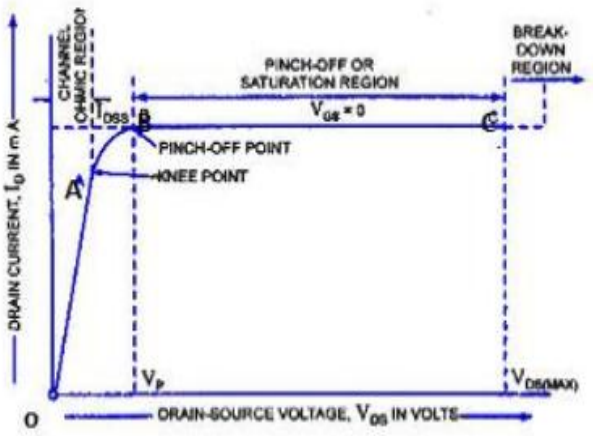
1. The reverse saturation current in semiconductor devices changes with temperature. The reverse saturation current approximately doubles for every 10^0 c rise in temperature.
2. As the leakage current of transistor increases, collector current (Ic) increases
3. The increase in power dissipation at collector base junction.
4. This in turn increases the collector base junction causing the collector current to further increase.
5. This process becomes cumulative. & it is possible that the ratings of the transistor are exceeded. If it happens, the device gets burnt out. This process is known as 'Thermal Runaway'.

Thermal runaway can be avoided by
1) Using stabilization circuitry
2) Heat sink

e) Draw drain characteristic of FET showing different operating region and briefly describe each region .

Ans : (Drain characteristic-2M, Operating region-2M)

Drain/output Characteristics of JFET:



JEFT Drain Characteristic With Shorted Gate

- **Ohmic region**: This region is shown as line OA in the figure. In this region the ID increases linearly with increase in VDS obeying ohms law. ***(1 mark)***

- **Pinch off region:** It is also called as saturation region or constant current region. In this region the ID remains constant at its maximum value (IDSS) ***(1 mark)***

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})\text{^}2$$

f) Compare half wave ,center tap FWR and bridge FWR on the basis of (i) Ripple factor (ii) Rectification efficiency (iii) TUF and (iv) Waveforms

Ans . [Any four points: 4 M]

Sr.No	Parameters	Half Wave	Centre tap	Bridge Full Wave
I	Ripple Factor	1.21	0.482	0.482
ii	Rectification efficiency efficiency, η_{max}	40.6%	81.2%	81.2%
iii	Transformer utilization factor(TUF)	0.324	0.671	0.813
iv	Waveforms