Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

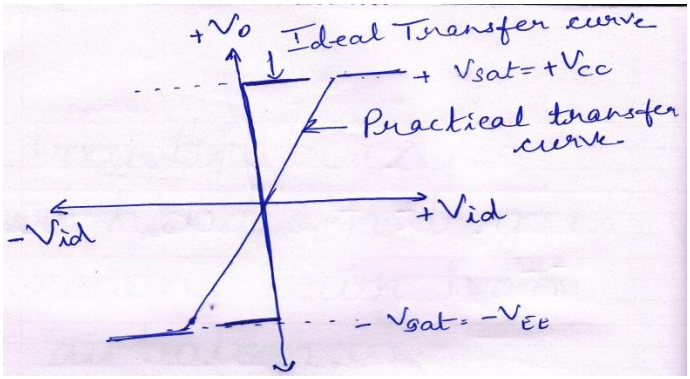
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1) a) Attempt any Six of the following: (12 Marks)

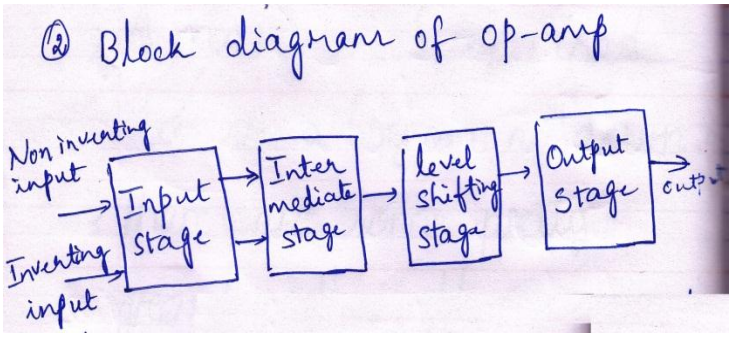
i) Draw ideal and practical transfer characteristics of op-Amp.

Ans: - (Ideal: 1M, practical: 1M)



ii) Draw Block diagram of op-Amp. State function of each block.

Ans:- Block Diagram of op-Amp: (diagram 1M, Explanation 1M)

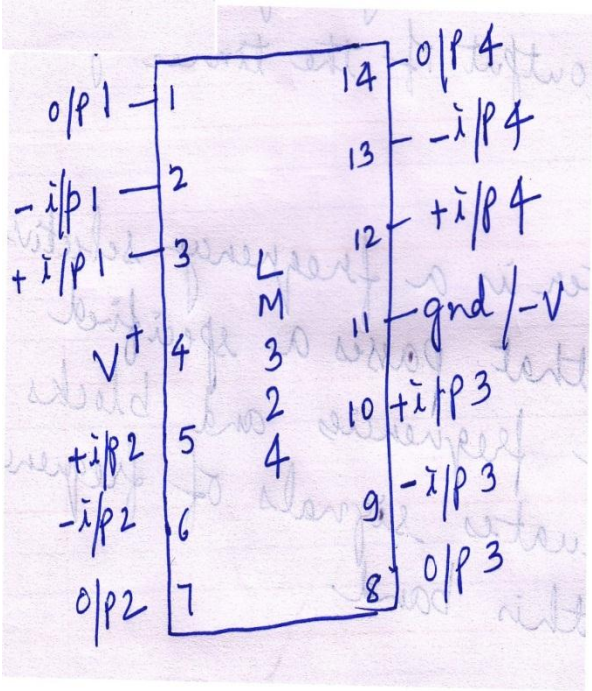


The input stage is the dual input balanced output differential amplifier provides most of the voltage gain Intermediate stage provides additional gain Level shifter shifts the de level of the output to Zero volt with respect to ground. The output stage increases current output voltage swing and provides low output resistance.

iii) Draw Pin diagram of IC LM324.

Ans:- Pin Diagram of IC LM324 : (2M)

It is a low power quad operational amplifier.



iv) State functions of the following pins of IC555.

Ans:- **(1M each)**

1) **Control: -** The dc Voltage at this pin is 2/3 $V_{cc.}$ An external voltage applied to this changes threshold as well as trigger voltage to obtain pulse width modulated output.

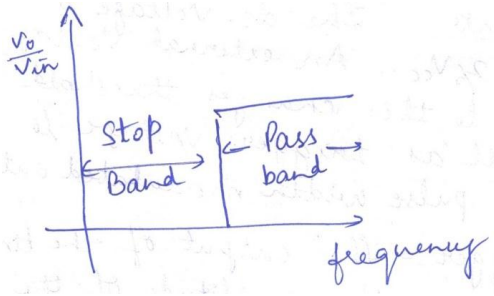
2) **Trigger: -** The output of the timer depends on the amplitude of the pulse applied to this pin. Output is low of the voltage at this pin is greater than 2/3 V_{cc} . When the voltage goes below 1/3 $V_{cc,}$ output of the timer goes high.

v) State the function of filter. Draw response of high pass filter.

Ans:- **(Definition 1M, Diagram1M)**

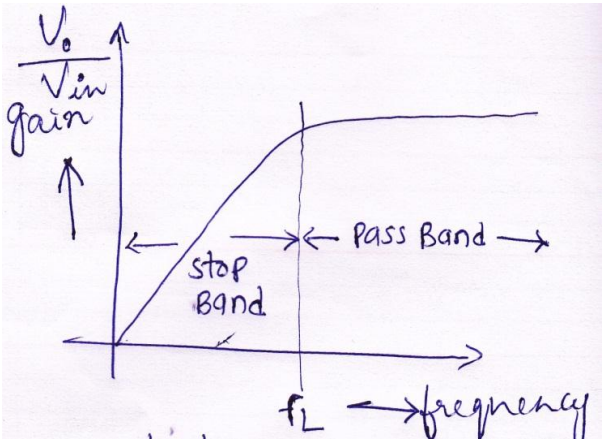
Filter is a frequency selective circuit that passes a specified band of frequency and blocks or attenuates signals of frequencies outside this band.

Ideal response:-



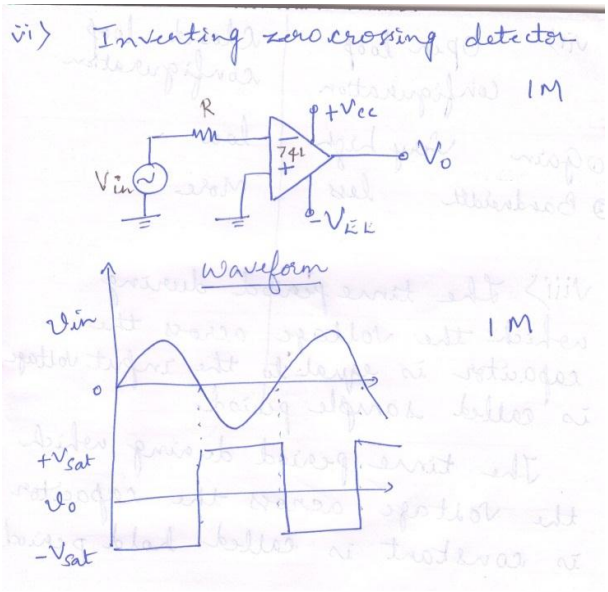
Or

Practical Response:-



vi) Draw inverting Zero crossing detector and its waveform with circuit diagram.

Ans: - Inverting Zero Crossing Detector: - (Circuit 1M, Waveform 1M)



vii) Compare Open Loop and Closed Loop configuration on basis of:

1) **Gain.**
2) **Bandwidth.**

Ans:- (1M each)

Parameter	Open Loop Configuration	Closed Loop Configuration
Gain	Very High(∞)	Low(Depends upon feedback elements)
Bandwidth	Less (Ideal value 0)	More

viii) Define Sample and hold period with reference to S/H circuit.

Ans:- **(1M each)**

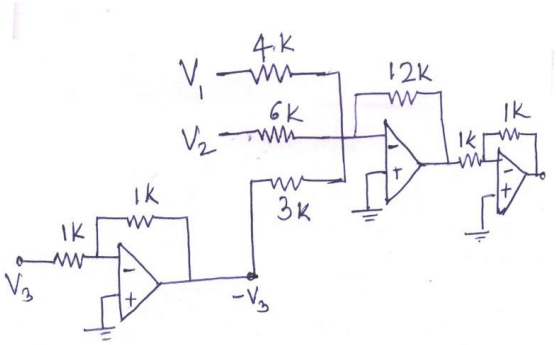
Sample Period:- The time period during which the voltage across the capacitor is equal to the input voltage is called sample period.

Hold Period:- The time period during which the voltage across the capacitor is constant is called hold period.

Q1) b) Attempt any Two of the following:- **(8 Marks)**

i) Draw circuit diagram to generate the following output using op- Amp:
$V_0 = 3V_1 + 2V_2 - 4V_3$.
V_1, V_2, V_3, are input voltages.

Ans:- **(4M)**



$$V_0 = 3V_1 + 2V_2 - 4V_3$$

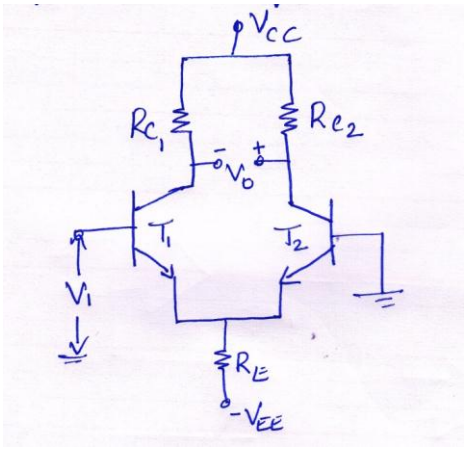
$$V_0 = \frac{12K}{4K}V_1 + \frac{12K}{6K}V_2 - \frac{12K}{3K}V_3$$

Note:- Any other circuit which gives the same output should be considered.

ii) Draw single i/p balanced o/p differential amplifier and define the term balanced o/p and unbalanced o/p.

Ans:- **(diagram 2M, Definition 2M)**

Single input balanced output differential amplifier:



In this circuit, one input is applied at the base of one transistor and the base of other transistor is grounded. The output is taken across the collector of the both transistor.

Definition of Balanced output:-

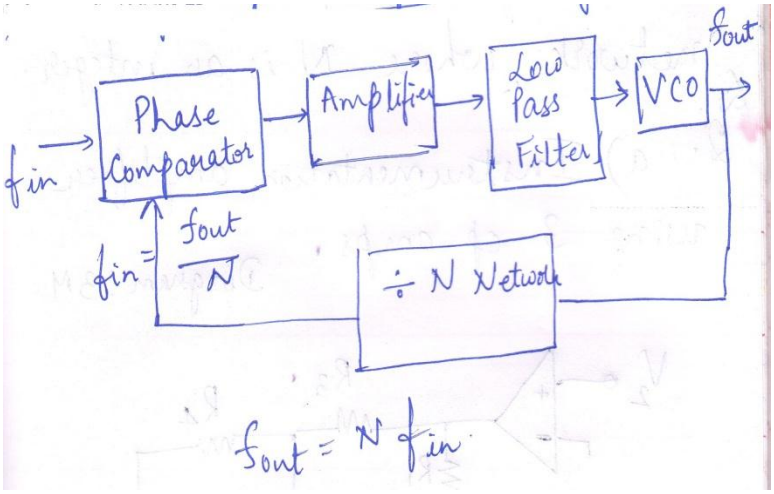
When the output is taken between the collectors of T_1 & T_2, it is called balanced output.

Definition of Unbalanced output:-

When the output is taken across the collector of T_1 or T_2 with respect to grounded, it is called unbalanced output.

iii) Draw block diagram of frequency multiplier and describe its working using PLL.

Ans:- Frequency multiplier using PLL : (diagram 2M, explanation 2M)



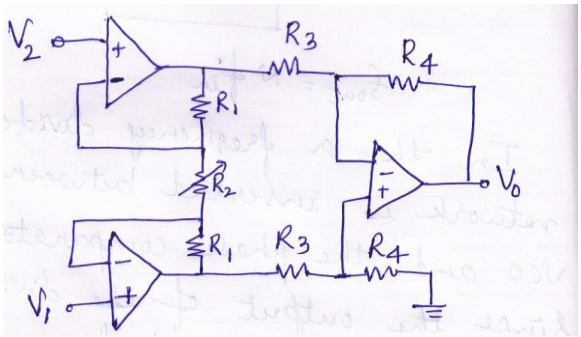
In this a frequency divider network is inserted between the VCO and the phase comparator since the output of the divider is locked to the input frequency f in, the VCO is actually running at a multiple of the frequency.

The desired amount of multiplication can be obtained by selecting a proper divide by N network, Where N is an integer.

Q2) Attempt any Four of the following:- (16 Marks)

a) Draw instrumentation amplifier using 3 op-Amps. State its voltage gain equation.

Ans: - Instrumentation amplifier using 3 op-Amps: (Diagram 3M)

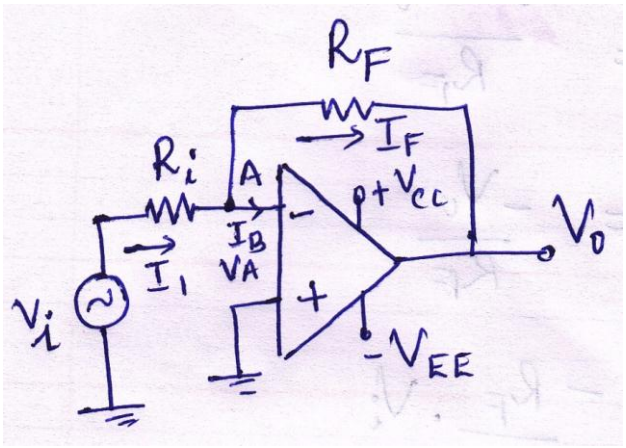


Equation:- (1M)

$$V_O = \frac{R4}{R3}\left(1 + \frac{2R1}{R2}\right)(V1 - V2)$$

b) Draw closed loop inverting amplifier and derive expression for voltage gain.

Ans:- Closed Loop Inverting amplifier: (Diagram 2M, Derivation 2M)



Apply KCL at point A,

$I_1 = I_B + I_F$ —— (1)

But $I_B = 0$ due to virtual grounding

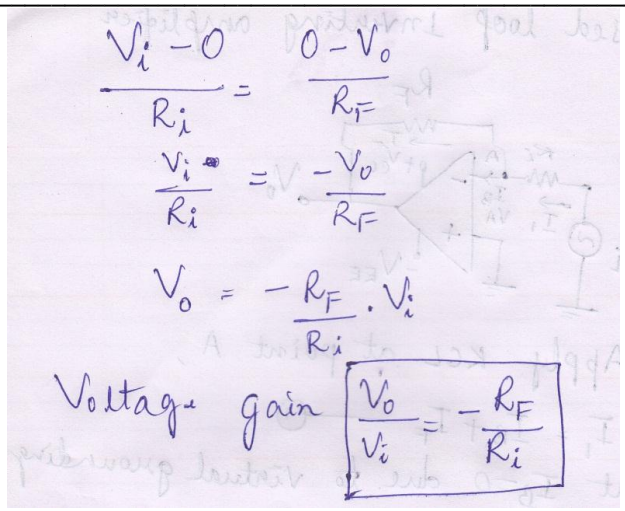
So $I_1 = I_F$ — (2)

Ohm's law $I = \frac{V}{R}$

$I_1 = \frac{V_i - V_A}{R_i}$ & $I_F = \frac{V_A - V_0}{R_F}$

$\therefore \frac{V_i - V_A}{R_i} = \frac{V_A - V_0}{R_f}$

$V_A = 0$, due to virtual grounding.



c) State ideal and typical value of the following parameters of IC741.

i) Supply voltage rejection ratio SURR.

ii) Common mode rejection ratio (CMRR).

iii) Slew rate.

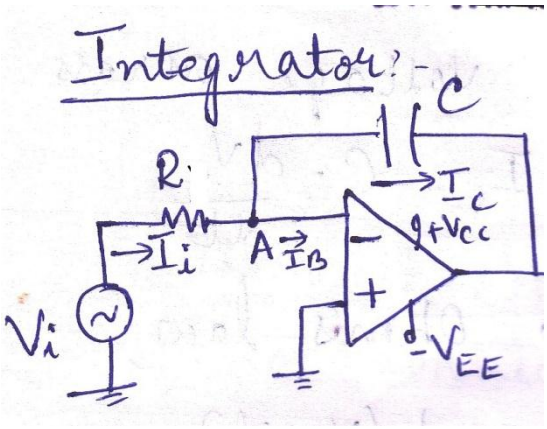
iv) Unity gain bandwidth.

Ans:- **(1M each)**

Parameter	Ideal	practical
Supply voltage rejection ratio (SURR)	**0**	**150µ v/v**
Common mode rejection ratio (CMRR).	∞	**90 dβ**
Slew rate.	∞	**0.5v/ µs**
Unity gain bandwidth.	∞	**1MHz**

d) Draw basic integrator and derive the expression for its output voltage.

Ans:- Integrator: **(2M diagram, 2M Explanation)**



A circuit in which the output voltage waveform is the integral of the input voltage is called integrator. In this the feedback resistor of an inverting amplifier is replaced by a capacitor.

Apply KCL at node A,

$$I_i = I_B + I_C$$
$$= I_C \quad \because I_B = 0$$

The relationship between current through and voltage across capacitor is

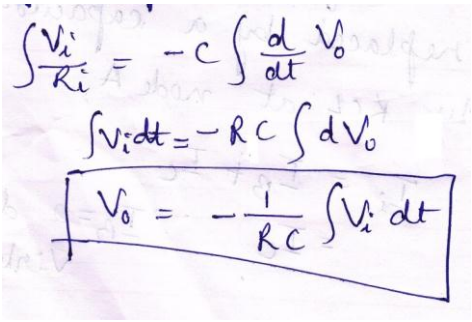
$$I_C = C \cdot \frac{dV_c}{dt}$$

According to Ohm's law

$$\frac{V_i - V_A}{R} = C \cdot \frac{d(V_A - V_o)}{dt}$$
$$\frac{V_i}{R} = C \cdot \frac{d}{dt}(-V_o) \quad \because V_A = 0$$

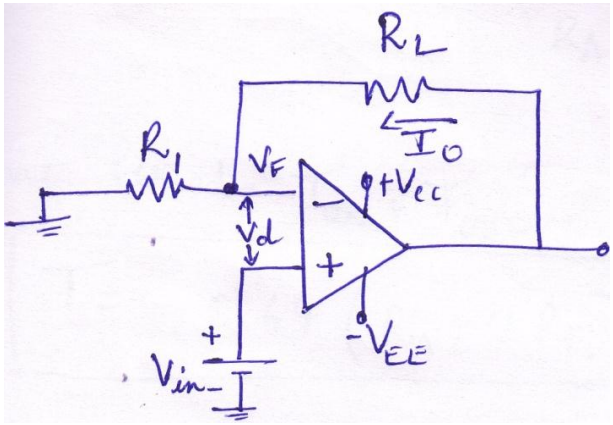
,

Integrating both sides,



e) Draw circuit diagram of V-I converter of floating load. Derive expression for its output.

Ans**: - V-I converter of floating load: (2M diagram, 2M Explanation)**



The load resistor R_2 is floating in, not connected to ground.

The input voltage is applied to the non-inverting input terminal and the feedback voltage across R_1 drives the inverting terminal.

Writing KVL to the input loop,

$Vin = Vid + V_F$

But Vid= Ov since A is very large,

$Vin = V_F$

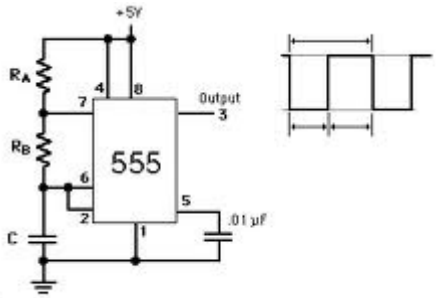
$Vin = R_1 I_o$ **OR** $I_o = \frac{Vin}{R1}$

Output current is proportional to input voltage. Input voltage is converted into an output current.

f) Draw circuit diagram of astable M/V using IC555. State its frequency equation, duty cycle, time period.

Ans:- **(each 1M)**

Astable multivibrator using 555:



Duty cycle =

$$\frac{T_{ON}}{T} = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

Time period =

$$\text{Time Period} = T_{ON} + T_{OFF}$$

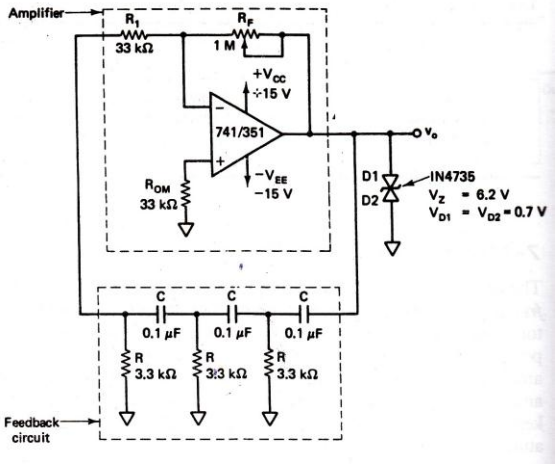
$$T = 0.69 (R_A + 2R_B) C$$

Frequency f = $\frac{1.45}{(RA + 2RB)\,C}$

Q. 3) Answer any FOUR of the following: (16Marks)

a) Draw phase shift oscillator using IC 741. Explain the function of each component in it. State the equation for o/p frequency.

Ans: (Dig. – 2M, Explanation- 1 M, Equation- 1 M)



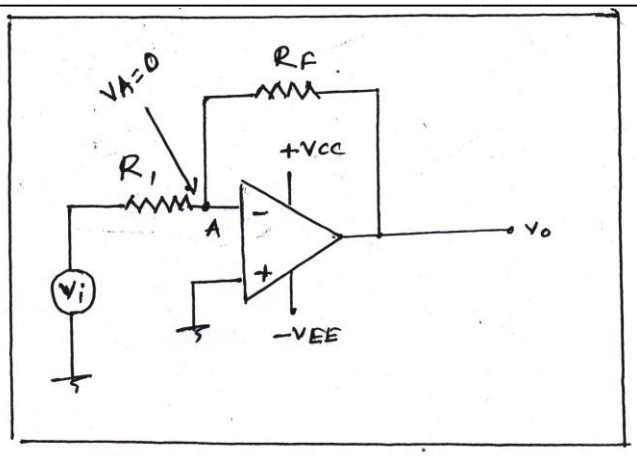
- The feedback circuit provides feedback voltage from the output back to the input of the amplifier.
- The op-Amp is used in inverting mode therefore any signal appears at the inverting terminal is shifted by 180^0 at the output.
- Three RC cascaded networks provides additional 180^0 phase shift required for oscillation.
- Equation for output frequency:

$$f_o = \frac{1}{2\pi\sqrt{6}RC} = \frac{0.065}{RC}$$

b) Describe the concept of virtual ground with reference to op-Amp.

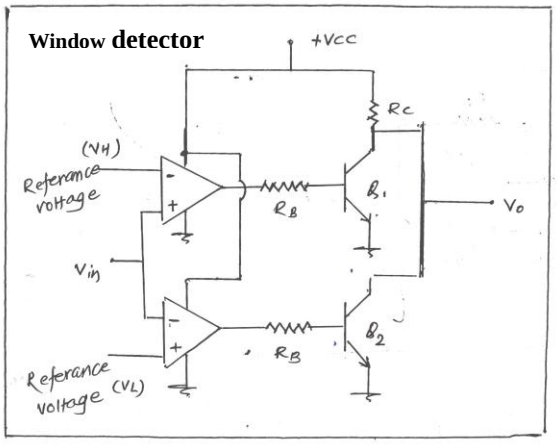
Ans: (4 Marks)

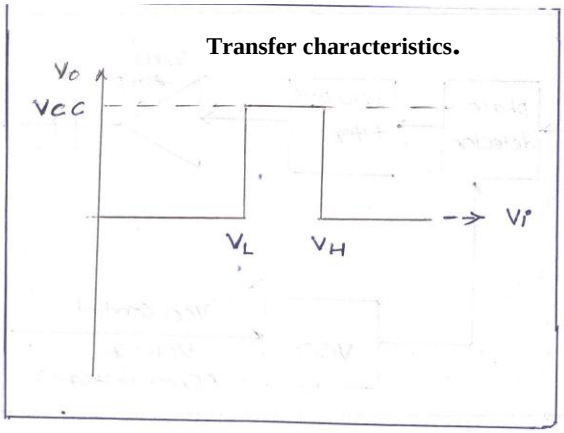
In circuit point V_A is virtual ground. Figure shows inverting amplifier using op-amp. In this circuit non-inverting terminal is connected to the actual ground. Due to this potential of inverting terminal become zero. Thus, inverting terminal is not actually connected to the ground. There after its potential is zero. Thus point V_A is known as virtual ground point. This phenomenon of having zero potential without actually grounding is known as virtual ground concept.



c) Draw window detector using op-Amp & give transfer characteristics.

Ans: **(Diagram – 2 M, Characteristics- 2M)**





d) Compare comparator & Schmitt trigger on basis of

- **i) Definition**
- **ii) Feedback**
- **iii) Hysteresis**
- **iv) External reference voltage.**

Ans: **(1 M Each)**

Comparison:

Sr. No.	Parameter	Comparator	Schmitt trigger
1	**Definition**	It compares the two input voltages.	It converts any wave shape into square waves.
2	**Feedback**	In Comparator, open loop system	It uses positive feedback
3	**Hysteresis**	It does not exhibit hysteresis	It exhibit hysteresis
4	**External reference voltage.**	It has only one reference voltage	It has two reference voltage V_{UTP}

e) What do you mean by active filter? State its advantages over passive filter (any four). Define pass band & stop band with respect to filter.

Ans: (Definition – 1 M, Advantages- 1 M, Definition – 1 M Each)

Active Filter:

Active Filter is formed by using active element along with the passive components.

Advantages of Active filter over Passive filter:

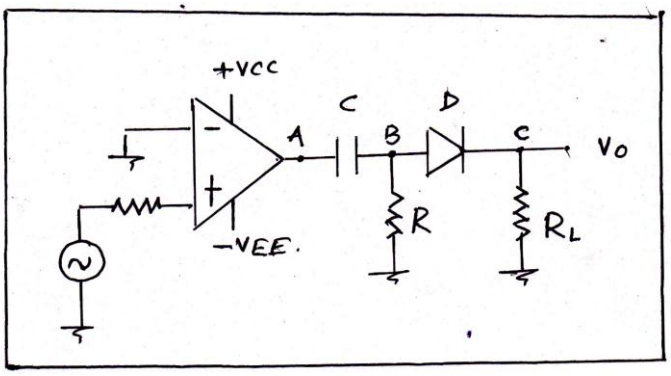
- High value of pass band gain can be obtained.
- It is very easy to select cut-off frequency.
- They will not produce loading effect because the output impedance is low.
- They are not using inductor so designing of Active filter is simple, cost is less & they occupy less space.

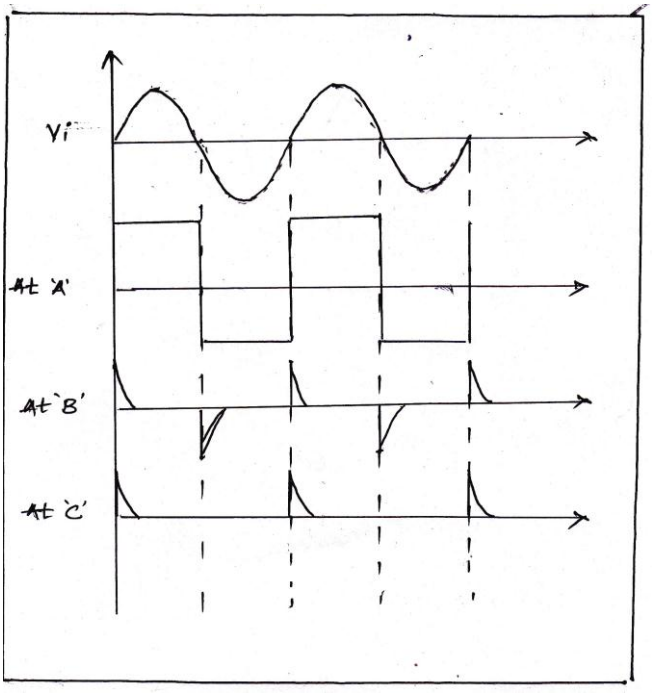
Pass Band Filter: The frequency range which is permitted to pass is known as pass band.

Stop Band Filter: The frequency range which is attenuated is known as stop band.

f) Draw & explain operation of phase detector.

Ans: **(Circuit Dig. – 2 M, Explanation- 2 M)**





- In phase detector, the op-Amp basically acts as a zero crossing detector. If a sine wave is applied at the i/p, we get square wave at the op-Amp o/p (at point A).
- The capacitor C & resistor R, from a passive differentiator so across R we get positive Negative spikes at the point B.

- When positive pulse or spike reaches at the anode of the diode. Hence diode becomes forward biased. Therefore it allows the spike to pass through the load.
- When negative spike will reach at point B, diode is reverse biased. Hence it does not pass the negative spike towards load. Thus we get the output across R_L or only positive spike.
- It can be used to measure phase angle & two voltages under the phase measurement are applied to two different pulse generation. These voltages are then converted into positive trigger pulse. These pulses are applied to two channel of the CRO. The time duration between the pulses corresponding to voltages represent the phase between them.

Q4) Attempt Any FOUR of the following: (16 Marks)

a) Design second order Butterworth high pass filter of cut off frequency 10KH$_Z$.

Ans:

Given Data :- cut-off freq $(f_L) = 10$ kHz

Solution :- Let $R_2 = R_3 = R$

$C_2 = C_3 = C = 0.1\ \mu F$ or (any other value bet^n 0.1μF to 1μF

Now

$$R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi \times 10\times10^3 \times 0.1\times10^{-6}}$$

$\therefore R = 159.15\ \Omega$ —— (01) Mark

Since $A_{Vf} = 1 + \frac{R_f}{R_1} = 1.586$

$\therefore R_F = 0.586 \cdot R_1$

Choose $R_1 = 10\ k\Omega$

$\therefore R_f = 0.586 \times 10 \times 10^3$

$\therefore R_f = 5.86\ k\Omega$ —— (01) Mark

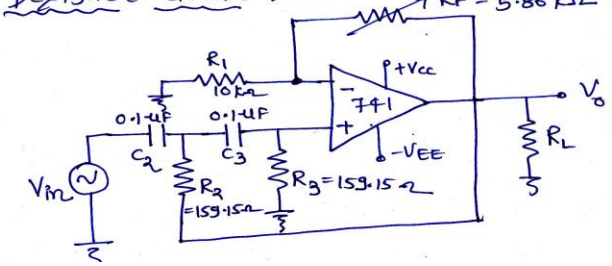
Hence the designed circuit component values are

$C_2 = C_3 = 0.1\mu F$

$R_1 = 10\ k\Omega$, $R_F = 5.86\ k\Omega$

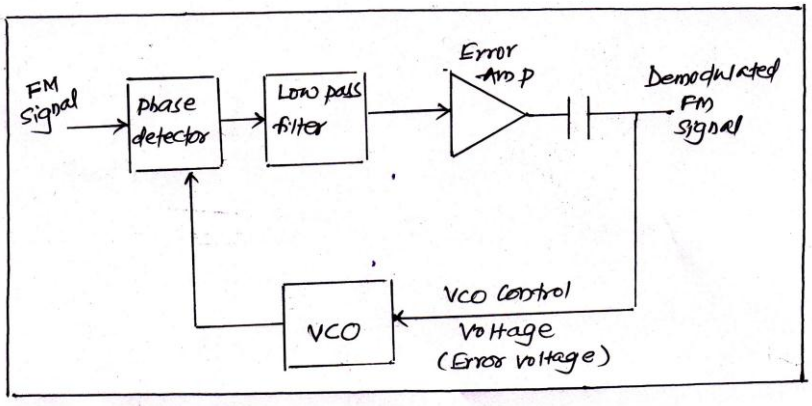
$R_2 = R_3 = 159.15\ \Omega$

Designed circuit :- —— (02) Mark.



b) Draw block diagram of PLL as a FM demodulator. Explain function of each block.

Ans: (Block diagram - 2 M, Explanation- 2M)

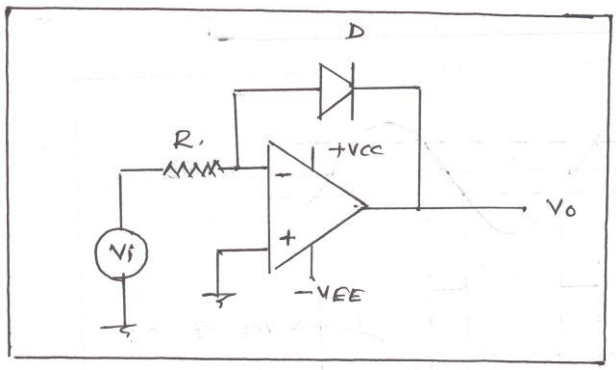


Operation:

- The FM signal which is to be demodulated is applied at the input of the PLL.
- the PLL is locked to the FM
- The error voltage produced at the output of the amplifier is proportional to the deviation of the input frequency from the center frequency of FM. Thus, the at component of the error voltage represents the modulating signal. Thus at the error amplifies output we get demodulated
- The FM demodulator using PLL ensures a high Linearity, between the instantaneous input frequency and VCO control voltage (error amplifier output)

c) Draw circuit diagram of a logarithmic amplifier. State its equation for output voltage.

Ans: (Circuit diagram – 3M, Equation- 1 M)



$$V_o = -\eta V_T \log_e \left[\frac{V_i}{V_{ref.}}\right]$$

d) Compare active integrator & active differentiator on basis of

i) Output voltage

ii) Feedback element

iii) Application in filter

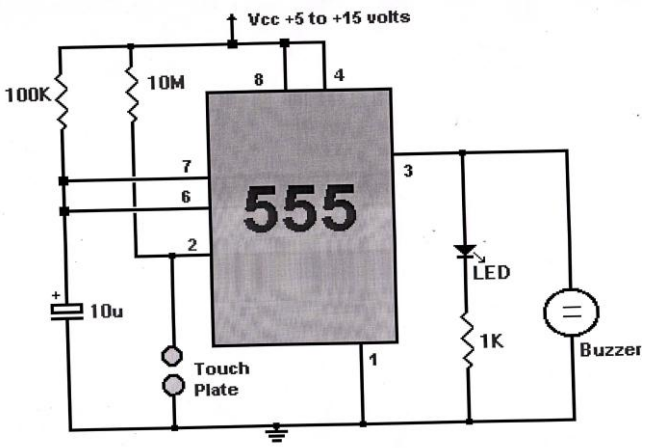
iv)Gain

Ans : (1 M Each)

Sr.no	Parameter	Active integrator	Active differentiator
1	**Output voltage**	$\therefore V0 = -\frac{1}{Ri.c}\int Vi.dt$	$\therefore V0 = -Ri.C.\frac{d}{dt}(Vi)$
2	**Feedback element**	Capacitor	Resistor
3	**Application in filter**	-A/D Converters -P/D controllers -filters -waveform generator	-logic circuits - pulse shaping filter - PID controllers
4	**Gain**	Decreased with increased in frequency	Increased with increased in frequency

e) Draw & explain touch plate switch using IC555.

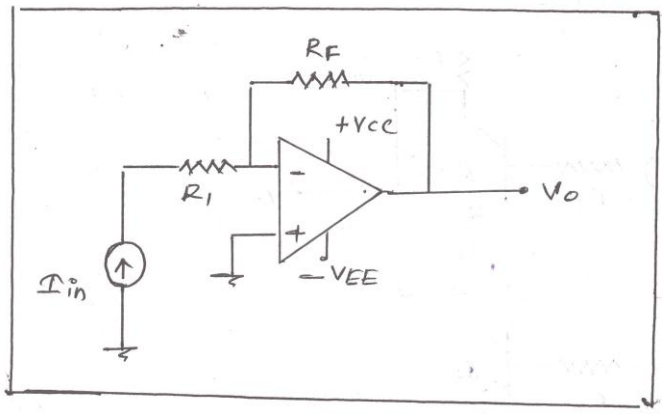
Ans:- **(Circuit Diagram. – 2 M, Explanation-2 M)**



It is construct form monostable multivibrator , when metal plates touch by finger then voltage at pin number 2 goes to below 1/3 Vcc then output of lower comparator becomes high hence flip flop set and output of timer goes high at the same time external capacitor start charging towards Vcc and when the voltage across capacitor slightly greater than 2/3 Vcc then output of upper comparator goes high hence flip flop reset then output of timer goes low and it low till up to the metal plates touch by finger **.**

f) Draw I-V converter using op-Amp. Derive expression for its output voltage.

Ans: **(Circuit Diagram. – 2 M, Derivation-2 M)**



The open loop gain A_V of the op-amp is very large. So as per the concept of virtual short, the input impedance of the op-amp is very high.

Therefore, the current entering into the two terminals is very small,

$I_{B1} = I_{B2} = 0$

The gain of inverting amplifier is

$$A_{V=\frac{V0}{Vin}=\frac{Rf}{R1}}$$

$$V_{0=-\frac{Rf}{R1}Vin--------1}$$

But, $V_1 = V_2$ & V_1 is connected to ground.

$V_1 = 0$

$$\therefore V_2 = 0$$

Thus the inverting terminal also is at ground potential & the entire I/P voltage across R_1 is

$$I_{in=\frac{Vin}{R1}}$$

$$\therefore V_{in} = I_{In\ R1-------2}$$

Now put the value Vin in equation 1 we get

$$V_o = \frac{-RF}{R1} * R1 * Iin$$

$$\therefore Vo = -Rf * Iin$$

Q. 5. Attempt any four of the following: (16 Marks)

a) Draw the circuit diagram of op-Amp based filter circuit which provides the following response. Describe its operation.(Refer Fig. No. 1)

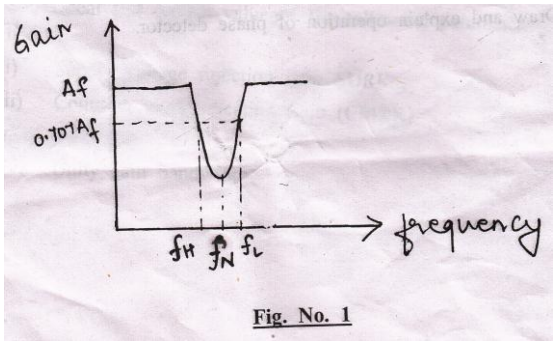
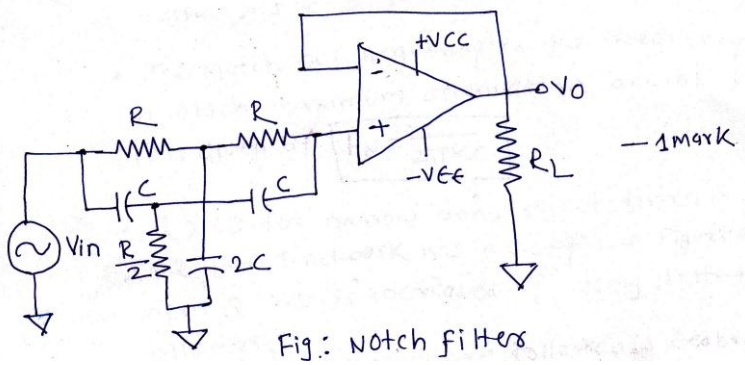


Fig. No. 1

Ans : Given response is a frequency response of notch filter.

OR

This is frequency response of narrow band reject filter. **(1 M)**



— 1mark

Fig.: Notch filter

Description of Operation: (2 M)

- Fig. shows a narrow band reject active filter often called as notch filter. It uses a Twin T-network.
- The Twin T-network is a passive filter consists of two T- shaped networks.
- One T-network is made up of two resistors and a capacitor while the other uses two capacitors and a resistor.
- The Notch out frequency is the frequency at which maximum attenuation occurs. It is given by

$$F_N = \frac{1}{2\pi RC}$$

- Q > 10 narrow band reject filter.
- The Twin T- network has a very low figure of merit that means Q. This is increased by using voltage follower.
- The output of a voltage follower is fed back the Twin T-network. That means junction of R/2 & C.
- One typical application of filter is for rejection of single frequency. Such as 50 HZ power line frequency hum.

b) **Determine pulse width of monostable M/V using IC555 timer for c=0.047uF and R=56 K.**

Ans :

Given : C = 0.047 uF and R = 56 K.

To find tp =?

For a monostable multivibrator, the pulse width is given by the formula,

tp = 1.1 RC **(1 M)**

tp = $1.1 \times 56 \times 10^3 \times 0.047 \times 10^{-6}$

= 2.89×10^{-3} seconds.

tp = 2.89 msec. **(3 M)**

c) For the given circuit obtain the output voltage (refer Figure No. 2) (4 M)

Ans:

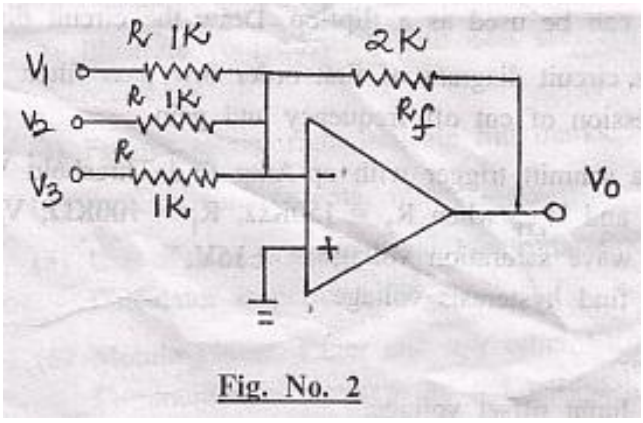


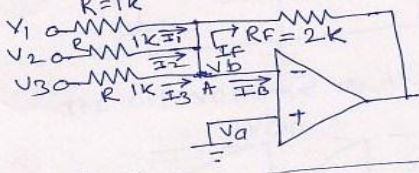
Fig. No. 2

Ans: Given $R_F = 2K$, $R = 1K$.

Soln:- Given circuit is inverting adder circuit.

output Expression for inverting amplifiers adder is

$$V_o = -\frac{R_F}{R_1}(V_1+V_2+V_3)$$



Derivation (4marks)

By applying KCL at node 'A'

$I = I_B + I_F$ —— (I)

and $I = I_1+I_2+I_3$

$R_{in} = \infty$ (ideally)

so that $I_B = 0$

hence, equation (1) becomes

$I = I_F$ hence we get.

$I_1+I_2+I_3 = I_F$

$$\frac{V_1-V_b}{R}+\frac{V_2-V_b}{R}+\frac{V_3-V_b}{R} = \frac{V_b-V_o}{R_F}$$

Applying virtual ground condition

$V_a = V_b = 0$

$$V_o = -\left[\frac{R_F}{R}V_1+\frac{R_F}{R}V_2+\frac{R_F}{R}V_3\right]$$

$$V_o = -\frac{R_F}{R}(V_1+V_2+V_3)$$

$$V_o = -\frac{2K}{1K}(V_1+V_2+V_3)$$

$$\boxed{V_o = -2(V_1+V_2+V_3)}$$

d) Draw and explain operation of wide band filter with the help of circuit diagram.

Ans: - (Circuit diagram -2 Frequency response with label -1M, Explanation- 1M)

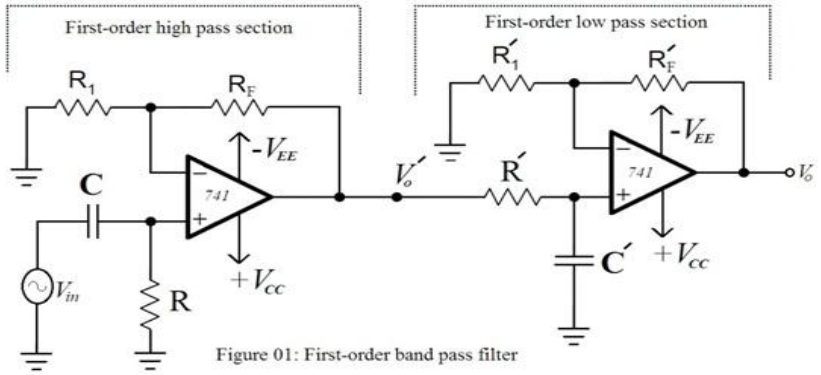


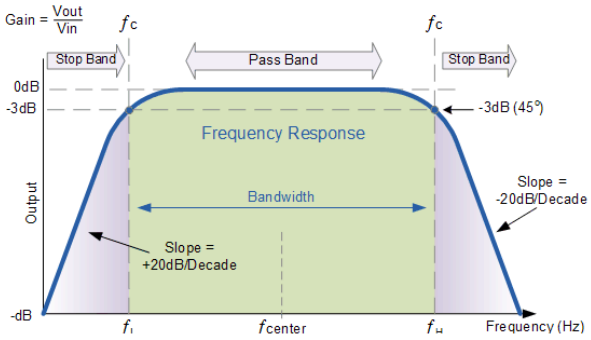
Figure 01: First-order band pass filter

OPERATION

- A **band-pass filter** passes all signals within a lower-frequency limit and an upper-frequency limit and rejects all other frequencies that are outside this specified band.
- This type of filter has a maximum gain at a *resonant frequency*.
- A band pass filter is the combination of high pass and low pass filter combination
- It has a pass band between two cut off frequency f_H and f_L such that $f_H > f_L$. Any input frequency outside this pass band is ***attenuated***.
- There are two types of band pass filters wide band pass and narrow band pass.
- If the quality factor Q < 10 and Q > 10 then it would be wide band pass and narrow band pass filter.
- The relationship between Q, the 3-dB ***bandwidth*** and the center frequency f_c is given by,

$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L}$$

$$\text{Where, center frequency } f_c = \sqrt{f_H - f_L}$$



e) Identify the circuit, redraw it . Draw the output of the circuit. State how you will obtain it. (Refer Fig. No.3) (4 M)

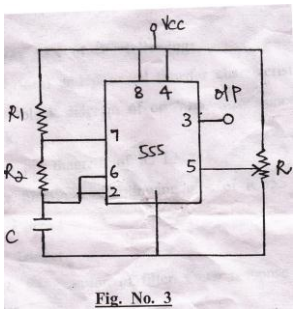
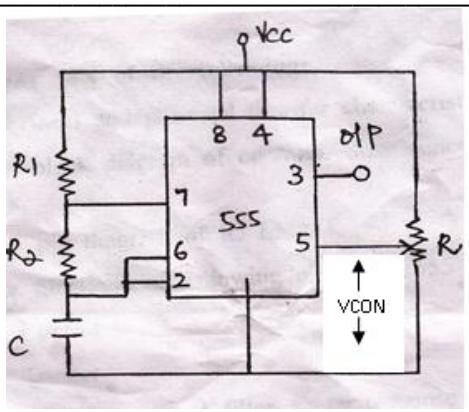
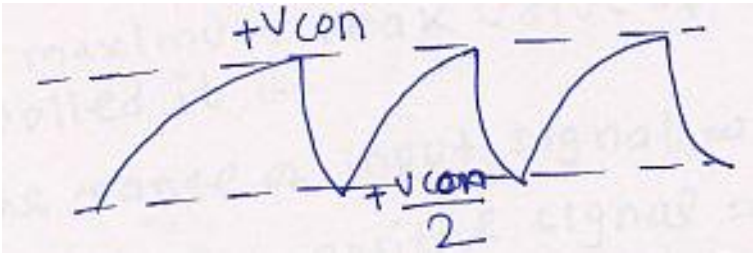


Fig. No. 3

Given circuit is VCO (Voltage controlled Oscillator) **OR** Voltage to frequency convertor **(1 M)**



Output of the circuit: (1 M)



Explanation: (2 M)

The VCO is a system whose frequency can be varied linearly with the input voltage. It is called as voltage controlled oscillator or voltage to frequency convertor. Pin no. 5 connects to the inverting input of upper comparator. Normally the control voltage is 2VCC / 3 because of internal divider inside the IC. Here the voltage from external potentiometer overrides the internal voltage. A control voltage can be varied by varying the value of R.(potentiometer). The voltage varies from + VCON /2 to +VCON. If we increase VCON, capacitor takes large time to charge or discharge and therefore the frequency decreases. Thus the frequency can be varied by varying the control voltage.

f) **State the need of peak to peak detector. Draw a circuit diagram. (4 Marks)**

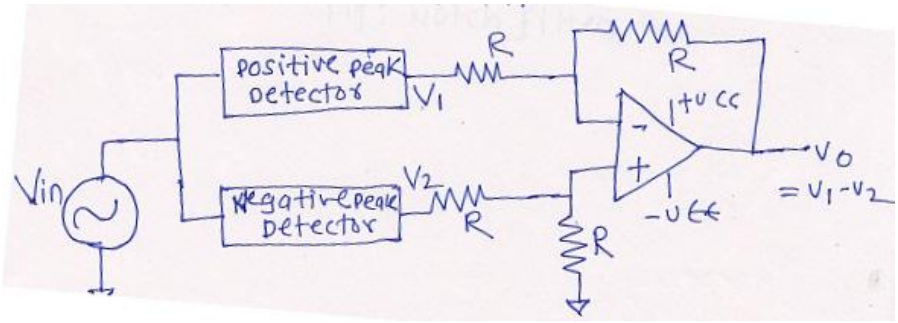
Ans :Needs: (1 M)

It is used to determine or detect the highest or maximum peak value of the input signal applied.

OR

It is used to determine the positive or negative peak **or** difference between the two peaks Of the input signal.

Circuit diagram of peak to peak detector:- **(3 M)**



Q6 a) Attempt any four of the following: **(4 M)**

a) Design a circuit to obtain the output voltage $V_0 = 10(V_1 - V_2)$.

Ans: **(Design:3M, Circuit diagram:1M)**

Given $V_0 = 10(V_1 - V_2)$, to find design the Circuit =?

Solution Since,

$V_0 = 10(V_1 - V_2)$

Hence it is differential amplifier or sub tractor

$\therefore V_0 = \frac{R_F}{R_1}(V_1 - V_2)$

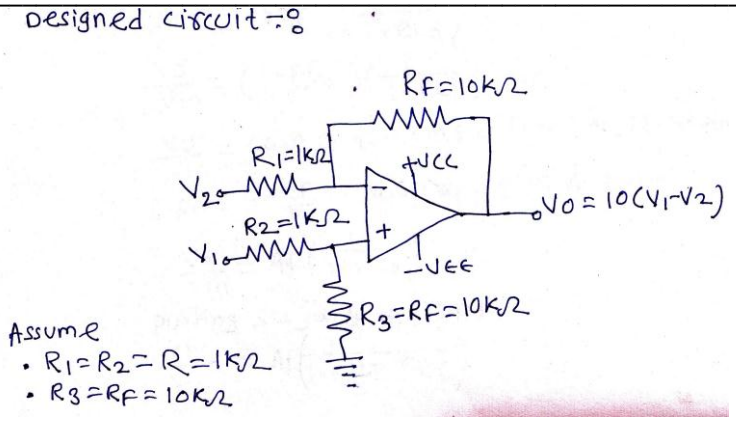
$\therefore \frac{R_F}{R_1} = 10$

$\therefore R_F = 10 R_1$

Assuming $R_1 = 1K\Omega$

$\therefore R_F = 10 \times 1K\Omega$

$\therefore R_F = 10K\Omega$

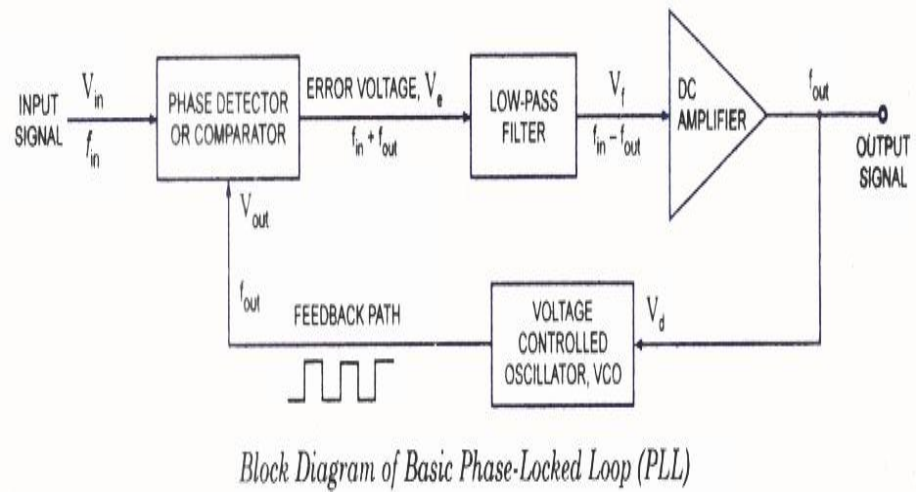


b) What is PLL? Explain its operation with a block diagram. (4 M)

Ans:- (PLL definition-1 M, Block diagram -1M,Operation- 2 M)

PLL - A phase-locked loop or phase lock loop is a control system that generates an output signal whose phase is related to the phase of an input signal

Block diagram



Block Diagram of Basic Phase-Locked Loop (PLL)

PLL Operation:-

The phase comparator compares the input frequency and the feedback frequency. And output DC Voltage is proportional to the phase difference between the two known as error voltage.

This voltage is applied to low pass filter which removes high frequency noise. This DC level is input to voltage controlled oscillator. Output frequency of VCO is directly proportional to the input DC level. The VCO frequency is compared with the input frequency and adjusted until it is equal to the input frequency. The phase – locked loop goes through three states free running capture and phase lock.

c) Define Multivibrator. State the types of multivibrator. Which M/V can be used as a flip-flop? Draw the circuit diagram.

Ans: (Define multivibrator-1mark,Types of multivibrator-1mark, BMV operate as a flip-flop - 1M,circuit diagram – 1 M)

Definition:-

A **multivibrator** is an electronic circuit that switches rapidly by means of positive feedback between two or more states. **OR**

A multivibrator is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops.

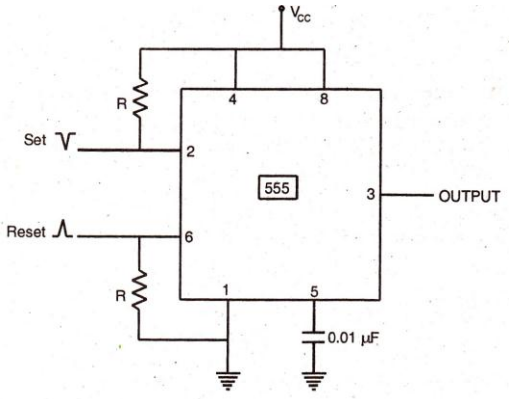
Types of multivibrator (1M)

There are three types of multivibrator circuit depending on the circuit operation:

- **Astable**, in which the circuit is not stable in either state —it continually switches from one state to the other. It does not require an input such as a clock pulse.
- **Monostable**, in which one of the states is stable, but the other state is unstable (transient). A trigger causes the circuit to enter the unstable state. After entering the unstable state, the circuit will return to the stable state after a set time. Such a circuit is useful for creating a timing period of fixed duration in response to some external event. This circuit is also known as a **one shot**.
- **Bistable**, in which the circuit is stable in either state. The circuit can be flipped from one state to the other by an external event or trigger. The bistable multivibrator is simply a **latch (flip-flop)**

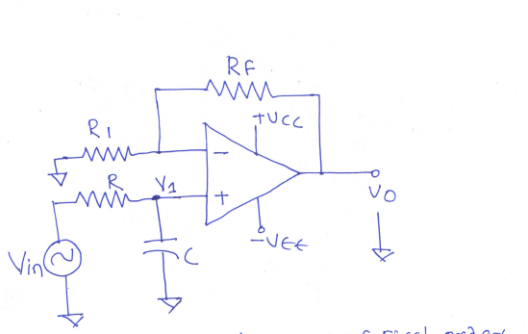
Bistable Multivibrator: it can operate as a flip-flop, 1M

Circuit diagram 1M



d) Draw circuit diagram of first order low pass filter. Give expression of cut off frequency and gain.

Ans: **(Circuit diagram – 2M, Expression – 1 M Each)**



Circuit diagram of first order Active Low pass filters.

The cut-off frequency (F_H)

$$FH = \frac{1}{2\pi RC}$$

Gain:

$$\left|\frac{Vo}{Vin}\right| = \frac{AF}{\sqrt{1+\left(\frac{f}{fH}\right)^2}}$$

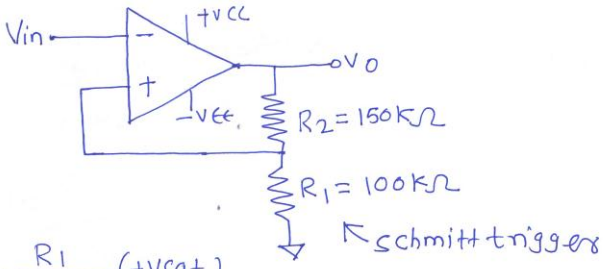
e) For a Schmitt trigger with op-Amp find threshold voltage V_{UTP} When R_2 = 150KΩ, V_{in} = 500mV,
Sine wave saturation voltage =_+15V,
Also find hysteresis voltage.

Ans:

Given data: R_1= 100KΩ
R_2= 150KΩ
Vin= 500 mv
Vsat= = ±15V

To find 1) V_{UTP} =?
2) V_{LTP} = ?
3) V_H = ?

Solution:-



1) $V_{UTP} = \frac{R_1}{R_1+R_2}(+V_{sat})$

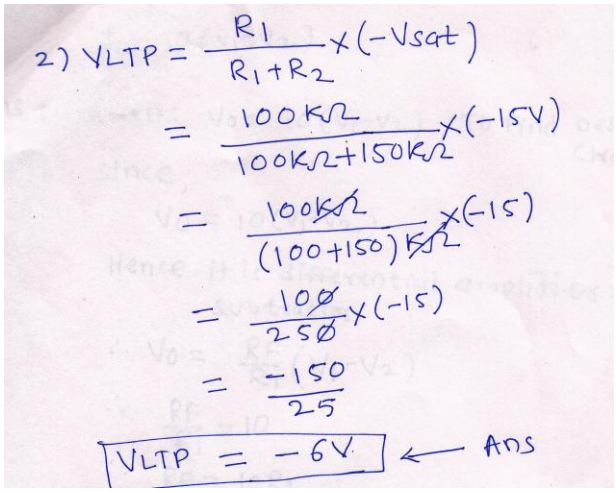
$= \frac{100K\Omega}{100K\Omega+150K\Omega} \times (15)$

$= \frac{100 \times 10^3}{(250) \times 10^3} \times 15$

$= \frac{100 \times 15}{250}$

$$V_{UTP} = \frac{1500}{250} = \frac{150}{25}$$

V_{UTP} = 6V ----------Answer



3) V_H= Threshold Voltage

The hysteresis voltage of Schmitt trigger is given

$V_H = V_{UTP} - V_{LTP}$

=6-(-6)

V_H= 6+6

V_H= 12V ---------Answer

f) Define:

i) Input Offset Voltage
ii) Input offset Current
iii) Input Bias Current
iv) Output offset voltage

Ans: **(Each definition 1M)**

Definition of parameters of OPAMP is follows:

i) Input Offset Voltage:

Input offset voltage is defined as the voltage that must be applied between the two input terminals of an OPAMP to null or zero the output

ii) Input offset Current:

The input offset current I_{io} is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier.

iv) **Input Bias Current:**

The input bias current I_B is the average of the current entering the input terminals of a balanced amplifier.

iv) Output offset voltage:

Output offset voltage is the output of an operational amplifier when the two inputs are shorted together (and often tied to ground) and output voltage is obtained non zero such voltage is output offset voltage of op-amp.