Summer 2015 Examination

Subject Code: 17445 **Model Answer**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

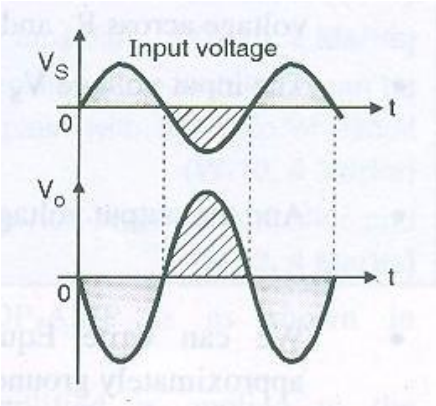
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. a) Attempt any SIX of the following: 12 marks

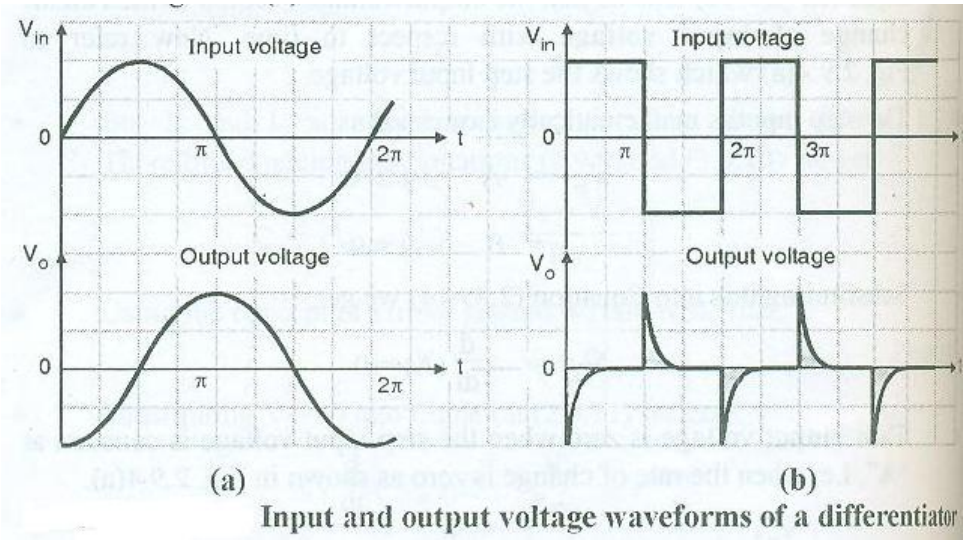
i. Draw input and output waveform, when the input signal is applied to the inverting input terminal of OP- AMP.

Ans i. **(Input Waveform-1Mark, Output Waveform- 1Mark)**



ii) Draw output waveforms for active differentiator for sine and square wave input.

Ans ii. **(O/P Waveform for Sine Input- 1Mark, O/P Waveform for Square Input- 1Mark)**



Input and output voltage waveforms of a differentiator

iii) State the need of signal conditioning and signal processing.

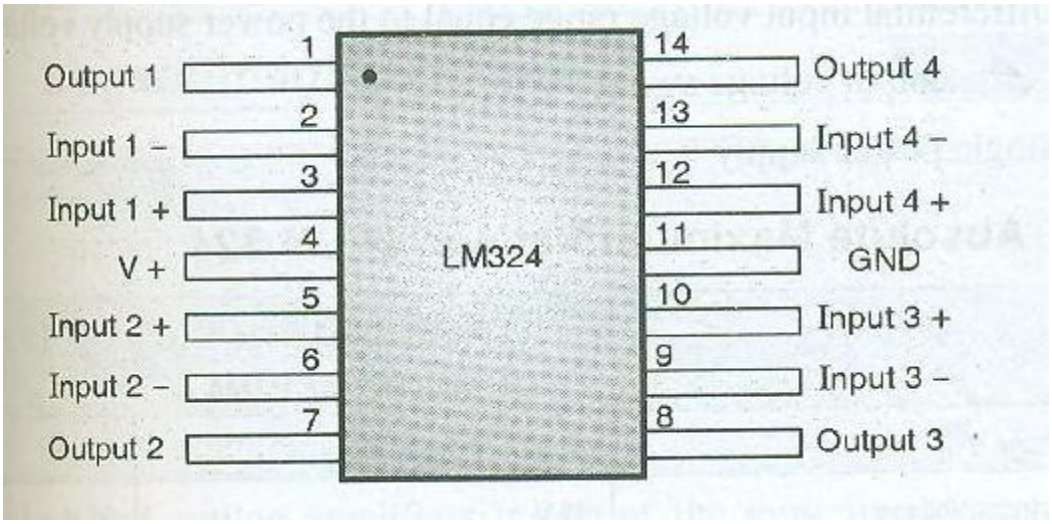
Ans iii. **(Need of Signal Conditioning- 1Mark, Need of Signal Processing- 1Mark)**

- In an instrumentation system, a transducer is used for sensing various parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc.
- However the transducer output cannot be used directly as an input to the rest of the instrumentation system.

- In many applications, the signal needs to be conditioned and processed. The signal conditioning can be of different types such as rectification, clipping, clamping etc. Sometimes the input signal needs to undergo certain processing such as integration, differentiation, amplification etc.

iv) Draw pin diagram of IC LM324.

Ans iv.**(Correct Pin diagram- 2Marks)**



Pin diagram of IC LM 324

v. Draw the output waveforms of inverting ZCD with sine wave input is $5V_{PP}$

Ans v. **(Correct O/P Waveform- 2marks)**

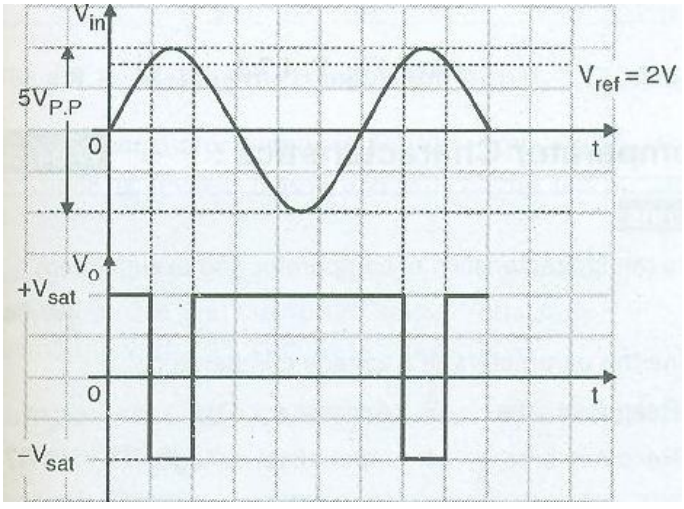


Fig: Output waveforms of inverting ZCD with sine wave input is $5V_{PP}$

vi. Classify filters based on frequency response characteristics.

Ans vi. **(Classification- 2Marks)**

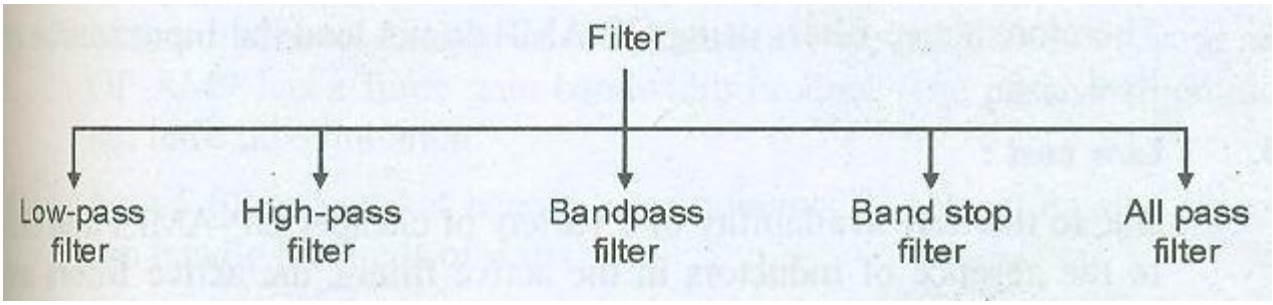


Fig: Classification of filters based on their frequency response characteristics.

vii. Give the relation between roll off rate and order of filter.

Ans vii. **(Correct Relation – ½ mark each)**

Order of Filter	Roll off Rate
1	20dB/ decade
2	40dB/ decade
3	60dB/ decade
4	80 dB/ decade

viii. Define multivibrator and give its classification.

Ans viii. **(Definition- 1Mark, Classification- 1 Mark)**

- Multivibrator: An electronic circuit in which the output continuously changes between two states i.e. stable and unstable state is known as multivibrator.
- Depending upon number of stable or unstable states, there are three types of multivibrator:
    i. Astable multivibrator.
    ii. Monostable multivibrator.
    iii. Bistable multivibrator.

b. Attempt any TWO of the following: 8 marks

i. Define the following parameters of OP- AMP and give their ideal values.

1. CMRR
2. Input offset voltage
3. Slew rate
4. Supply voltage rejection ratio.

Ans i. **(Each Definition- 1Mark)**

1. **CMRR**: It defined as the ratio of differential gain to the common mode gain. It is the ability of an amplifier to reject the common mode signal.

- Ideally CMRR= ∞

2. **Input offset voltage (V_{io})**: It is the input voltage that must be applied between both the input terminals of op- amp to make output offset voltage zero.

- Ideally value = 0

3. **Slew Rate:** It is defined as the maximum rate of change of output voltage per unit time.

- Ideally Slew Rate = ∞

4. **Supply voltage rejection ratio:** It is defined as the ratio of change of input offset voltage to the change in one supply voltage while keeping other supply voltage constant.

- Ideally**,** SVRR= 0

ii. Draw the block diagram of OP- AMP. State the function of each block.

Ans ii. **(Block Diagram- 2Marks, Function of each block– ½ marks)**

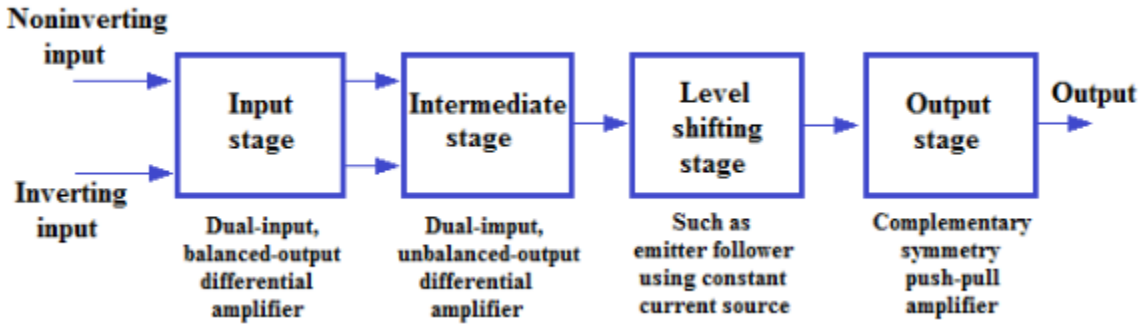


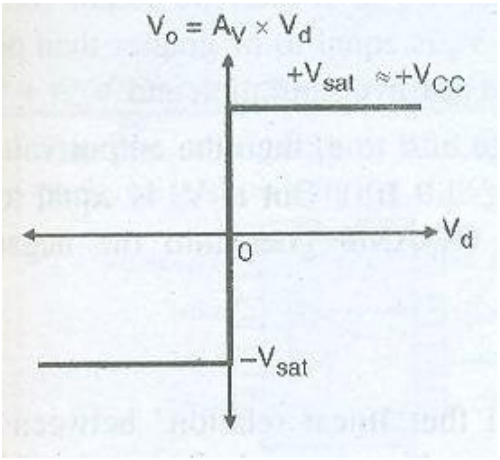
Fig: Block diagram of OP- AMP

1. An op- amp is a direct coupled differential amplifier usually consisting of one or more differential amplifier and followed by level shifter and output stage.

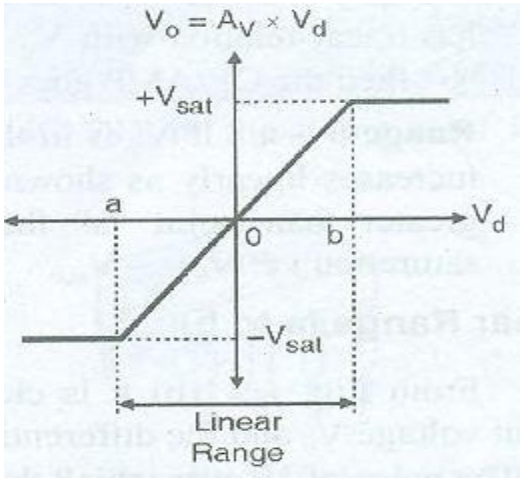
2. **Input stage:** In this stage dual input balanced output differential amplifier is used. Due to this circuit the voltage gain and input resistance of op amp increases to a high value.
3. **Intermediate stage:** This stage uses dual input unbalanced output differential amplifier. This stage is driven by the output of the first stage.
4. **Level shifting stage:** In this stage common emitter follower circuit is used. If the output of intermediate stage is shifted above or below the DC level, the level shifter stage brings back the signal to its original position.
5. **Output stage:** This stage uses complementary symmetry push pull amplifier. This stage provides low output resistance and hence increases the current supplying capability of op-amp and also this stage increases the output voltage swing.

iii. Draw ideal and practical voltage transfer characteristics of OP- AMP.

Ans iii. **(Ideal- 2Marks, Practical- 2Marks)**



Ideal voltage transfer characteristics of an ideal OP- AMP



Voltage transfer curve of practical OP- AMP

2. Attempt any FOUR of the following: 16 marks

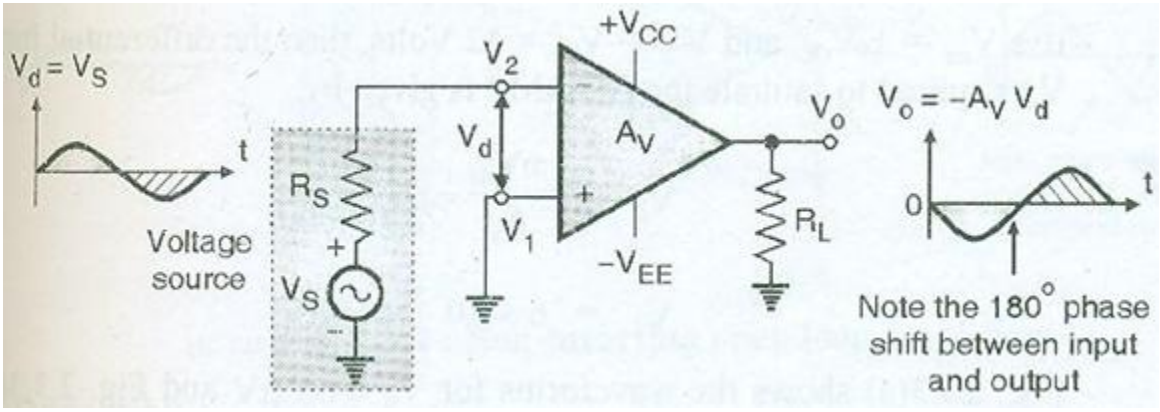
a. Compare open loop and closed loop configuration of OP- AMP with respect to input resistance, output resistance, bandwidth and application.

Ans a. **(4 points- 4marks)**

Sr. No	Parameter	Open loop configuration	Closed loop configuration
1	Input resistance	Very High	Depends on the circuit
2	Output resistance	Low	Very Low
3	Bandwidth	High	Very High
4	Application	Comparator	Linear amplifier, oscillators etc

b. Draw the circuit of Op- Amp without feedback in inverting mode. Derive the output voltage.

Ans b. **(Circuit diagram – 2 marks, Derivation – 2 marks)**



- As the non-inverting terminal is connected to ground V_1=0
- As the voltage drop across R_S is zero (as current drawn by the OP- AMP is zero) the voltage at the inverting terminal.

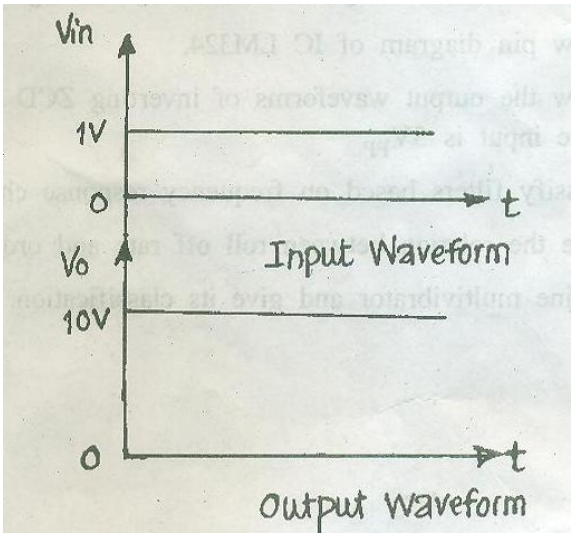
  $V_2 = V_S$
- The differential voltage $V_d = V_1 - V_2 = 0 - V_s$
- Therefore $V_d = - V_S$
- Therefore the output voltage is given by,

  $V_o = A_V \text{ X } V_d$

  Therefore, $V_o = A_V \text{ X } - V_S$

  Therefore, $V_o = - A_V V_S$.

c. Design a circuit of OP- Amp for the following input and output waveforms. Refer Figure No.1



Ans c. **(Derivation– 2 marks, Design diagram – 2 marks)**

- The required circuit is a non-inverting amplifier with gain of 10
- The output voltage is given by,

  $V_o = (1+R_F/R_1)\ V_i$

  But $1+R_F/R_1 = 10$ ……..(given)

  Therefore,

  $R_F/R_1 = 9$

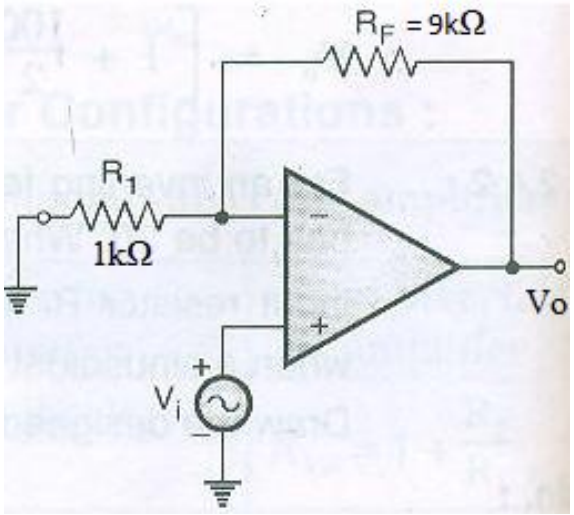
  Therefore,

  $R_F = 9\ R_1$

  Let $R_1 = 1k\Omega$

  Therefore,

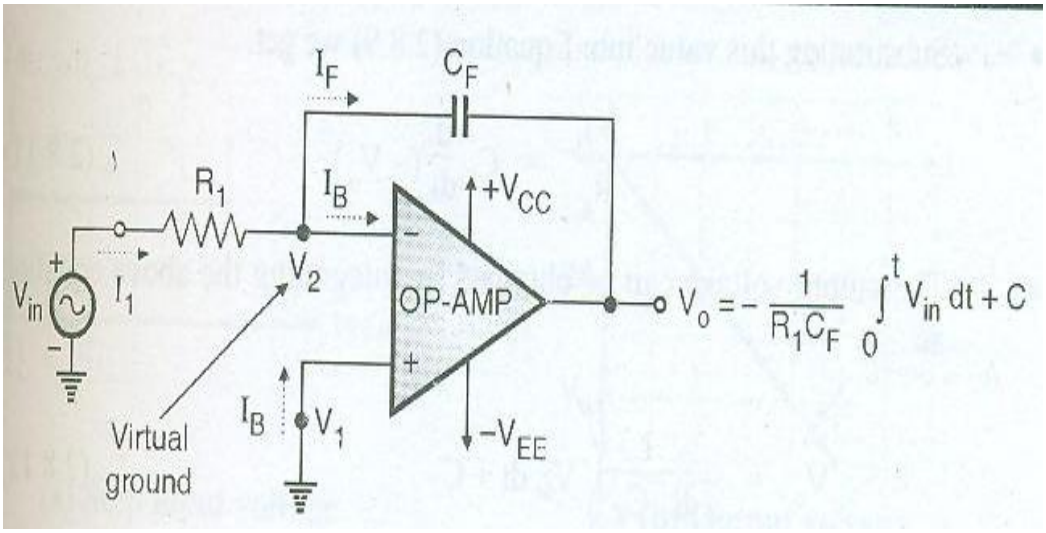
  $R_F = 9\ k\Omega$



d. Draw the circuit diagram and output waveform for sine and square wave input for output voltage.

$$V_o = -\frac{1}{RC}\int_0^t Vin\,dt + C$$

Ans d. **(Circuit Diagram – 2 marks, correct waveforms – 1 mark each)**



Circuit Diagram

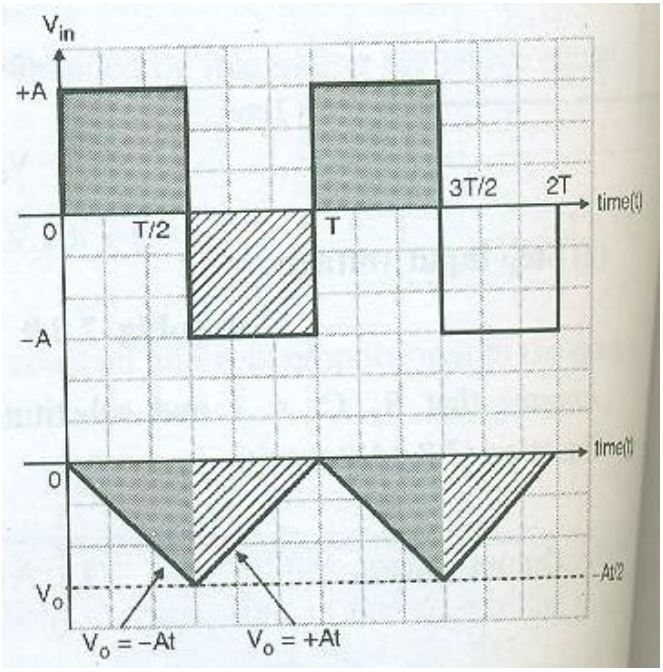


Fig: Input output voltage waveform for a square wave input

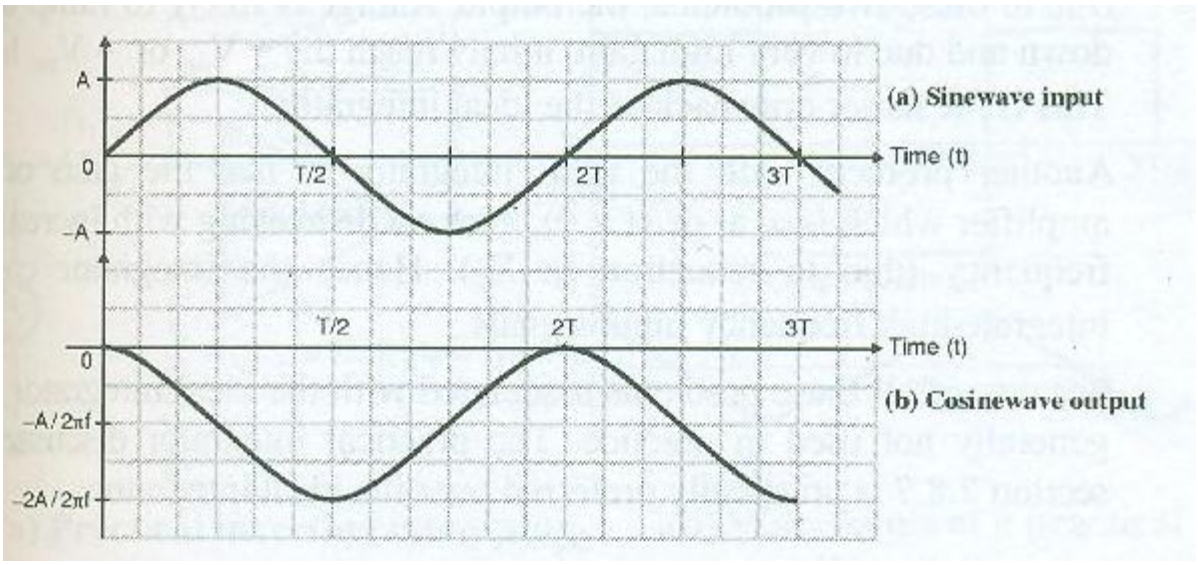


Fig: Input and output voltage waveforms for a sine wave input

e. Using Op-Amp, draw the circuit to show the output $V_0= 3(V_1-2V_2)$ where V_1 and V_2 are input voltages.

Ans e. **(Derivation – 2 marks, Design Diagram – 2 marks)**

$V_o =3(V_1-2V_2)$

$=3V_1-6V_2$

Therefore,

$V_o= (R_F/R_1)V_1 – (R_F/R_2)V_2$

Now,

$R_F/R_1 =3$

Therefore, choose $R_F =30K\Omega$ and $R_1 = 10K\Omega$

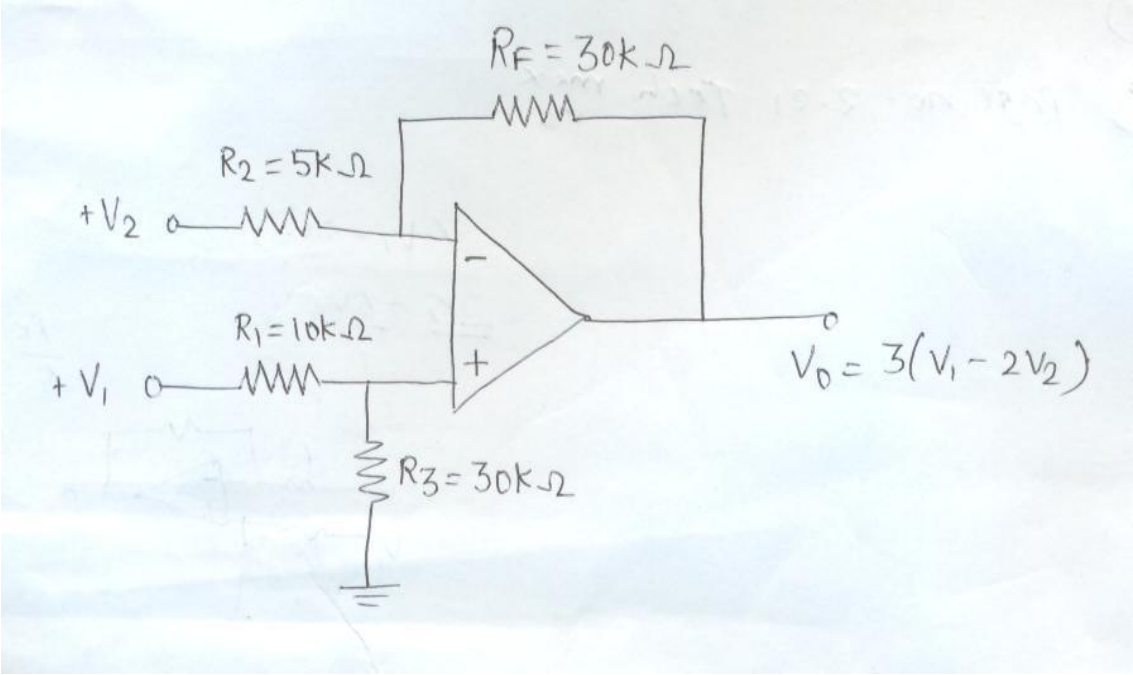
$R_F/R_1= 30/10 = 3$

Now, $- R_F/R_2 = -6$

Therefore, $R_2 = 5K\Omega$

$R_F = R3 = 30K\Omega$

The required circuit is,



f. If $R_1 = 2K\Omega$, $R_F = 100K\Omega$, $V_{CC} = \pm 15V$ and rms input voltage, $V_i = 20$ mV. Calculate output voltage in inverting and non- inverting mode.

Ans f. **(Inverting output – 2 marks, Non-inverting output – 2 marks)**

Given: $R_1 = 2K\Omega$, $R_F = 100K\Omega$, $V_{CC} = \pm 15V$ and rms input voltage, $V_i = 20$ mV

1. Output voltage for an inverting amplifier:
   For an inverting amplifier the output voltage,
   $V_0 = A_{VF} \times V_i$ Therefore, $V_0 = -(R_F/R_1) \times V_i$
   Substituting the values we get,
   $V_{0=} -100/2 \times 20x\ 10^{-3} = -1V$ ……Ans

2. Output voltage for the non-inverting amplifier:
   For the non-inverting amplifier the expression for output voltage is,
   $V_0 = A_{VF} \times V_i = [1 + R_F/R_1] \times V_i$
   Substituting the values we get,
   $V_0 = [1 + 100/2] \times 20x\ 10^{-3} = 1.02V$ ……Ans

3. Attempt any FOUR of the following: 16 marks

a. Draw the circuit diagram of instrumentation amplifier using 3 OP- AMPs. Give the expression at the output of each OP- AMP.

Ans a. (**Diagram – 2 marks, Expression of 1st and 2nd Op-Amp – 1 mark, final Op-Amp 1 Mark)**

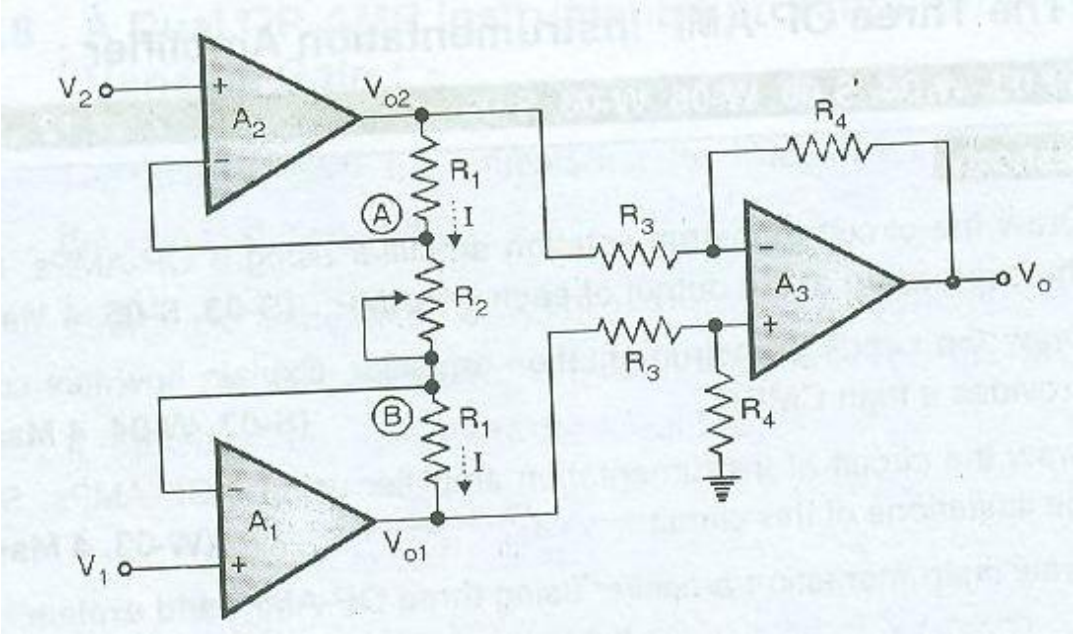


Fig: Instrumentation amplifier using three Op-Amp

$Vo_1 = [1+R_1/R_2\ ]\ V_1 – R_1/R_2\ V_2$

$Vo_2 = [1+R_1/R_2\ ]\ V_2 – R_1/R_2\ V_1$

$V_o = Vo_2 - Vo_1$

$= [1+ 2\ R_1/ R_2]\ (V_2 - V_1)$

b. Draw and explain the circuit of V to I converter with floating load using OP- AMP.

Ans b. (**Diagram: 2Marks; Explanation: 2Marks)**

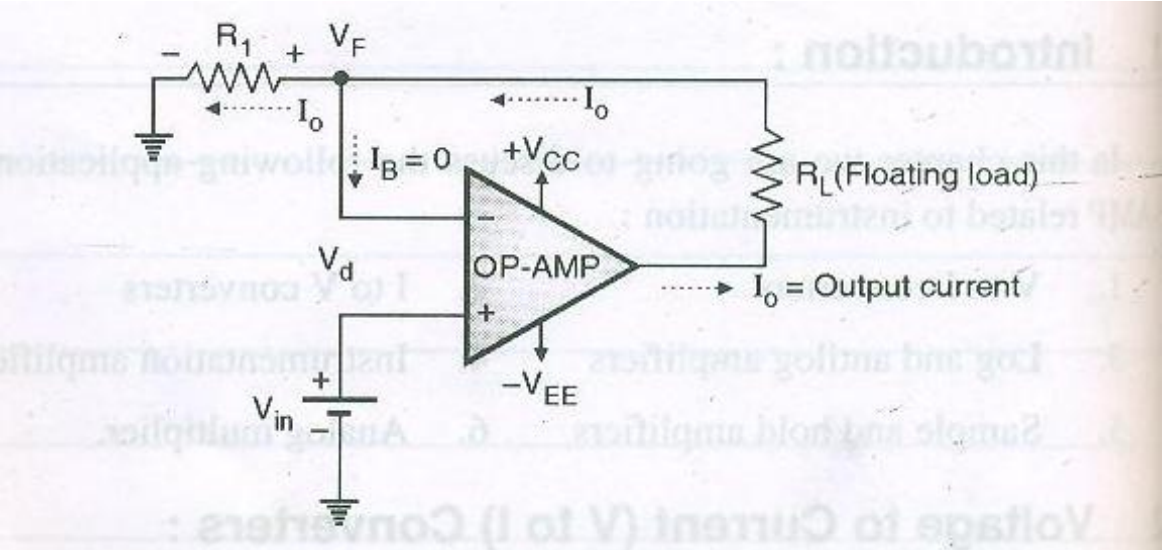


Fig. : Voltage to current converter with floating load

- The input voltage is applied to the non-inverting (+) input terminal of the OP- AMP. Load resistance R_L is connected in place of the feedback resistor R_F (in the conventional non-inverting amplifier)
- This circuit is also called as current series negative feedback amplifier.
- This is because the feedback voltage across R_1 is proportional to the output current I_o and appears in series with the input voltage.
- Apply KVL to the input loop

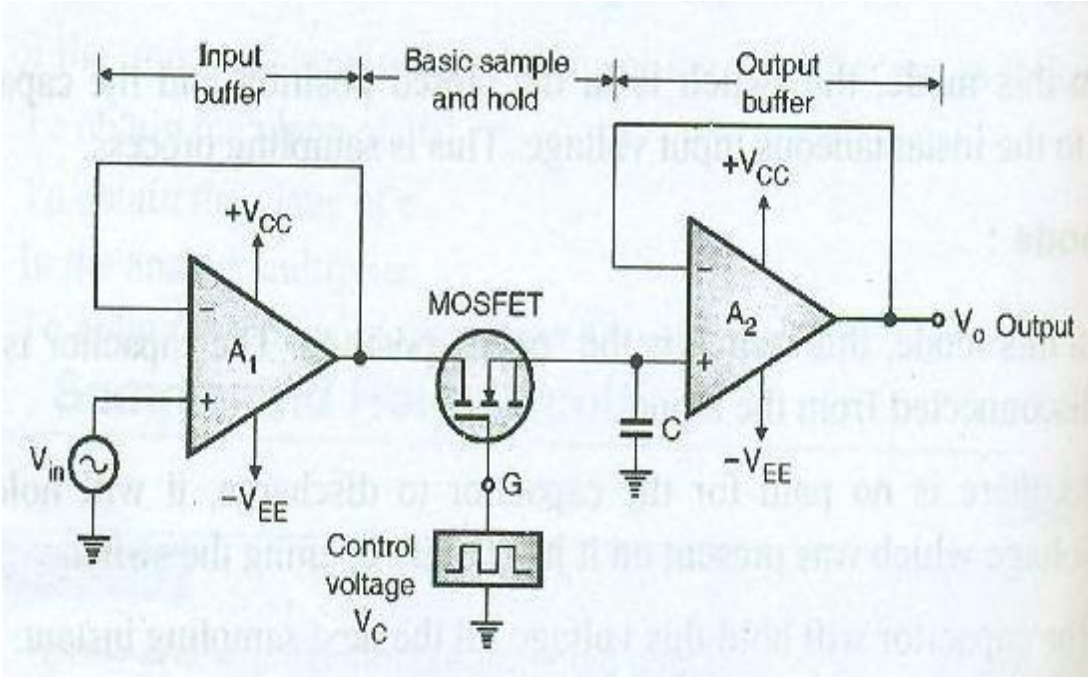
  $V_{in} = V_d + V_f$
- But as the open loop gain A_v of this OP- AMP is very large $V_d \approx 0$
- Therefore $V_{in} = V_F$

  But $V_{in} = R_1 \times I_o$ ……(as $I_B \approx 0$)

  Therefore $I_o = V_{in} / R_1$

c. Draw the circuit diagram of sample and Hold circuit using OP- AMP.

Ans c. **(Any relevant correct diagram – 4 marks)**



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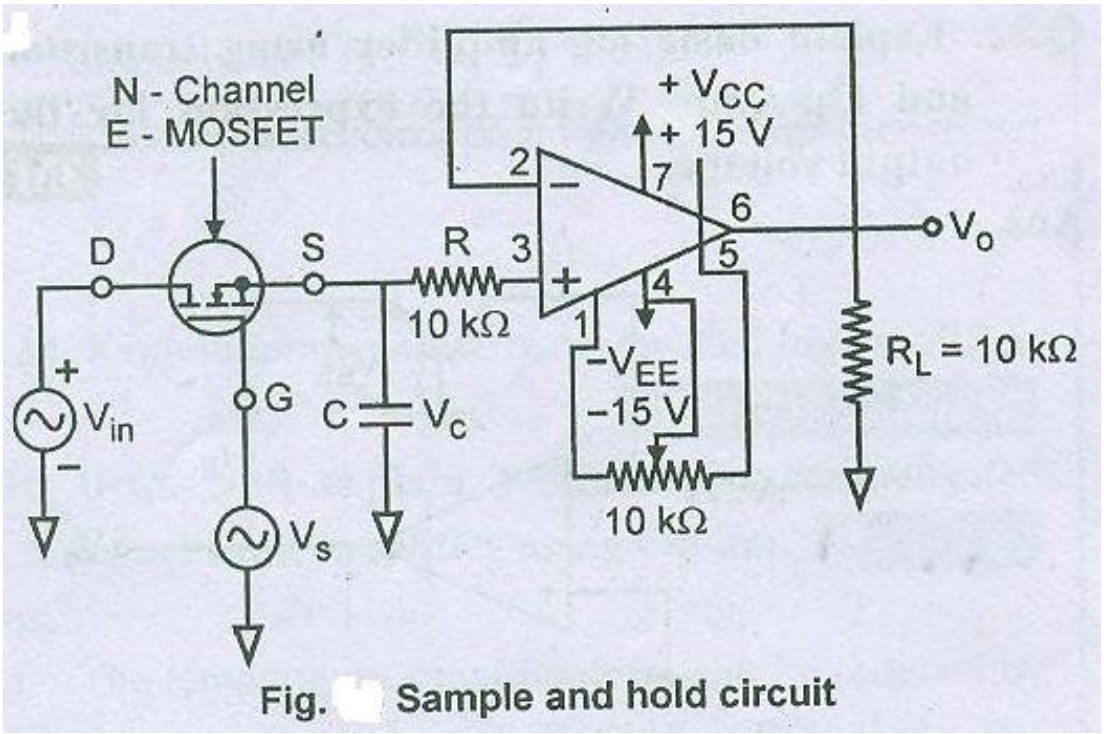
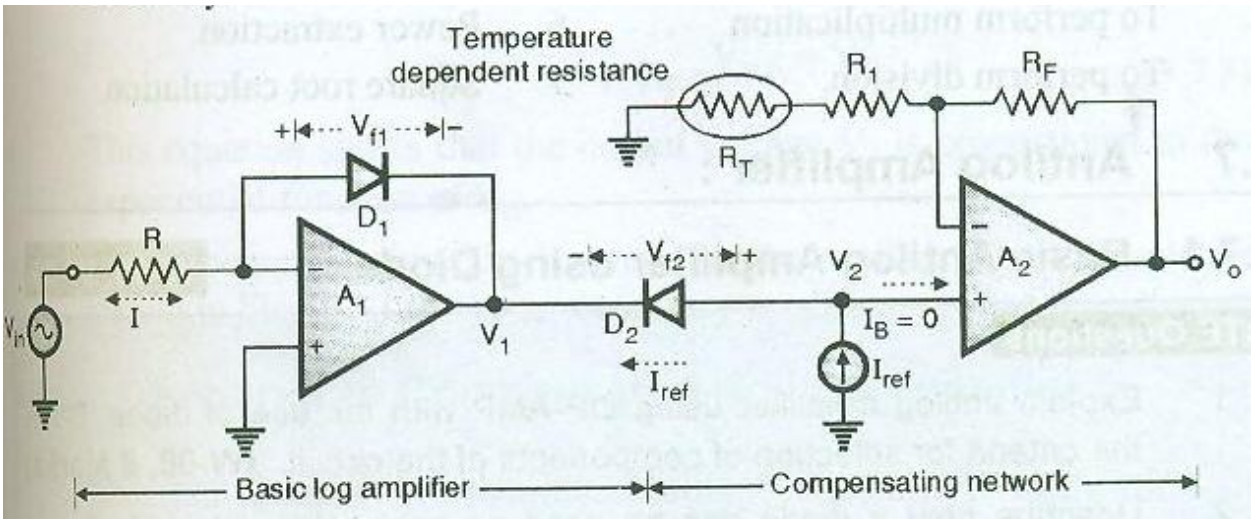


Fig. Sample and hold circuit

d. Draw circuit diagram of temperature compensated log amplifier using OP- AMP.

Ans d. **(Any relevant correct diagram – 4 marks)**



Circuit diagram of temperature compensated log amplifier using OP- AMP

e. Explain working of active negative peak detector with neat circuit and waveforms.

Ans e. (**Diagram: 2 Marks; Working: 1 Mark, waveform: 1 mark)**

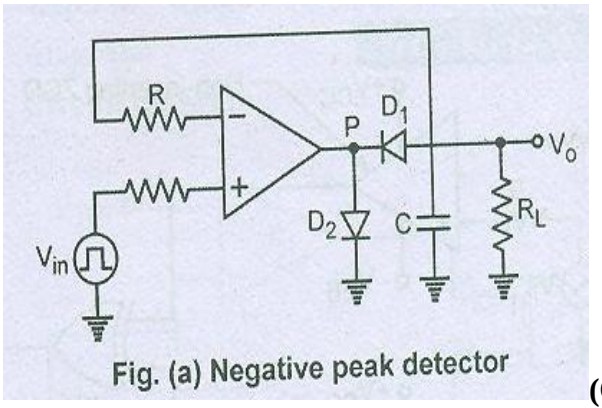


Fig. (a) Negative peak detector

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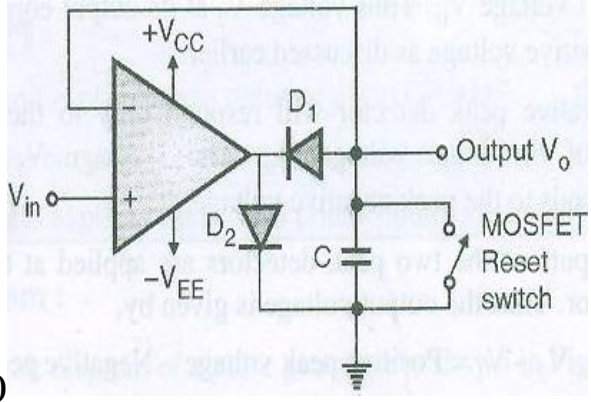
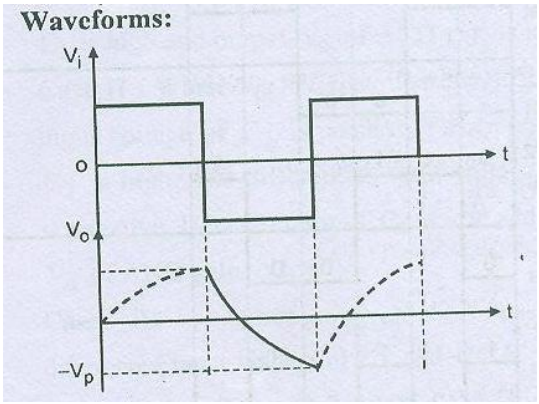
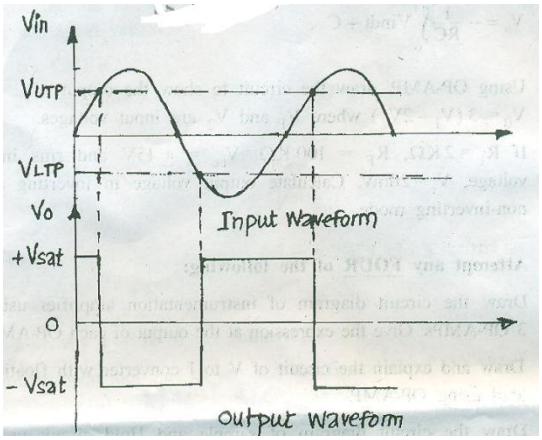


- During the positive half cycle, the potential B at point P is positive.
- Hence, Diode D_1 is reverse biased and D_2 is forward biased.
- Hence D_2 by passes the positive voltage towards ground and capacitor C remains un-charged.
- During negative half cycle, potential P becomes negative, hence D_1 is forward biased.
- Now, capacitor C starts charging for negative half cycle. And it charges up till the negative peak value.
- As, the capacitor charges for the negative half cycle, hence, it is called as negative peak detector.

- The MOSFET switch connected across the capacitor is to reset the circuit. By turning on this switch momentarily, we can discharge the capacitor completely.

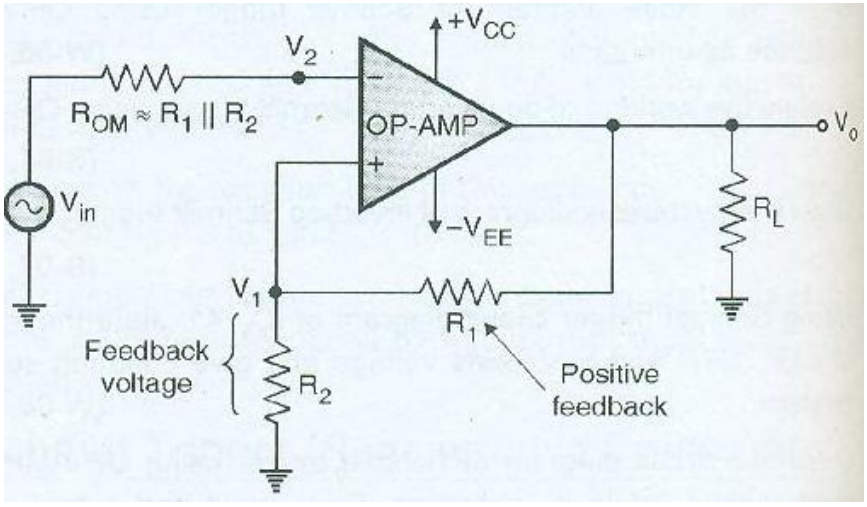


f. Identify the following waveforms. Label the circuit name and draw the circuit diagram for the same (Refer Figure No .2)



Ans f. **(Identification & labeling – 2 marks, Correct circuit – 2 marks)**

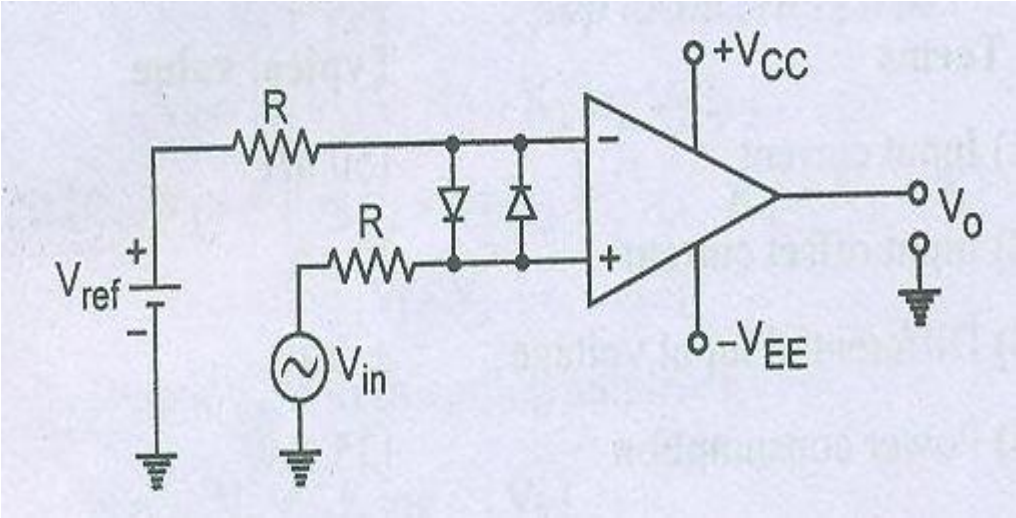
- The above waveforms are input and output waveform of Schmitt Trigger.



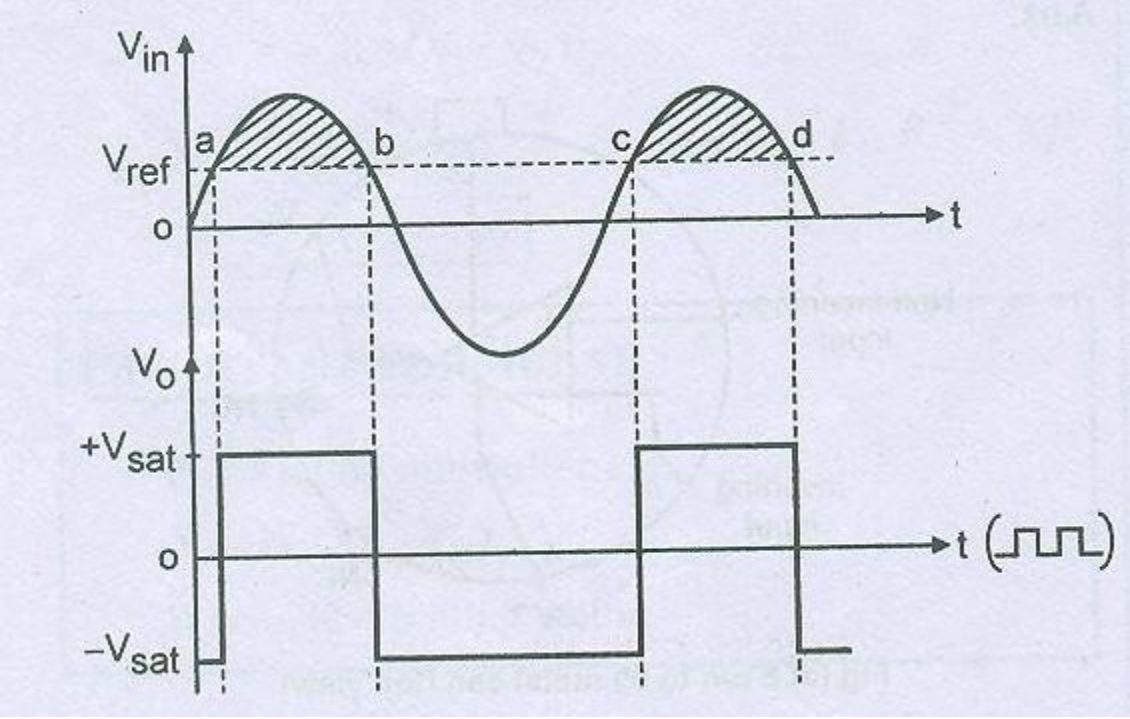
4. Attempt any FOUR of the following **16 marks**

a. Draw the circuit diagram and waveforms for non-inverting comparator using OP-AMP.

Ans a. **(Circuit Diagram: 2M; Waveforms: 2M)**



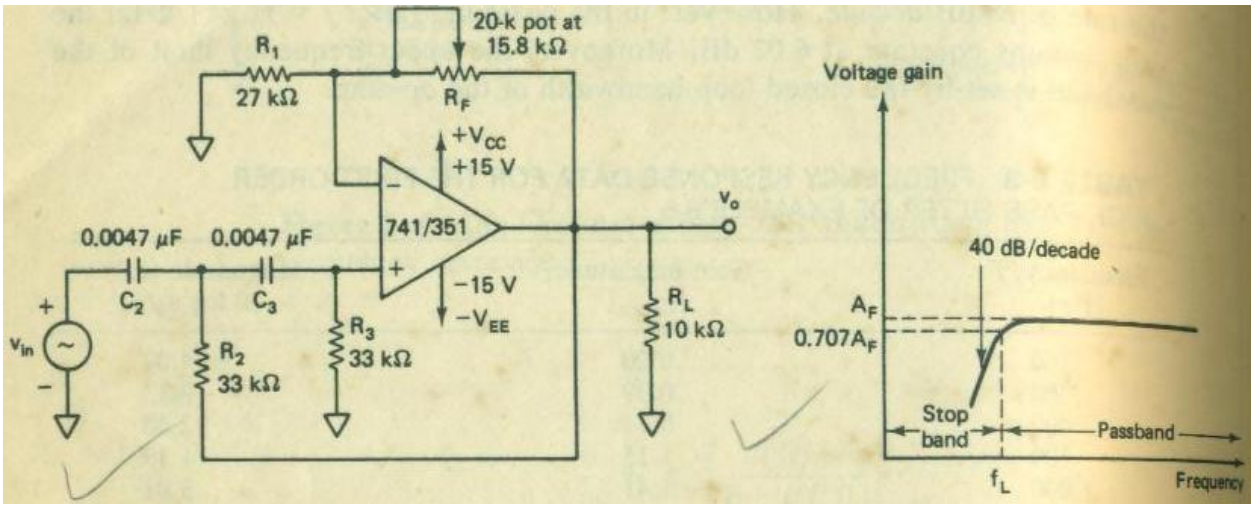
Circuit Diagram for non-inverting comparator using OP-AMP



Waveforms for non- inverting comparator using OP-AMP

b. Draw the circuit diagram of second order high pass Butterworth filter with frequency response. Give expression for cut off frequency and gain.

Ans b. **(Circuit – 2 marks, response – 1 mark, expression – ½ mark each)**



Cut-off Frequency $f_L = \frac{1}{2\pi \sqrt{R_2 C_2 R_3 C_3}}$

Gain $A_f = 1 + \frac{R_f}{R_1}$

c. Design a first order Butterworth low pass filter for pass band gain 2 and cut- off frequency 10KHz.

Ans c. **(Any relevant design with correct formula – 2 marks, final design circuit – 2 marks)**

Given: Pass band gain (A_f)= 2

Cut-off Frequency (f_c) = 10 kHz

Pass band Gain (A_f) is given by the formula

$A_f = 1 + \frac{R_f}{R_1}$

Here, $A_f = 2$

Therefore, $2 = 1 + \frac{R_f}{R_1}$

So, $1 = \frac{R_f}{R_1}$

Therefore, $R_f = R_1$

Let R_f = 10kΩ

Therefore, R_1= 10kΩ

Assume C = 0.01uF

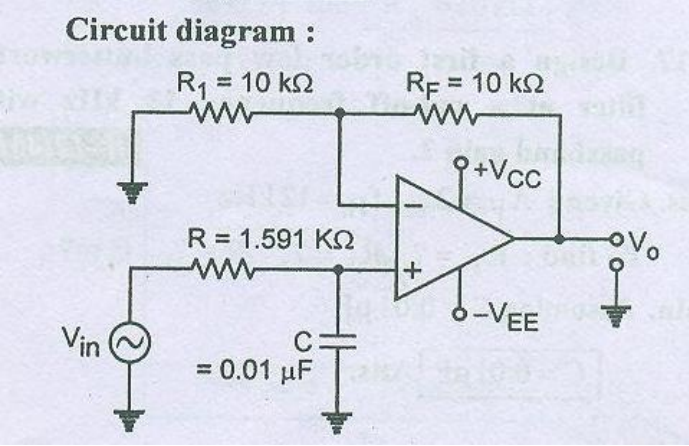
But $f_c = \frac{1}{2\pi RC}$

But f_c = 10 kHz

Therefore, 10 kHz = $\frac{1}{2\pi RC}$

So, R = $\frac{1}{2\pi \text{ x } 10 \text{ x} 10^3 \text{x } 0.01 \text{ x } 10^{-6}}$

Therefore, R = 1.59kΩ.



d. State two merits and two demerits of active filters over passive filters.

Ans d. **(any 2 merits – 2 marks, 2 demerits – 2 marks)**

Merits:

1. Gain and frequency adjustment
2. No loading problem
3. Cost is less

Demerits:

1. Stability consideration limits the uses of most of the filters below 100kHz.
2. The selectivity and the centre frequency are often very sensitive function of gain of op- amp or absolute value of feedback.

3. To obtain required absolute tolerance control, active filter requires additional process steps such as the use of thin film or hybrid technology.

e. Draw a neat circuit diagram of all pass filter and explain its working.

Ans e. (**Diagram: 2Marks; Explanation: 2Marks)**

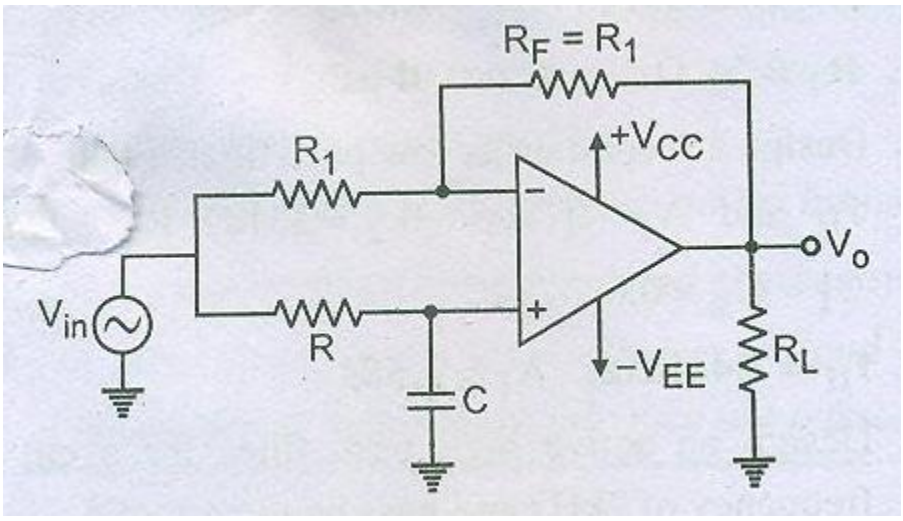


Fig: All pass filter

- It is a special type of filter which passes all the frequency components of the input signal to output without any attenuation. But it introduces a predictable phase shift for different frequencies of the input signal.
- The all pass filters are also called as delay equalizers or phase correctors.
- Figure shows an all pass filter with $R_F = R_1$.
- The input signal is applied to both the input of the OP-AMP.

f. Suggest and draw OP- AMP based filter circuit to fulfill following response. (Refer Figure NO.3)

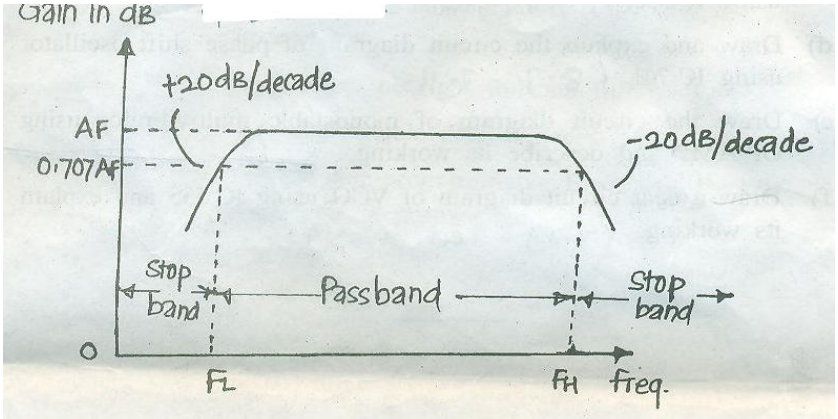


Figure 3.

Ans f. **(Naming of circuit – 1 mark, circuit diagram – 3 marks)**

- The given diagram is the frequency response of Wide Bandpass Filter.

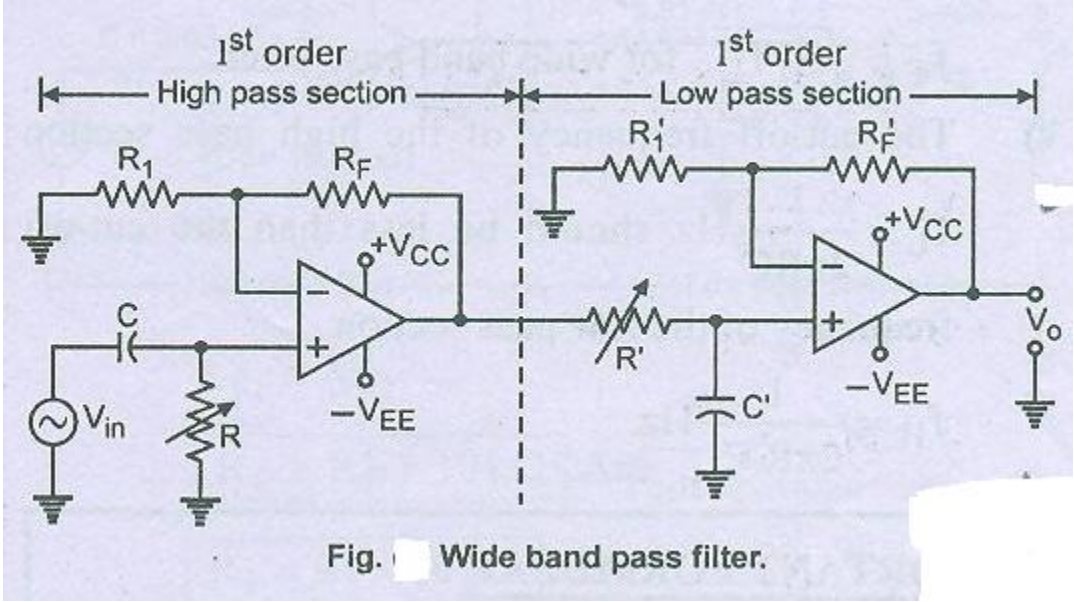


Fig. Wide band pass filter.

5) Attempt any FOUR of the following: 16 marks

a. Draw the circuit diagram of touch plate switch using IC 555 and describe its operation.

Ans a. **(Circuit Diagram- 2Marks, Operation- 2Marks)**

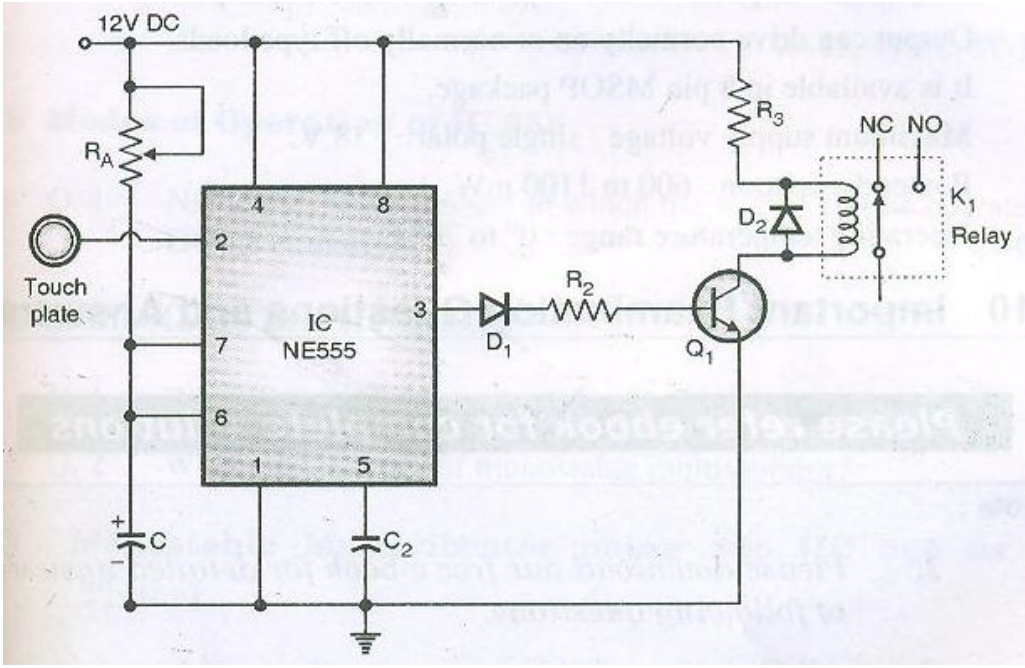


Fig: Touch switch circuit diagram

- A touch plate (push to ON) is used to turn on the timer and active the relay.
- As soon as touch plate is switched ON (pushed), a trigger pulse is produced and applied to pin no. 2 of IC 555, and the output of IC 555 goes high.
- It will remain high for a period of T_{ON}= 1.1 R_AC. The high output of IC 555 activates the transistor Q_1 which in turn energize the relay coil, and closes the N.O (Normally open) contact of the relay.

b. Calculate the value of UTP and LTP for Schmitt trigger using IC 555 if V_{CC} = 15V

Ans b. **(Correct Value of UTP- 2Marks, Correct Value of LTP- 2Marks)**

Given : V_{CC} = 15V, UTP= ? , LTP= ?

UTP= 2/3 V_{CC} = 2/3 x 15 =10V

LTP= 1/3 Vcc= 1/3 x 15= 5V

Therefore,

UTP= 10V & LTP= 5V

c. Design Monostable multivibrator using IC 555 for pulse width t_p= 10ms. Draw the designed circuit.

Ans c. **(Derivation: 2 Marks, Circuit Diagram: 2Marks)**

Given: t_p=10mS

Step1: For a monostable multivibrator:

Pulse width, t_p = 1.1 RC

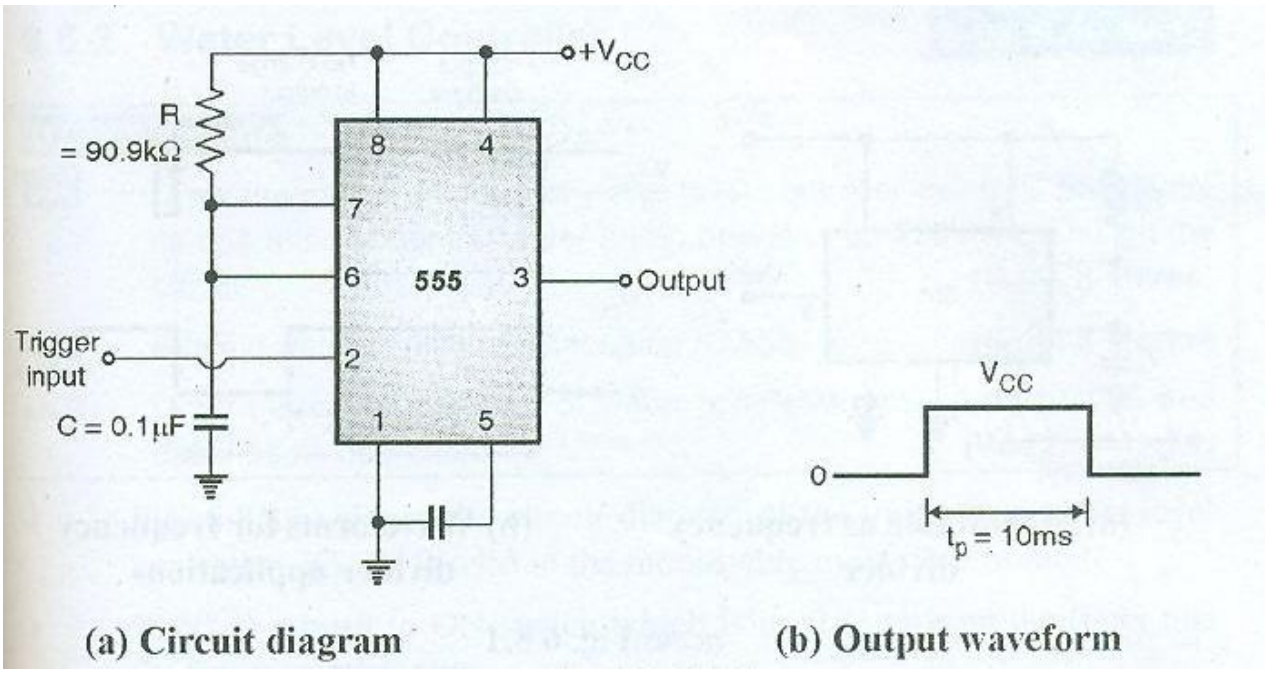
Assume, C= 0.1μF

Therefore,

$10 \times 10^{-3} = 1.1 \times R \times 0.1 \times 10^{-6}$

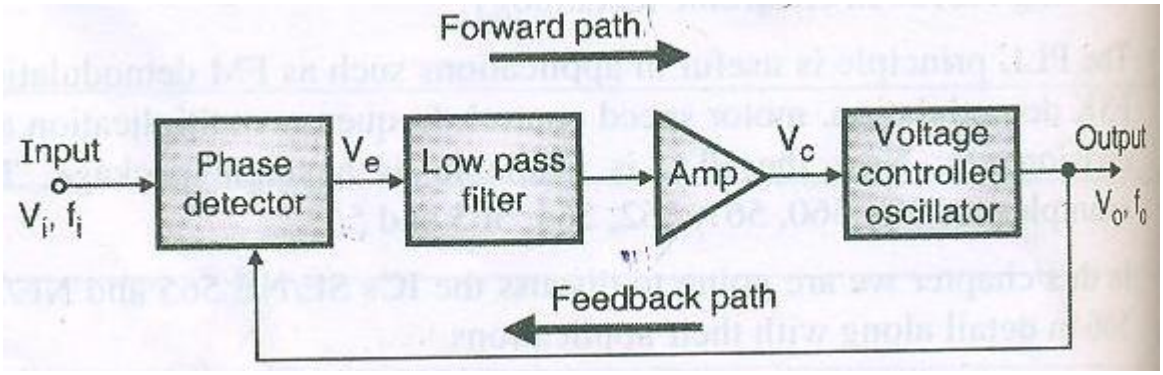
Therefore,

$R = 10 \times 10^{-3} / 1.1 \times 0.1 \times 10^{-6} = 90.9\ k\Omega$



d. Draw and explain block diagram of PLL.

Ans d. **(Block diagram- 2Marks, Explanation:2Marks)**



Phase locked loop consists of:

- A phase detector or phase comparator
- A low pass filter
- An error amplifier
- A voltage controlled oscillator (VCO)

Phase detector or phase comparator:

- The two points to a phase detector or comparator are the input voltage V_s at frequency f_s and the feedback voltage from a voltage controlled oscillator (VCO) at the frequency f_o

- The phase detector compares these two signals and produces a dc voltage V_e which is proportional to the phase difference between f_s and f_o. The output voltage V_e of the phase detector is called as error voltage.
- This error voltage is then applied to a low pass filter.

Low pass filter:

- The low pass filter removes the high frequency noise present in the phase detector output and produces output and produces a ripple free dc voltage.
- This dc voltage is amplified to an adequate level by the amplifier and applied to a voltage controlled oscillator (VCO). The dc amplifier output voltage is called as the control voltage V_C.

Voltage controlled oscillator (VCO):

- The control voltage V_C is applied at the input of a VCO.
- The output frequency of VCO is directly proportional to the dc control voltage V_C. The VCO frequency f_o is compared with the input frequency f_s by the phase detector and it (VCO frequency) is adjusted continuously until it is equal to the input frequency f_s i.e. $f_o = f_s$

The three states of operation through which the VCO undergoes are:

- Free running: There is no control on VCO output frequency f_o
- Capture: The comparison of f_o and f_s begins. The control voltage V_c starts adjusting f_o to bring it closer to f_s.
- Phase lock: When f_o is exactly equal to f_s the PLL is said to be phase locked. Once locked. One locked $f_o = f_s$ except for a finite phase difference φ

e. Draw and explain the working of FM demodulator using PLL.

Ans e.**(Figure- 2Marks, Explanation-2Marks)**

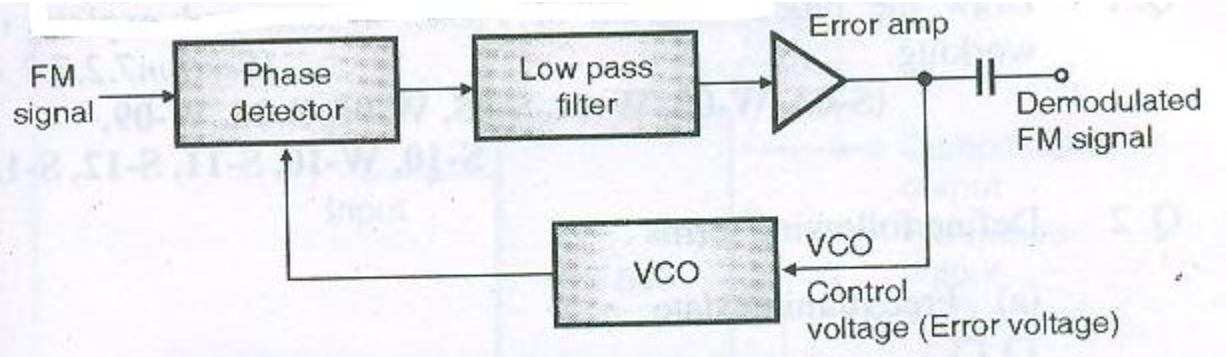


Fig. : PLL used as FM demodulator

Operation:

- The FM signal which is to be demodulated is applied at the input of the PLL.
- As the PLL is locked to the FM signal, the VCO starts tracking the instantaneous frequency in the FM input signal.
- The error voltage produced at the output of the amplifier is proportional to the deviation of input frequency from the centre frequency of FM. Thus the ac component of the error voltage represents the modulating signal. Thus at the error amplifier output we get demodulated FM output.
- The FM demodulator using PLL ensures a highly linear relationship between the instantaneous input frequency and VCO control voltage (error amplifier output)

f . Draw and explain the circuit diagram of multiplier using PLL.

Ans f. **(Diagram- 2Marks, Explanation- 2Marks)**

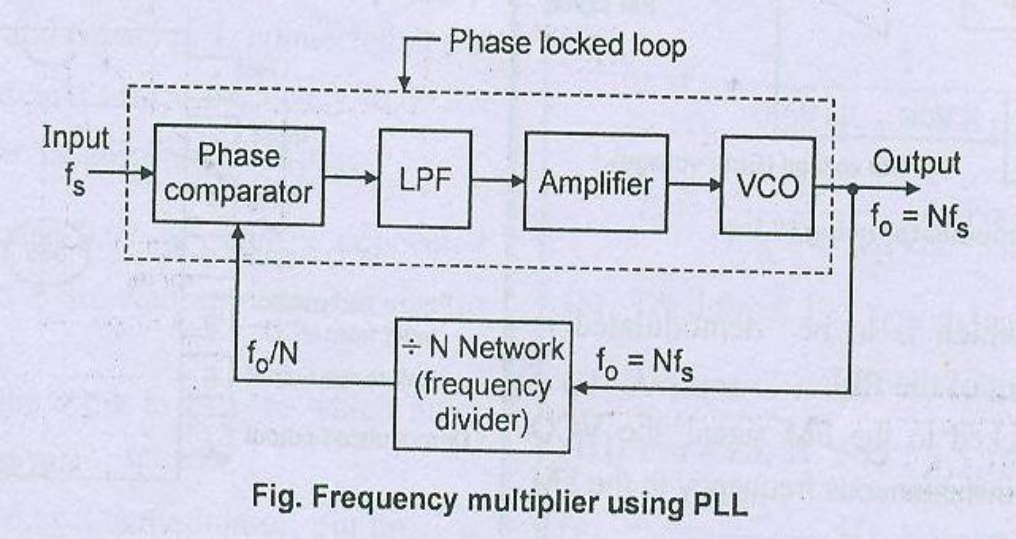


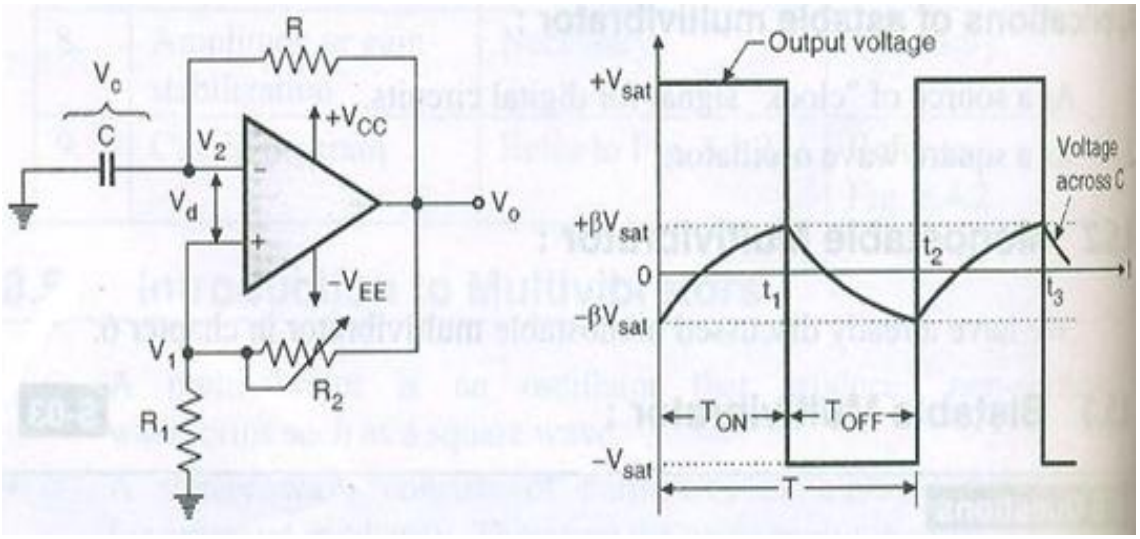
Fig. Frequency multiplier using PLL

- Figure shows block diagram of a frequency multiplier using PLL.
- A divide by N network is connected externally between the VCO output and phase comparator input.
- Since the output of the divider network is locked to the input frequency f_s, the VCO actually operates at a frequency which is N times higher than f_s.
  Therefore, $f_o = Nf_s$
- The multiplying factor can be obtained by proper selection of the scaling factor N.

6. Attempt any FOUR of the following: 16 marks

a. Draw the circuit diagram of Astable multivibrator using IC741 and describe its working.

Ans a. **(Circuit Diagram-2Marks, Working- 2Marks)**



- Let the voltage on the capacitor C is zero when power is applied to the circuit. Therefore initially voltage at the inverting (-) input terminal is zero, V_2= 0. Note that V_2 will be equal to the capacitor voltage V_c (V_2- V_c)
- Due to some output offset voltage present at the output of the OP- AMP, the voltage V_1 at the non- inverting (+) terminal is non zero and will have a value that depends on the output offset voltage and the values of resistances R_1 and R_2.
- Hence the differential input voltage V_d is equal to the voltage V_1

Operation from 0 to t_1:

- The voltage V_1 will start driving the OP- MAP output towards saturation. For eg, if V_1 is positive initially then it will drive the compartor output to +V sat (As V_d is positive).
- With the OP- AMP output equal to +Vsat the capacitor C starts charging through R and V_C starts increasing exponentially in the positive direction as shown
- The voltage V_1 across R_1
  $V_1 = R_1 / (R_1 + R_2)\ V_{sat}$
  therefore $V_1 = \beta\ V_{sat}$ where, $\beta = R_1 / R_1 + R_2$
  β is the feedback factor.

Operation from t_1 to t_2 :

- At $t = t_1$ the capacitor voltage V_c is equal to $\beta V_{sat.}$

- As soon as the voltage on C becomes slightly more positive than V_1, the differential voltage V_d changes its polarity and the OP- AMP output will suddenly switch to a negative saturation $-V_{sat}$.
- Due to this sudden changeover voltage V_1 also becomes negative as
  $V_1 = R_1 / (R_1 + R_2)\ V_{sat}$
  $V_1 = -\beta\ V_{sat}$
- The capacitor C starts discharging through R and the output stage of the OP- AMP.
- As soon as V_C becomes slightly more negative than V_1, the differential voltage polarity will be at $t = t_2$ reversed and the OP- AMO output will suddenly switch to a positive saturation i.e. $+V_{sat}$
- This process will repeat itself to generate a square waveform at the output of OP- AMP. The equivalent circuits along with the output voltage waveforms.

b. Draw the circuit diagram of Wein bridge oscillator using IC 741 and give expression for frequency of oscillation.

Ans b. **(Circuit Diagram – 3 marks, Expression – 1 mark)**

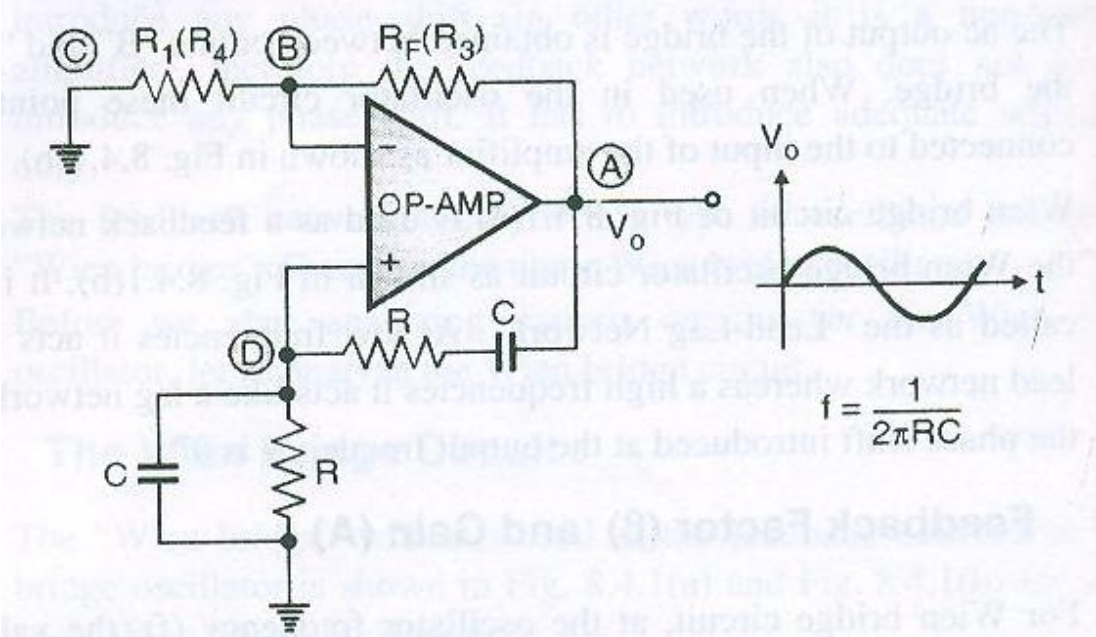


Fig. : Wien bridge oscillator using OP-AMP

- The expression for oscillator frequency is
  $F = 1/2\pi RC$

c. Draw the circuit diagram and waveforms of Bistable multivibrator using IC 555.

Ans c. **(Circuit Diagram- 2Marks, Waveforms- 2Marks)**

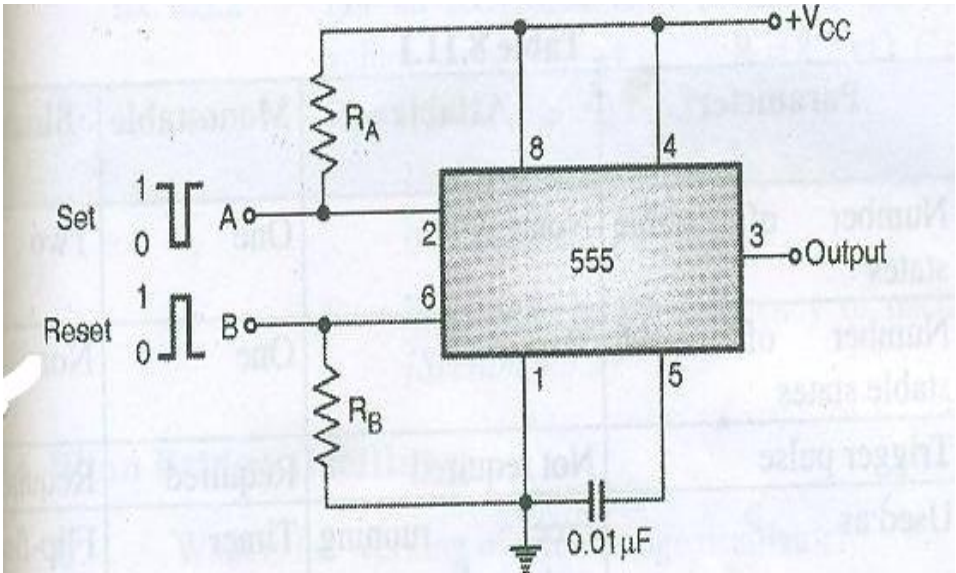


Fig. : A bistable multivibrator using IC 555

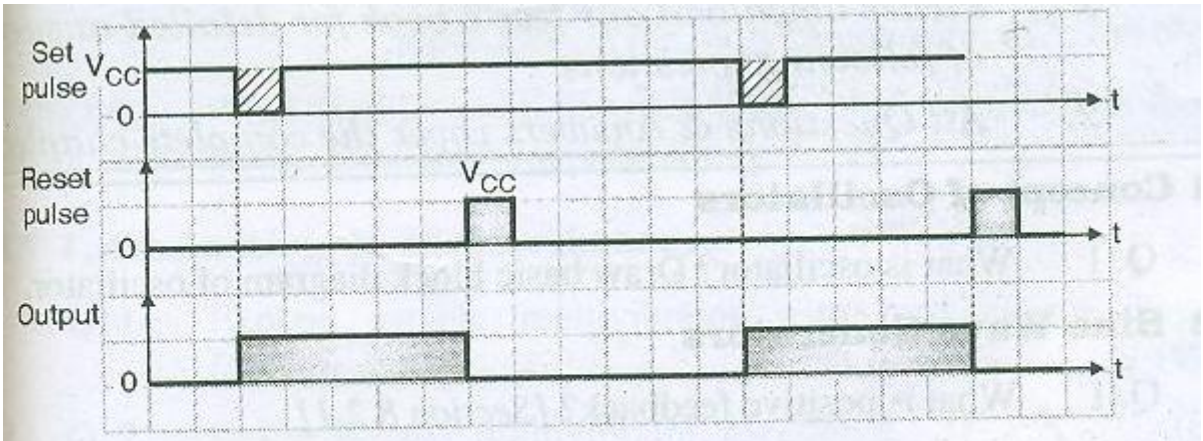


Fig. : Waveforms of the bistable multivibrator circuit using IC 555

d. Draw and explain the circuit diagram of phase shift oscillator using IC741.

Ans d. **(Circuit Diagram- 2 Marks, Explanation- 2Marks)**

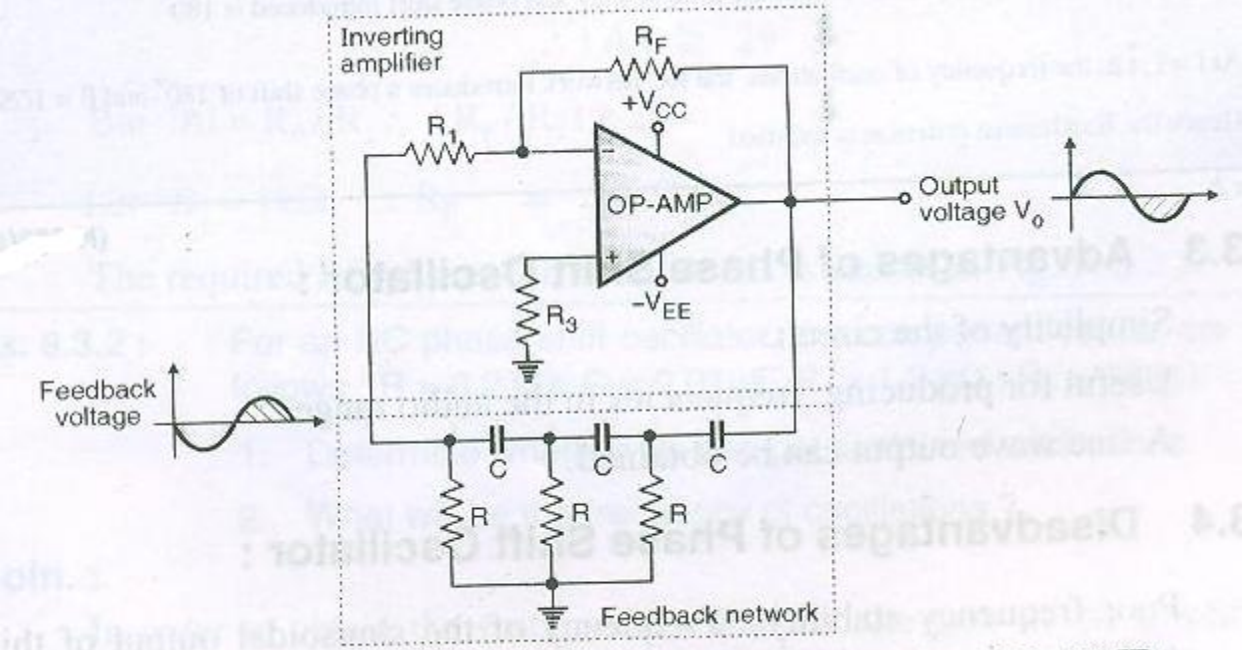


Fig. : RC phase shift oscillator using OP-AMP

- The Op- Amp is used as an inverting amplifier. Therefore it introduces a phase shift of 180^0 between its input and output.
- The output of the inverting amplifier is applied at the input of the RC phase shift network . As discussed earlier, this network attenuates the signal at its input and feeds it to the amplifier input. The level of attenuation is decided by the feedback factor β.
- The gain of the inverting amplifier is decided by the values of R_F and R_1. This gain is adjusted in such a way that the product $|A\beta|$ is slightly greater than 1.
- It can be proved that the value of feedback factor β at the frequency of oscillations is β =1/29. For sustained oscillations, the loop gain $|A\beta| \geq 1$. Therefore, in order to make the loop gain $|A\beta| \geq 1$, the gain of the inverting amplifier $|A|$ should be greater than or equal to 29.
- Gain of the inverting amplifier is given by
  $|A| = R_F / R_1$ Therefore, $R_F / R_1 \geq 29$ or $R_F \geq 29R_1$
- These values of R_F and R_1 will insure sustained oscillations.
- The expression for frequency of oscillations of an RC phase shift oscillator using OP-AMP is given by
  $f_o = 1/ 2\pi \sqrt{6}\, RC$

e. Draw the circuit diagram of Monostable multivibrator using OP- AMP and describe its working.

Ans e. **(Circuit Diagram- 2 Marks, Working- 2Marks)**

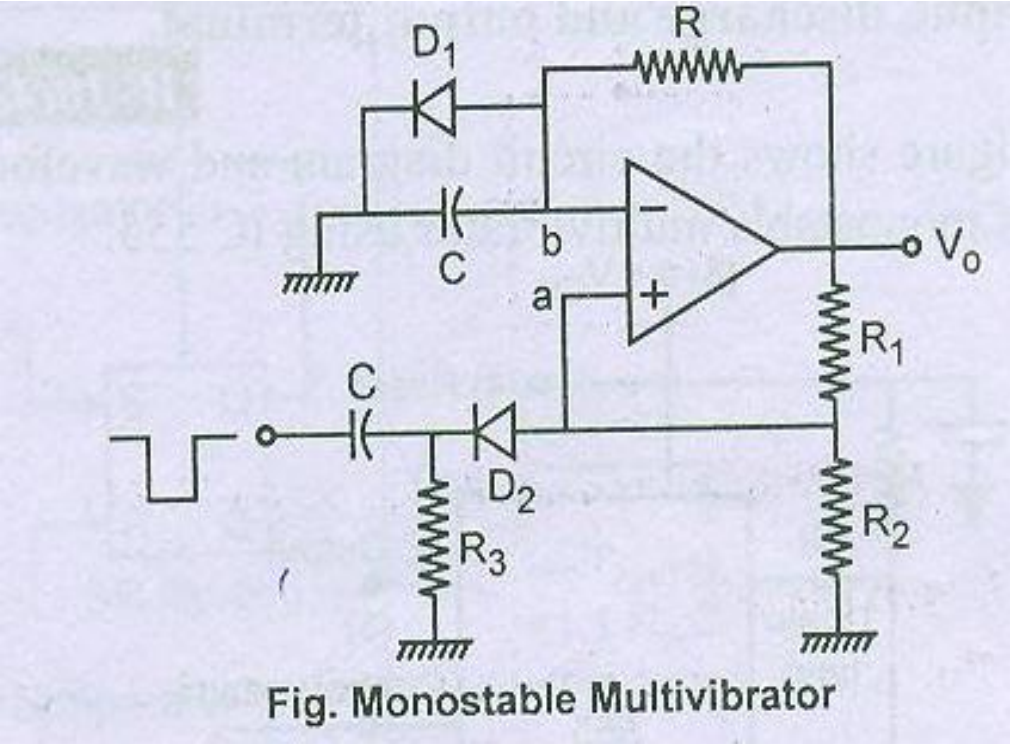


Fig. Monostable Multivibrator

- The connection of a diode in parallel with the timing capacitor C in an astable multivibrator circuit may be used to prevent the inverting input of the op- amp from going positive, thus, resulting in monostable multivibrator.
- In the stable state, the amplifier circuit is at positive saturation (V_{os}). In this condition, terminal b is clamped to ground by diode D_1 and terminal 'a' is positive with respect to ground.
- A narrow negative triggering pulse can be introduced through D_2 to the non-inverting terminal.
- R_3 is assumed to be greater than D_2 so that its loading effect may be neglected.
- The diode D_2 avoids any positive noise spike present in the triggering line.

f. Draw a neat circuit diagram of VCO using IC 555 and explain its working.

Ans f. **(Circuit Diagram- 2 Marks, Working- 2Marks)**

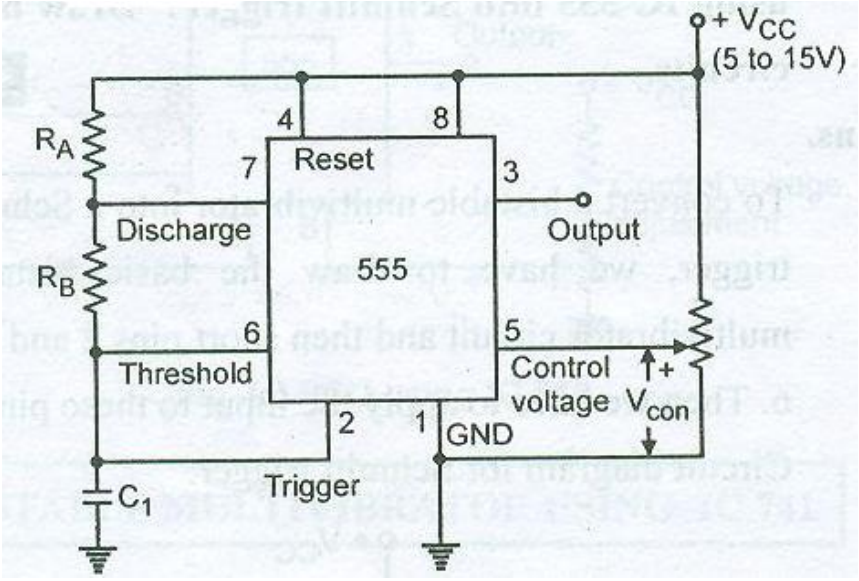


Fig: Circuit diagram of VCO using IC 555

- The constant current source/ sink block is used to charge and discharge the externally connected timing capacitor C_T linearly.
- The value of charging and discharging current is dependent on the control voltage V_C applied at pin number (5) modulating input.
- This current can also be changed by varying the external timing resistor R_T.
- The potential difference between pins (5) and (6) I almost zero. That means these pins are equipotential.
- Therefore if we increase the modulating voltage V_C at pin number (5), the voltage at pin number (6) will increase with the same amount.
- This reduces the voltage drop across R_T and reduces the charging current.
- The voltage across the capacitor is thus triangular wave. This triangular wave is applied to a buffer A_1.
- The buffer is connected in order to avoid to avoid any possible loading of the capacitor. The buffer output is taken out at pin number (4) as triangular wave output.
- The buffer output is also applied to a Schmitt trigger A_2, which converts the triangular wave into square waveform.
- Resistors R_a and R_b is a potential divider generating the reference levels for the upper and lower trigger voltages. This square wave is inverted by inverter A_3 and made available at pin number (3).