Winter – 15 EXAMINATIONS

Subject Code: **17445** **Model Answer**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. A) Attempt any SIX of the following: 12 Marks

i. Draw equivalent circuit of an op-amp.

Ans i: **Correct circuit diagram: 2M**

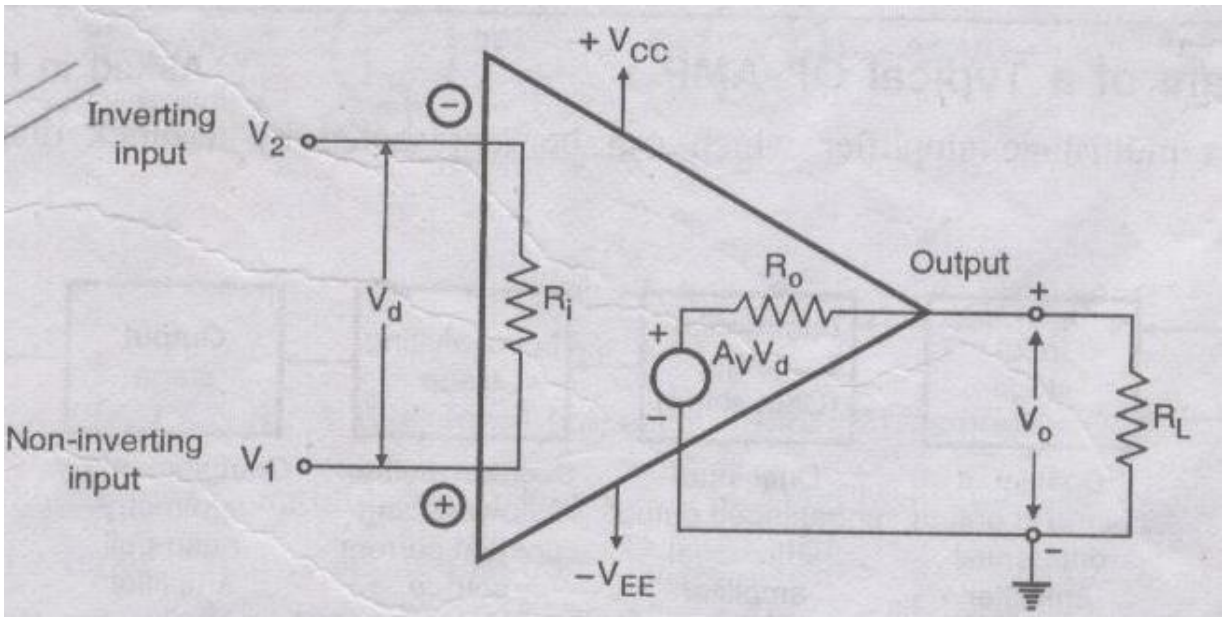


Fig: Equivalent circuit of an OP-AMP

ii. Draw circuit diagram of basic integrator using op- amp.

Ans ii. **Correct circuit diagram: 2M**

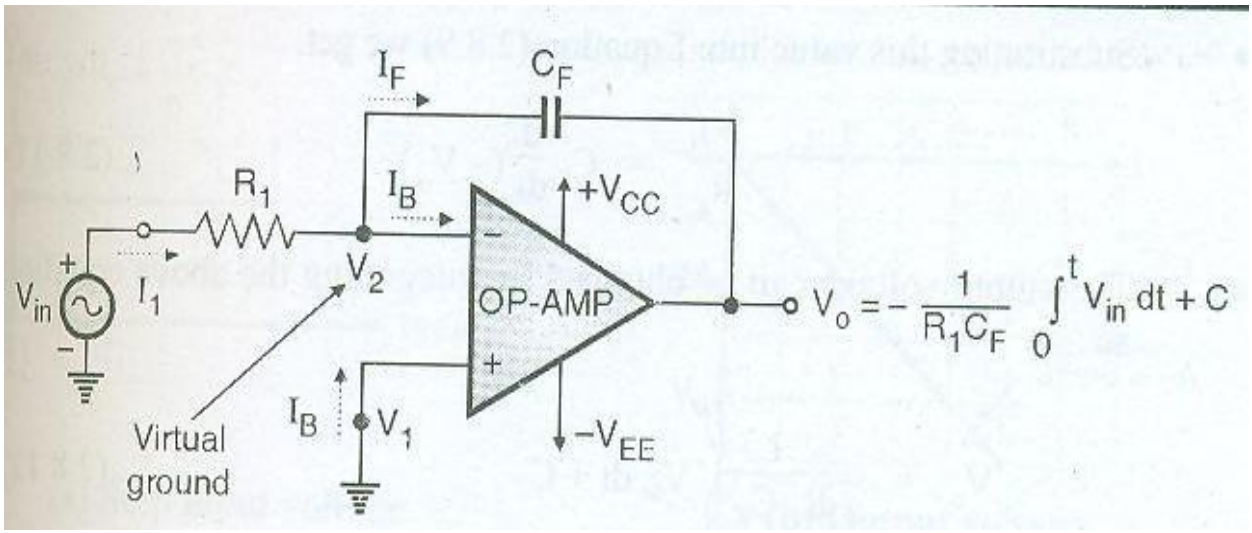


Fig: Circuit diagram of basic integrator using op- amp.

iii. State the need of signal conditioning.

Ans iii. **Signal conditioning- 2M**

- In an instrumentation system, a transducer is used for sensing various parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc.
- However the transducer output cannot be used directly as an input to the rest of the instrumentation system.
- The signal needs to be conditioned and processed. The signal conditioning can be of different types such as rectification, clipping, clamping etc.

iv. List any four specifications of LM 324

Ans iv. **Specifications of OP-amp LM 324 (any four points)- 2M**

- LM324 is a Low power Quad OP-amp. This IC contains four OP-amps.
- Can operate with single power supply (from 3V to 32V)
- Large DC voltage gain of 100 db
- Wide bandwidth of 1MHz
- Low input biasing current of 45 nA
- Low input offset voltage of 2 MV
- Low input offset current of 5 nA
- Very low supply current drain of approx. 700 microamperes.
- Low power drain makes it suitable for battery operated circuits.
- LM 324 is compatible with all forms of logic families.

v. Draw diagram of non- inverting amplifier.

Ans v. **Diagram: 2M**

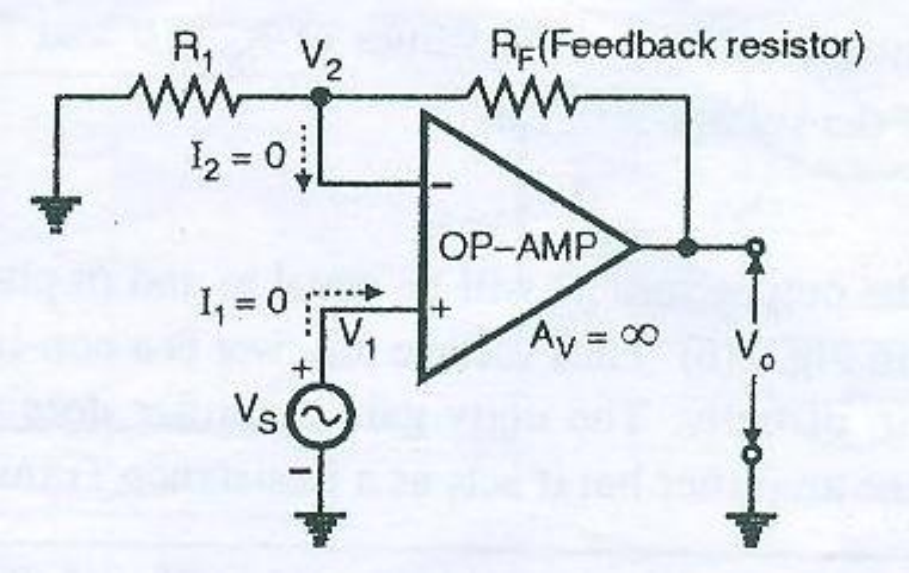


Fig: Non- inverting amplifier.

vi. Define following terms related with filter.

1. Cut- off frequency – **1M**
2. Stop Band- **1M**

Ans vi.

Cut off frequency: It is the frequency at which signal strength drops by 3 db (i.e. Signal power becomes half)

Stop Band: It is the band or range of frequencies which are not allowed to pass through to the output by the filter.

vii. Draw ideal and practical response of band reject filter with proper labeling

Ans vii. **Ideal response- 1M; Practical response: 1M**

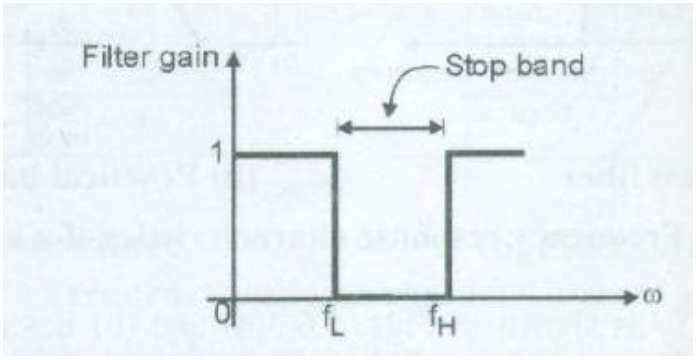


Fig: Ideal response

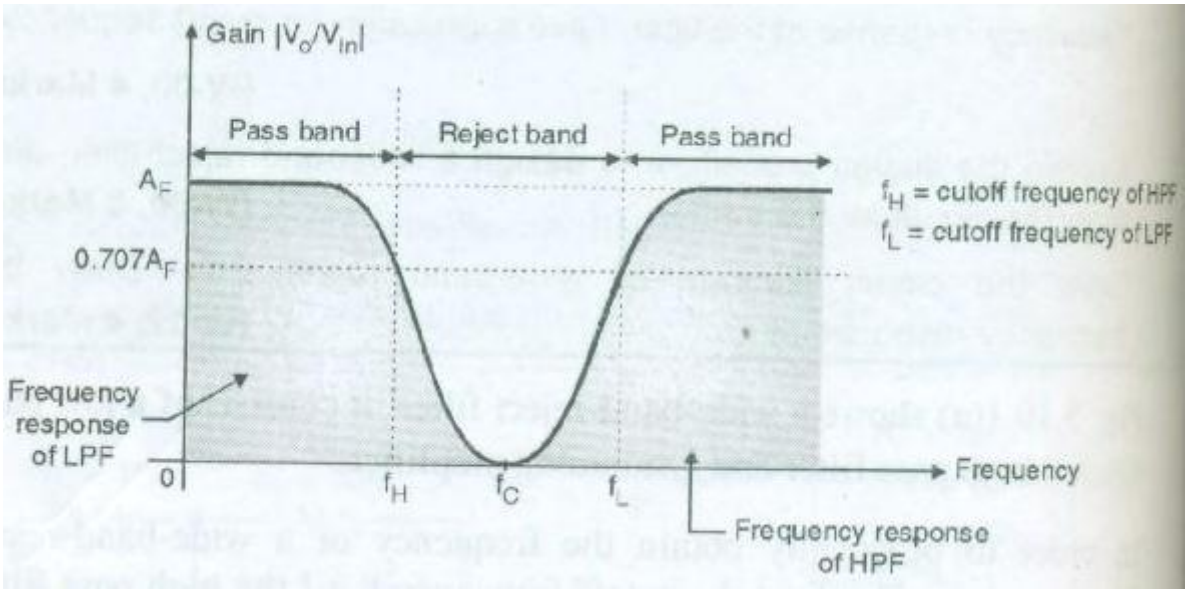


Fig: **Practical response**

viii. Draw pin diagram of IC- 555.

Ans viii. **Pin Diagram- 2M**

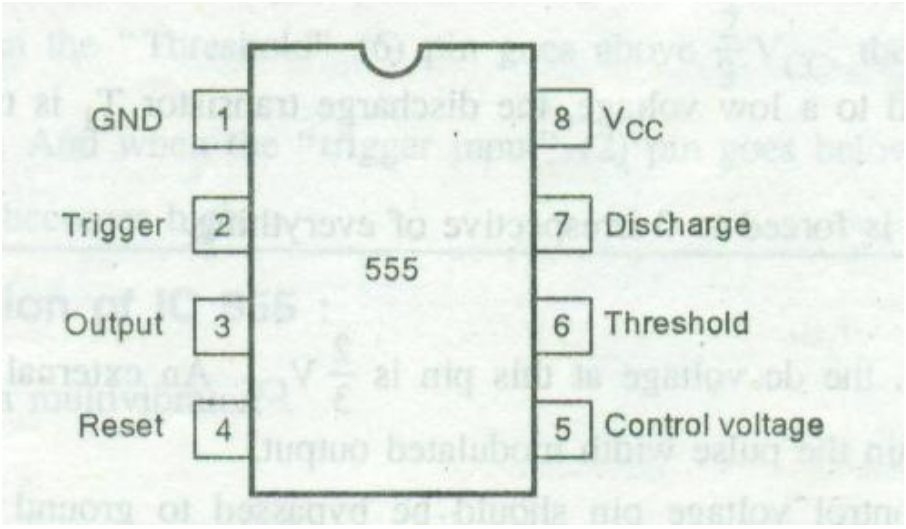


Fig: Pin diagram of IC -555

b. Attempt any TWO of the following: 8 Marks

i. Define:

1. Supply voltage rejection ratio**.- 1M**
2. Input offset voltage- **1M**
3. Slew rate- **1M**
4. Input bias current- **1M**

Ans b.

- **Supply voltage rejection ratio:** It is defined as the ratio of change of input offset voltage to the change in one supply voltage while keeping other supply voltage constant.
  Ideally**,** SVRR= 0
- **Input offset voltage (Vio)**: It is the input voltage that must be applied between both the input terminals of op- amp to make output offset voltage zero.
  Ideally value = 0
- **Slew rate:** It is defined as the maximum rate of change of output voltage per unit time.
  S.R.= Vo / t at max ; Unit = V/μs.
- **Input bias current:** It is defined as the average of the two currents flowing through inverting and non-inverting terminals of op amp

ii. List the ideal characteristics of op- amp with their ideal values **(any four)**

Ans ii.

Ideal characteristics of OP- amp : 4M

i) Voltage gain AV is infinite.

ii) Input Resistance RIN is infinite Ω

iii) Output resistance is 0 Ω

iv) Input offset voltage is 0 Volts

v) Input bias current is 0 nA

vi) Bandwidth is infinite

vii) CMRR is infinite

viii) Slew rate is infinite

ix) PSRR is zero

x) Input offset current is zero

xi) Output offset voltage is zero volts.

iii. Describe the term dual input balanced output differential amplifier and dual input unbalanced output differential amplifier and draw single input unbalanced output differential amplifier.

Ans iii. **(Description – 2 marks, diagram – 2 marks)**

Dual input balanced output differential amplifier:

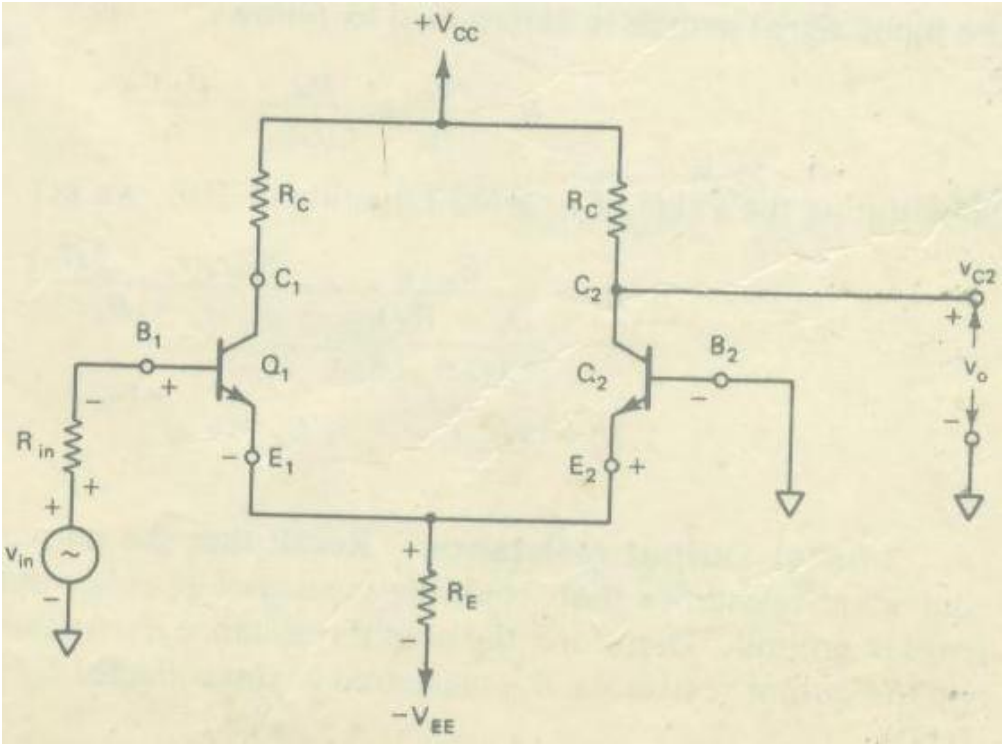
If We Use Two Input Signals The Configuration Is Said To Be Dual Input And If The Output Voltage Is Measured Between Two Collectors It Is Referred To As Balanced Output Because Both Collectors Are At Same Dc Potential With Respect To Ground.

Dual input unbalanced output differential amplifier:

If We Use Two Input Signals The Configuration Is Said To Be Dual Input And If The Output Is Measured At One Of The Collectors With Respect To Ground The Configuration Is Called As Unbalanced Output.

Two Matched Semiconductors of the Same Type (BJT'S Or FET'S) Are Required For The Differential Amplifiers.

Diagram of single input unbalanced output differential amplifier



2) Attempt any FOUR of the following: **16 Marks**

a. Compare open loop and close loop configuration on the following basis.

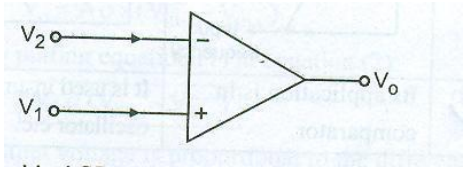
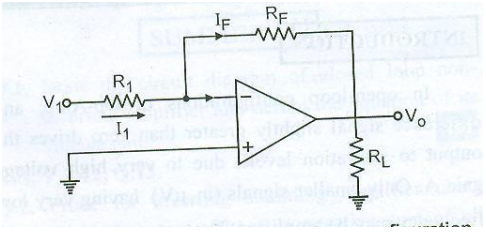
i. Circuit diagram-**1M**

ii. bandwidth- **1M**

iii. Gain- **1M**

iv. Applications- **1M**

Ans a.

Sr. No	Parameters	Open loop	Closed Loop
1	Circuit Diagram		
2	Bandwidth	Bandwidth is low	Bandwidth is high
3	Gain	Voltage gain is very high	Voltage gain is low as compared to open loop.
4	Application	Comparator ,zero crossing detector	It is used in linear amplifier, oscillator etc

b. Draw diagram of voltage follower. Why it is called voltage follower? State its one application.

Ans b. **Diagram:2 M; Voltage follower: 1M; Application: 1M**

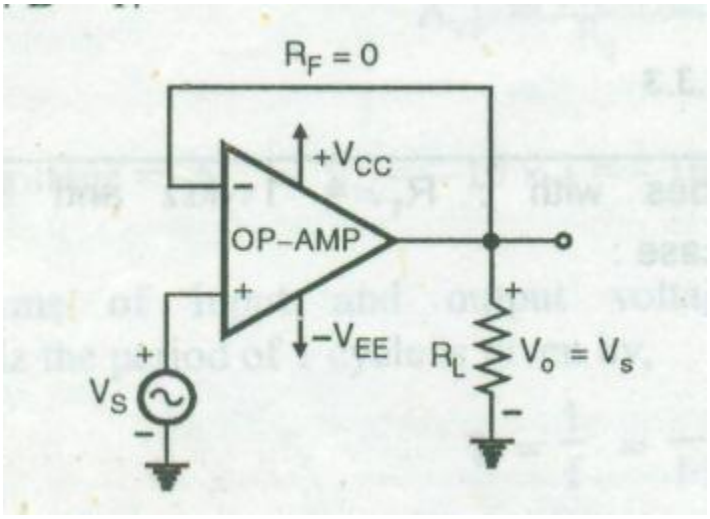


Fig: Voltage Follower

- When $R_1 = \infty$ and $R_F = 0$ the non-inverting amplifier gets converted into a voltage follower or unity gain amplifier.
  When the non- inverting amplifier is configured so as to obtain a gain of 1, it is called as voltage follower or unity gain non- inverting buffer.
- **Applications: Any one**
  1. As a buffer amplifier so as to avoid the loading of the source.
  2. As the output stage.
  3. For impedance matching.

c. Describe the operation of instrumentation amplifier using three op- amp.

Ans c. **(diagram – 2 marks, explanation – 2 marks)**

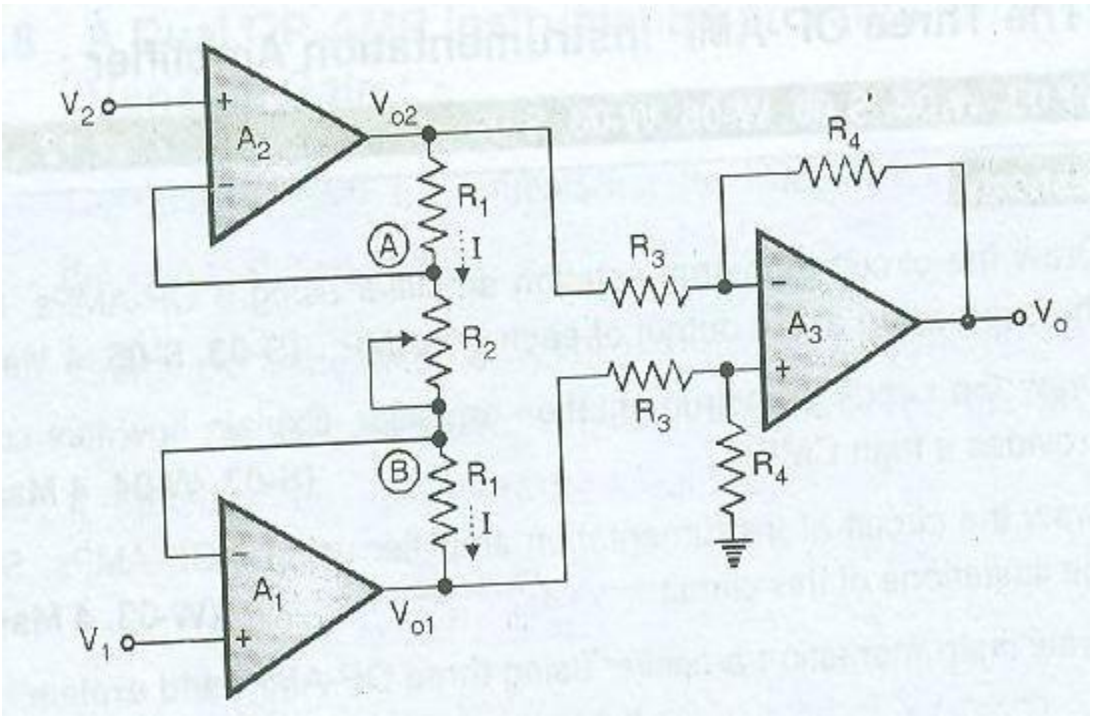
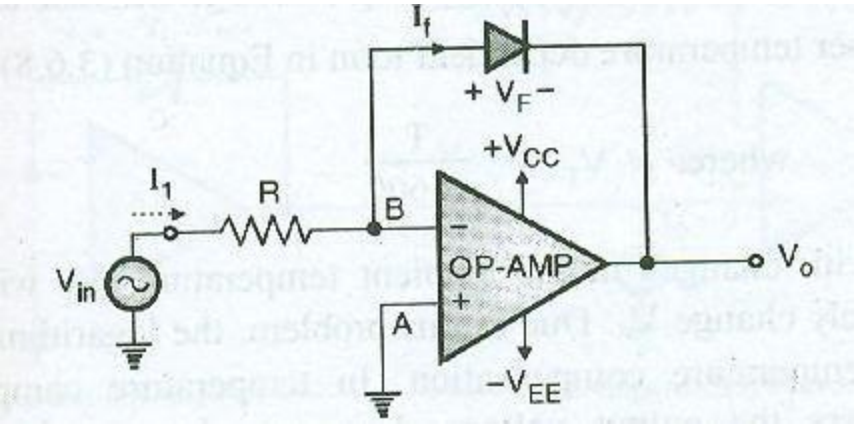


Fig: Instrumentation amplifier using three Op- Amp

- The high impedance instrumentation amplifier using cross coupled difference amplifiers is as shown in fig.
- A_1 and A_2 in Fig are basically non inverting amplifiers with their inverting (-) terminal connected to resistors R_2 instead of connecting it to ground.
- As the input impedance of all OP- AMPs used in assumed to be infinite their input current is zero. Therefore current flowing through the resistors R_1, R_2 and R_3 is same i.e.I.
- The overall gain of Av of the three Op-Amp instrumentation amplifier is given by
  $Av = Av_1 \times Av_2$
  Therefore, $Av = \left[1 + \frac{2R1}{R2}\right] \times \frac{R4}{R3}$
- Hence by using a variable resistor R2 the overall gain can be easily and linearly varied.
- The output is then given by
  $Vo = Av \times (V_1 - V_2)$

d. Draw the diagram of log amplifier using op- amp and derive expression for its output voltage.

Ans d. **(diagram – 2 marks, derivation – 2 marks)**



A p-n junction diode is connected in the feedback path. Therefore the output voltage is nothing but the voltage across this diode.

- Therefore Vo= -VF --------1
- Due to high impedance of OP- AMP the current going into the inverting terminal is zero
- Therefore I1= IF= Vin/R--------2

$$V_o = -\eta V_T [\log_e (I_f) - \log_e (I_o)]$$

$$= -\eta V_T [\log_e (V_{in}/R) - \log (I_o)]$$

$$\text{Thus } V_o = -\eta V_T \log_e \left[\frac{V_{in}}{R \cdot I_o}\right]$$

$$\therefore V_o = -\eta V_T \log_e \left[\frac{V_{in}}{V_{ref}}\right]$$

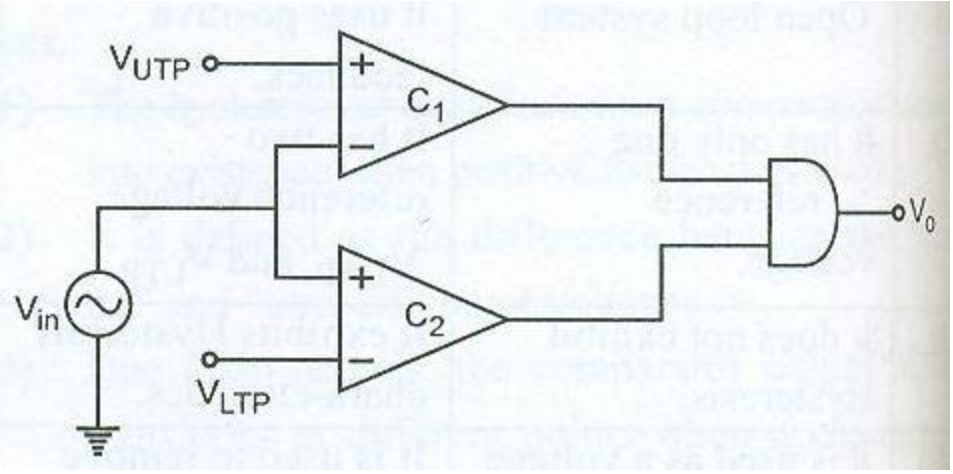
where $V_{ref} = R \cdot I_o$ = fixed dc voltage.

- The output voltage is proportional to the logarithm of input voltage.

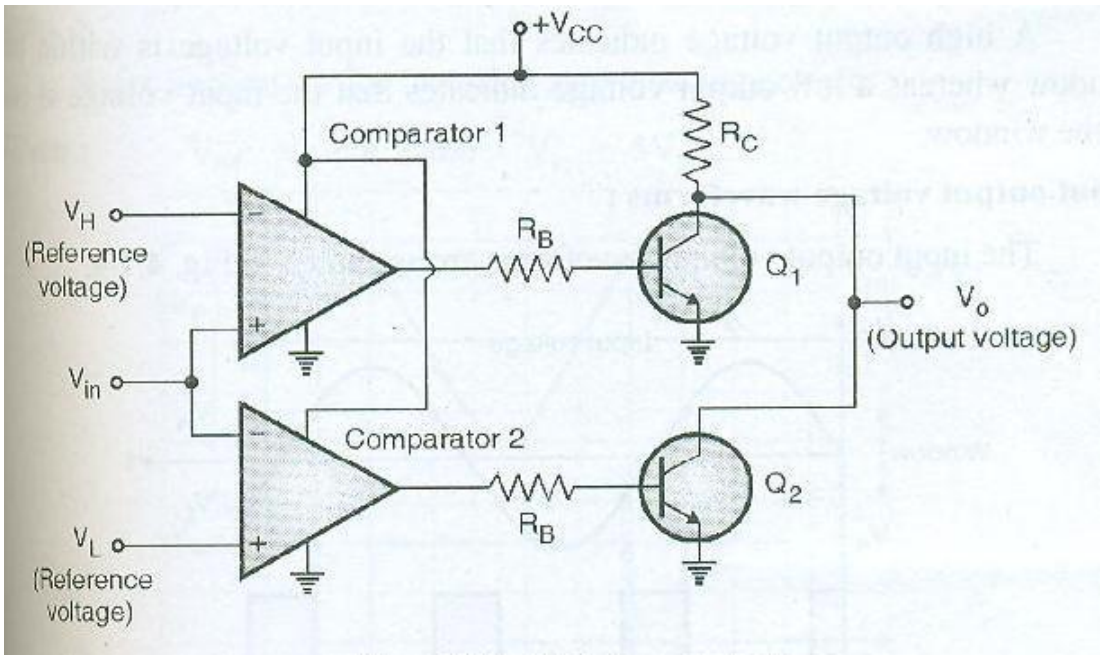
- The output is in terms of natural log i.e. loge. If we want the output to be in terms of log10 then we should use the following conversion equation: log10 Vi = 0.434 loge (Vi)

e. Draw the circuit diagram of window detector and describe its operation.

Ans e. **(diagram – 2 marks, explanation – 2 marks)**



OR



- The window detector uses two comparators C1 and C2.
- The reference voltage of inverting comparator C1 is VUTP and the reference voltage of the non-inverting comparator C2 is V_{LTP}. Assume $V_{LTP} < V_{UTP.}$
- Case I: When Vin< V_{UTP} then the differential voltage of C2 is negative. Hence output of C2 is low. Vin is also less than V_{UTP}. Hence output of C1 is high and output Vo of AND gate is low.
- Case II: When Vin> V_{UTP}, then the differential input voltage of C2 is high. The differential input voltage of C1 is negative. The differential input voltage of C1 is negative. Hence output of C1 is low and output Vo of AND gate is low.
- Case III: When V_{LTP}< Vin< V_{UTP}, the differential input voltage of C1 and C2 is positive and output is high. The output of AND gate is high.

f. Design and draw low pass filter with cut – off frequency 1KHz and pass band gain of 2.

Ans f. **(any relevant correct design – 2 marks, final design diagram – 2 marks)**

Given: Pass band gain (A_f) = 2

Cut-off Frequency (f_c) = 1 kHz

Pass band Gain (A_f) is given by the formula

$A_f = 1 + R_F / R_1$

Here $A_F = 2$

Therefore $2 = 1 + R_F / R_1$

So, $1 = R_F / R_1$

Therefore, $R_F = R_1$

Let $R_F = 10k\Omega$, Therefore $R_1 = 10k\Omega$

Assume C= 0.01 µF

But $F_c = 1 / 2\pi RC$.

But F_c= 1kHz

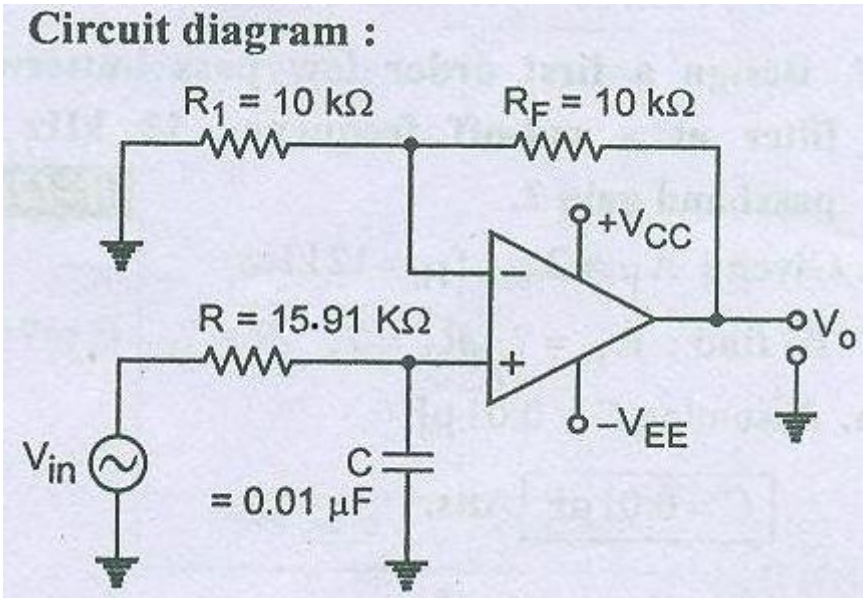
Therefore, 1 kHz= $1 / 2\pi RC$

So,

$R = 1 / 2\pi \times 1 \times 10^3 \times 0.01 \times 10^{-6}$

$R = 1 / 0.0628 \times 10^{-3}$

Therefore, R= 15.91 kΩ



Q 3. Attempt any FOUR of the following: (16 marks)

a) Design and draw the circuit for the following operation using op-amp. Vo= V1+ V2 -2 V3.

Ans:- **(any relevant correct design – 2 marks, final design diagram – 2 marks)**

Assume R = 1kΩ,

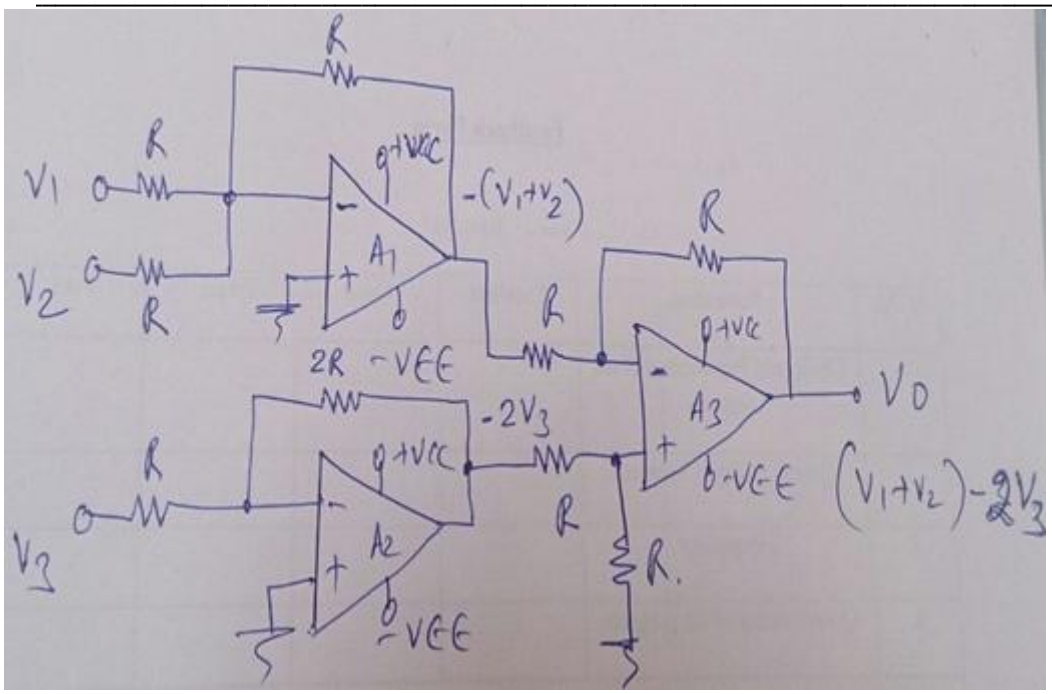
Hence output of first inverting amplifier $Vo1 = \frac{-R}{R}(V_1 + V_2) = -(V_1 + V_2)$

Output of second inverting amplifier is $V02 = \frac{-2R}{R}(V_3) = -2V_3$

Therefore, final output of third difference amplifier is derived as

$Vo = Vo2 – Vo1 = [-2V_3 + (V_1 + V_2)] = V_1 + V_2 - 2V_3$

The designed circuit to get the o/p



b) Explain the concept of frequency compensation of op-amp and offset nulling.

Ans: **Frequency compensation for op- amp: (2M)**

In an op- amp many number of stages are present. Each stage produces it's own capacitive component. Therefore there many break frequencies present in uncompensated op- amp. The uncompensated op- amp having multiple break frequencies are unstable.

In order to make them stable, their frequency response should be modified in such a way that there is only one break frequency. This is done by a technique called as frequency compensation. This is achieved by adding a small capacitor either internally or externally.

In op- amp like IC 741 an internal capacitance of 30pF is added to provide internal frequency compensation. In some op- amps internal capacitor is not added to provide internal frequency compensation. Such op- amps can be externally compensated by adding external capacitor in the circuit to get only one break frequency & achieve stability.

Offset nulling: (2M)

The 741 type op – amp the manufacturer recommends that a 10 kΩ potentiometer be placed across offset null pins 1 and 5 and a wiper be connected to the negative supply pin 4 . Adjustment of this pot will null the output. By varying the position of the wiper on the 10kΩ potentiometer, we are trying to remove the mismatch between inverting and non- inverting input terminals of the op- amp. Adjust the wiper until the output offset voltage is reduced to zero.

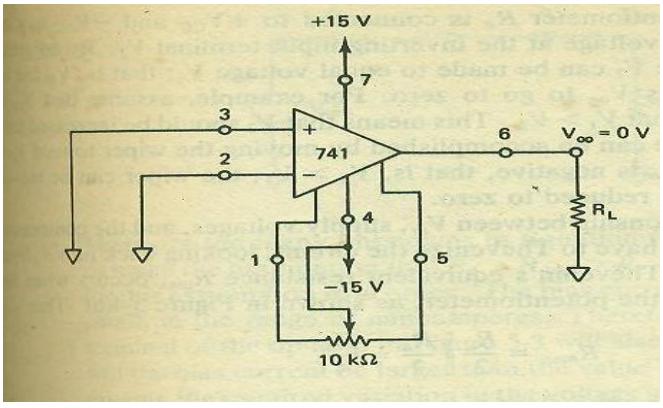


Fig: Voltage offset null circuit

c) Design the circuit to obtain output voltage Vo= -5 (V1+V2). Draw the designed circuit.

Ans:- **(any relevant correct design – 2 marks, final design diagram – 2 marks)**

Required o/p,

$$V_0 = -5(V_1 + V_2) \quad \ldots(1)$$

We know, $V_0 = \frac{-R_F}{R_1}[V_1 + V_2]$ $\ldots(2)$

As it is an inverting adder with gain = – 5 by comparing equation (1) & (2)

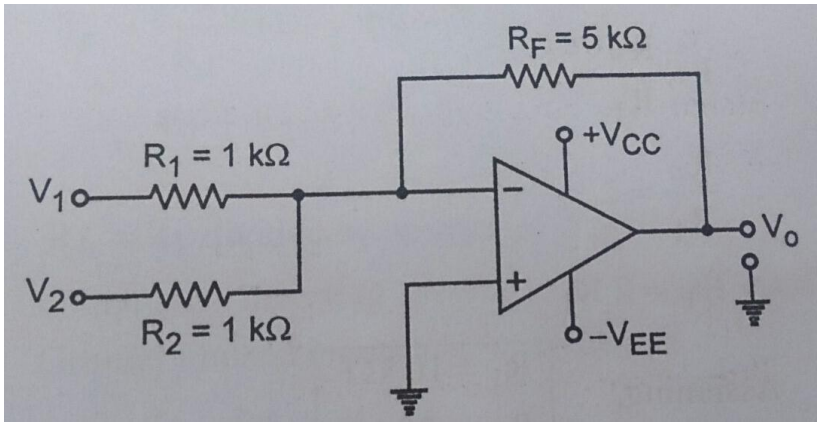
$$\therefore \frac{R_F}{R_1} = 5$$

$$\therefore R_F = 5 \times R_1$$

Assuming $R_F = 5\,k\Omega$

$$R_1 = 1k\Omega$$

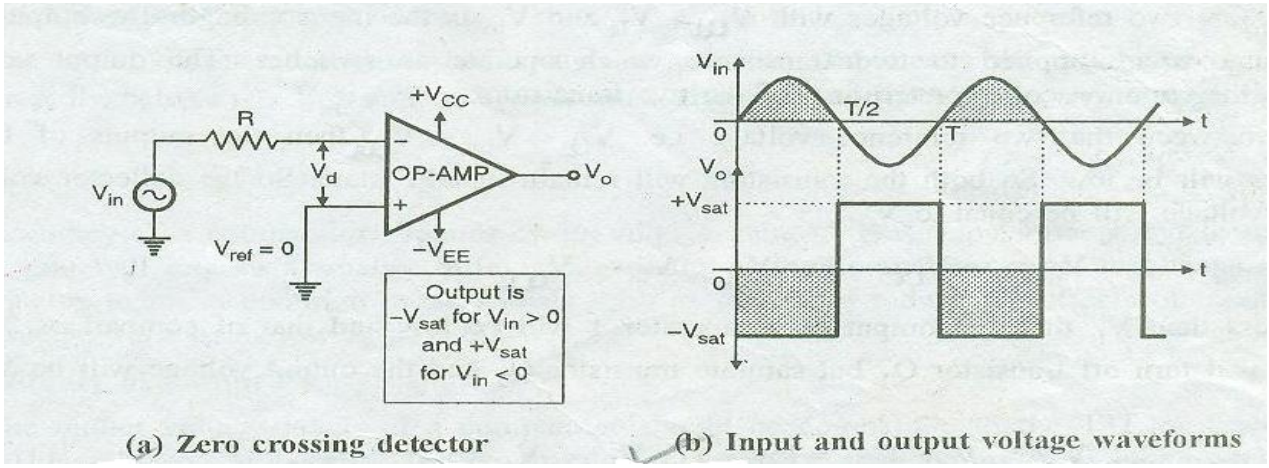
Designed circuit



d) Draw the circuit diagram and input output waveforms of inverting ZCD and non-inverting ZCD.(zero crossing detector).

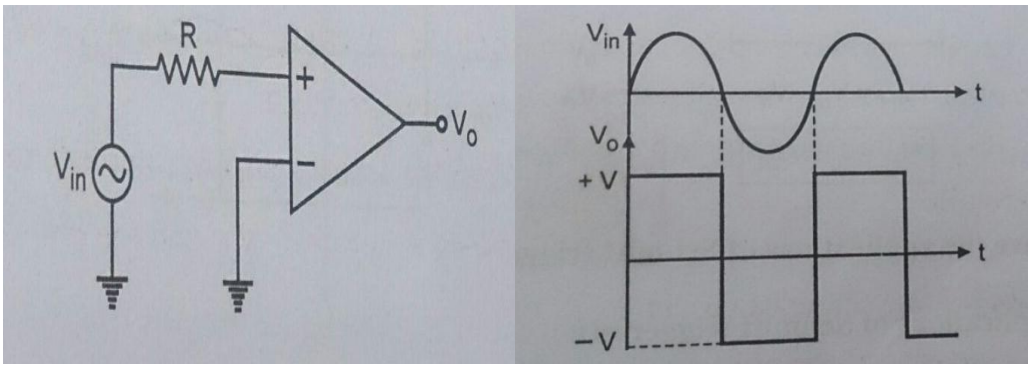
Ans: **(diagram, waveforms - 1 mks each)**

Inverting ZCD:



(a) Zero crossing detector (b) Input and output voltage waveforms

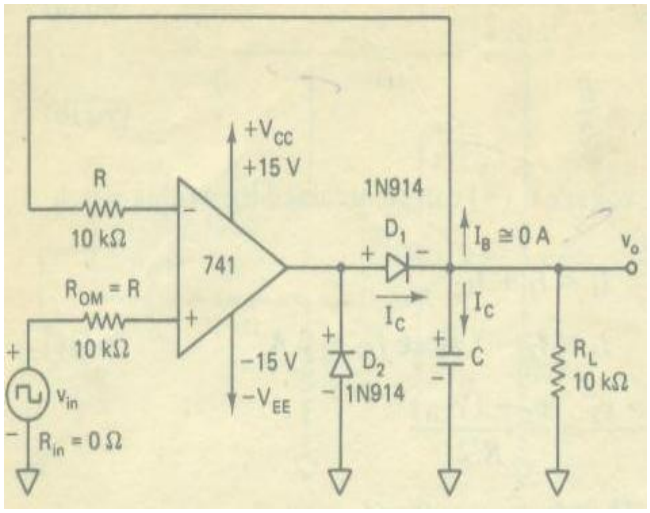
Non-inverting ZCD:



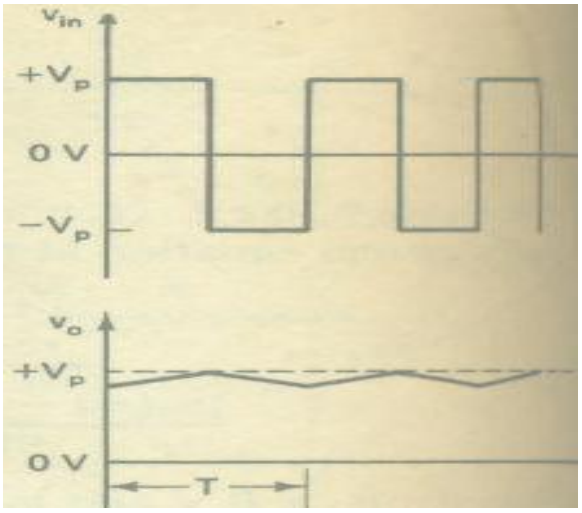
e) Draw circuit diagram of peak detector and explain with input output waveforms.

Ans: (**Diagram: 2 Marks; Working: 1 Mark, waveform: 1 mark)**

Note: Positive or Negative Peak Detector should be considered and marks to be given



Positive peak detector



input / output waveform

Operation: - Peak detector measures the positive peaks of the values of the square wave input. During the positive cycle of Vin, the output of the Op-Amp drives the D1 ON, charging capacitor C to the positive peak value Vp of the input voltage Vin. Thus when D1 is forward biased, the Op-Amp operates as a voltage follower. On the other hand, during the negative half cycle of Vin Diode D1 is reverse biased, and voltage across C is retained. The only discharge path for C is through RL since the input bias current Ib is negligible.

For proper operation of circuit, the charging time constant (C Rd) and discharging time constant (C R_L) must satisfy the following condition:

C Rd $\leq$ T / 10

Where Rd = resistance of forward biased diode, T = time period of input waveform.

And $CR_L \geq 10$ T

Where R_L is the load resistor

(OR)

Negative peaks of input signal Vin can be detected simply by reversing diodes D1 and D2.

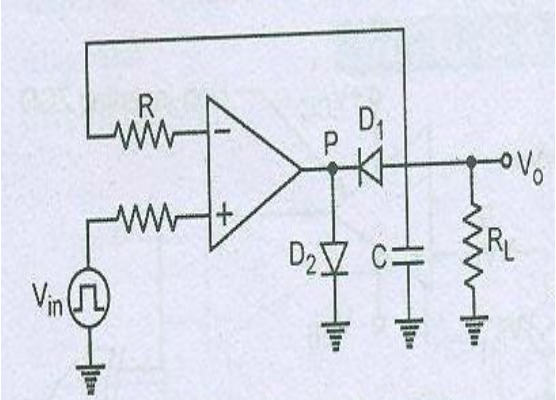


Fig. (a) Negative peak detector

f) Draw circuit diagram and frequency response of wideband pass filter.

Ans: **(circuit diagram 2M, frequency response - 2 marks)**

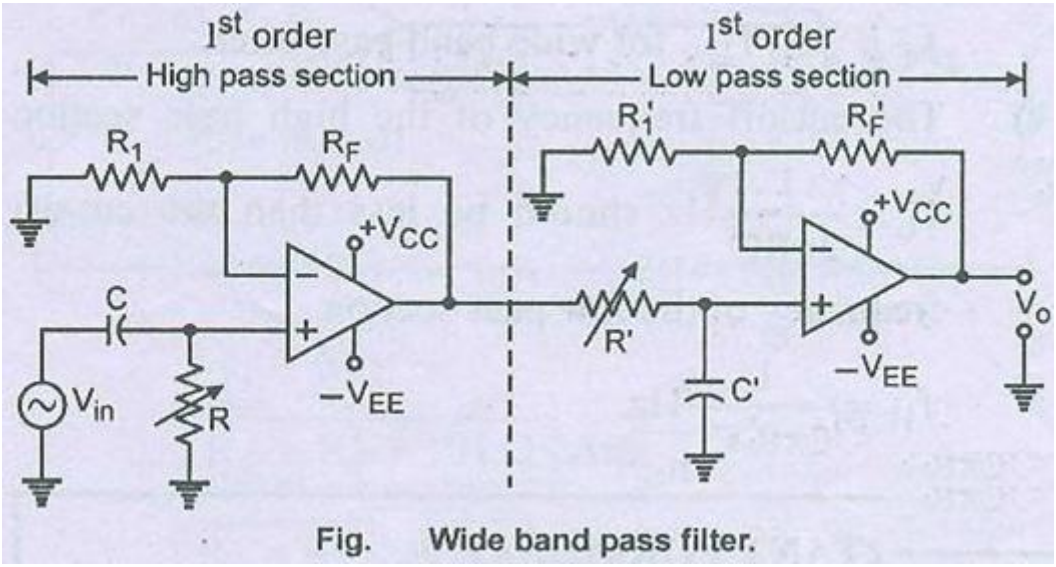
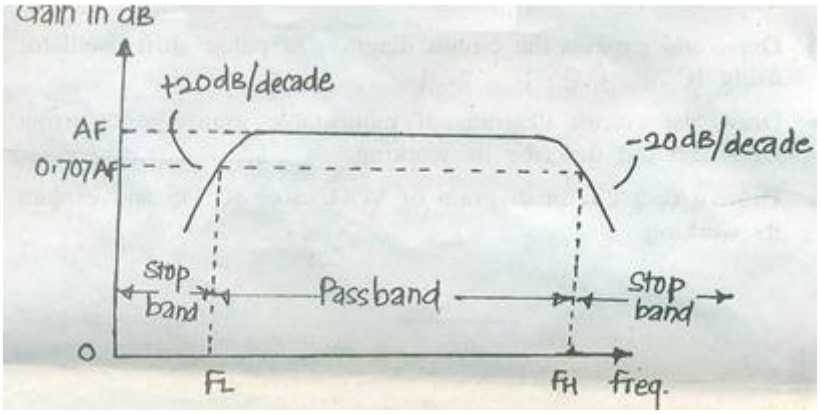
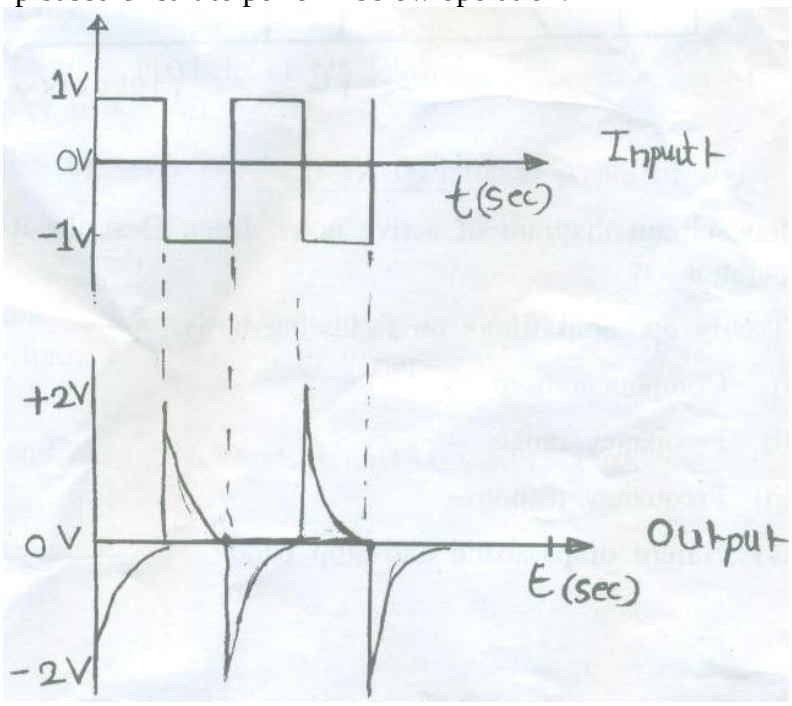


Fig. Wide band pass filter.



Q4. Attempt any four of the following **16 marks**

a) Suggest the op-amp based circuit to perform below operation.



Ans: **(Correct answer 4 mks, diagram optional)**

As the input square waveform is converted into spikes, the circuit suggested is differentiator.

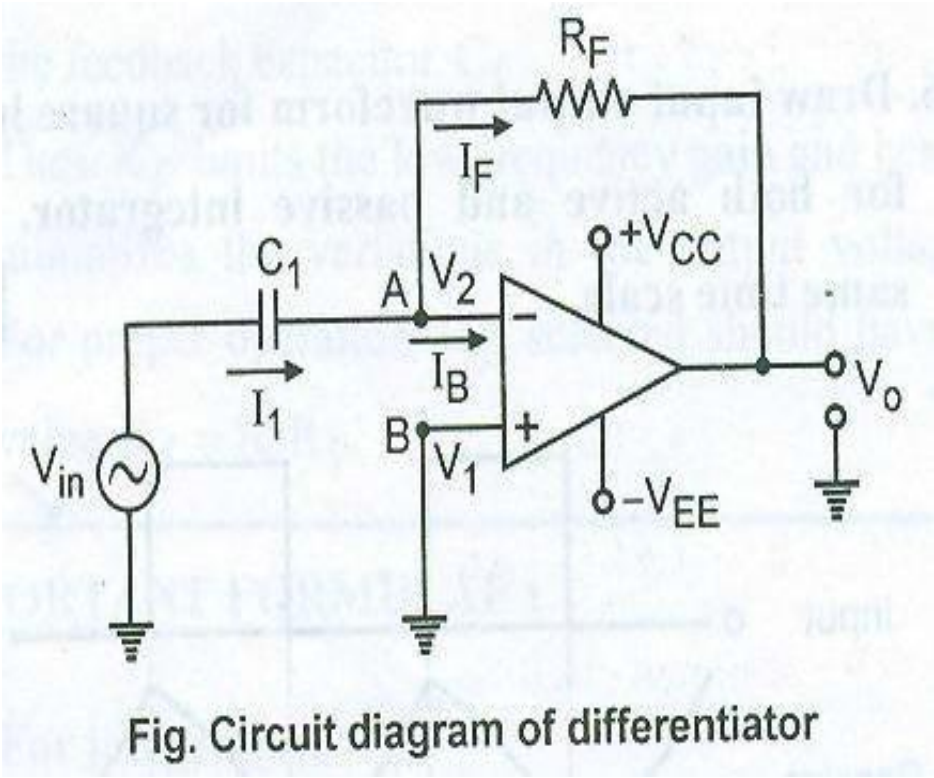


Fig. Circuit diagram of differentiator

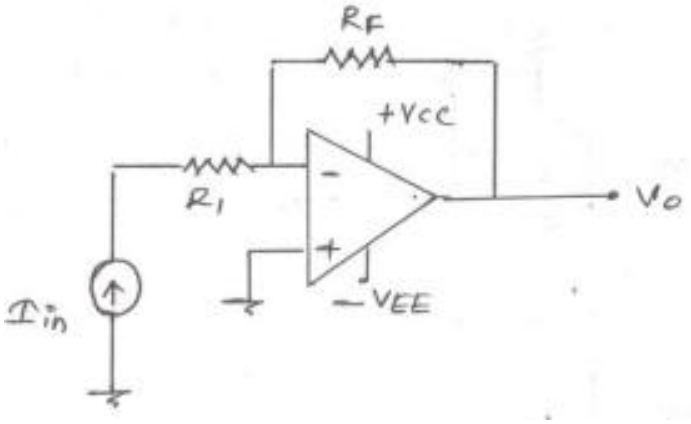
b) Draw circuit diagram of current to voltage converter and derive the expression for its output.

Ans:- **(diagram – 2 marks, derivation – 2 marks)**

A current to voltage convertor is a circuit ion which the o/p voltage is a function of i/p current,

i.e., $V_o \alpha I_i$

Consider the current to voltage convertor circuit shown below Op-amp is in Inverting mode



The open loop gain A_V of the op-amp is very large. So as per the concept of virtual short, the input impedance of the op-amp is very high.

Therefore, the current entering into the two terminals is very small,

$I_{B1} = I_{B2} = 0$

The gain of inverting amplifier is

$$A_{V=}\frac{V0}{Vin}=\frac{Rf}{R1}$$

$$V_{0=}-\frac{Rf}{R1}Vin--------1$$

But, $V_1 - V_2$ & V_1 is connected to ground.

$V_1 = 0$

$$\therefore V_2 = 0$$

Thus the inverting terminal also is at ground potential & the entire I/P voltage across R_1 is

$$I_{in=}\frac{Vin}{R1}$$

$$\therefore V_{in} = I_{In\ R1}-------2$$

Now put the value Vin in equation 1 we get

$$V_o = \frac{-RF}{R1} * R1 * Iin$$

$$\therefore Vo = -Rf * Iin$$

c) Describe the operation of op-amp based Schmitt trigger for sine to square wave conversion with the help of circuit diagram.

Ans: **(Circuit diagram -2 marks, operation -2 marks)**

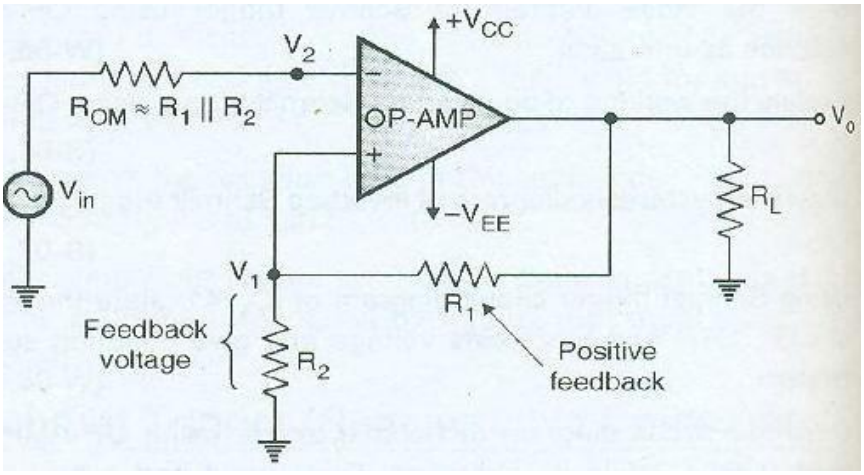


Figure shows an inverting comparator with positive feedback. The input voltage triggers the output, every time it exceeds certain voltage level called upper threshold voltage and lower threshold voltage.

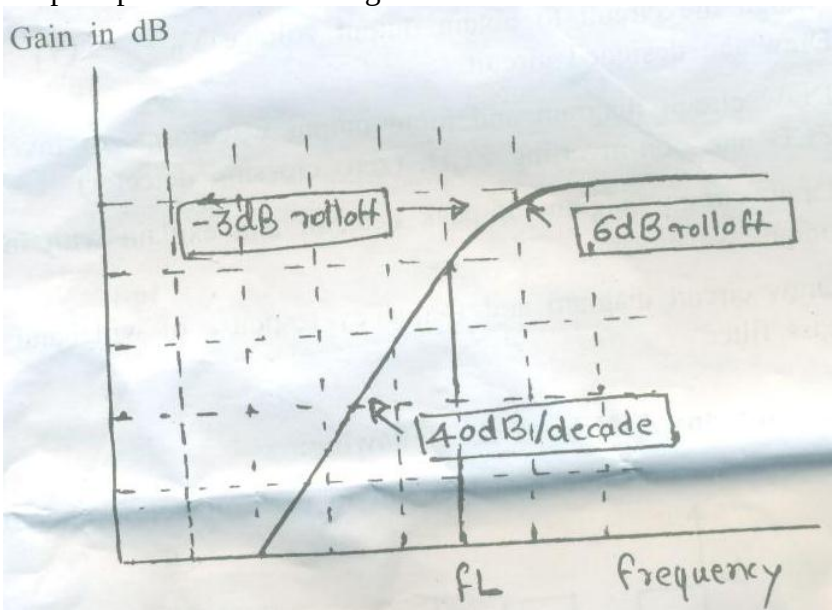
The threshold voltage is obtained by the divider circuit R1-R2. The voltage across R1 is variable reference threshold voltage, which depends on the value and polarity of the output voltage Vo.

When Vo=+Vsat the voltage across R1 is called the upper threshold voltage, Vut. The input Vin is greater than Vlt and this causes Vo to switch from +Vsat to –Vsat.

As long as Vin < Vut, Vo is +Vsat. On the other hand, when Vo = -Vsat, the voltage across R1 is referred to as lower threshold voltage Vlt.

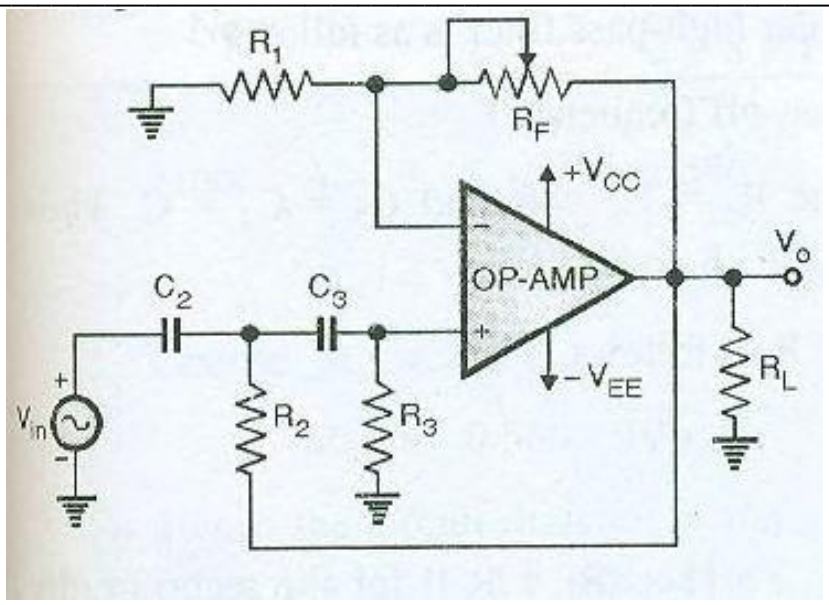
Vin must be slightly more negative than Vlt in order to cause Vo to switch from –Vsat to +Vsat.

d) Suggest and draw op-amp based circuit using Butterworth filter to fulfill following response.



Ans: **(suggestion proper- 2 mks, diagram – 2mks)**

The Butterworth filter suggested **is second order high pass filter**



Second order high pass filter

e) Draw circuit diagram of active notch filter. Describe its operation.

Ans: (**Circuit: 2M; Description with frequency response-1 mks each)**

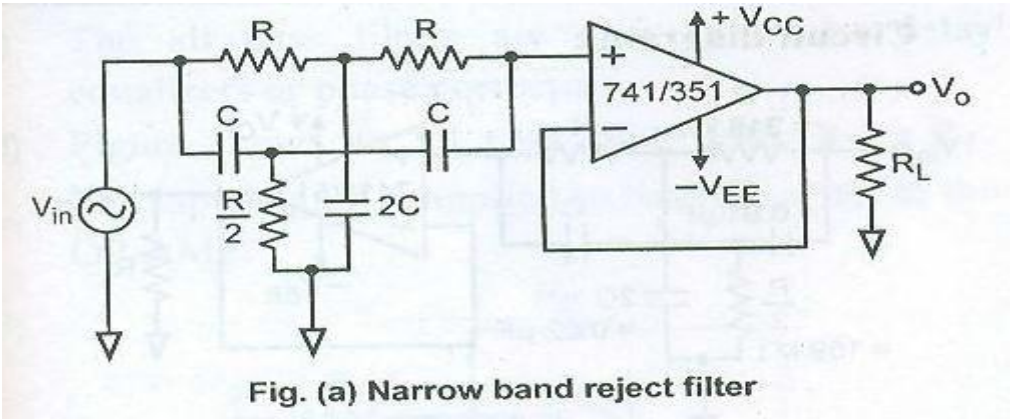


Fig. (a) Narrow band reject filter

- Fig. shows a narrow band rejects active filter often called as Notch filter. It uses a twin T-network.
- The twin T- network is a passive filter composed of two T- shaped networks.
- One T- network is made up of two resistors and capacitors while the other uses two capacitors and a resistor.
- The notch out frequency is the frequency at which maximum attenuation occurs, it is given by
  - $f_N = 1/ 2\pi RC$ (Hz)
- The twin T- network has very low figure of merit Q. this is increased by using it with a voltage follower as shown in fig. The output of the voltage follower is fed back to the junction of R/2 and C.
- Q> 10 for narrow band reject filter.
- One typical application of such filter is for rejection of single frequency, such as
  - 50 Hz power line frequency hums. This notch filter is also used in communication and Bio- medical instruments for eliminating undesired frequencies.
- Frequency in equation (1) is the frequency to be rejected. Choosing $C \leq 1\mu F$ and
  - then calculate for R, from the equation.

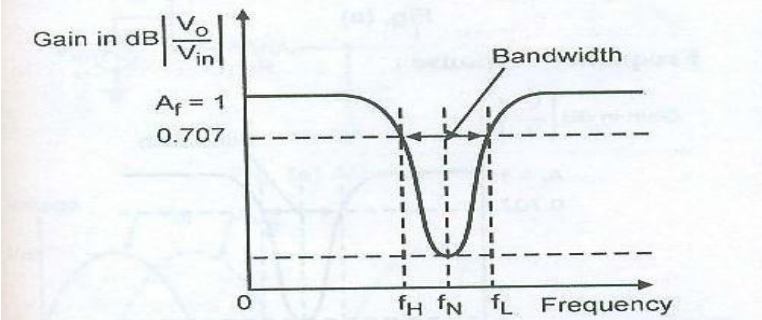


Fig. (b) Frequency response of narrow band reject filter

f) Classify op-amp filters on the following basis:
   i) component used
   ii) frequency range
   iii) frequency response
   iv) nature of passband and stop band

   Ans **: (each correct classification – 1 mark)**

1) On the basis of component used, filters can be divided as active and passive filters.

2) On the basis of frequency range, can be divided as AF (audio frequency) or RF (radio frequency) filters.

3) On the basis of frequency response filters can be divided as high pass, low pass, band pass and band reject filters.

4) On the basis of nature of pass band and stop band, they can be divided as narrow band pass, wide band pass, narrow band reject and wide band reject filters.

Q 5. Attempt any four of the following (16 marks)

a) Draw and describe the operation of touch plate switch using IC-555.

Ans: (**Circuit Diagram- 2Marks, Operation- 2Marks)**

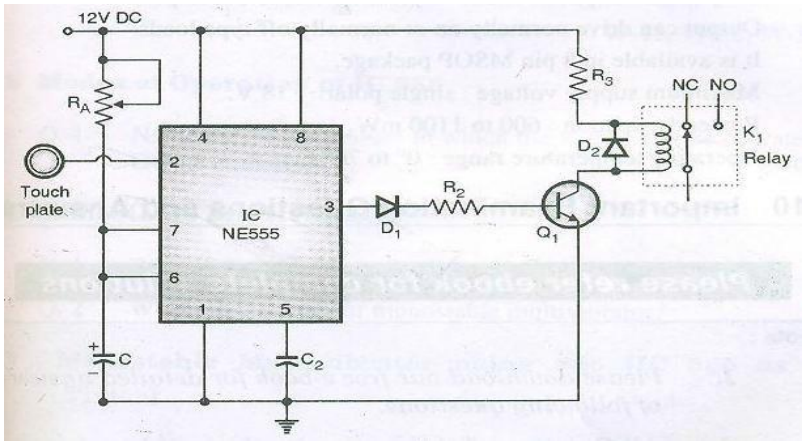


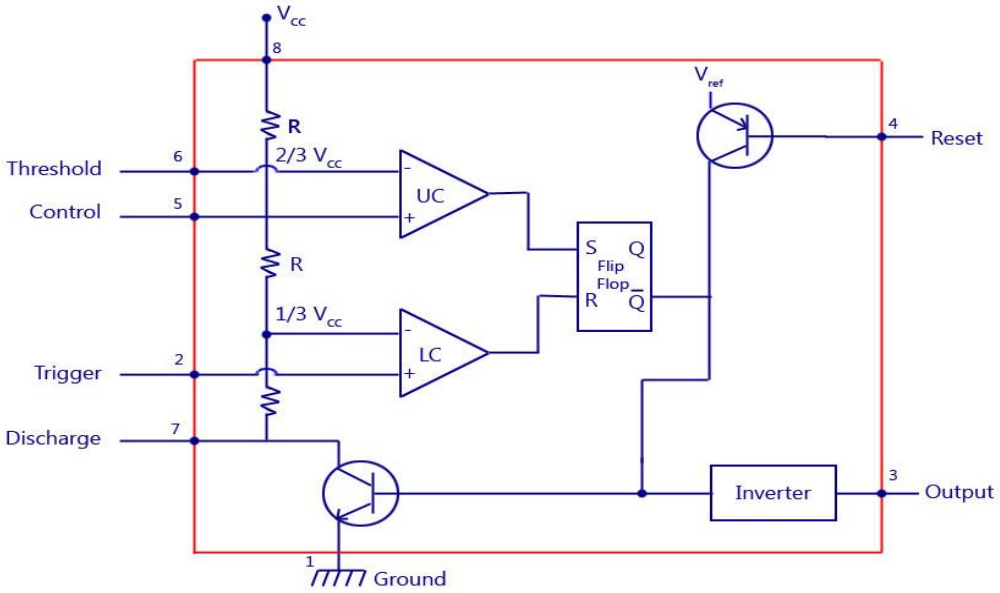
Fig: Touch switch circuit diagram

Operation: - A touch plate (push to ON) is used to turn on the timer and active the relay. As soon as touch plate is switched ON (pushed), a trigger pulse is produced and applied to pin no. 2 of IC 555, and the output of IC 555 goes high.

It will remain high for a period of T_{ON}= 1.1 R_AC. The high output of IC 555 activates the transistor Q_1 which in turn energize the relay coil, and closes the N.O (Normally open) contact of the relay.

b) Draw block diagram of SE 555. State function of both internal transistors in IC 555.

Ans: **(2 marks diagram, 1 mark each for function of transistors)**



Function of internal transistors:-

1) Transistor Q1(NPN) called as discharge transistor, which is connected between discharge pin 7 and ground pin 1, provides discharge path for external timing deciding capacitor.
2) Transistor Q2 (PNP) called as reset transistor is used to reset the IC 555(by providing a negative pulse) if required. For normal operation pin 4 is connected to +Vcc (pin 8).

c) Define and state the expression for lock range and capture range of PLL.

Ans: **(2 marks for lock range and 2 marks for capture range)**

Lock range: the range of frequencies over which the PLL can maintain the phase lock with the incoming signal Fs, is defined as the lock in range.

Lock range = $f_{L=} 2 \Delta f_L$

Where $f_L = 8 f_0 / V$

Capture range : it is defined as the range of frequencies over which the PLL can acquire lock with the input signal Fs

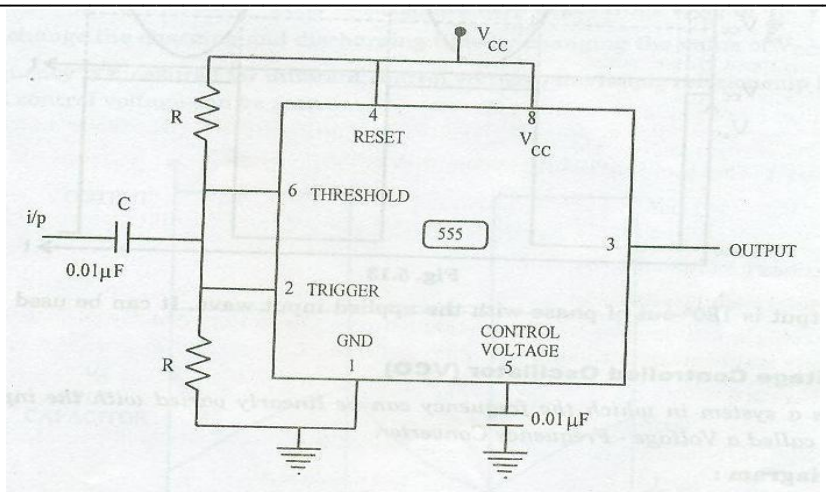
Capture range = $2 \Delta f_c$

Where $f_c = f_L / (2\pi * 3.6 * 10^3 * C)$

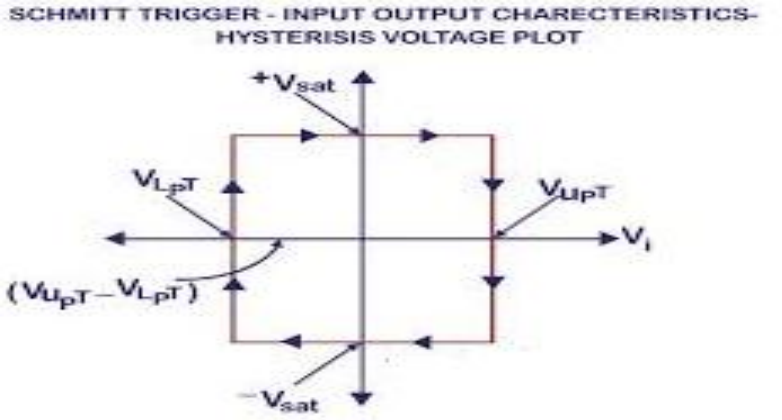
d) Define Schmitt trigger. Draw Schmitt trigger using IC-555. Draw its hysteresis diagram.

Ans: **(Definition 1 mark, circuit diagrams - 2 marks, hysteresis plot - 1 mks)**

A **Schmitt trigger** is a comparator circuit with hysteresis implemented by applying positive feedback to the non-inverting input of a comparator or differential amplifier. It is an active circuit which converts any i/p into square wave o/p.



Schmitt trigger using IC 555.



Hysteresis curve

e) Design and draw op-amp based phase shift oscillator for frequency 200 Hz.

Ans: **(Proper design with proper selection of components R & C -2 marks, Diagram for 2 Marks)**

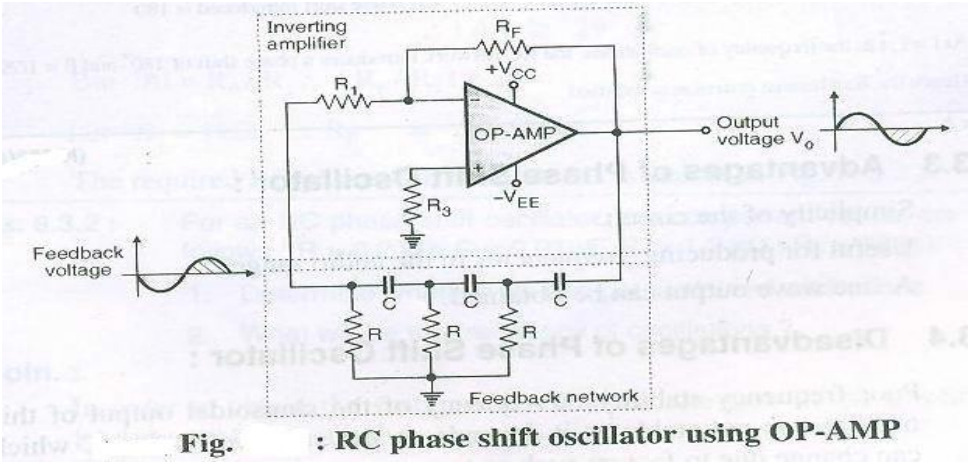


Fig. : RC phase shift oscillator using OP-AMP

For phase shift oscillator , output frequency is given as

Fo = 0.065/ RC

Lets Assume C=0.1μF

200= 0.065/(R * 0.1 *$10^{-6)}$

Hence, R = 3250Ω=3.2KΩ

For oscillator, the gain A> 29

A=1 + Rf/R1>29

Let R1= 1 kΩ

Hence Rf = 28 kΩ

f) For IC 555 configured as astable multivibrator. R1=5.8KΩ, R2= 2.8 KΩ and C=0.1μF. Find the frequency of oscillation and duty cycle. Draw output waveform.

Ans:

Given: R_1= 5.8KΩ , R_2= 2.8KΩ and C= 0.1 μ F

Solution: The time period of one cycle of the output voltage waveform is given by,

$T = T_{on} + T_{off}$

$= 0.693 (R_1 + 2R_2) C$

$= 0.693 [5.8 \times 10^3 + 2x (2.8 \times 10^3)] \times 0.1 \times 10^{-6}$

$= 7.9 \times 10^{-4}$

T= 0.79 msec **(1M)**

Therefore,

Hence the frequency of oscillations is given by,

F= 1/T

$F= 1/ 0.79 \times 10^{-3}$

F = 1.26 KHz **(1M)**

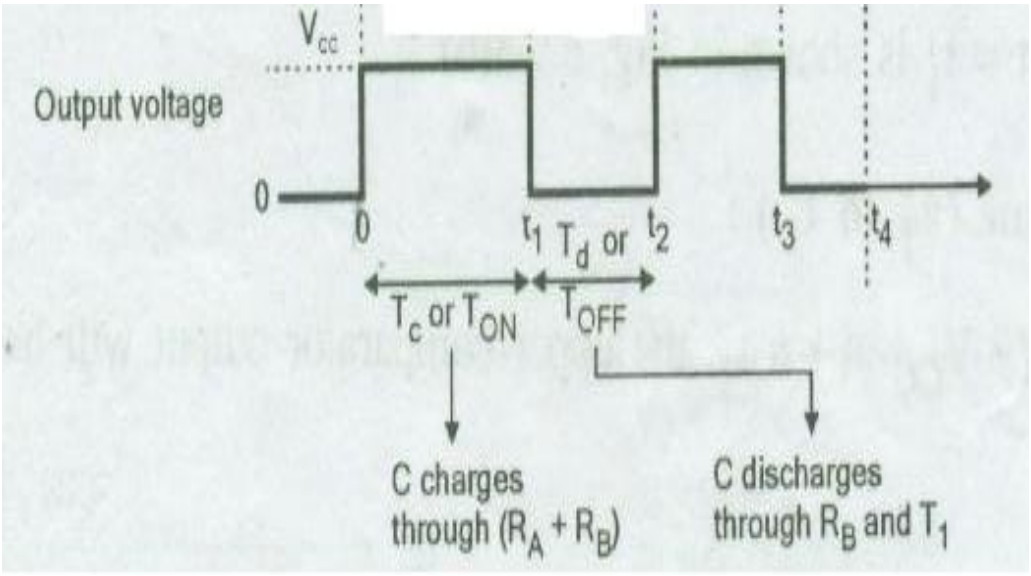
Duty cycle (D) = $R_1 + R_2 \quad / R_1 + 2R_2$

$= (5.8 \times 10^3) + (2.8 \times 10^3) / (5.8 \times 10^3) + 2(2.8 \times 10^3)$

$= 8600/ 11400$

$= 0.75$

Therefore, % D = 75.43% **(1M)**



(1 M)

Q6. Attempt any four of the following: (16 marks)

a) Design and draw Monostable multivibrator using IC555 with Tp= 1 ms.

Ans:- **(Derivation: 2 Marks, Circuit Diagram: 2Marks)**

Given: t_p=1mS

Step1: For a monostable multivibrator:

Pulse width, t_p = 1.1 RC

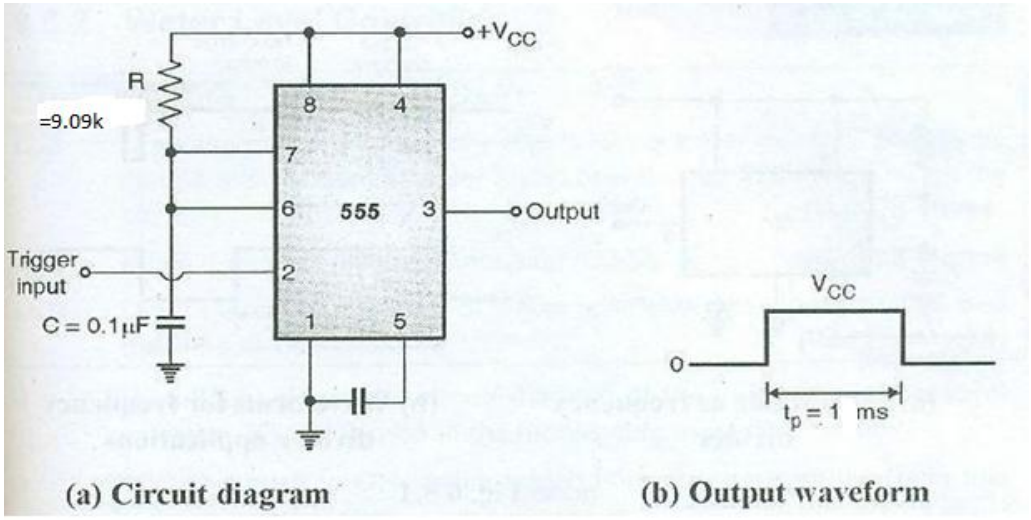
Assume, C= 0.1μF

Therefore,

$1 \times 10^{-3} = 1.1 \times R \times 0.1 \times 10^{-6}$

Therefore,

$R = 1 \times 10^{-3} / 1.1 \times 0.1 \times 10^{-6} = 9090.90\Omega = 9.09k\Omega$



b) Describe with the help of block diagram the operation of multiplier using PLL.

Ans :. **(Diagram- 2Marks, Explanation- 2Marks)**

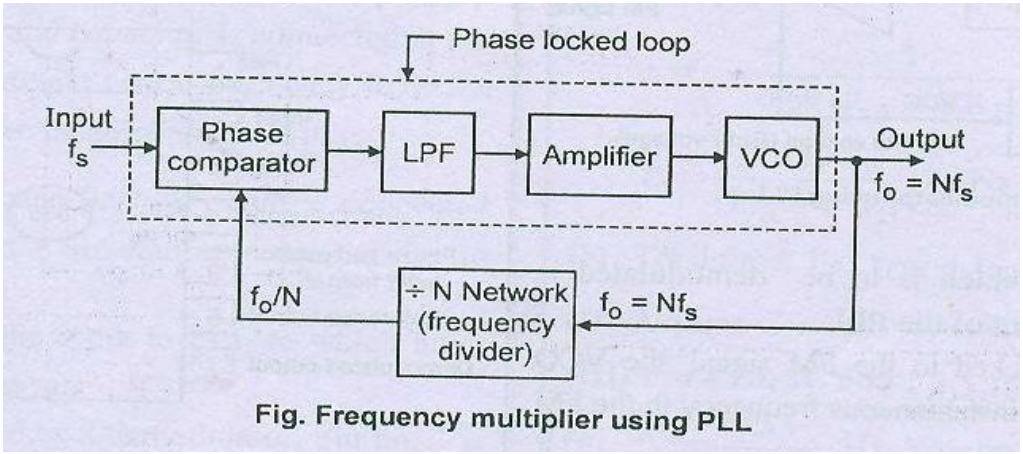


Fig. Frequency multiplier using PLL

Figure shows block diagram of a frequency multiplier using PLL.

A divide by N network is connected externally between the VCO output and phase comparator input. Since the output of the divider network is locked to the input frequency f_S, the VCO actually operates at a frequency which is N times

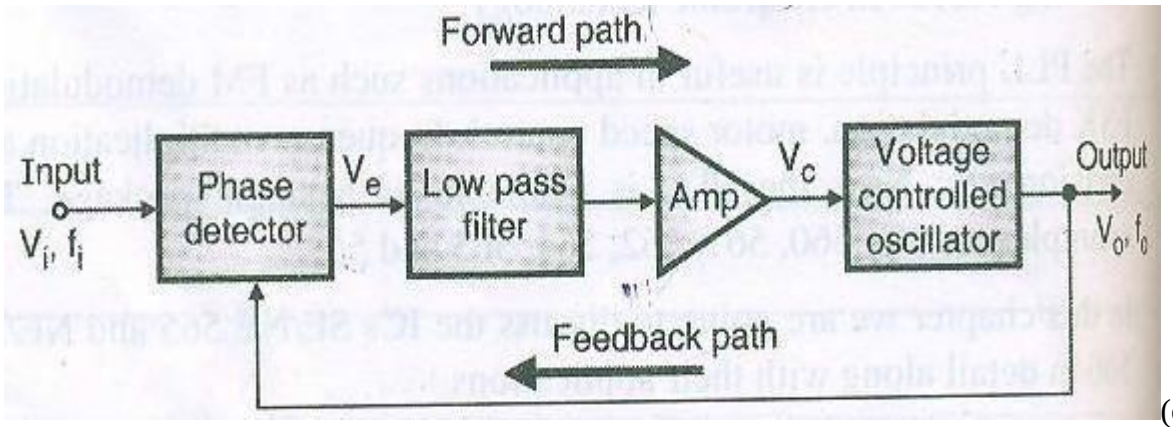
higher than f_S.

Therefore, $f_O = N.f_S$

The multiplying factor can be obtained by proper selection of the scaling factor N.

c) Describe the operation of phase detector and role of VCO in PLL.

Ans**: (2 marks for phase detector and 2 marks for VCO)**



(optional)

Phase detector or phase comparator:

The two points to a phase detector or comparator are the input voltage V_S at frequency F_S and the feedback voltage from a voltage controlled oscillator (VCO) at the frequency F_O . The phase detector compares these two signals and produces a dc voltage V_e which is proportional to the phase difference between F_S and F_O. The output voltage V_e of the phase detector is called as error voltage. This error voltage is then applied to a low pass filter.

Role of Voltage controlled oscillator (VCO):

The control voltage VC is applied at the input of a VCO The output frequency of VCO is directly proportional to the dc control voltage VC. The VCO frequency F_O is compared with the input frequency F_S by the phase detector and it (VCO frequency) is adjusted continuously until it is equal to the input frequency F_S i.e. $F_O=F_S$.

d) Draw and describe WEIN bridge oscillator using op-amp.

Ans**: (Circuit Diagram: 2M; Working: 2M)**

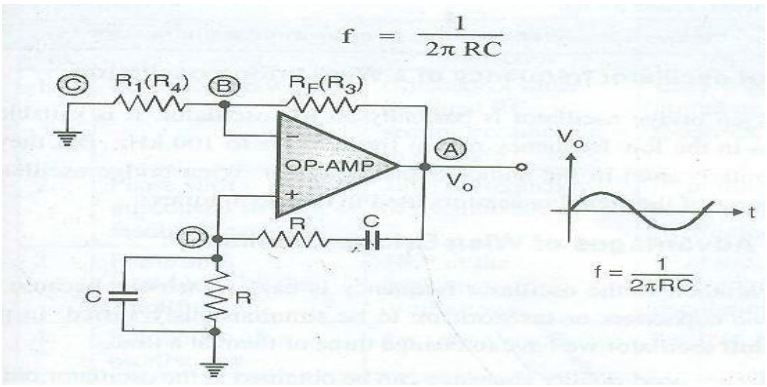


Fig: Wein bridge oscillator using OP-AMP

- The wein bridge oscillator using OP- AMP instead of transistor is as shown in fig.
- The OP- AMP output is applied as an input voltage to the Wein Bridge between points A and C. The output of the Wein Bridge which acts as the feedback network is applied to the OP-AMP input between points D and B.
- The R and C components in the frequency sensitive arms of the bridge will decide the

oscillator frequency. The expression for oscillator frequency is,

- The resistor R3 gets connected in the feedback path of OP- AMP whereas resistor R4 get connected from the inverting (-) terminal to ground. Thus the amplifier configuration is called as the non-inverting amplifier.
- The gain of this configuration is given by: A= 1+ R3 /R4
- We know that at the oscillating frequency the value of feedback factor is β =1/3 and the gain should be A ≥ 3.
- Therefore, (1+ R3 /R4) ≥ 3

Therefore, R3 /R4 ≥ 2

- Thus R3 should be greater than two times the value of R4 to ensure sustained oscillations.
- The oscillator frequency can be varied by varying both the capacitors (C) simultaneously and the amplifier gain can be changed by changing the value of resistor R3.

e) Draw block diagram of VCO using IC-555. Describe how output frequency varies with variation in voltage applied to pin 5 of IC 555.

Ans : **(Circuit Diagram- 2 Marks, Working- 2Marks)**

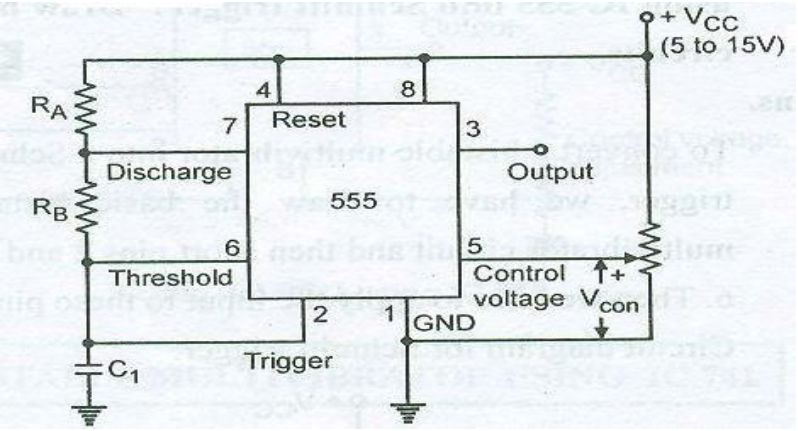


Fig: Circuit diagram of VCO using IC 555

Operation- The value of charging and discharging current is dependent on the control voltage V_C applied at pin number (5) modulating input. This current can also be changed by varying the external timing resistor R_T.The potential difference between pins (5) and (6) I almost zero. That means these pins are equipotential.

Therefore if we increase the modulating voltage V_C at pin number (5), the voltage at pin number (6) will increase with the same amount. This reduces the voltage drop across R_T and reduces the charging current. The voltage across the capacitor is thus triangular wave. This triangular wave is applied to a buffer A1.

The buffer is connected in order to avoid avoiding any possible loading of the capacitor. The buffer output is taken out at pin number (4) as triangular wave output.

The buffer output is also applied to a Schmitt trigger A2, which converts the triangular wave into square waveform. Resistors R_a and R_b is a potential divider generating the reference levels for the upper and lower trigger voltages. This square wave is inverted by inverter A3 and made available at pin number (3).

f) Draw and describe Bistable multivibrator using IC-555

Ans:- **(Ckt Diagram- 2Marks,Working-1Marks,waveforms– 1mks)**

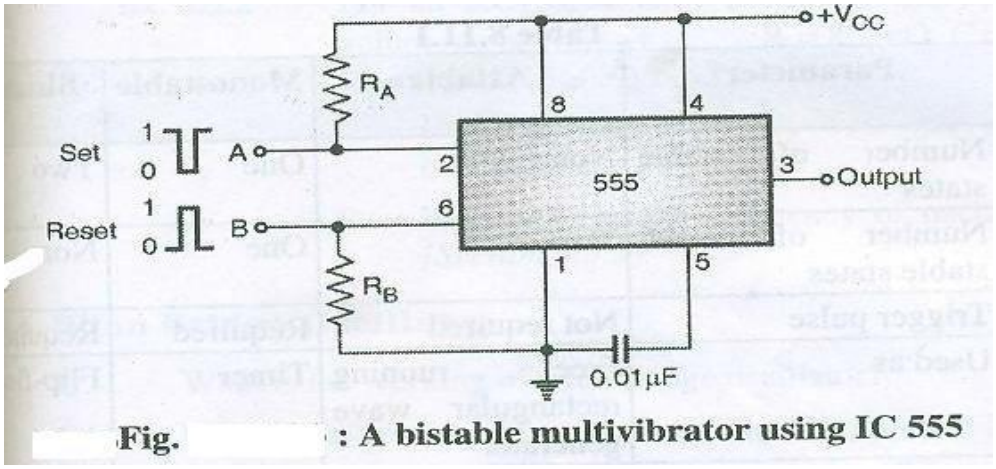
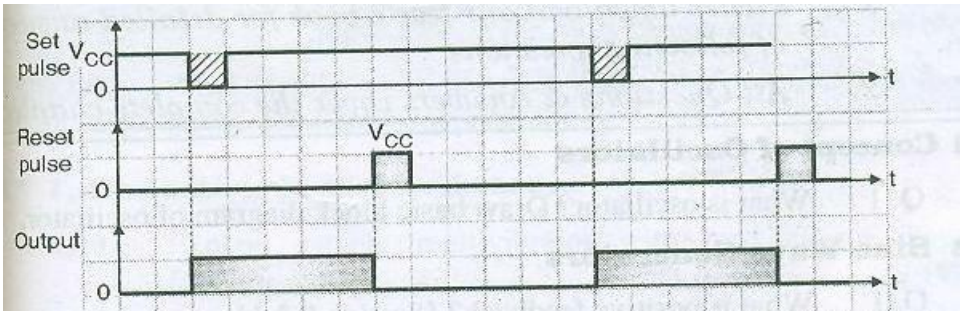


Fig. : A bistable multivibrator using IC 555



Waveforms of the Bistable multivibrator using IC 555

Operation- The IC 555 also provides a direct relay driving capability. In the figure, the negative pulses are applied to the trigger input that sets the flip flop. The output goes high with the positive pulse applied to the threshold resets the flip flop and the output goes low. Thus with the help of trigger, the output is forced to go from one stable state to the other.