SUMMER – 14 EXAMINATION

Model Answer

Subject Code : **17320** Page No: 1/34

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

Marks

1. Attempt any ten of the following **20**

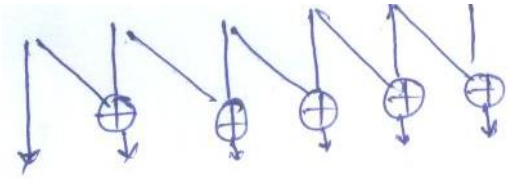
a) Convert given numbers :

i) $(110100)_2 = (\ldots)_{Gray}$ ii) $(1111)_{Gray} = \ldots_B$

i) Ans: correct Ans: 1 Mark each.

Solution :

	MSB					LSB
	B_S	B_4	B_3	B_2	B_1	B_0
Given Binay Number :	1	1	0	1	0	0

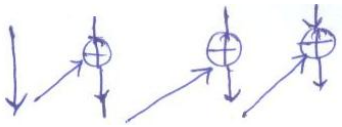


Equivalent Gray Code :	1	0	1	1	1	0
	G_S	G_4	G_3	G_2	G_1	G_0

Ans : $(110100)_2 = (101110)_{Gray}$

ii) Solution :

Given Gray Code :	G_3	G_2	G_1	G_0	
	1	1	1	1	

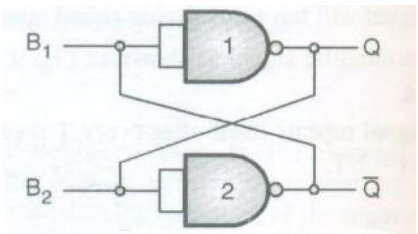


Equivalent Binary Number :	1	0	1	0	

Ans : $(1111)_{Gray} = (1010)_B$

b) Draw the logic circuit diagram of 1 bit memory cell using NAND gate.

Ans : diagram: 2 marks.



c) State the necessity of multiplexers.

Ans : any two points: 2 Marks.

- In most of the electronic systems, the digital data is available on more than one lines. It is necessary to route this data over a single line.
- Under such circumstances we require a circuit which select one of the many inputs at a time.
- This circuit is nothing else but a multiplexer which has many inputs, one output and some select inputs.
- Multiplexer improves the reliability of the digital system because it reduces the number of external wired connections.

d) Differentiate between RAM and ROM (any 2 points).

Ans :Any two points: 2 Marks.

	RAM	**ROM**
1	RAM is Random Access Memory	ROM is Read Only Memory
2	RAM is used for reading and writing purpose,	ROM is used only for reading purpose.
3	RAM is used for Temporary Data Storage	ROM is used for Permanent Data Storage.
4	Types : SRAM, DRAM	Types : PROM, EPROM, EEPROM
5	Applications : Calculators, Computers.	Applications : Computers, Microprocessors.

e) Subtract $(32)_{10}$ from $(85)_{10}$ using 2's complement binary arithmetic.

Ans :

Solution :

$(32)_{10} = (00100000)_2$ ……1/2 mark

$(85)_{10} = (01010101)_2$ ……1/2 mark

$(32)_{10} - (85)_{10} = (32)_{10} + (-85)_{10}$

2's complement of $(85)_{10}$

Now,

2's complement of $(85)_{10}$ = is complement of $(85)_{10}+1$

1's complement of $(85)_{10} = (01010101)_2 = (10101010)_2$

2's complement = 10101010+1 = 10101011 ……. 1/2 Mark

Therefore, $(32)_{10}$ = 0 0 1 0 0 0 0 0

$+ (-85)_{10}$ = + 1 0 1 0 1 0 1 1

1 1 0 00 1 0 1 1

↑

No carry

Therefore, there is no carry it indicates that result is negative and in 2's complement form.

Therefore, 2's complement of (11001011) is

1's complement + 1

= 00110100 + 1

= $(110101)_2$

$(53)_{10}$

Ans : $(32)_{10}$ - $(85)_{10}$ = $(-53)_{10}$ …….1/2 mark

f) Give two applications of A/D converter.

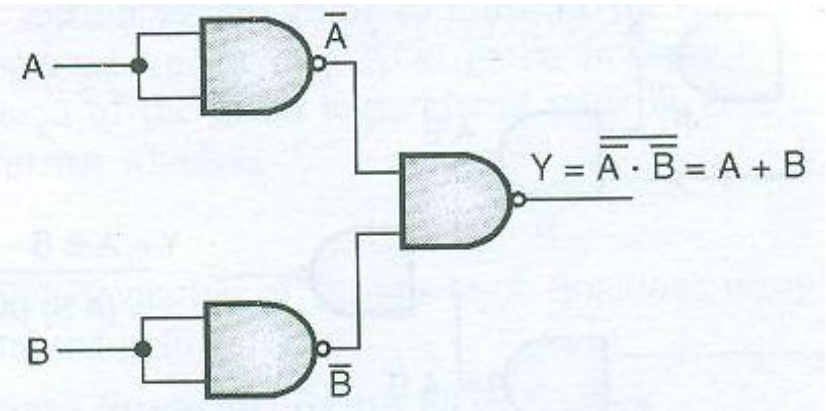
Ans : any two applications: 2 Marks

1. In the digital instruments such as digital voltmeter, frequency counter etc.
2. In the data acquisition system.
3. In the digital tachometers for speed measurement and feedback.
4. In digital recording and reproduction.
5. In computerized instrumentation systems.
6. NC and CNC machines.

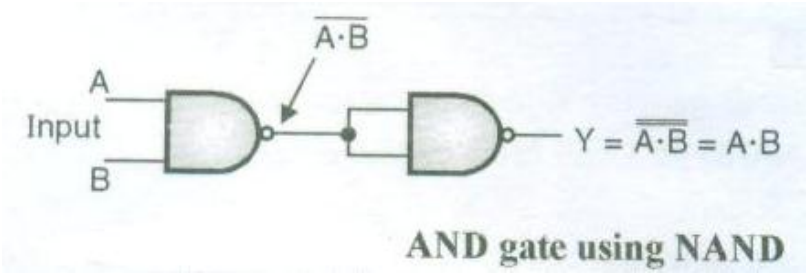
g) Draw OR and AND gate using NAND gate only.

Ans : 1 mark each

OR gate using NAND

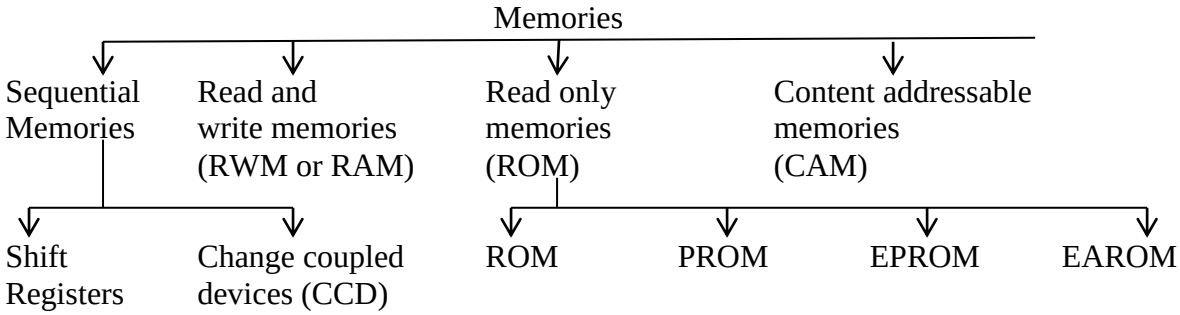


AND gate using NAND



h) Classify memories on the basis of principle of operation :

Ans : 2 marks



i) Write truth table and the expressions of half subtractor

Ans : truth table : 1 Mark, Expression : 1 Mark

Truth Table for half subtractor

Inputs		**Outputs**	
A	**B**	**Difference D**	**Borrow**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$\text{Difference (D)} = A \oplus B$

$\text{Borrow} = \bar{A}B$

j) Perform $(52)_{10}$ - $(89)_{10}$ using 9's and 10's complement method.

Ans : 1 Mark each

Using 9's complement method :

Solution :

Step 1 : Obtain 9's complement of $(89)_{10}$

9's complement of $(89)_{10}$ = 99 – 89 = 10

Step 2 : Add $(52)_{10}$ and 9's complement of $(89)_{10}$:

```
   0 1 0 1  0 0 1 0    (52)10 in BCD
+
   0 0 0 1  0 0 0 0    9's complement of (89)10
        1                        Carry
 0  0 1 1 0  0 0 1 0    Result
```

Final carry = 0. So the result is negative and in 9's complement form .

Step 3: Take the 9's complement of the result :

```
   1 0 0 1   1 0 0 1   (99)10 in BCD
-
   0 1 1 0   0 0 1 0   Result from step 2
   1 1       1 1 __    Borrow
   0 0 1 1   0 1 1 1   Final answer

     3         7
```

Therefore, $(52)_{10}$ - $(89)_{10}$ = - $(37)_{10}$

OR

Using 9's complement method :

Solution :

$(52)_{10}$ - $(89)_{10}$ = $(52)_{10}$ + $(-89)_{10}$

9's complement of $(9)_{10}$

9's complement of $(89)_{10}$ = 99 – 89 = 10

Therefore, $(52)_{10}$ = $(52)_{10}$

\+ $(89)_{10}$ = $+ (10)_{10}$

□ (62)

Carry = 0

Therefore, Carry = 0

Result is negative & in 9's complement from (99) – (62) = $(37)_{10}$

= $(-37)_{10}$

ii) Using 10's complement method :

Step 1 : Obtain 10's complement of $(89)_{10}$

9's complement of $(89)_{10}$ = [99 – 89]+1 = 11

Step 2 : Add $(52)_{10}$ and 9's complement of $(89)_{10}$:

0 1 0 1 0 0 1 0 $(52)_{10}$ in BCD

\+

0 0 0 1 0 0 0 1 10's complement of $(89)_{10}$

1 Carry

0 | 0 1 1 0 0 0 1 1 Result

→ Final carry = 0. So the result is negative and in 10's complement form .

Step 3: Take the 10's complement of the result :

1 0 0 1 1 0 0 1 $(99)_{10}$ in BCD

\-

0 1 1 0 0 0 1 1 Result from step 2

1 1 1 1 Borrow

0 0 1 1 0 1 1 0

\+ 1

0 0 1 1 0 1 1 1

3 7

Therefore, $(52)_{10}$ - $(89)_{10}$ = - $(37)_{10}$

OR

$(52)_{10}$ - $(89)_{10}$ = $(52)_{10}$ + (- $89)_{10}$

↑

10's complement of $(89)_{10}$

10's complement of $(89)_{10}$ = 9's complement of $(89)_{10}$

$[(99)_{10} - (89)_{10}]$ + 1

= 10 + 1 = $(11)_{10}$

Therefore, $(52)_{10}$ = $(52)_{10}$

\+ $(-89)_{10}$ = + $(11)_{10}$

$(63)_{10}$

↑

Carry = 0

Therefore, Carry = 0

Result is negative & in 10's complement from [(99) – (63)]+1 = $(36)_{10}$+1= $(37)_{10}$

$(-37)_{10}$

K) Draw the truth table of following IC's
i) IC – 7432 ii) IC - 7486
Ans : 1 Mark each

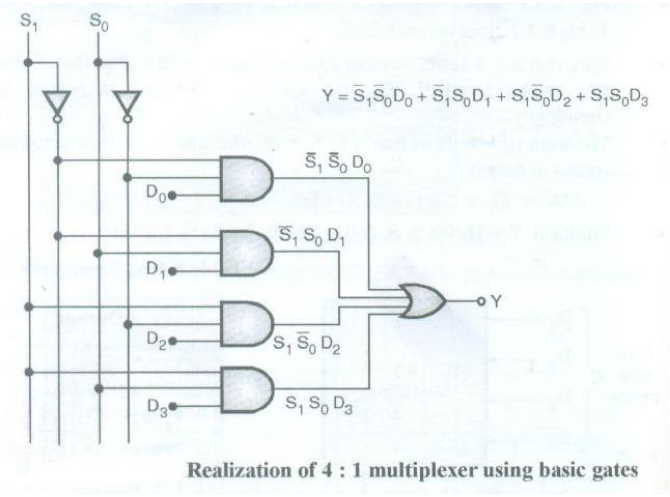
i) Truth Table of IC 7432

Input		Output
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

ii) Truth Table of IC 7486

Input		Output
A	B	Y = A⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

l) Draw circuit diagram of 4 : 1 multiplexer
Ans : diagram: 2 marks



Realization of 4 : 1 multiplexer using basic gates

m) Give various methods of D/A converter.

Ans : **1 mark each**

Various methods of D/A converter

i. Binary Weighted register DAC
ii. R-2R Ladder type DAC

n) State the applications of Flip-Flops.

Ans : **any two applications: 2 Marks**

Applications of Flip-Flops are :

1. Elimination of keyboard debounce.
2. As a memory element
3. In various types of registers
4. In counters / timers
5. As a delay element.

2. Attempt any four of the following : 16

a) Perform the following operations :

i) $(11100)_2$ / $(100)_2$ ii) $(1010.11)_2$ x $(11)_2$

Ans : 2 marks each

i) $(11100)_2$ / $(100)_2$

```
      111
100) 11100
     - 100
      0110
     - 100
        0100
      - 100
         000
```

Therefore, Quotient = $(111)_2 = (7)_{10}$

Remainder = $(000)_2 = (0)_{10}$

ii) $(1010.11)_2$ x $(11)_2$

```
      1 0 1 0 . 1 1
    X           1 1
    -----------------
      1 0 1 0 1 1
    1 0 1 0 1 1 -
    1 1 1 1 1
    -----------------
  1 0 0 0 0 0 . 0 1
```

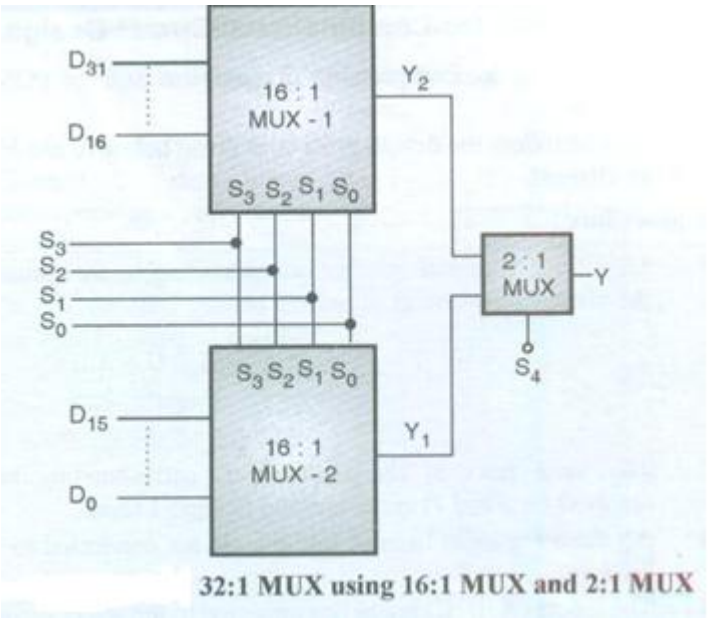
Therefore

Ans : $(1010.11)_2$ x $(11)_2$ = (100000.01)

b) Design 32 : 1 multiplexer using 16 : 1 multiplexer and 2 : 1 multiplexer.

Ans : Diagram : 4 marks.

Solution :

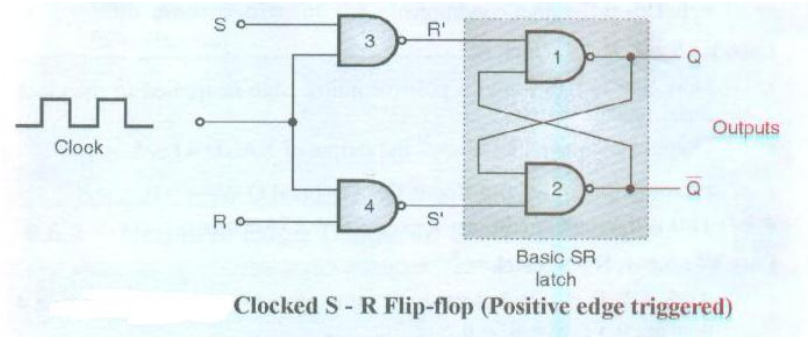


32:1 MUX using 16:1 MUX and 2:1 MUX

c) Draw the circuit diagram of S-R Flip Flop using NAND gate and describe its working.

Ans : Circuit diagram : 2 marks, explanation : 2 marks. (note : weightage is to be given for any clocked S-R flip flop)

Figure shows the positive edge triggered S-R flip-flop. It is also called as clocked SR FF



Clocked S - R Flip-flop (Positive edge triggered)

- This circuit will operate as an SR flip-flop only for the positive clock edge but there is no change in output if clock = 0 or even for the negative going clock edge.

Operation :

Case I : S = X, R = X, clock = 0

- Since clock = 0, the outputs of NAND gates 3 and 4 will be forced to be 1 irrespective of the values of S and R. That means R'= R' = 1. These are the inputs of the SR latch.

- Hence the outputs of basic SR/F/F i.e. Q and Q will not change. Thus if clock = 0, then there is no change in the output of the clocked SR flip-flop.

Case II : S = X, R=X, clock = 1 (High level)

- As this flip flop does respond not respond to levels applied at the clock input, the outputs Q and Q will not change. So, $Q_{n+1} = Q_{n+1} = Q_n$

Case III : S = R = 0 : No change

- If S=R=0 then outputs of NAND gate 3 and 4 are forced to become 1.
- Hence R'and S'both will be equal to 1. Since S' and R' are the inputs of the basic S – R flip-flop using NAND gates. There will be no change in the state of outputs.

Case IV : S =1, R = 0, clock = ↑

- Now S=0, R=1 and a positive going edge is applied to the clock input.
- Output of NAND 3 ie. R' = 0 and output of NAND 4 i.e. S' = 1.
- Hence output of SR flip-flop is Q_{n+1} = and Q W_{n+1} = 0.
- This is the reset condition.

Case V : S =1, R = 0, clock = ↑

- Now S=0, R=1 and a positive edge is applied to the clock input.
- Since S=0, output of NAND – 3 i.e. R´= 1. And as R = 1 and clock = 1 the output of NAND-4 i.e. S´ = 0. Hence $Qn + 1 = 0\ and\ Qn = 1 = 1$. This is the reset condition.

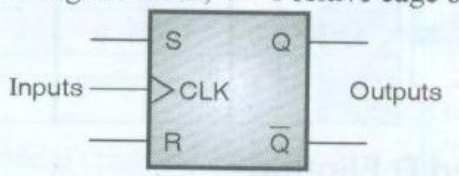
Case VI : S =1, R = 1, clock = ↑

- As S=1, R=1 and clock = 1, the outputs of NAND gates 3 and 4 both are 0 i.e. S' = R' =0.
- Hence the "Race" condition will occur in the basic SR flip-flop.
- The symbol of positive edge triggered SR flip flop is as shown in figure and the truth table is also shown in figure.

Truth table of a positive edge triggered SR flip flop

Inputs			Outputs		Remark
CLK	S	R	Q_{n+1}	$\bar{Q}_{n+1}$	
0	×	×	Q_n	$\bar{Q}_n$	No change (NC)
1	×	×	Q_n	$\bar{Q}_n$	No change (NC)
↓	×	×	Q_n	$\bar{Q}_n$	No change (NC)
↑	0	0	Q_n	$\bar{Q}_n$	No change (NC)
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	Race	Race	Avoid

↓ = Negative edge of clock, ↑ = Positive edge of clock



Symbol of positive

- Note that for clock input to be at negative or positive levels as the edge triggered flip flop does not respond. Similarly it does not respond to the negative edge of the clock.
- The flip-flop will respond only to the positive edge of clock.
- With positive edge of the clock, the SR flip flop behaves in the following way :

$S = R = 0 \rightarrow$ No change in output

$S = 0, R = 1 \rightarrow Q_{n+1} = 0, \bar{Q}_{n+1} = 1$ Reset condition

$S = 1, R = 0 \rightarrow Q_{n+1} = 1, \bar{Q}_{n+1} = 0$ Set condition

$S = R = 1 \rightarrow$ Race condition.

d) Simplify the following expression using Boolean laws.

i) y = (A+B) (A+C) **ii) y = ABC + $A\bar{B}C$ + $AB\bar{C}$**

Ans : 2 marks each

i) y = (A+B) (A+C)

= A.A + A.C + A.B + B.C

= A + AC + AB + BC

= A (1+C+B) + BC

= A + BC

ii) $y = ABC + A\bar{B}C + AB\bar{C}$

$= AC(B + \bar{B}) + AB\bar{C}$

$= AC(1) + AB\bar{C}$

$= AC + AB\bar{C}$

$= A(C + B\bar{C})$

$= A\left[(C+B) \cdot (C+\bar{C})\right]$

$= A\left[(C+B) \cdot 1\right]$

$Y = A(C+B)$

e) How many bits are required for a resolution of 5 mV and full scale voltage in 15V ?

Ans :

Solution :

Given : $V_{FS} = 15$ V

Resolution = 5mV

N = ?

Resolution $= V_{FS} / 2^n - 1$ …..(1 mark)

Therefore $5 \times 10^{-3} = 15 / 2^n - 1$ …..(1 mark)

Therefore $2^n = 1 + 15 / 5 \times 10^{-3}$

$= 1 + 3000$

$2^n = 3001$ …..(1 mark)

Therefore $n = 10g_2\ 3001$

$= 10g_{10}\ 3001 / 10g_{10}\ 2 \approx 12$ bits

Ans : No. of bits = 12 …..(1 mark)

f) Identify the following circuit as combinational circuit or sequential circuit.

i) 3 – bit ring counter **ii) Full adder**

iii) Clocked J-K F/F **iv) 4 : 1 MUX**

Ans : 1 mark each.

i) 3 – bit ring counter => Sequential Circuit

ii) Full adder => Combinational Circuit

iii) Clocked J-K F/F => Sequential Circuit

iv) 4 : 1 MUX => Combinational Circuit

3. Attempt any four of the following: **16**

a) State and prove De-Morgan's 1st and 2nd theorem.

Ans : 2 Marks each theorem

i) $\overline{AB} = \overline{A} + \overline{B}$

It states that compliment of product is equal to sum of their compliments.

1	2	3	4	5	6
A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Column 03 = column 06

i.e. $\overline{AB} = \overline{A} + \overline{B}$

Hence proved

ii) $\overline{A+B} = \overline{A} \cdot \overline{B}$

It states that complement of sum is equal to product of their complements.

1	2	3	4	5	6
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

Column 03 = column 06

$\therefore \overline{A+B} = \overline{A} \cdot \overline{B}$

Hence proved.

b). Describe the operation of single digit BCD adder using IC-7483 with circuit diagram.
Ans : 2Marks diagram, 2Marks explanation

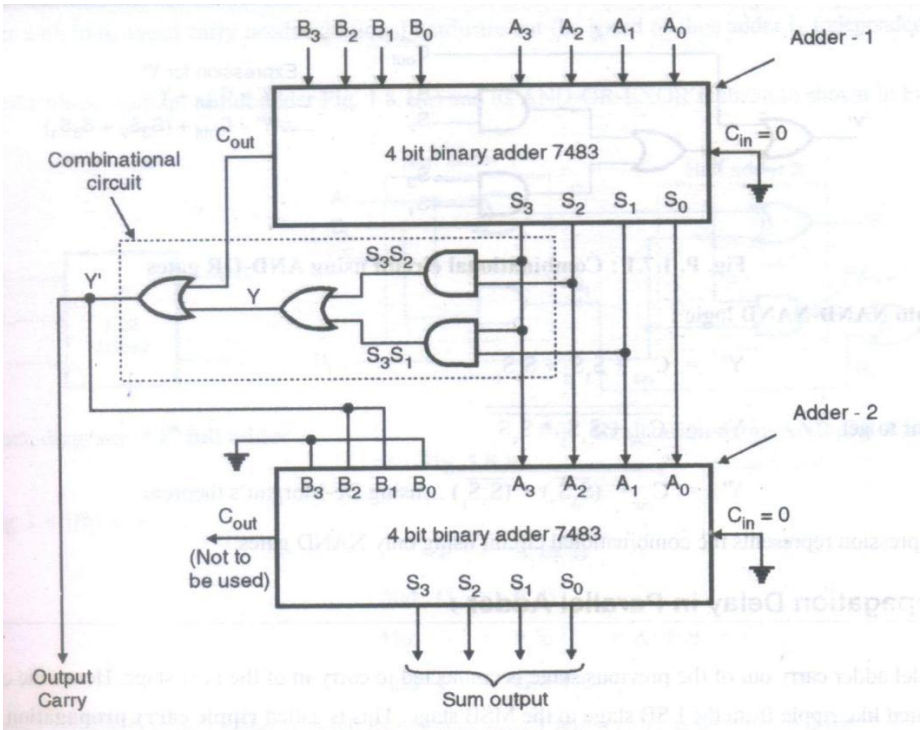


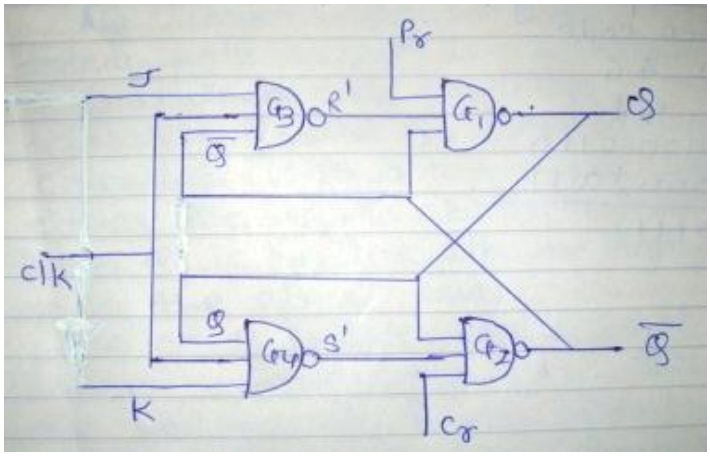
Fig. 1.7.3 : 4-bit BCD adder

- A BCD adder adds two BCD digits and produces a BCD digit.
- The two given BCD numbers are to be added using the rules of binary addition.
- If sum is less than or equal to 9 and carry=0 then no correction is necessary.The sum is correct and in the true BCD form.
- But if sum is invalid BCD or carry=1 then the result is wrong and needs correction.
- The wrong result can be corrected by adding six(0110) to it.

c) State the working principle of J-K Flipflop with neat diagram.
Ans : 1 Mark diagram, 1Mark truthtable, 2Mark explanation, Working of JK FF.

Truth Table

CLK	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q}n$



The clock signal is applied to CK input. NAND gates G1 and G2 form an SR latch. The other two NAND gates G3 and G4 have three inputs which are J, Q and CK and K, Q and CK respectively.
IF CK =0 than F/F is disabled and O/P Q and $\overline{Q}$ do not change
If CK= 1 and J=K=O then as S'=R'=1 the output Q and $\overline{Q}$ will not change their state.
If J=0 and K= 1 then JK flip flop will reset and Q= 0 & $\overline{Q}$=1
If J=1 and K=0 then output will be set and Q=1 & $\overline{Q}$=0
If J= K=1 then Q & $\overline{Q}$ outputs are inverted and FF will toggle

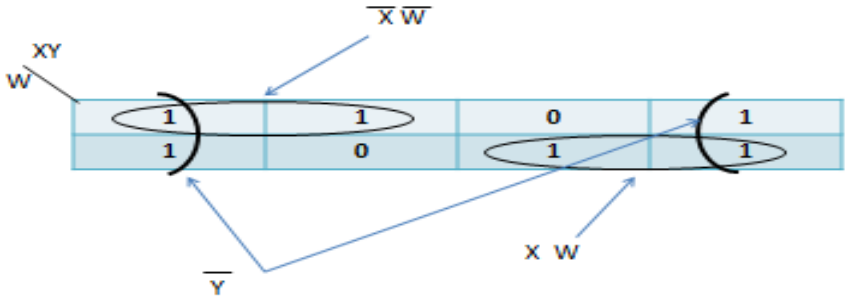
d) Minimize the following expression using K-map.

i) F (w,x,y) = ∑ m(0,1,2,4,6,7)

ii) f(A,B,C,D) =∏ M(0,2,7,8,9,10,13)

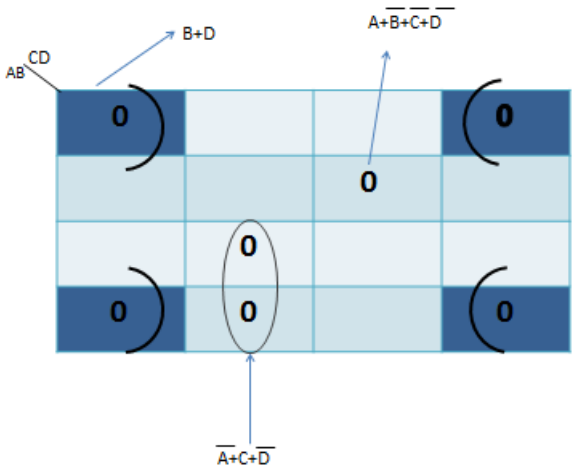
Ans : 2 Marks –each expression

i)



$$f(w,x,y)=\overline{X}\,\overline{W}+X\,W+\overline{Y}$$

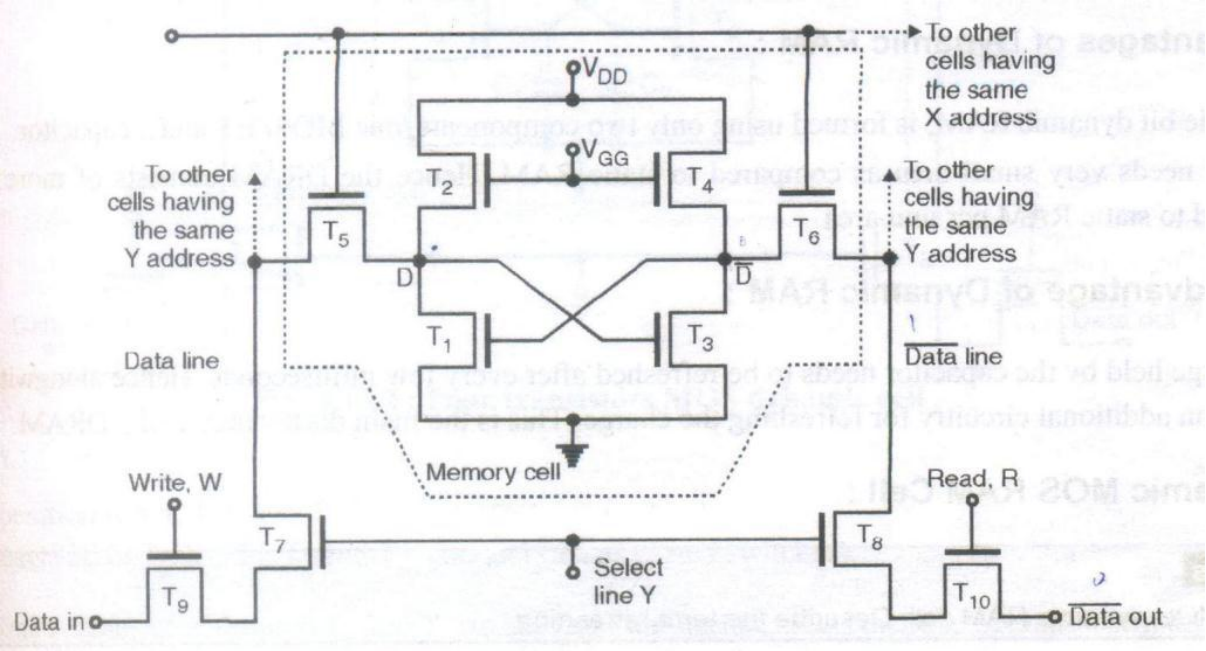
ii)



$$f(A,B,C,D)=(B+D).(\overline{A}+C+\overline{D}).(A+\overline{B}+\overline{C}+\overline{D})$$

e) Describe with circuit diagram the working operation of static RAM cell.
Ans : 2 Marks diagram, 2 Marks working

Static RAM cell with NMOS CELL



T2 & T4 are acting as resistances. X & Y lines are used for addressing cell.
When X=Y=1 (high) ,the cell is selected . When X=1, the MOSFETS T5 & T6 are turned ON .,which will connect memory cell to the data line and data bar line.
When Y=1 ,the MOSFETS T 7 & T8 are turned ON .,which will make read & write operation possible
f) Study the given circuit as shown in fig no.1 intial o/p condition is QA QB QC = 010, write truth table of output $Q_AQ_BQ_C$

4. Attempt any four of the following: 16

a) Encode the following decimal number in BCD code and excess-3 code.
Ans : 1 Mark for each conversion.

i) $(48)_{10}$
$(48)_{10}$

BCD code:
0100 1000

Excess-3 code:
0100 1000
+0011 0011
$(0111\ 1011)_{\text{excess-3 code}}$

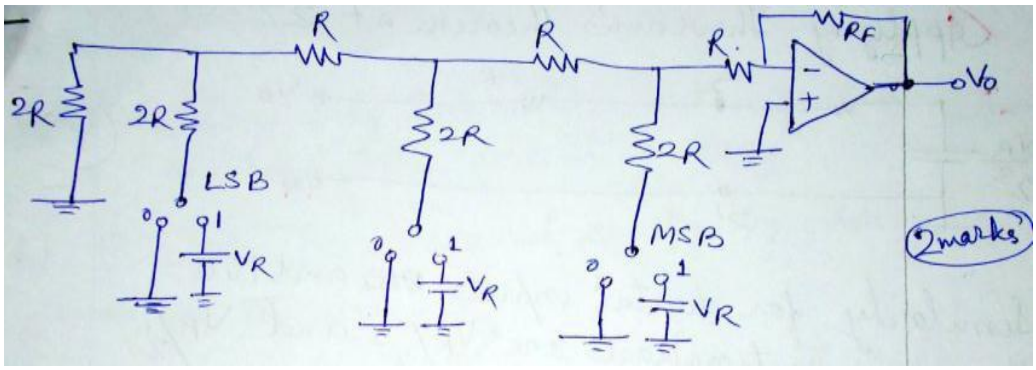
ii) $(228)_{10}$

BCD code:
0010 0010 1000

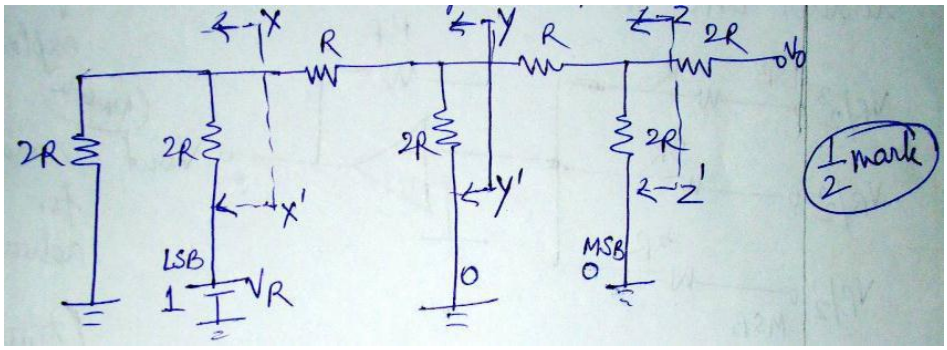
Excess-3 code:
0010 0010 1000
+0011 0011 0011
$(0101\ 0101\ 1011)_{\text{excess-3 code}}$

b) Describe R-2R ladder network method of D/A conversion with neat circuit diagram.
Ans : Circuit diagram : 2 marks, description: 2 marks.

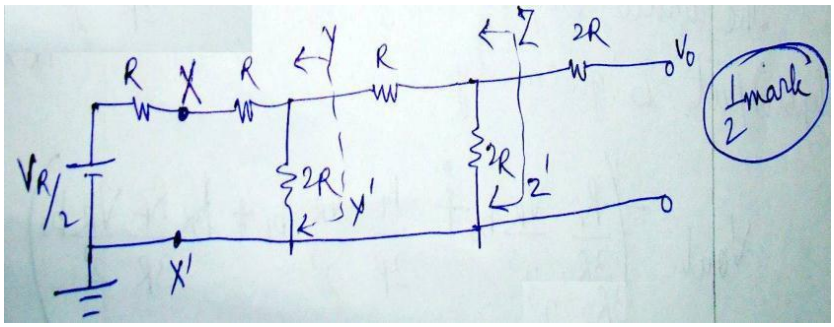
R -2R ladder DAC uses two resistors R & 2R. The input is applied through digitally controlled switches.



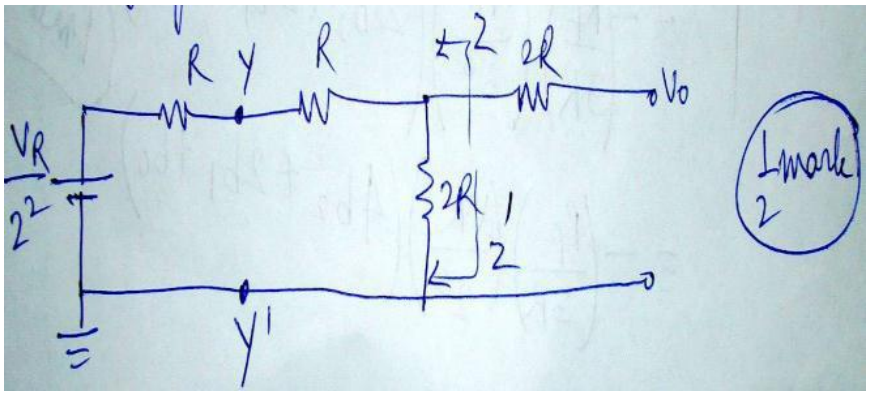
For example if the digital input is 001



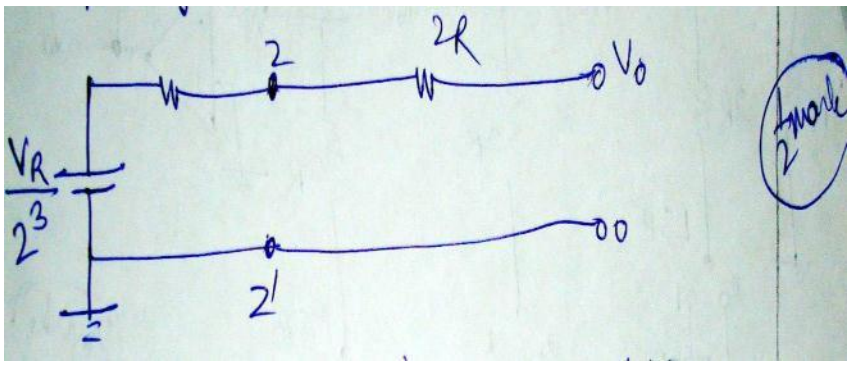
Applying Thevenins theorem at XX´



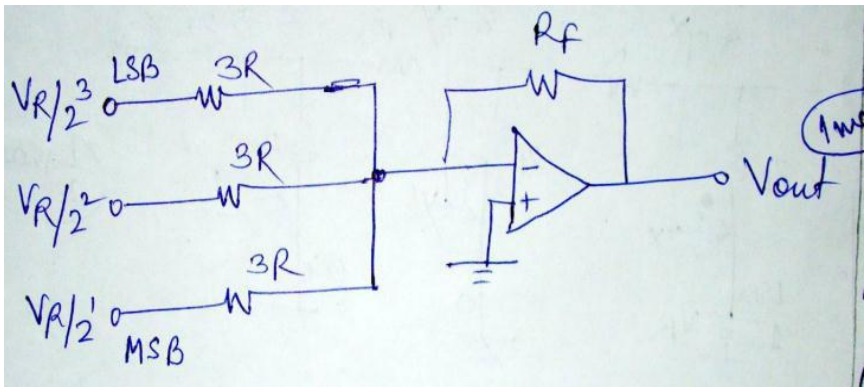
Applying Thevenins theorem at yy′



Applying Thevenins theorem at zz′



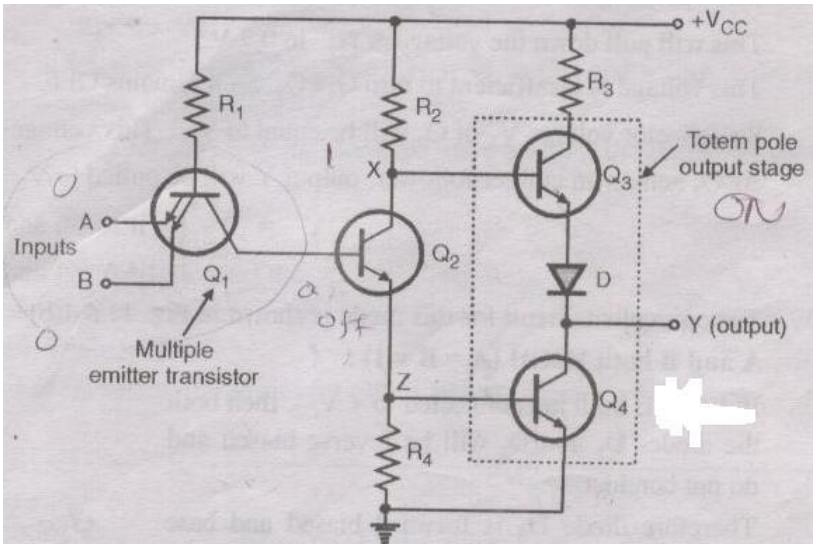
Similarly for digital input 010 and 100 the equivalent voltages are $V_R/2^2$ And $V_R/2^1$ respectively. The equivalent resistance is 3R in each case.
So the simplified circuit of 3bit R-2R ladder DAC is



The analog output voltage for a given digital input is given by **(1/2m)**

Vout = - (RF/3R VR x b0/2^3 + RF/3R VR x b1/2^2 + RF/3R VR x b2/2^1)
= - (RF/3R) (VR/2^3) (2^2b2 + 2^1b1 + 2^0 b0)
= - (RF/3R) (VR/2^3) (4b2 + 2b1 + b0)

c) Explain the operation of TTL logic using NAND gate.
Ans : diagram: 2 marks, operation : 2 marks.



Input		Output
A	B	$Y=\overline{A.B}$
0	0	1
1	0	1
0	1	1
1	1	0

Operating Principle:

1. A and B both LOW (A = B =0):

- If A and B both are connected to ground, then both the B- E junctions of transistors Q1 are forward biased.
- Hence diodes D1 and D2 will conduct to force the voltage at point C to 0.7 V.
- This voltage is insufficient to forward bias base emitter junction of Q2. Hence **Q2 will remain OFF.**
- Therefore its collector voltage Vx rises to Vcc.
- As transistor Q3 is operating in the emitter follower mode, output Y will be pulled up to high voltage.

Therefore, Y =1 (HIGH) …..
For A =B= 0 (LOW)

2. Either A or B LOW (A =0, B=1 or A=1, B=0):

- If any one input (A or B) is connected to ground with the other terminal left open or connected to +Vcc, then the corresponding diode (D1 & D2) will conduct.
- This will pull down the voltage at "C" to 0.7 V.
- This voltage is insufficient to turn ON **Q2. So it remains OFF.**
- So collector voltage Vx of Q2 will be equal to Vcc. This voltage acts as base voltage for Q3.
- As Q3 acts as an emitter follower, output Y will be pulled to Vcc.
- **Y= 1 ---- if A=0 and B=1**
- **-----if A=1 and B=0**

3. A and B both HIGH (A=B=1):-

- If A and B both are connected to +Vcc, then both the diodes D1 & D2 will be reverse biased and do not conduct.
- Therefore diode D3 is forward biased and base current is supplied to transistor Q2 via R1 and D3.
- As Q2 conducts, the voltage at X will drop down and **Q3 will be OFF,** whereas voltage at Z (across R3) will increase **to turn ON Q4.**
- As Q4 goes into saturation, the output voltage Y will be pulled down to a low voltage, **Y=0.**

d) Design a full subtractor circuit using K-map with truth tables.

Ans : 1Mark truth table, 1Mark map, 2Marks diagram

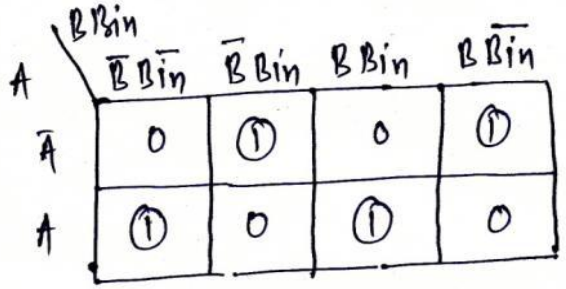
No of Inputs = 3 (A,B, Bin)

No. of Outputs=2 (D and Bout)

Truth Table

Input			Output	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-map simplification for Difference Output (D)



$$D = \bar{A}\,\bar{B}\,B_{in} + \bar{A}\,B\,\bar{B}_{in} + A\,\bar{B}\,\bar{B}_{in} + ABB_{in}$$

$$= B_{in}\,(\bar{A}\,\bar{B} + AB) + \bar{B}_{in}\,(\bar{A}B + A\,\bar{B})$$

$$= B_{in}\,\overline{(A \oplus B)} + \bar{B}_{in}\,(A \oplus B)$$

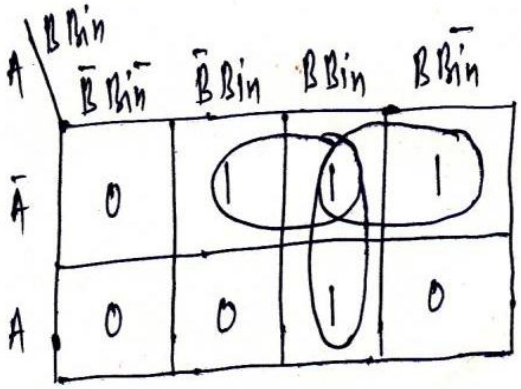
Put $A \oplus B = x$

$$D = B_{in}\,\bar{x} + \bar{B}_{in}\,x$$

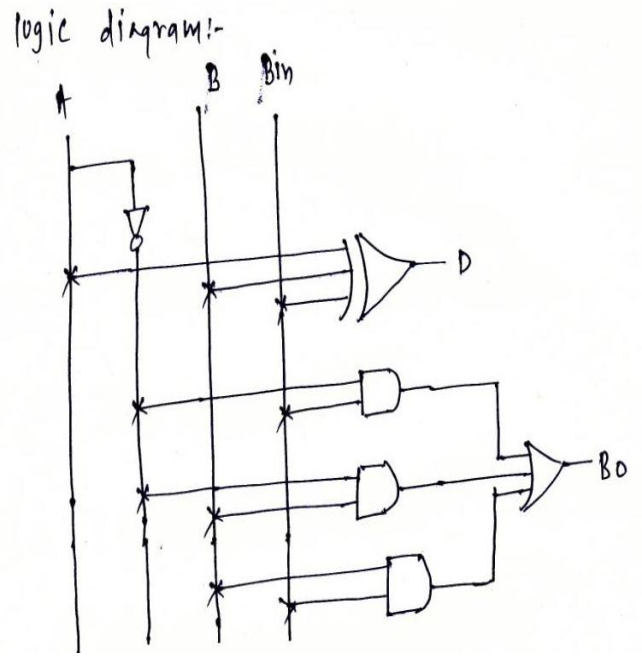
$$D = B_{in} \oplus x$$

$$D = A \oplus B \oplus B_{in}$$

K-map simplification for Borrow (Bo



$B_0 = \bar{A}B_{in} + \bar{A}B + BB_{in}$



e) For 3 bit synchronous up-counter.

1) Draw circuit diagram (use T-Flip Flop)

2) Write truth table.

Ans : 2 Marks circuit diagram, 2 Marks truth table

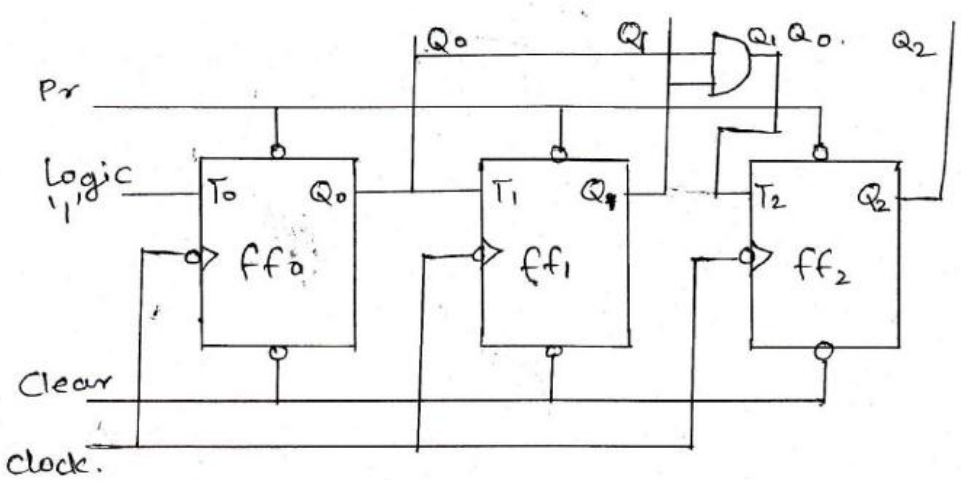
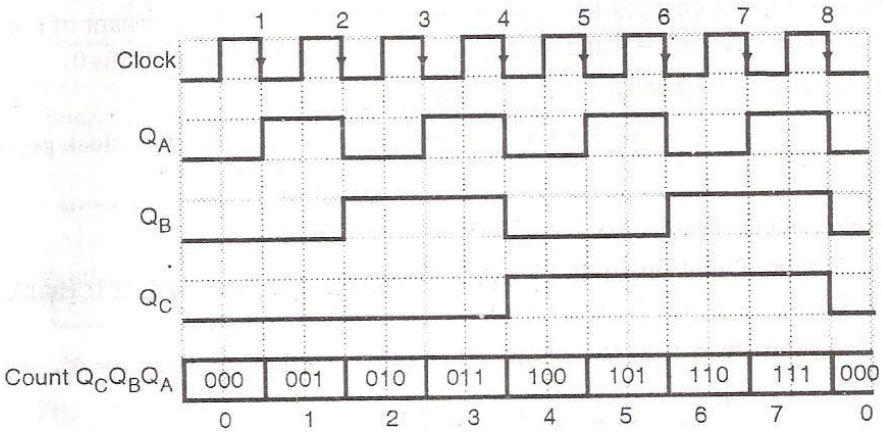


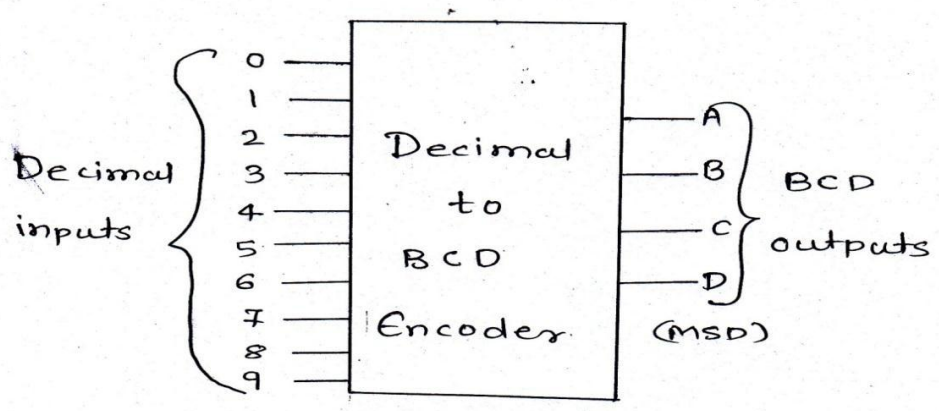
Fig: bit synchronous counter

Fig: Truth Table and waveforms

Clock	Q_C	Q_B	Q_A
0	0	0	0
1st (↓)	0	0	1
2nd (↓)	0	1	0
3rd (↓)	0	1	1
4th (↓)	1	0	0
5th (↓)	1	0	1
6th (↓)	1	1	0
7th (↓)	1	1	1



f) Draw block diagram of decimal to BCD encoder with its truth table.
Ans : Block Diagram:2 marks, Truth table: 2 marks.
Marks can be given for active low input and active low output truth table also



One of the most commonly used input device for a digital system is a set of ten switches, one for each numeral between 0 to 9. These switches generate 1 or 0 logic levels in response to turning them OFF or ON. When a particular number is to be fed tothe digital circuit in BCD code the switch corresponding to that number is pressed. The block diagram is as shown above and truth table for active high input and active high output is as shown below

Active High Input										Active high Output			
0	1	2	3	4	5	6	7	8	9	D	C	B	A
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1

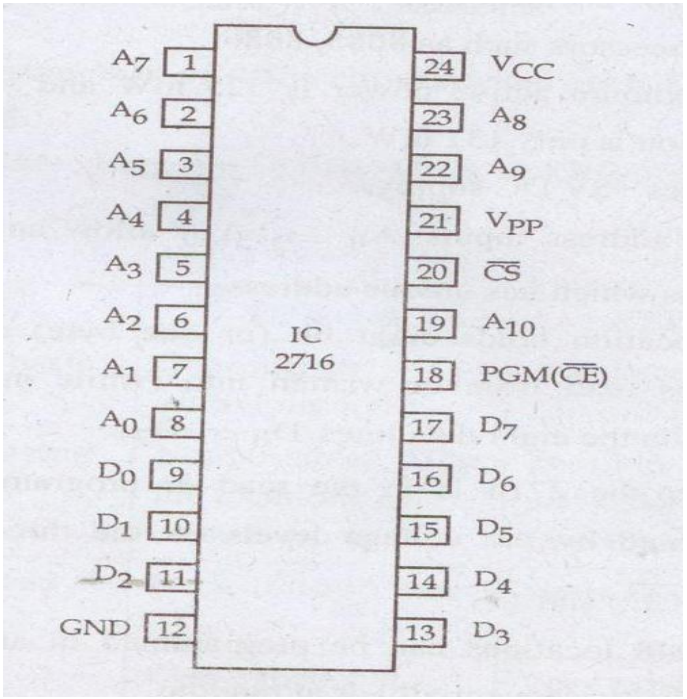
Q 5. Attempt any four of the following: **16**

a) Compare combinational and sequential logic circuits (any four points).

Ans:- (Any 4 points: 4 marks)

Sr no	**Combinational ckt**	**Sequential ckt**
1	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
2	No memory element required in the circuit.	Memory element required to store bit
3	Clock not necessary	Clock is necessary
4	E.g. Adders, Subtractors ,Code converters , comparators etc.	E.g. Flip flop, Shift registers, counters etc,
5	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

b) Draw pin out diag. of 2716 EPROM and state its operation.
Ans:- (Pin Diagram: 2 marks, operation: 2 marks)



Operation:-

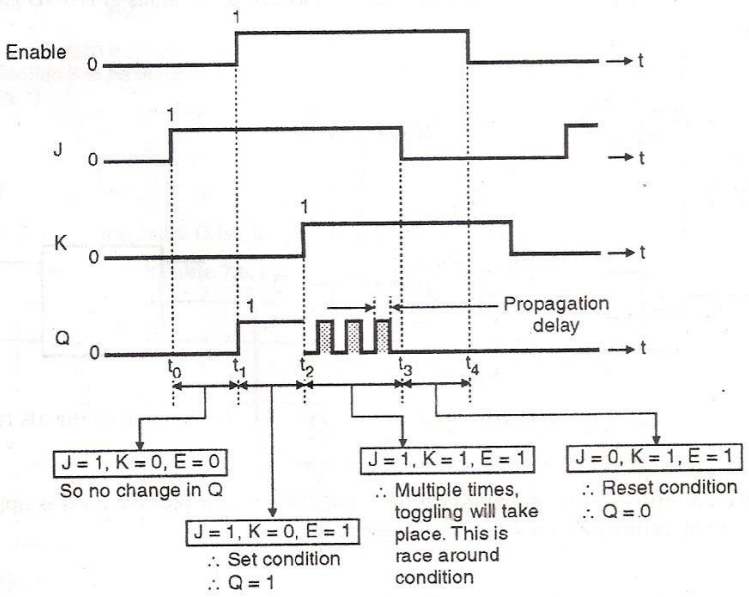
2716 has 3 modes of operation

1. Read mode :-
   a. Read operation requires $\overline{G}=V_{IL}$, $\overline{EP}=V_{IL}$ and address is stabilized
   b. Valid data will appear on the output pins after time t_{AVQV} or t_{ELQV}
2. Deselect Mode
   a. 2716 is deselected by $\overline{G}=V_{IH}$. This is independent of $\overline{EP}$ and condition of addresses
   b. Outputs of high impedance (Hi-Z) when $\overline{G}=V_{IH}$. This allows tied-OR of two or more IC's
3. Stand-by Mode (Power Down)
   a. 2716 is powered down by $\overline{EP}=V_{IH}$.
   b. Independent of $\overline{G}$ automatically puts the output in Hi-Z state. Power is reduced by 25% of normal operating power.

IC 2716 IS A 2084X 8 memory,so 4 ICs are required to get 8KB memory.

c) Explain race around condition in J-K Flip-Flop.
Ans:- (Waveforms 2 mks, explanation 2 mks)

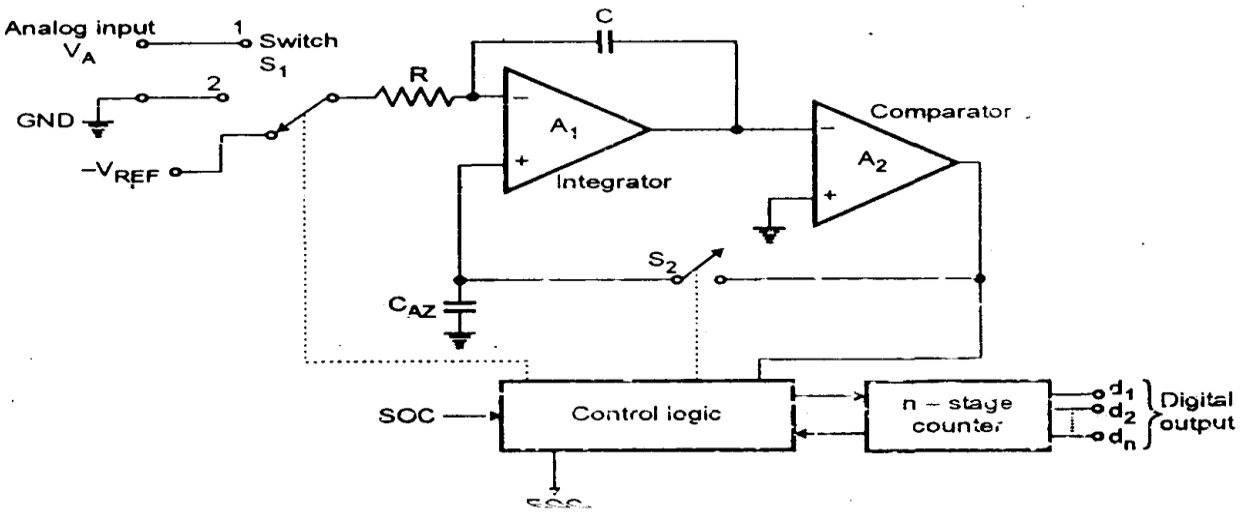
Race around condition occurs in J K Flipflop only when J=K=1 and clock/enable is high (logic 1) as shown below-



Explanation:-In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state) ,but due to multiple feedback output changes/toggles many times till the clock/enable is high. Thus toggling takes place more than once, called as racing or race around condition. Thus to avoid RAC following methods can be used-
1. Design the clock with time less than toggling time (this method is not economical)
2. Use edge triggering.
3. Use Master Slave J K Flip-flop.

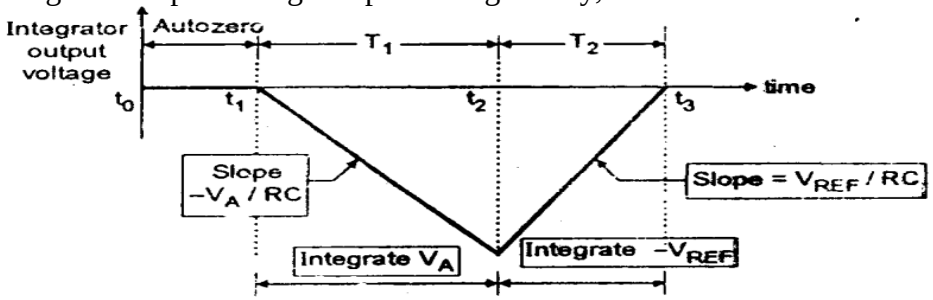
d) Describe the working of dual slope A/D converter.
Ans:- (Diagram 2 marks, operation 2 marks)

The dual slope ADC consists of OPAMP‘s being used as integrator and comparator. The control logic accepts the SOC signal and generates EOC signal when the conversion is over. It also controls the two switches S1 and S2 out of which S1 is a single pole three way switch whose one terminal is connected to analog voltage VA, second one is connected to ground and the third one is connected to a negative reference voltage -VREF.



Operation:-At the out Initially assume that the integrator output voltage V0= 0 and the counter is in RESET condition i.e. counter
output is 00.

1. At t = t0 switch S1 is connected to ground and switch S2 is closed. The capacitor CAZ gets connected across the comparator output .
2. Any offset voltage present in the OP-AMPs will appear across the capacitor C. This will provide an automatic compensation for the input offset voltage of all the amplifiers. Therefore integrator output voltage is zero for the interval t0 to t1 .
3. At instant t1 the SOC command is given to the control logic. Switch S1 is connected to VA and Switch S2 is open circuited. CAZ acts as a memory to hold the voltage required to keep the offset zero. Hence CAZ is known as the auto zero capacitor.
4. From t1 to t2 ,this ADC will integrate the analog input VA, for a fixed duration of clock cycles. This time interval is requited for the counter to advance through all its possible output states, because for an n-bit counter there will be 2n possible output states.
5. The counter output then reduces to zero. The time duration t1 to t2 t is represented by T1.The integrator output during this period is given by,



$$V_o = -\frac{1}{RC}\int_{t_1}^{t_2} V_A\, dt = \frac{-V_A T_1}{RC}$$

6.This expression represents a straight line with a slope of - VA / RC. Thus we get a decreasing ramp. The time period T is thus represented by 2n clock cycles.
T = 2n x T where T = One clock cycle period

7. At the end of interval T1 the integrator input is connected to a fixed negative reference voltage (-V REF) via switch S1

8. The integrator output now starts increasing towards zero with positive slope. The slope of the line is VREF / RC for the duration t2 to t3.

9. The counter starts counting from 0. The integration will continue till the integrator output is non-zero. At instant t3 the integrator output reduces to zero then the comparator output goes from HIGH to LOW and the clock pulses given to the counter are stopped.

10. At t3. the counter output shows a number corresponding to N clock cycles it has counted during period t2 to t3.

11. Thus this number N represents the time taken for integrator output to reduce from -VA to 0. Hence N represents the desired digital output code proportional to the analog input VA.

12. If VA increases, then the integrator capacitor vi1l charge to a higher negative voltage during the time interval T Therefore the time T required to reduce the integrator output to zero increases.

13. Therefore the counter output count (N) will be higher. Thus N is proportional to VA.

e) Compare TTL and CMOS logic families.

Ans:- (Any 4 points-4 marks)

Parameters	CMOS	TTL
Device used	P- Channel & N-Channel MOSFET	BJT (transistor)
Noise Margin	1.45 v	0.4v
Noise immunity	Better than TTL	Less than CMOS
Propagation delay	105 nsec	10 nsec
Switching speed	Less than TTL	Faster than CMOS
Power dissipation	Less 0.1 mW	More 10 mW
Fan out	50	10
Unused input	Connect to ground or VCC	Input can remain floating & treated as logic 1
Operating region	Ohmic & cutoff region	Saturation or cutoff region
Component density	Need Smaller space	Need more space than CMOS

f) In the given fig. 2, the control signal S_2S_3 of 1:4 demux changes from 00 through 11. Write its truth table.

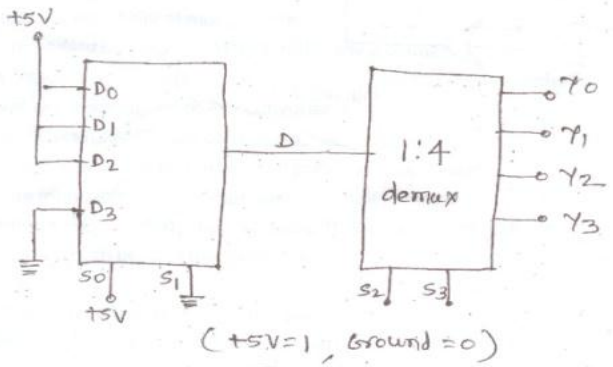


Fig. No. 2

Ans:- truth table: 4 marks

Truth Table

S_0	S_1	D	S_2	S_3	Y_0	Y_1	Y_2	Y_3
1	0	1	0	0	1	0	0	0
1	0	1	0	1	0	1	0	0
1	0	1	1	0	0	0	1	0
1	0	1	1	1	0	0	0	1

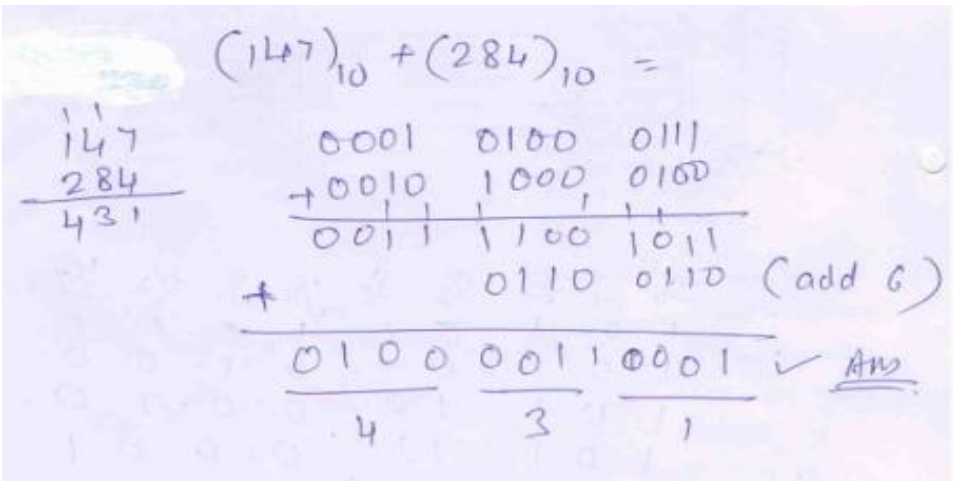
Q 6. Attempt any four of the following: **16**

a) Add $(147)_{10}$ and $(284)_{10}$ in BCD code.
Ans :

$(147)_{10}$= (0001 0100 0111)$_{BCD}$ …. 1 mark.

$(284)_{10}$= (0010 1000 0100)$_{BCD}$ … 1 mark.

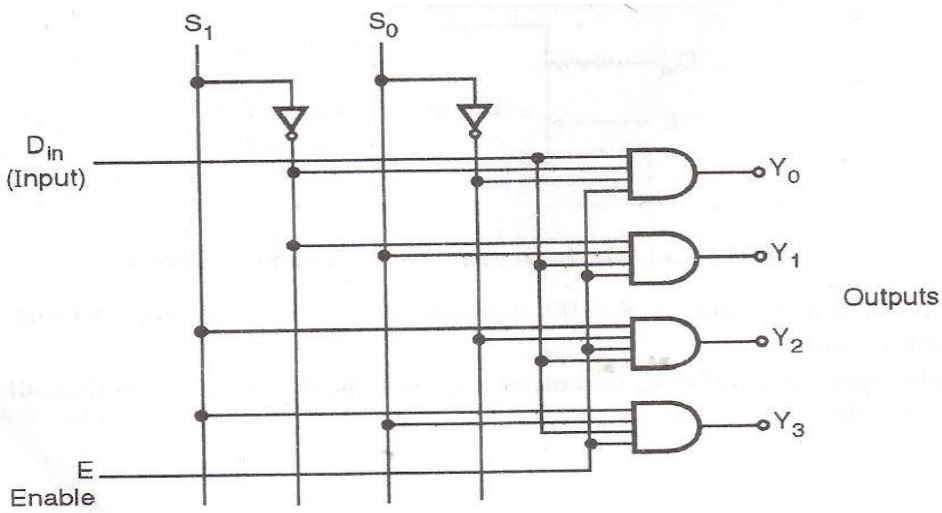
Adding 6 decimal …. 1 mark.
Correct answer …. 1 mark.



b) Explain the operation of 1:4 de-multiplexer using logic gate.

Ans:- (Diagram 2 mks,truth table 2 mks)

The internal logic diagram of 1:4 demultiplexer and its truth table is as shown –

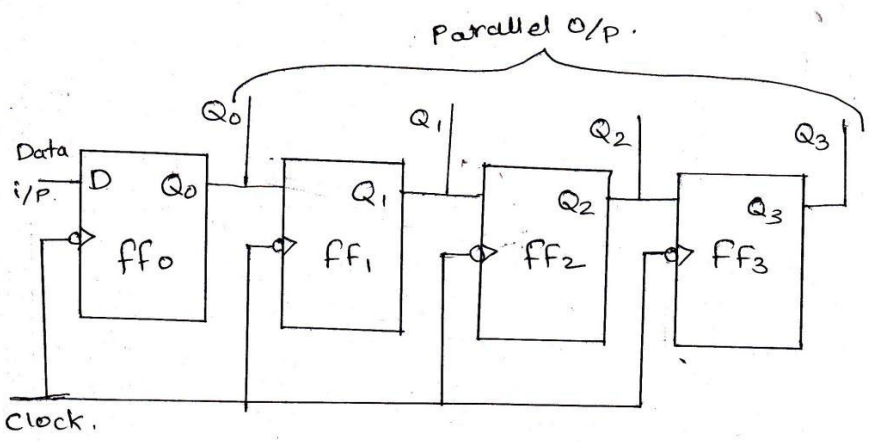


Truth table 1:4 demux

E	S0	S1	Y0	Y1	Y2	Y3
0	X	X	0	0	0	0
1	0	0	D	0	0	0
1	0	1	0	D	0	0
1	1	0	0	0	D	0
1	1	1	0	0	0	D

c) Describe operation of SIPO shift register with circuit diagram.

Ans:- (Diagram: 2mks, truth table 1 mks, explanation 1 mks)



In serial In Parallel Out shift register, data is shifted in serially, but shifted out in parallel. The data bits are entered into the register serially from data input. In order to shift the data out in parallel, it is simply necessary to have all the data bits available as outputs at the same time this is done by connecting the output of each flip-flop to an output pin. Once the data bits are stored, each bits appears on its respective output line and all bits are available simultaneously.

Truth Table:

CLK	Data i/p	Q3	Q2	Q1	Q0
0	1	0	0	0	1
1	1	0	0	1	1
2	1	0	1	1	1
3	1	1	1	1	1

d) A RAM IC has 12 address lines and 8 data lines. If its first location has address 9000H what will be the address of the last location?

Ans:-

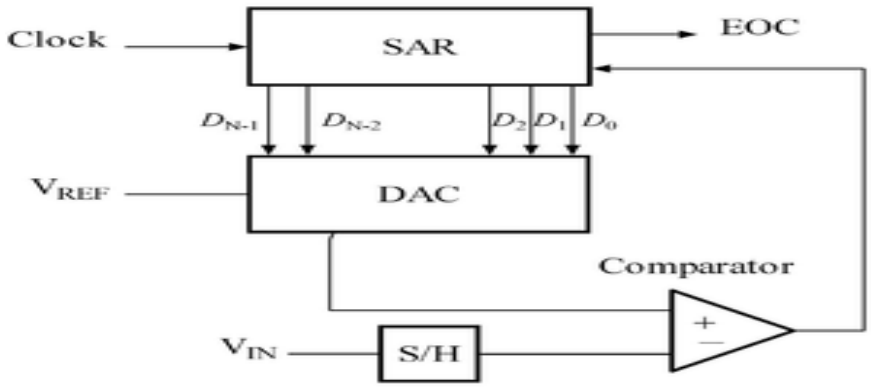
As the address lines are 12, therefore it is a 4K RAM. To find out the address of the last location, mapping is required and is follows.
By full decoding method, as the starting address is 9000H, the address of the last location will be 9FFFH as shown below.

Memory Map

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Memory address
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Starting 9000H
1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	Last/End 9FFFH

e) Describe the working principle of successive approximation method ADC with block diagram.

Ans : (Diagram: 2 mks, operation: 2 mks)



DAC = Digital-to-Analog converterEOC = end of conversion
SAR = successive approximation register
S/H = sample and hold circuit
V_{in} = input voltage
V_{ref} = reference voltage

The successive approximation Analog to digital converter circuit typically consists of four chief sub circuits:

1. A sample and hold circuit to acquire the input voltage (V_{in}).
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register(SAR).
3. A successive approximation register sub circuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in}.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing

this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

f) For a given logical diagram, derive Boolean expression for output Y by simplifying it as much as possible.

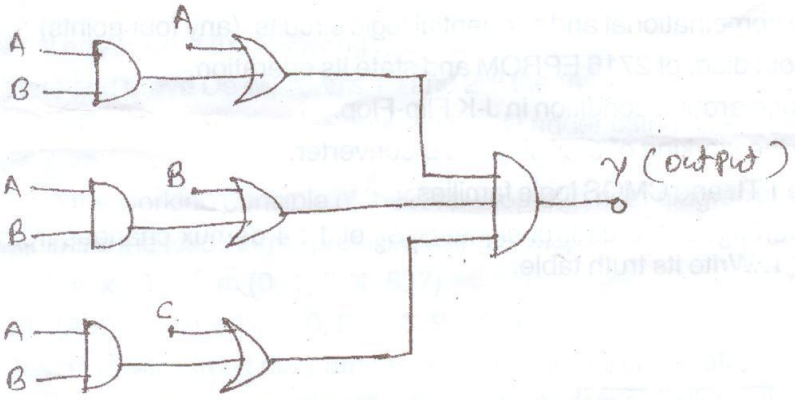


Fig. No. 3

Ans:- 4 marks