WINTER– 14 EXAMINATION

Subject Code: **17320** **Model Answer**

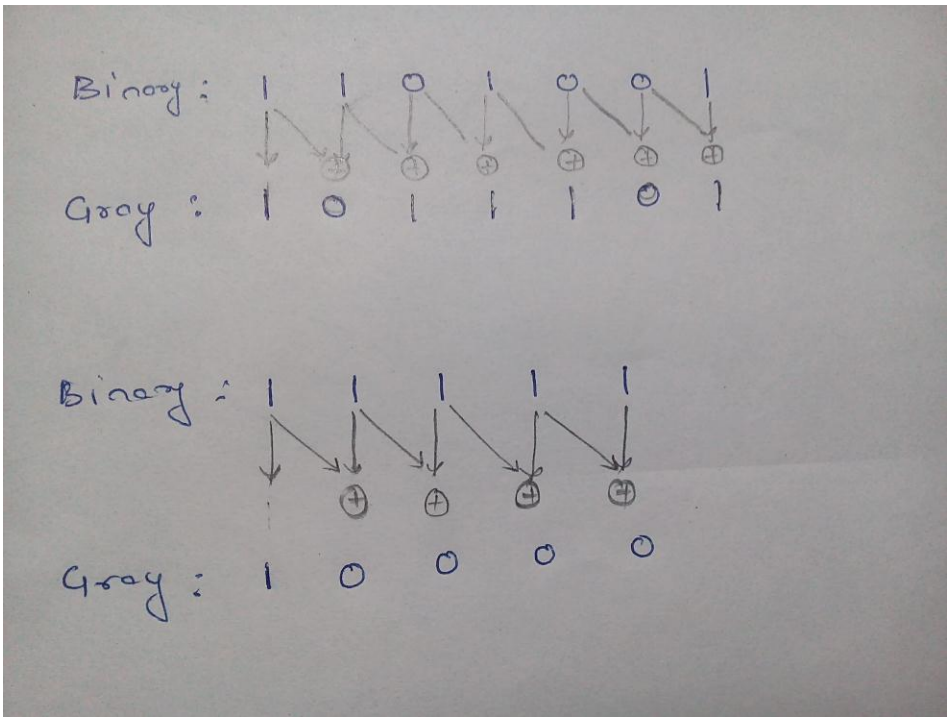
Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. A)Attempt any six. **12 Marks**

a) Convert the following binary number to gray code i) 1101001 ii) 11111.

Ans: **1 Mark for each correct answer**



b) Write any two advantages of MUX.

Ans:- 1 Mark for each advantage

1. It reduces the number of wires.
2. So it reduces the circuit complexity and cost.
3. We can implement many combinational circuits using MUX.

4. It simplifies the logic design.
5. It does not need the k maps and simplification.

c) What is meant by modulus of a counter?
Ans:- 2 Marks for correct answer

Modulus of a counter represents the number of states through which the counter progresses during its operation. It is denoted by N.Thus MOD-N counter means the counter progresses through N states.
The 2-bit ripple counter is called as MOD 4 counter and will have 4 states and 3-bit ripple counter is called as MOD-8 counter and will have 8 states. So in general an N-bit ripple counter is called as modulo-N counter where MOD number = $2^{N.}$

.

d)) Define bi-directional shift register.
Ans: - 2 Mark for correct answer

1. If a binary number is shifted left by one position then it is equivalent to multiplying the original number by 2. Similarly, if a binary number is shifted right by one position then it is equivalent to dividing the original number by 2.
2. Hence if we want to use the shift register to multiply and divide the given binary number, then we should be able to move the data in either left or right direction.
3. Such a register is called a bi-directional register.

e) Write any two applications of analog to digital converter.
Ans:- 1 Mark for each application

1) In digital acquisition system
2) In digital instruments such as digital voltmeter, frequency counter etc.
3) In computerized instrumentation system
4) NC and CNC machines.

f) Write the types of RAM memory with its definitions.
Ans:- 1 Mark for types of RAM, 1/2 Mark for definition of each

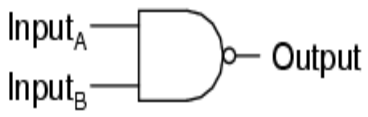
Random access memory is also called as read-write memory.
There are two types of RAMs:

1. Static RAM
   - This type of memory can be implemented by bipolar as well as MOS technology.
   - Its possilble to store data as long as power is applied to the chip.
   - The basic cell in SRAM is a flip-flop

2. Dynamic RAM
   - In dynamic RAM, the data is stored in the form of charge on the capacitor.
   - Its formed using MOSFET and capacitor.
   - It needs to be refreshed after every few milliseconds.

g) Draw symbol of IC 7400 and also write the truth table and Boolean expression.
Ans:- 1 Mark for symbol ,1/2 Mark for truth table,1/2 Mark for Boolean expression
(IC pin diagram is also a valid answer)

Symbol of NAND gate **Truth Table**

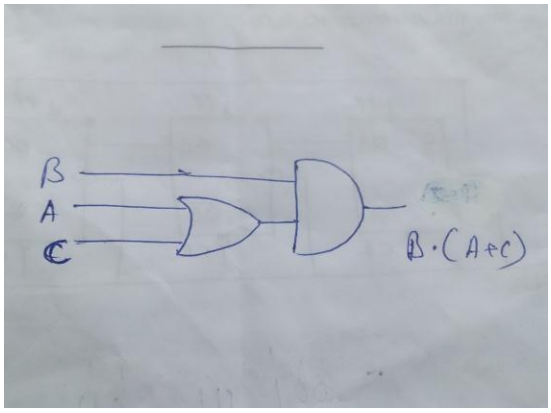


A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Boolean expression

Y= $\left(\overline{AB}\right)$

h) Draw the given Boolean expression use one AND gate and one OR gate.
y = AB + BC.
Ans:- AB+BC= B(A+C)



B) Attempt any two : 8 Marks
a) Add the binary number i) 1011.11 and 1100.01 ii) 0101.1 and 1111.01

a) Answer (2mark)

i) 1011.11
1100.01
1111 1

11000.00 (result)

0101.1 **(2mark)**
1111.01
111

10100.11 (result)

b) Convert the following expression into their standard SOP form
y = A + BC + ABC
Ans. **4 Marks for correct answer**

i. Y= A+ BC+ ABC

Step 1: Find the missing literal from each of the following term

$Y = \underset{\text{B\&C are missing}}{A} + \underset{\text{A is missing}}{BC} + \underset{\text{All literals are present.}}{ABC}$

Step 2: AND each term with (missing literal + Its complement) and simplify the expression to get canonical SOP

$$\therefore \quad Y = A(B+\bar{B})(C+\bar{C}) + (A+\bar{A})BC + ABC$$

$$\therefore \quad Y = (AB + A\bar{B})(C+\bar{C}) + ABC + \bar{A}BC + ABC$$

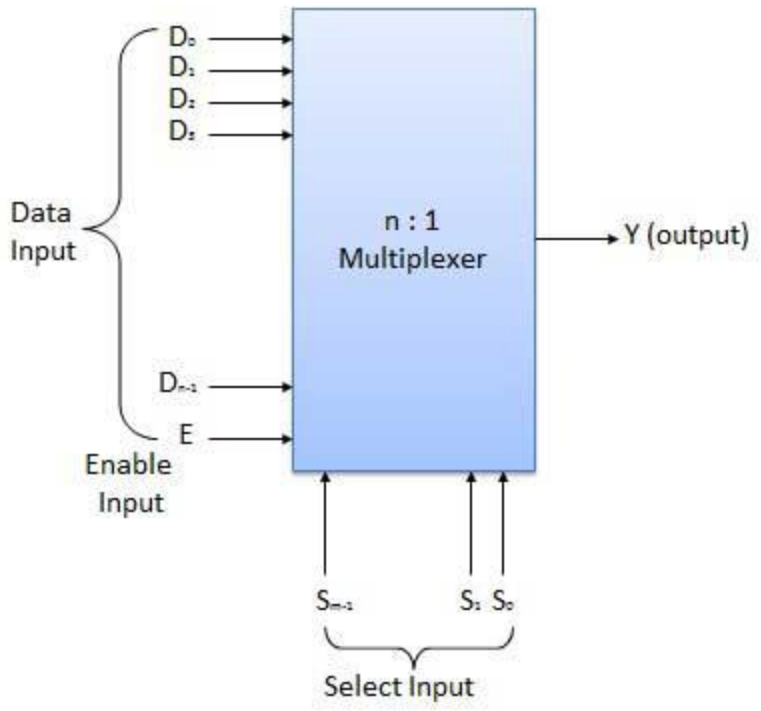
$$Y = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\,\bar{C} + ABC + \bar{A}BC + ABC$$

$$Y = AB\bar{C} + A\bar{B}C + A\bar{B}\,\bar{C} + \bar{A}BC + ABC$$

[as ABC + ABC + ABC = ABC]

$$\therefore \quad Y = AB\bar{C} + A\bar{B}C + A\bar{B}\,\bar{C} + \bar{A}BC + ABC$$

C) Draw the general block diagram of MUX and write its operation.
Ans:- 2Marks for diagram, 2 Marks for explanation



Operation

The multiplexer is a digital circuit which has many input lines and one output line.
D_0 to D_{n-1} are the input lines and y is the output line.
The function of the mux is to select one of the input lines and connect it to the output.
S_0 to S_{n-1} are the select lines. The selection of the desired input is done by means of selection lines.
E is the strobe or enable input and (is generally active low) and used to enable or disable the MUX operation.

2) Attempt any four : 16 Marks

a) Convert following numbers into binary and add them $(173)_8 + (741)_8$

Ans. 4 Marks correct Answer

$(173)_8 = (011\ 111\ 011)_2$ $(741)_8 = (111\ 100\ 001)_2$

Add both the numbers

Carry	**1**	**1**	**1**	**1**					**1**	**1**	
+A		**0**	**0**	**1**		**1**	**1**	**1**		**0**	**1**	**1**
+B		**1**	**1**	**1**		**1**	**0**	**0**		**0**	**0**	**1**
	1	**0**	**0**	**1**		**0**	**1**	**1**		**1**	**0**	**0**

Writing in to octal form-

$001\ 001\ 011\ 100 = (1134)_8$

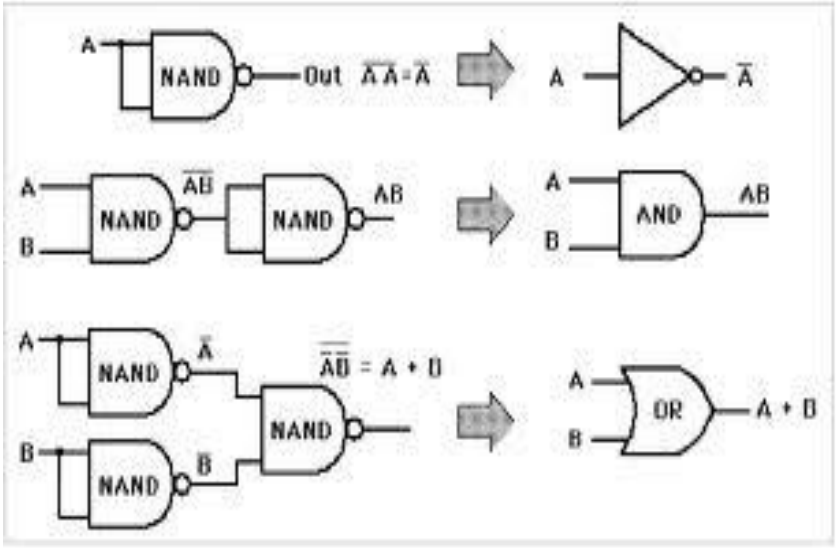
b) Why NAND gate is called universal gate ? Implement basic gates using NAND gate only.
Ans:- 1 Mark explaination,1 Mark each for implementation of basic gates

1. We can implement any other gate (AND, OR, NOT, EX- OR, EX- NOR) using NAND gate.

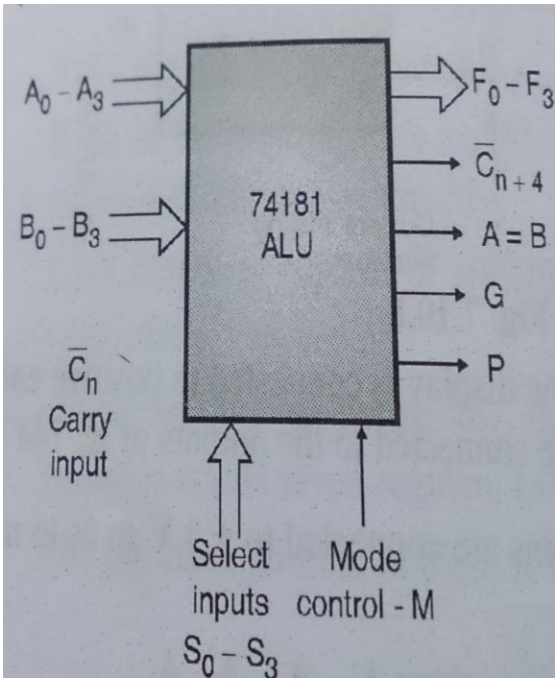
2. It is possible to implement any Boolean expression with the help of only NAND gates.

3. Hence a user can build any combinational circuit of any complexity with the help of only NAND gates .

AND ,OR and NOT gate using NAND is as shown below-



c) Draw the block diagram of ALU IC74181 and also write its operation.
Ans- Diagram 2 mks, explanation 2 mks



Explanation- IC 74181 is an high speed, 24 pin IC DIL package. widely used combinational logic, capable of performing the arithmetic as well as logical operations. It is the heart of microprocessor.

A and B are the two 4 bit input variables,

F is the 4 bit o/p variable, S are the 4 bit select lines that decides various (either arithematic as well as logical operations)

M= mode control that decides whether ALU will perform arithmetic or logical operations

If M= 1, Logical operations (16 AND,OR ,NOR etc operations ,depending upon the 4 bit combination of select lines)

If M=0, Arithmetic operations (16 addition, subtraction, division etc operations ,depending upon the 4 bit combination of select lines)

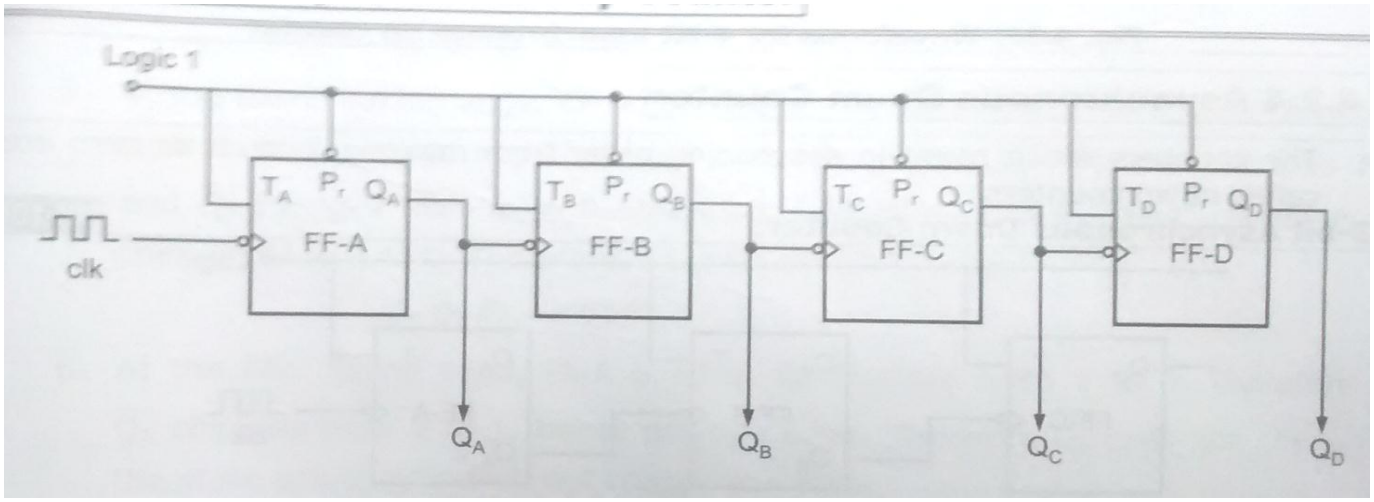
A=B ,Comparator equality o/p

G and P are the generate and carry propagate o/ps used for cascading of ALUs

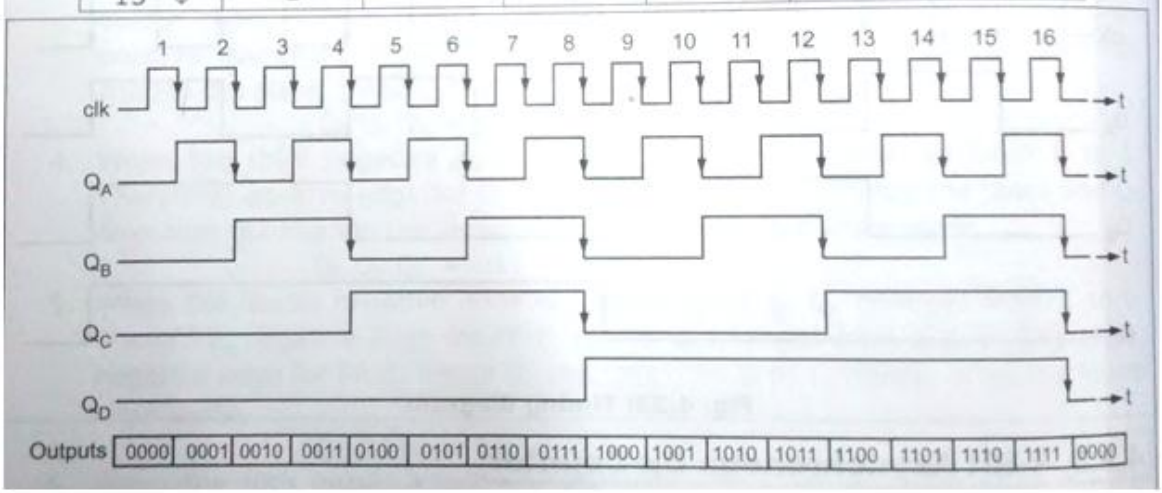
d) Write the difference between combinational and sequential logic circuit. (any four points).
Ans:- 1Mark for each difference

Sr no	Combinational ckt	Sequential ckt
1	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
2	No memory element required in the ckt	Memory element required to stored bit
3	Clock input not necessary	Clock input necessary
4	E.g. Adders, Subtractors ,Code converters , comparators etc.	E.g. Flip flop, Shift registers, counters etc,
5	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

e) Design 4 bit asynchronous up-counter also write the truth table and draw the waveform.
Ans:- 2Mark diagram,1 Mark truth table ,1 Mark waveform



Clock	Flip-flop outputs				State	Decimal count
	Q_D	Q_C	Q_B	Q_A		
Initially	0	0	0	0	1	0
1st ↓	0	0	0	1	2	1
2nd ↓	0	0	1	0	3	2
3rd ↓	0	0	1	1	4	3
4th ↓	0	1	0	0	5	4
5th ↓	0	1	0	1	6	5
6th ↓	0	1	1	0	7	6
7th ↓	0	1	1	1	8	7
8th ↓	1	0	0	0	9	8
9th ↓	1	0	0	1	10	9
10th ↓	1	0	1	0	11	10
11th ↓	1	0	1	1	12	11
12th ↓	1	1	0	0	13	12
13th ↓	1	1	0	1	14	13
14th ↓	1	1	1	0	15	14
15th ↓	1	1	1	1	16	15



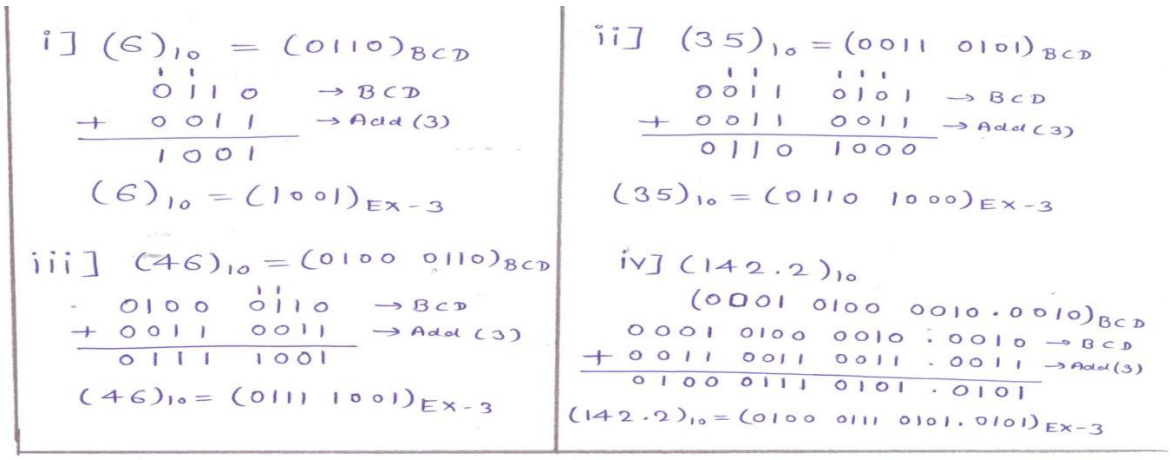
f) Compare between R-2R ladder DAC and weighted resistor DAC (4 points).
Ans: 1 Mark for each difference

Sr No.	Parameter	Weighted Resistor	R-2R Ladder Network
1.	Simplicity	Simple	Slightly complicated
2.	Range of resistor values	Wide range is required	Resistors of only two values are required
3.	Number of resistors per bit	One	Two
4.	Ease of expansion	Not easy to expand for more number of bits	Easy to expand

Q3 Attempt any four. **16 Marks**

a) Convert the following decimal number into Excess-3 code,
1) $(6)_{10}$ 2) $(35)_{10}$ 3) $(46)_{10}$ 4) $(142.2)_{10}$

Ans: 1 Mark for each correct answer



b) Compare totem pole & open collector outputs.(any four points)

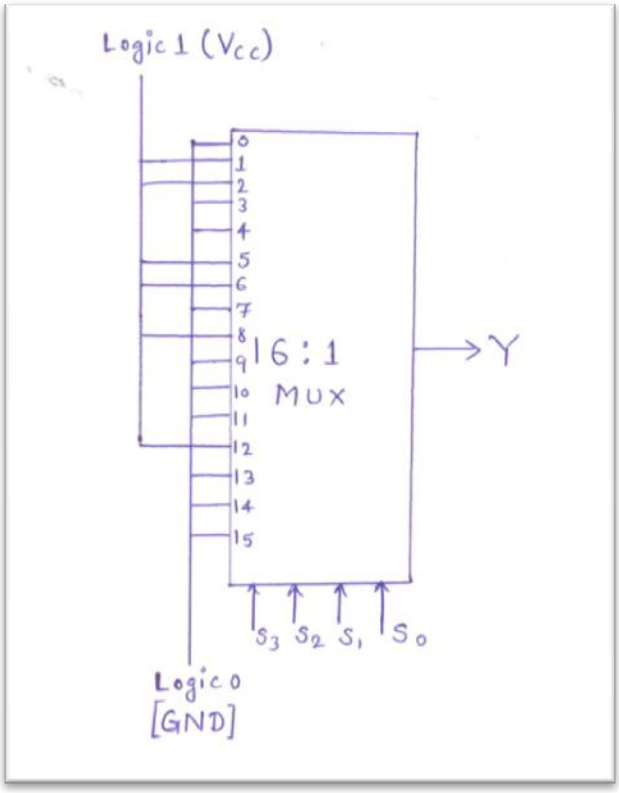
Ans: Totem pole & open collector outputs (4 points, 4 mks)

Parameter	Totem-Pole	Open Collector
1)Circuit components on the O/P side	Q3 (pull up transistor),D & Q4 (pull down transistors)are used.	Only the pull down transistor Q4 is used.
2)Wired ANDing	Cannot be done	Easily be done
3)External pull up resistor	Not required	Required to be connected
4)Speed	Operating speed is high	Operating speed is low
5)Power Dissipation	Low	High

c) Implement the following using 16:1 multiplexer,

$y=\sum m\ (1,2,5,6,8,12)$.

Ans: For correct implementation 4 Marks.



d) Write the use of preset & clear terminal in a flip-flop.

Ans: 2 Mks for explanation & 2 Mks for Truth Table.

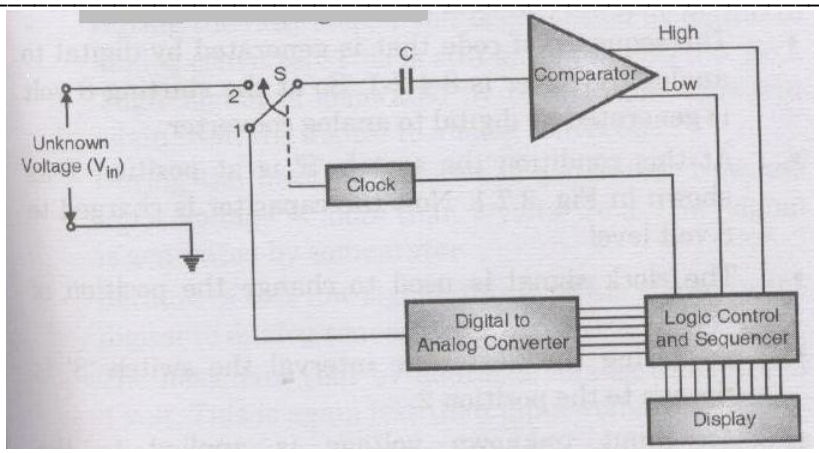
In the Flip-flop when the power is switched ON, the state of the circuit is uncertain.
It may be set (Q=1) or reset (Q=0) state.
In many applications it is desired to initially set or reset the flip-flop i.e. the initial state of flip-flop is to be assigned. This is done by using preset (Pr) & clear (Cr) inputs.
There inputs may be applied at any time between clock pulses & are not in synchronism with the clock.
Truth Table with Preset & Clear I/P.

Input			Output	Operation
CLK	Cr	Pr	Q	preformed
1	1	1	Q_{n+1}	Normal FF
×	0	1	0	FF is reset
×	1	0	1	FF is set

So, the O/P of the flip-flop changes whenever a clock signal is applied, it is necessary to set the output or reset the output i.e. to start with some definite intial state,then two additional inputs Preset & Clear are used.
These inputs sets or resets the flip-flop independent of clock.

e) Draw the block diagram of successive approximation type ADC & write the function of each block.

Ans: (2 mks for Diagram , 2mks explanation)



Working:- (Explanation in short should be considered)

Consider that unknown voltage to be measured is 3.2135 volts.

Also consider that digital to analog converter generates the codes 8- 4- 2- 1.

Initially the digital to analog converter is reset. The sequence of code that is generated by digital to analog converter is 8-4-2-1. So at the starting 8 volt is generated by digital to analog converter. At this condition the switch „So is at position 1. Now the capacitor is charged to 8 volt level. The clock signal is used to change the position of switch. So during the next time interval the switch „So is thrown to the position 2. An input unknown voltage is applied to the capacitor.

The capacitor was charged to 8 volt. If input voltage is more than the voltage stored across the capacitor then the current flows into the comparator. However if this input voltage is less than the capacitor voltage then the current flows in opposite direction.

Now when the current flows into the comparator then high signal is generated. And when the current flows in opposite direction then low signal is generated by the comparator.

The generation of high signal causes the resetting of digital to analog converter.

While during the generation of low signal; the data generated by digital to analog converter is retained.

Here an input voltage to be measured is 3.2135. Initially the digital to analog converter generates 8 volts. The comparator compares these two voltages. Now a high signal is generated. This will reset the digital to analog converter. During the next step, 4 volts is generated by digital to analog converter. This is still more than 3.2135. So a high signal is generated by comparator. This will again reset the digital to analog converter. Because of this low signal; this 2 volt is stored in the digital to analog converter.

The next data sent by digital to analog converter is 1 volt. This is again less than input voltage. So a low signal is generated by the comparator. Now this 1 volt is retained in digital to analog converted, so the voltage level I it becomes 2 + 1 = 3 volts.

This process takes place continuously until the signal in digital to analog converter becomes equal to unknown input voltage.

f) Compare EPROM & EEPROM with any four points.

Ans: EPROM & EEPROM (4 points, 4 mks)

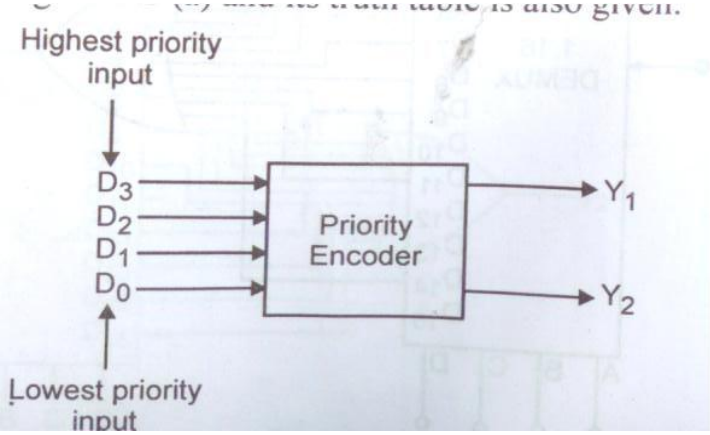
Parameters	EPROM	EEPROM
1)Technique used for erasing	Exposure to ultraviolet light	A voltage of 20 to 25 V is applied
2)Selective erasing	Not possible. All the locations get erased.	Possible. A particular location only can be erased.

3)Time required for erasing	Long 10 to 15 mins	Short 10 ms
4)Need to remove PROM from circuit	It is necessary to remove PROM	Not necessary to remove PROM
5) Cost	Less expensive	Very expensive

Q4. Attempt any four. **16 Marks**

a) What is Priority Encoder ? Draw the block diagram of Priority Encoder.
Ans : (2 marks for definition. 1 marks for diagram. 1 mark for Truth Table.)

Priority Encoder is a special type of encoder, that responds to just one input in accordance with some priority system, among all those that may be simultaneously high.
Priorities are given to the input lines.
If two or more inputs are 1, at the same time, then input line with highest priority will be considered.
Block Diagram of Priority Encoder.



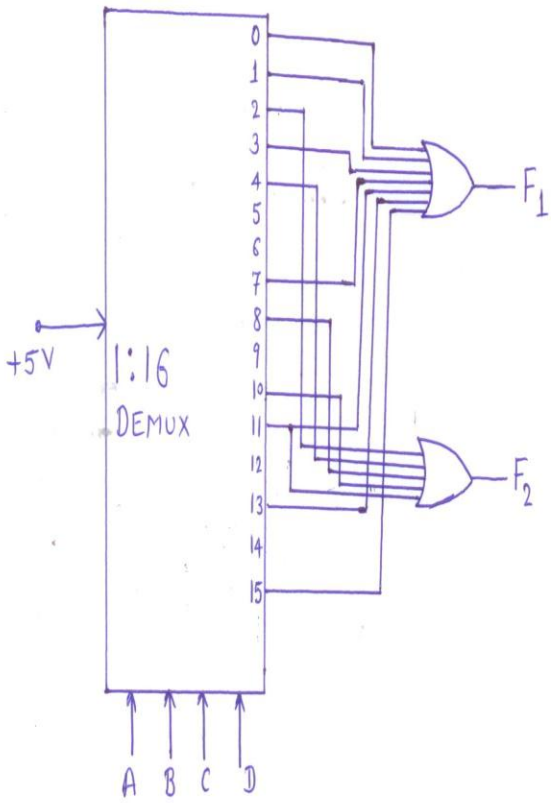
Truth Table of Priority Encoder.

Truth table :

Highest	Inputs		Lowest	Outputs	
D_3	D_2	D_1	D_0	Y_1	Y_0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

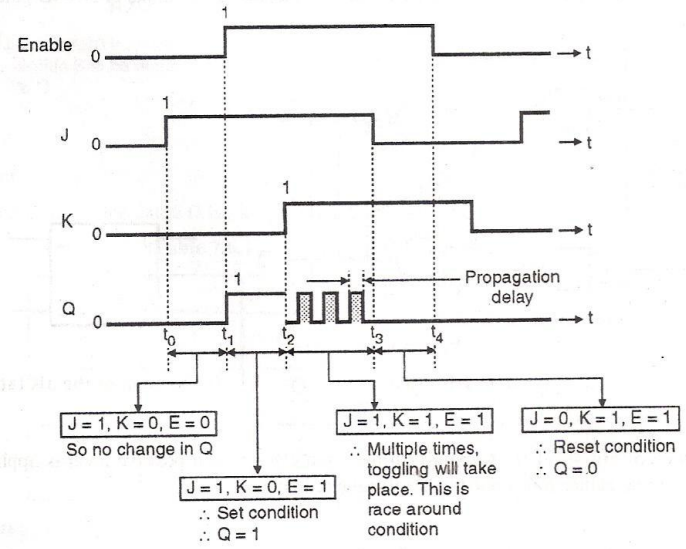
b) Realize the following function using De- multiplexer.
1) $F_1 = \sum m\ (0,1,3,7,11,13,15)$
2) $F_2 = \sum m\ (2,4,8,10,11)$.

Ans : 2Marks for each implementation.



C) What is race around condition? How it will be eliminated in J-K flip-flop
Ans: 2 mks explanation and 2 mks diagram

Race around condition occurs in J K Flipflop only when J=K=1 and clock/enable is high (logic 1) as shown below-



Explanation:-In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state) ,but due to multiple feedback output changes/toggles many times till the clock/enable is high. Thus toggling takes place more than once, called as racing or race around condition.

For elemination Edge Trigger J-K F/F is used Because in Edge Trigger J-K F/F, the positive clck pulse is present only for avery short time.

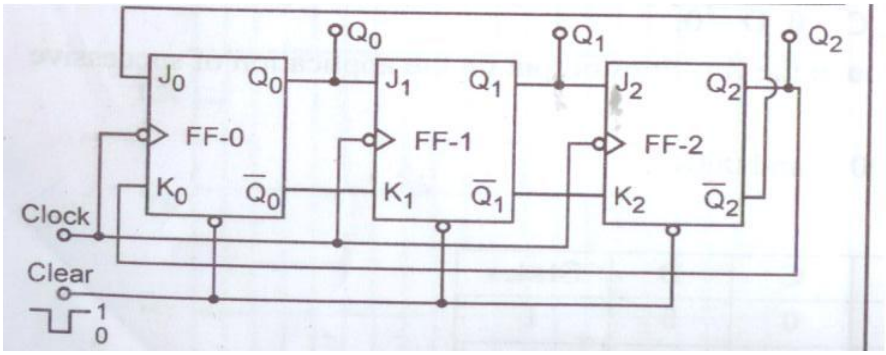
Hence by the time the changed o/p returns back to the i/p of NAND gate 3&4 , the clock pulse has died down to zero. Hence multiple toggling can not takes place.

Thus the edge triggering avoids race around condition.

d) Draw the diagram of 3- bit twisted ring counter using J-K flip-flop. Also write its truth table.

Ans: (2 Marks for diagram. 2 Marks for Truth Table.)

Diagram of 3- bit twisted ring counter using J-K flip-flop.



Truth Table for 3- bit twisted ring counter.

Truth table :

$\overline{CLEAR}$	CLK	Q_2	Q_1	Q_0	State Number
⊓	Initially	0	0	0	1
1	↓	0	0	1	2
1	↓	0	1	1	3
1	↓	1	1	1	4
1	↓	1	1	1	5
1	↓	1	1	0	6
1	↓	1	0	0	7
1	↓	0	0	0	8
1	↓	0	0	0	1

e) Write any three advantages & one disadvantage of dual slope ADC
Ans: Any three advantages [3 Marks] & Any One disadvantage [1 mark]

Advantages of dual slope ADC:
1) Off set correction can be introduced by a relatively simple circuit, facilitating auto-zeroing.
2) Low cost.
3) Accuracy of the dual-slope Adc can be of the order of 0.05% which is adequate for most applications.
4) Dual slope ADC is capable of rejecting noise & hum.

Disadvantage of dual slope ADC:
1)The only major drawback of a dule of ADC is its long conversion time as compared to other ADCs.

f) Compare SRAM & DRAM with any four point.
Ans :- Static RAM and dynamic RAM [4 points, 4 mks]

Parameter	Static RAM	Dynamic RAM
1) Circuit configuration	Each SRAM cell is a flip flop	Each cell is one MOSFET & a capacitor
2) Bits stored	In the form of voltage	In the form of charges
3) No. of components per cell	More	Less
4) Storage capacity	Less than DRAM	More than SRAM

5. Attempt any four. 16 Marks

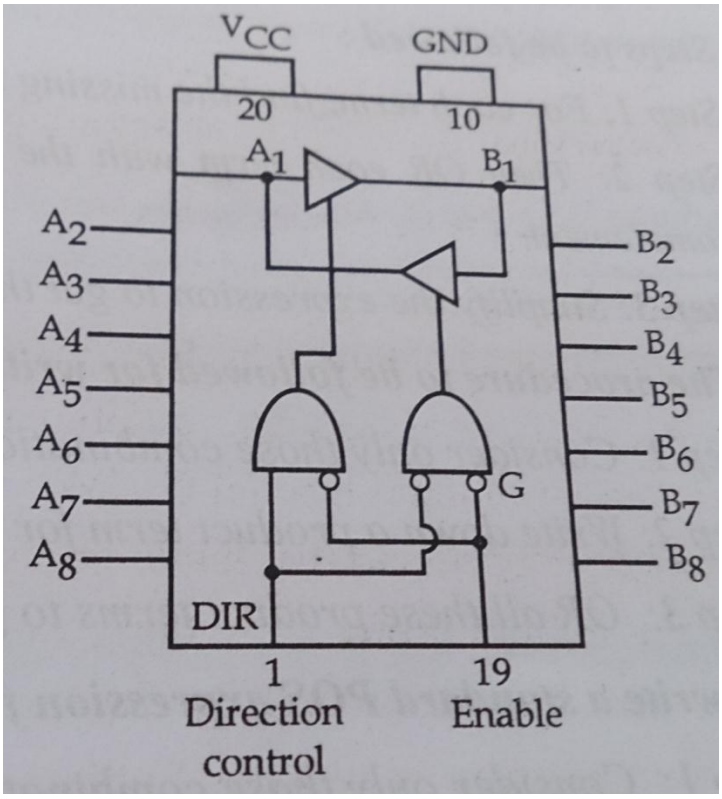
a) Write the four specifications of TTL logic family.

Ans:- Four specifications of TTL logic family (any 4 points-4 mks)

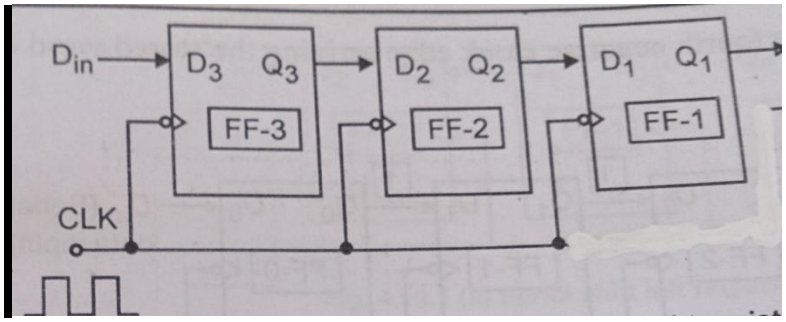
1) The basic gate is NAND gate.
2) Fan out is 10.
3) Propagation delay time is 10 nsec.
4) Power Dissipation is 10 Mw.
5) Supply voltage required is +5 V.
6) Noise margin is 0.4 V

b) Draw the logic diagram of bi-directional buffer IC 74245.

Ans:- Diagram 4 mks

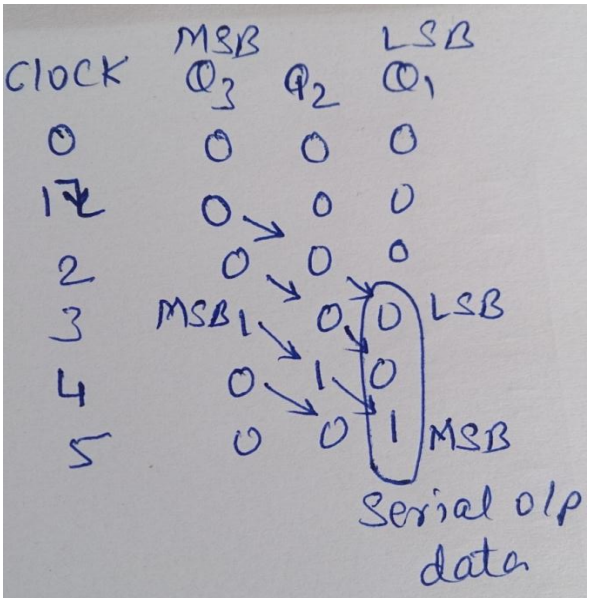


c) With neat diagram write the working of serial in serial out shift register.
Ans:- 3 bit Serial i/p and serial o/p shift register (2 mks diagram and 2 mks truth table)



Let data be- 100 (For shift right register)

Truth table



As shown

d) Write any four features of IC PCF 8591.

Ans:-Four features of IC PCF 8591 (any 4 features – 4 mks)

1) Single power supply voltage of 2.5 V to 6 V.
2) Low standby current .
3) Serial input/output via I^2C bus.
4) 8 bit successive approximation ADC.
5) Multiple DAC with one analog output.
6) On chip track and hold function.

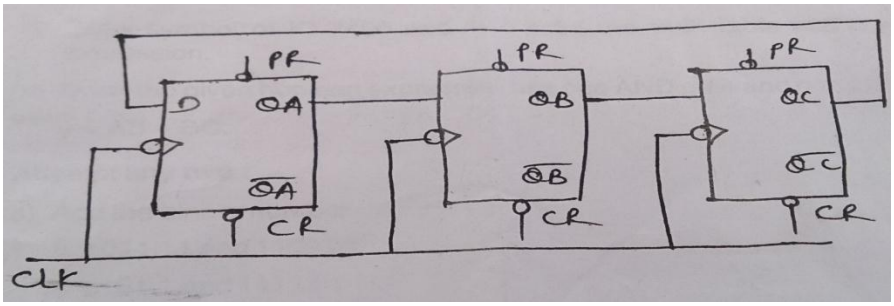
e) Compare between EPROM and Flash memory.

Ans;- (Any 4 relevant points -4 mks

Sr. No.	EPROM	FLASH
(1)	Data present in a cell erased one by one.	Large number of cells erased all at once.
(2)	Lifetime of cell is finite (i.e. greater than flash memories).	Lifetime of cell is less as compared to EPROM.
(3)	Speed of EPROM is less than flash memories.	Speed of flash memory is greater than EPROM.
(4)	It is more expensive.	It is less expensive.

)(

f) Study the given circuit as shown in figure initial output condition is $Q_AQ_BQ_C = 010$. write the truth table of output $Q_AQ_BQ_C$.



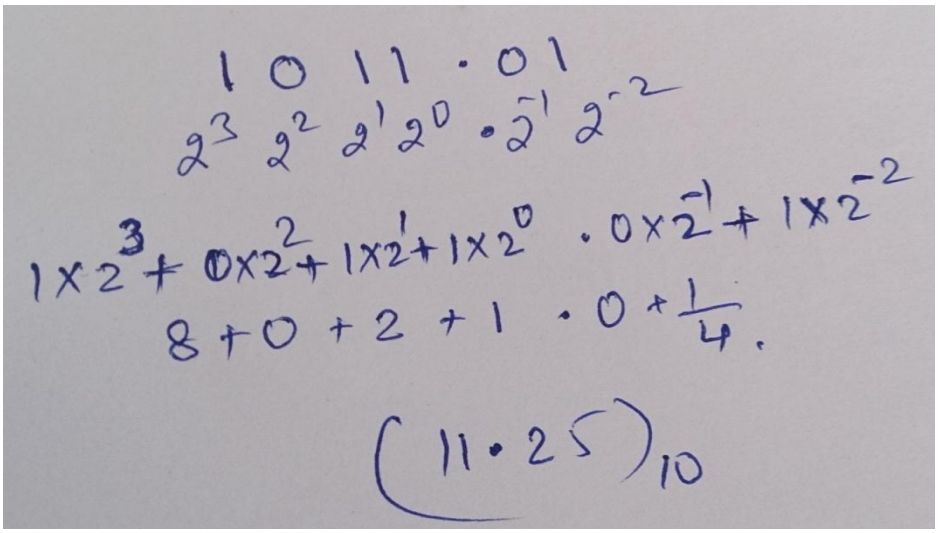
Ans ;- Truth Table of the given ring counter (4 mks)

clock	Q_A	Q_B	Q_C
0	0	1	0 (Initial count)
1	0	0	1
2	1	0	0
3	0	1	0
4	0	0	1
		⋮	

6. Attempt any four. **16 Marks**

a) Convert the number into its decimal equivalent $(1011.01)_2$.

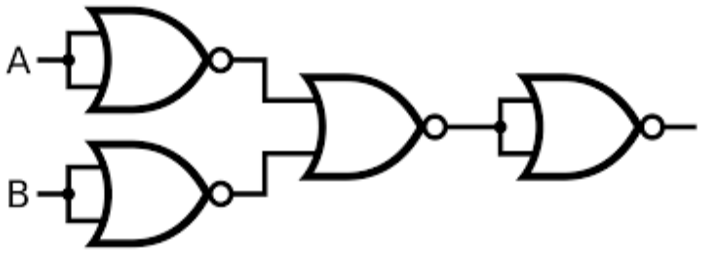
Ans:- Given decimal-1011.01



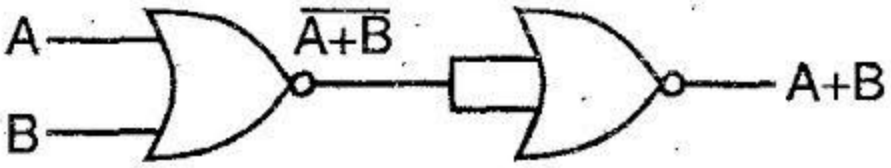
b) Draw the logical diagram of
   i) OR gate
   ii) NAND gate using NOR gate only.

Ans:- 2 mks each logical symbol

Logical diagram of NAND gate -(2 mks)



OR Gate (2 mks)



c) Write the De-Morgan's theorem and prove it.

Ans:- 2 mks each theorem (1mks for statement and 1 mk for proof using truth table)

Demorgans first theorem-

It states that-

Complement of Sum is equal to product of their individual complements.

i.e. $\overline{A+B}=\overline{A}\cdot\overline{B}$

Proof

Truth table :

A	B	A + B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}\cdot\overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

It states that-

Complement of product is equal to sum of their individual complements.

i.e. $\overline{A \cdot B} = \overline{A} + \overline{B}$

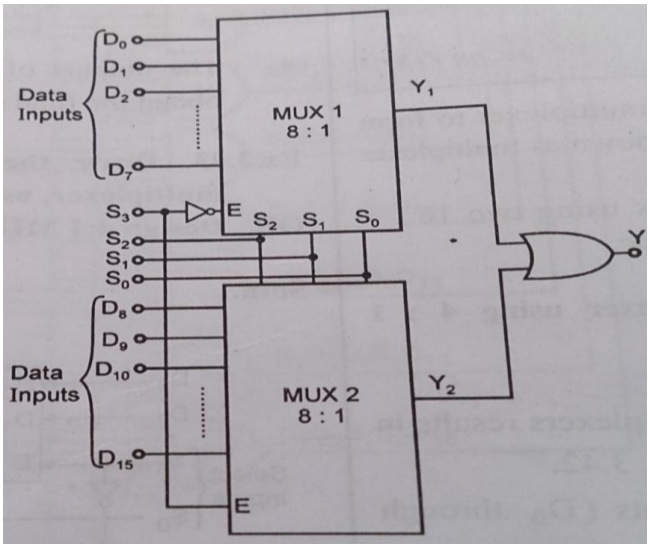
Proof

Truth table :

A	B	$\overline{A}$	$\overline{B}$	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A} + \overline{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

d) Design 16:1 MUX using 8:1 MUX.

Ans:- Diagram 2 mks , TT -2 mks

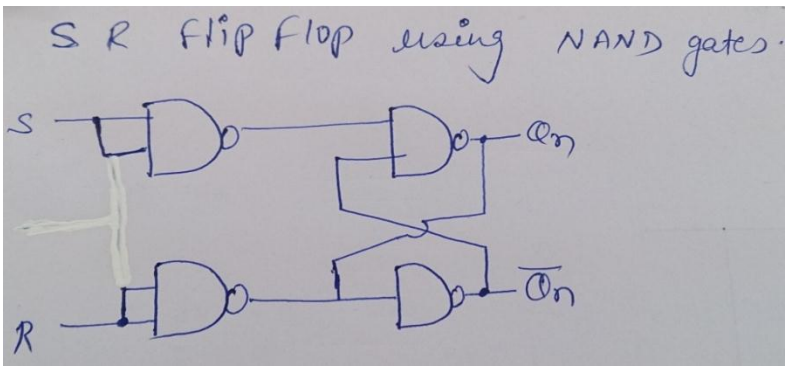


Truth Table

S_3	S_2	S_1	S_0	Y_1	Y_2	Y
0	0	0	0	D_0	0	D_0
0	0	0	1	D_1	0	D_1
0	0	1	0	D_2	0	D_2
0	0	1	1	D_3	0	D_3
0	1	0	0	D_4	0	D_4
0	1	0	1	D_5	0	D_5
0	1	1	0	D_6	0	D_6
0	1	1	1	D_7	0	D_7
1	0	0	0	0	D_8	D_8
1	0	0	1	0	D_9	D_9
1	0	1	0	0	D_{10}	D_{10}
1	0	1	1	0	D_{11}	D_{11}
1	1	0	0	0	D_{12}	D_{12}
1	1	0	1	0	D_{13}	D_{13}
1	1	1	0	0	D_{14}	D_{14}
1	1	1	1	0	D_{15}	D_{15}

e) Draw S-R latch using NAND gates only, also write about the received output for each condition using truth table of S-R flip flop.

Ans:- (Diagram 2 mks, Truth Table 2 mks, explanation can be done)

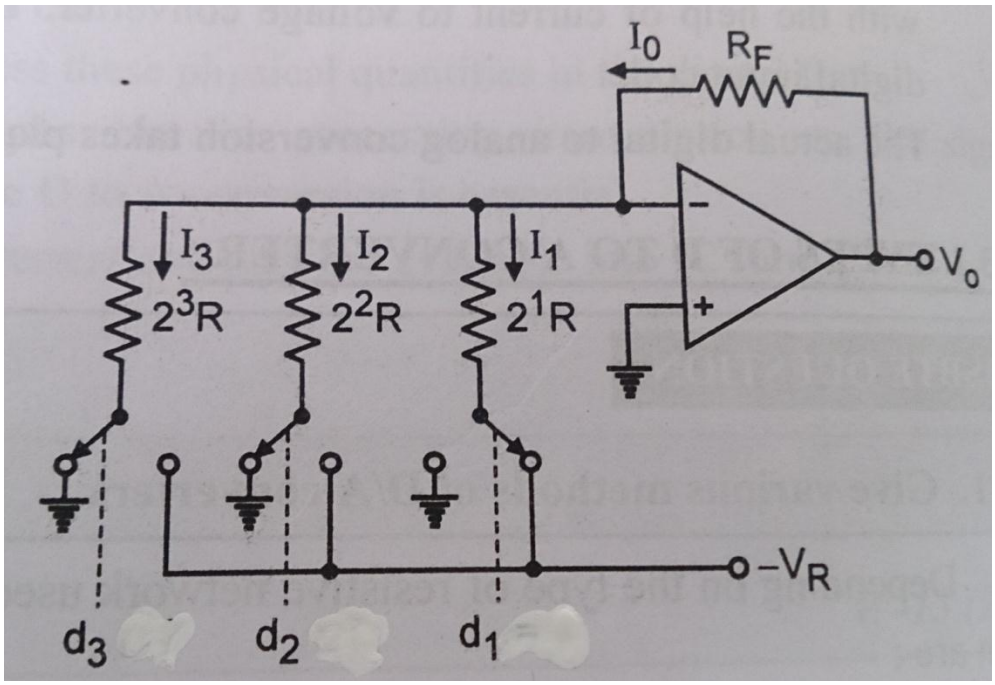


Truth table

S	R	Q_{n+1} (O/P)
0	0	Q_n (No change)
0	1	0
1	0	1
1	1	Not allowed

f) Draw the circuit diagram of 3-bit binary weighted Digital to Analog Converter (DAC) also write its mathematical derivation.

Ans:- (Diagram 2 mks, mathematical equation 2 mks)



$$\therefore \text{ Output voltage } V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$$

Where, V= Analog output voltage
d1, d2 ,d3 are n bit digital input word with d1 as MSB and d_3 as LSB.
V= Reference voltage.