MODEL ANSWER

SUMMER– 17 EXAMINATION

Subject Title: Principles of Digital Techniques Subject Code: 17320

Important Instructions to examiners:

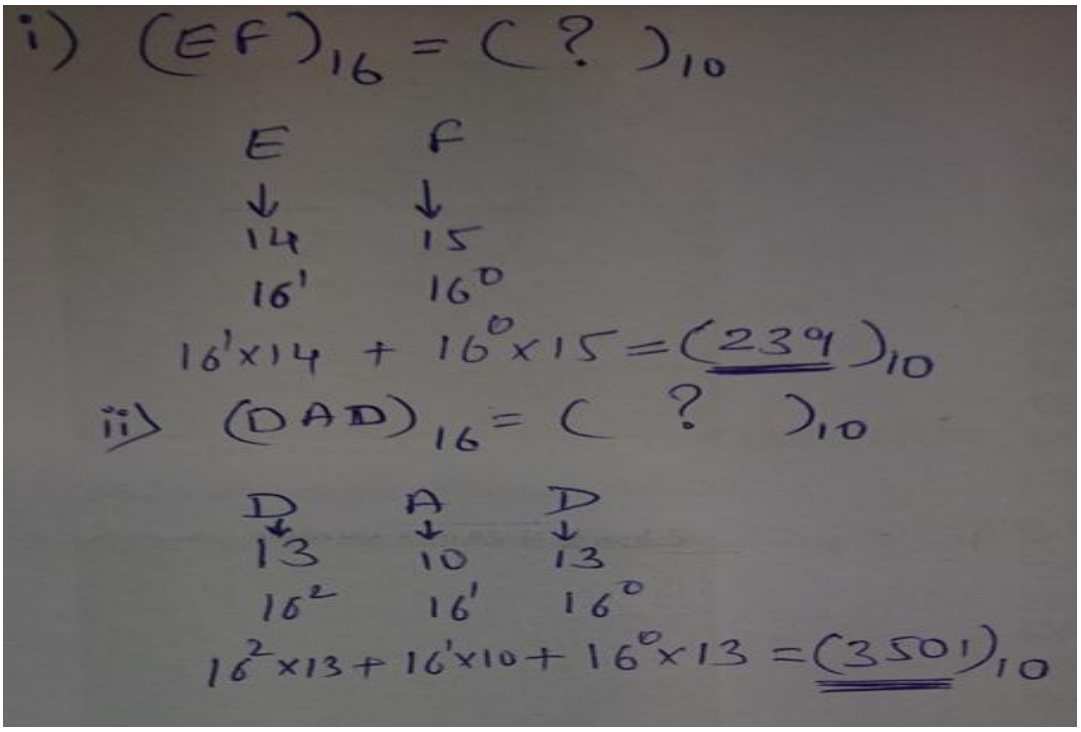
1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. Attempt any TEN of the following 20

a) Convert the following hexadecimal number to decimal

i) $(EF)_{16}$ Ii) $(DAD)_{16}$

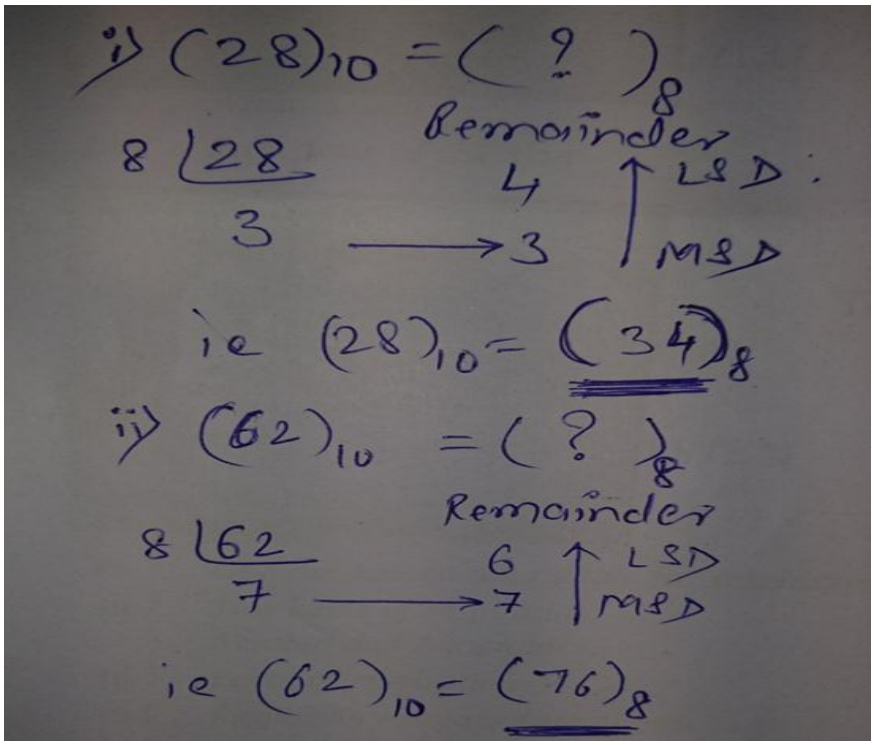
Ans:- (Each proper solution – 1 mks)



b) Convert the following decimal number to octal

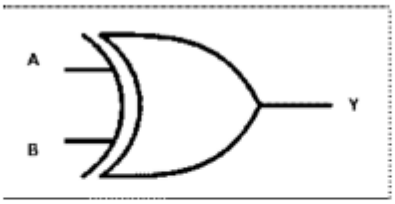
Ans:- (Each proper solution – 1 mks)

i) $(28)_{10}$ ii) $(62)_{10}$



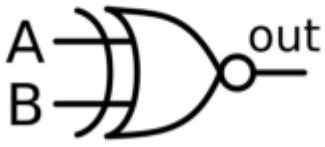
c) Draw the symbol of EXOR and EXNOR gate along with its logical equation.
Ans:- (each symbol- ½ mks, logical equation- ½ mks each)

EX-OR GATE:-



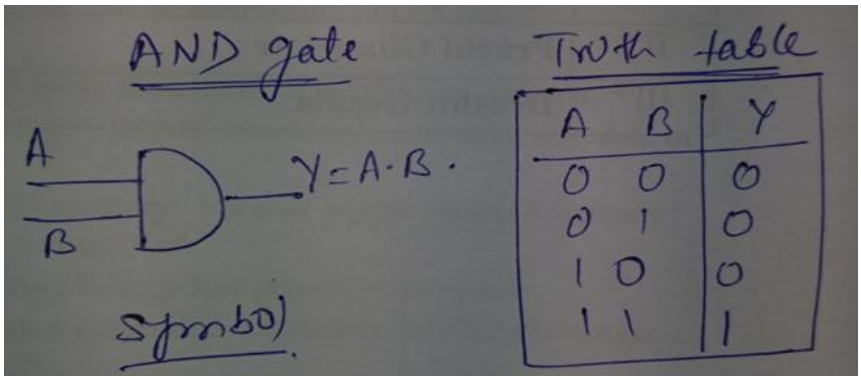
$A \cdot \overline{B} + \overline{A} \cdot B$

EX-NOR GATE:-



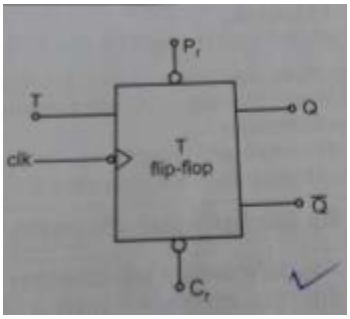
$A \cdot B + \overline{A} \cdot \overline{B}$

d) Draw symbol of AND gate and write its truth table.
Ans:- (Symbol- 1 mks, truth table- 1 mks)

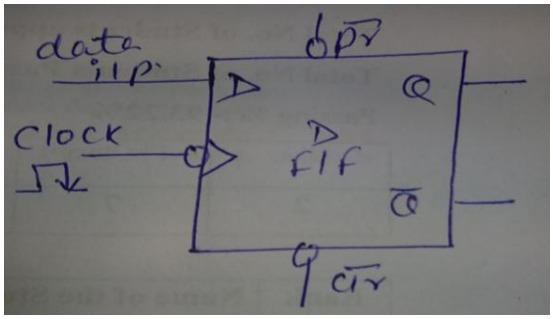


e) Draw the symbol of D flipflop and T Flipflop.
Ans:- (Each symbol- 1mks)

T Flipflop



D Flipflop



f) Define bidirectional shift register and Universal shift register.
Ans:- (Each definition- 1mks)

Bidirectional register- A register which can shift the data in either left to right direction (shift right register) or right to left direction (shift left register), which depends on mode control terminal.

Universal shift register- A register which can work in any of the 4 modes ie SISO, SIPO, PISO or PIPO is called as universal register.

g) State different triggering methods in digital circuits.
Ans:- (2 methods- 1 mks each)

Triggering is classified into two types:

1. Level Triggered-Positive level triggering
   -Negative level triggering
2. Edge Triggered Positive Edge triggering
   -Negative Edge triggering

h) State Demorgans theorems.

Ans:- (Each theorem with equation- 1 mks each)

a) De Morgan's First Theorem:

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

It states that the complement of sum equals the product of complements.

b) De Morgan's Second Theorem:

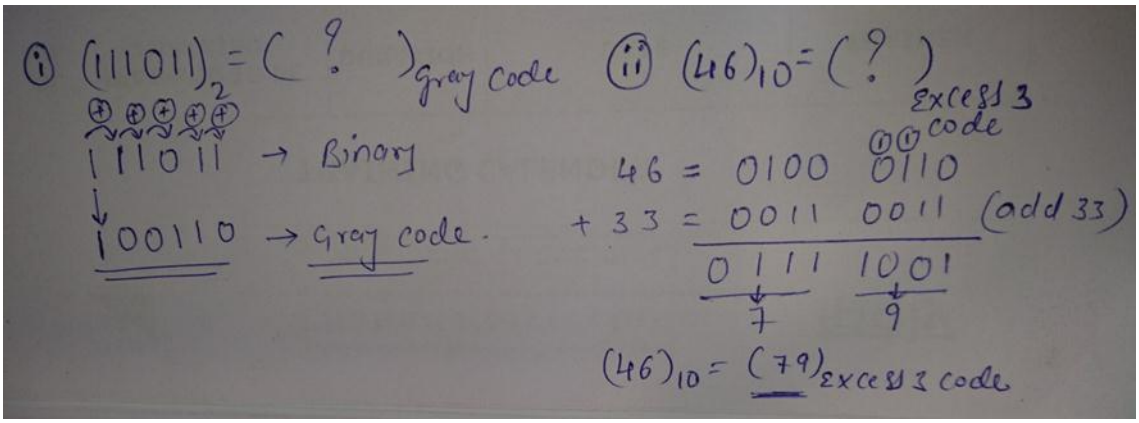
$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

It states that the complement of product equals the sum of the complements

i) Convert the following

i) $(111011)_2 = (?)_{\text{gray code}}$ ii) $(46)_{10} = (?)_{\text{excess 3 code}}$

Ans:- (Each proper conversion- 1 mks)



j) What is modulus of counter? How many flipflops are required for MOD 11 Counter.

Ans:- (Modulus definitopn- 1 mks, no of flipflop- 1 mks)

Modulus of a counter is defined as the no. of states or count through which the counter can progress. It depends on the no. of flipflops 'N' used . For 'N' no of flipflops used modulus or MOD is , MOD $=2^N$.

For MOD 11 counter , 4 flipflops are required .

k) What is flash memory?

Ans:- (Relevant explanation- 2 mks)

Flash Memory:-

- Flash memory is non-volatile RAM memory that can be electrically erased and reprogrammed.
- Flash memory can be written to in block size rather than bytes, it is eaiser to update it.
- Due to this, the flash memories are faster than EEPROMS which erase and write new data of byte level.
- This type of memory has been named as `flash memory ` because a large block of memory could be erased at one time, i.e in a single action or `flash`.
- Important features are high speed, low operating voltage low power consumption.
- Typically applications areas are digital camera`s embedded controllers, cellular phones etc.

l) Define resolution and linearity of DAC.

Ans:- (Each relevant definition- 1 mks)

Resolution:-

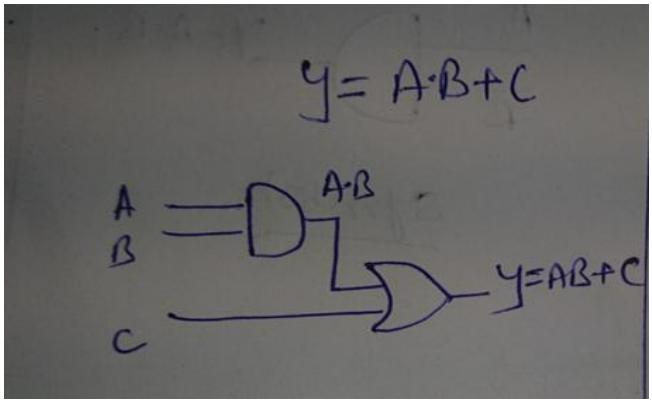
It is defined as the smallest possible change in the output voltage as a fraction or percentage of the full scale output range it can be produced by a single step change in digital input.

Linearity: -

In DAC converters, equal increments in the numerical significance of the digital input should result in equal increment in the analog output voltage. In a actual circuit, the input output relationship is not linear. This is due to the error in the resistor values and voltage across the switches. The linearity of the converter is a measure of the precision with which the linear input output relationship is satisfied.

m) Implement given logical equation using gates Y=AB+C.

Ans:- (Proper implementation- 2 mks)



n) Define accuracy and settling time w. r. to DAC.

Ans:- (Each proper definition- 1 mks)

Accuracy:-

The accuracy of DAC is a measure of difference between the actual output as a percentage of full scale or maximum output voltage.

Setting time or DAC speed:-

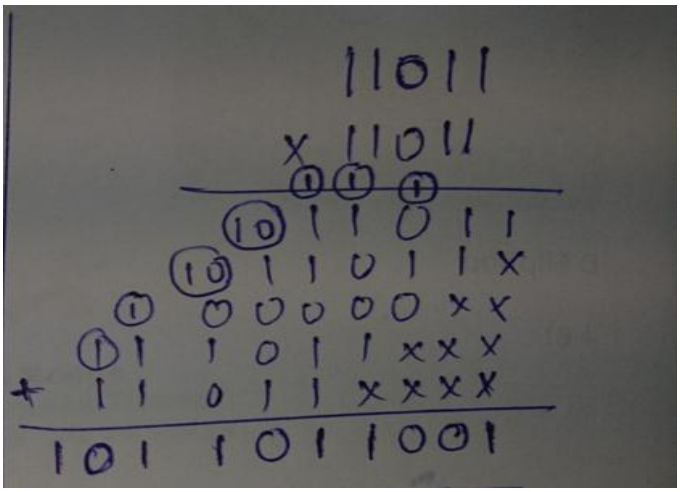
The operating speed of a DAC is usually specified by giving its setting time which is the time required for the DAC output to go from zero to full scale as the binary input is changed from 0 s to all 1s. Actually the setting time is measured as the time for the DAC output to settle within ±½ step size of its final value.

2 . Attempt any FOUR of the following 16

a) Perform the following:

$(11011)_2$ * $(11011)_2$

Ans:- (Proper solution – 4 mks)



b) State the rules for BCD addition explain with example.

Ans:- (Rules- 2mks)

1. Add the two BCD numbers.
2. If the sum is less or equal to 9, it is valid BCD result.
3. If the result is more than 9 or a carry is generated then add 6 (i.e. binary 0110) to the sum to make it a valid BCD result.

Example (any one)- 2 mks

i) $(37)_{10} + (65)_{10}$

0011 0111
0110 0101
1001 1100
0110 0110 [add 6 ie 0110 to each digit ie 4 bits.]
0001 0000 0010

ie $(102)_{10}$.

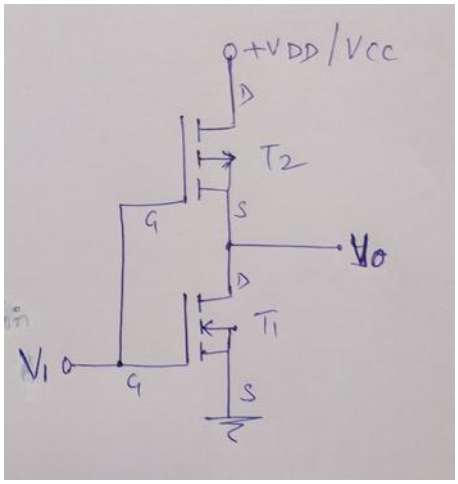
ii) $(45)_{10} + (24)_{10}$

0100 0101
+ 0010 0100
0110 1001

ie $(69)_{10}$.

c) Draw and explain the working CMOS invertor with circuit diagram.

Ans:- (Diagram – 2 mks, Explanation- 2 mks)



Description:-

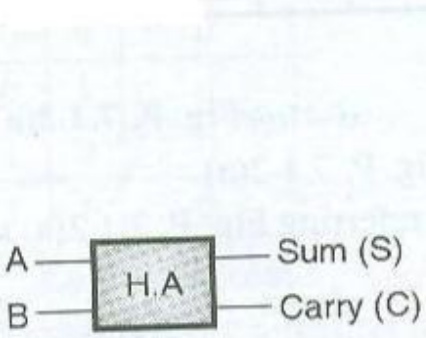
The basic CMOS logic circuit is an inverter shown in fig. For this circuit the logic levels are 0V (logic 0) and V_{cc} (logic 1). When $V_1 = V_{cc}$, T_1 turns ON and T_2 turns OFF. Therefore $V_0 \approx 0V$, and since the transistors are connected in series the current I_D is very small. On the other hand, when $V_1 = 0V$, T_1 turns OFF and T_2 turns ON giving an output voltage $V_0 \approx V_{cc}$ and I_D is again very small. In either logic state, T_1 or T_2 is OFF and the quiescent power dissipation which is the product of the OFF leakage current and V_{cc} is very low. More complex functions can be realized by combinations of inverters.

d) Design Half adder using K Map and implement using Gates.

Ans:-

[1M for Truth table; 1M for K- Map;1M for expression; 1M for Ckt. Diagram]

1. Half adder is a combinational logic circuit with two inputs and two outputs. It is the basic building for block for addition of two single bit numbers. This circuit has two outputs namely carry and sum.'
2. The half adder circuit is designed to add single bit binary numbers A and B.

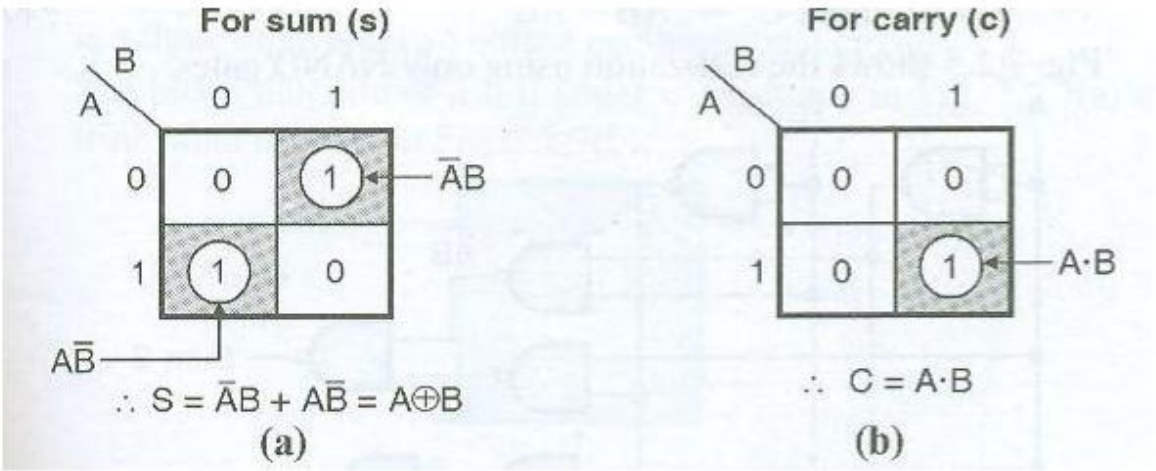


(a) Block diagram

		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(b) Truth table

Design using K- Map



Simplified **expressions** for two outputs are:

$$S = \bar{A}B + A\bar{B} = A \oplus B$$
$$C = AB$$

Hence the half adder circuit is as shown in Fig. 7.2.3.

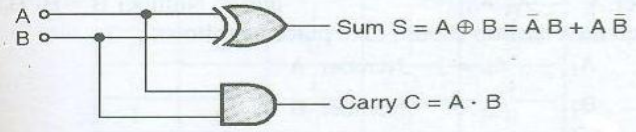


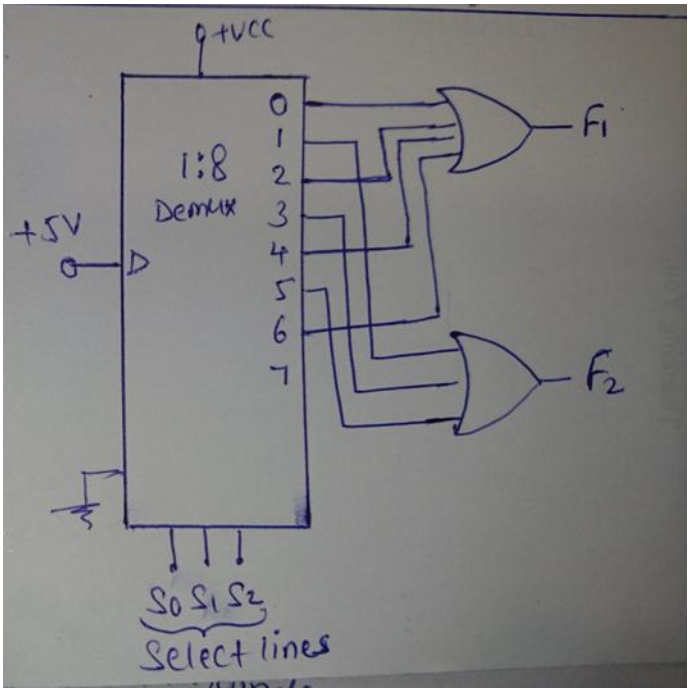
Fig. : Half adder circuit

e) Realize

F1 = Σm (0, 2, 4, 6)

F2 = Σm (1, 3, 5) using Demultiplexer.

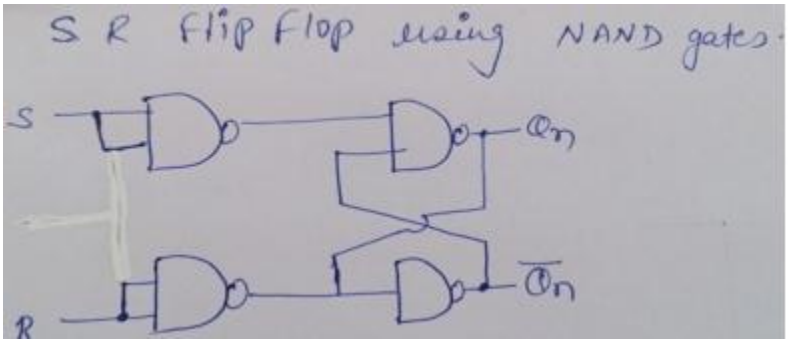
Ans:- (Each realisation- 2 mks)



f) Draw and explain S. R. and FlipFlop using NAND gate along with truth table.

Ans:- (Diagram- 2 mks, truth table – 1 mks, explanation-1 mks)

Description-



Truth table

S	R	Q_{n+1} (O/P)
0	0	Q_n (No change)
0	1	0
1	0	1
1	1	Not allowed

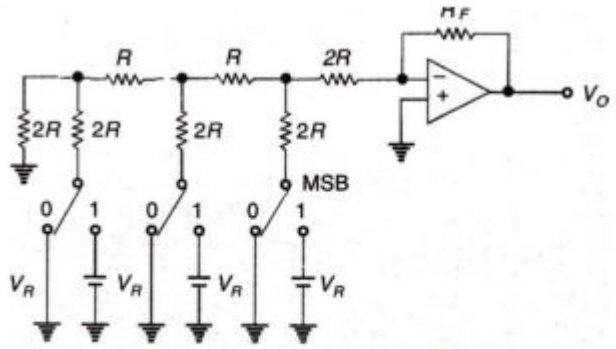
Description/explanation- As shown in the truth table,

For both inputs S=R= 0, o/p of flipflop remains unchanged.
For S=0, R=1, o/p of flipflop resets (Q=0)
For S=1, R=0, o/p of flipflop sets (Q=1)
For S=R=1, o/p of flipflop is forbidden or not allowed as Q=$\bar{Q}$.

3. Attempt any FOUR of the following: 16

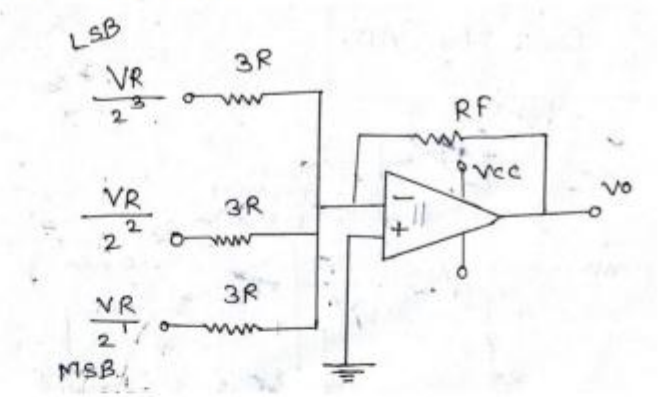
a) Draw and explain working of R-2R DAC.

Ans:- (Diagram – 2mks, explanation-2 mks)



3 bit R-2R ladder network DAC

Mathematical derivation for Digital input 101:-



Equivalent 3 bit R-2R DAC
Where VR is the reference voltage
RF is the feedback resistor
3R is equivalent input resistance in each case

$$V_o = -\left(\frac{R_F}{3R}\frac{V_R}{2^3}b_0 + \frac{R_F}{3R}\frac{V_R}{2^2}b_1 + \frac{R_F}{3R}\frac{V_R}{2^1}b_2\right)$$

$$V_o = -\frac{R_F}{3R}\frac{V_R}{2^3}\left[b_0 + 2b_1 + 4b_2\right]$$

given $i/p = 101 \therefore \boxed{b_0 = 1, b_1 = 0, b_2 = 1}$

$$V_o = \frac{-R_f}{3R}\frac{V_R}{2^3}\left[1 + 0 + 4\right]$$

$$\boxed{V_o = 5\left[\frac{-R_f}{3R}\frac{V_R}{2^3}\right]}$$

b) State different type of ROM and explain any one.

Ans:- (Types- 2 mks, any one explanation-2 mks)

There are five basic ROM types:

1. ROM - Read Only Memory.
2. PROM - Programmable Read Only Memory.
3. EPROM - Erasable Programmable Read Only Memory.
4. EEPROM - Electrically Erasable Programmable Read Only Memory.
5. Flash EEPROM memory.

Flash Memory:-

1. Flash memory is non-volatile RAM memory that can be electrically erased and reprogrammed.
2. Flash memory can be written to in block size rather than bytes; it is easier to update it.
3. Due to this, the flash memories are faster than EEPROMS which erase and write new data of byte level.
4. This type of memory has been named as 'flash memory' because a large block of memory could be erased at one time, i.e. in a single action or 'flash'.
5. Important features are high speed, low operating voltage low power consumption.
6. Typically applications areas are digital camera's embedded controllers, cellular phones etc.

OR

OR

Programmable Read Only Memories (PROM):-

PROM is electrically programmable i.e. the data pattern is defined after final packaging rather than when the device is fabricated. The programming is done with an equipment referred to as PROM programmer. The PROM are one time programmable. Once programmed, the information stored is permanent.

OR

Erasable Programmable Read Only Memories (EPROM):-

In these memories, data can be written in any number of times i.e. they are reprogrammable . Reprogrammable ROMs are possible only in MOS technology. For erasing the contents of the memory, one of the following two methods are employed:

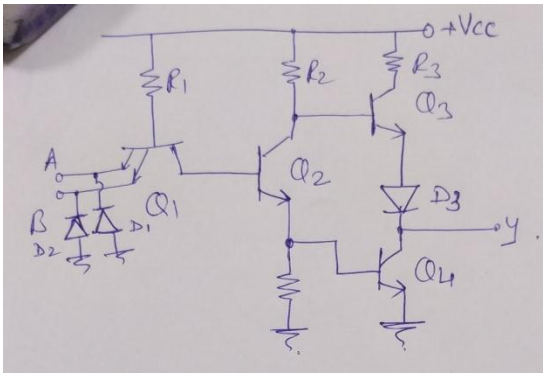
a) Exposing the chip to ultraviolet radiation for about 30minutes (UVEPROM)
b) Erasing electrically by applying voltage of proper polarity & amplitude. Electricity erasable Prom is also referred to as E^2PROM or EEPROM or EAROM (Electrically alterable ROM)

In this data is stored in the form of charge.

c) Draw circuit diagram of TTL NAND gate and explain its working.

Ans:- (Diagram- 2 mks, truth table- 1 mks, explanation- 1 mks)

Inputs		Y
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0



Operation-

1. A and B both LOW (A = B =0):

- If A and B both are connected to ground, then both the B- E junctions of transistors Q1 are forward biased.
- Hence diodes D1 and D2 will conduct to force the voltage at point C to 0.7 V.
- This voltage is insufficient to forward bias base emitter junction of Q2. Hence **Q2 will remain OFF.**
- Therefore its collector voltage Vx rises to Vcc.
- As transistor Q3 is operating in the emitter follower mode, output Y will be pulled up to high voltage. **Therefore, Y =1 (HIGH) …..For A =B= 0 (LOW)**

2. Either A or B LOW (A =0, B=1 or A=1, B=0):

- If any one input (A or B) is connected to ground with the other terminal left open or connected to +Vcc, then the corresponding diode (D1 & D2) will conduct.
- This will pull down the voltage at "C" to 0.7 V.

This voltage is insufficient to turn ON **Q2. So it remains OFF.**
So collector voltage Vx of Q2 will be equal to Vcc, voltage acts as base voltage for Q3.
As Q3 acts as an emitter follower, output Y will be pulled to Vcc.
Y= 1 ---- if A=0 and B=1 -----if A=1 and B=0

3. A and B =1

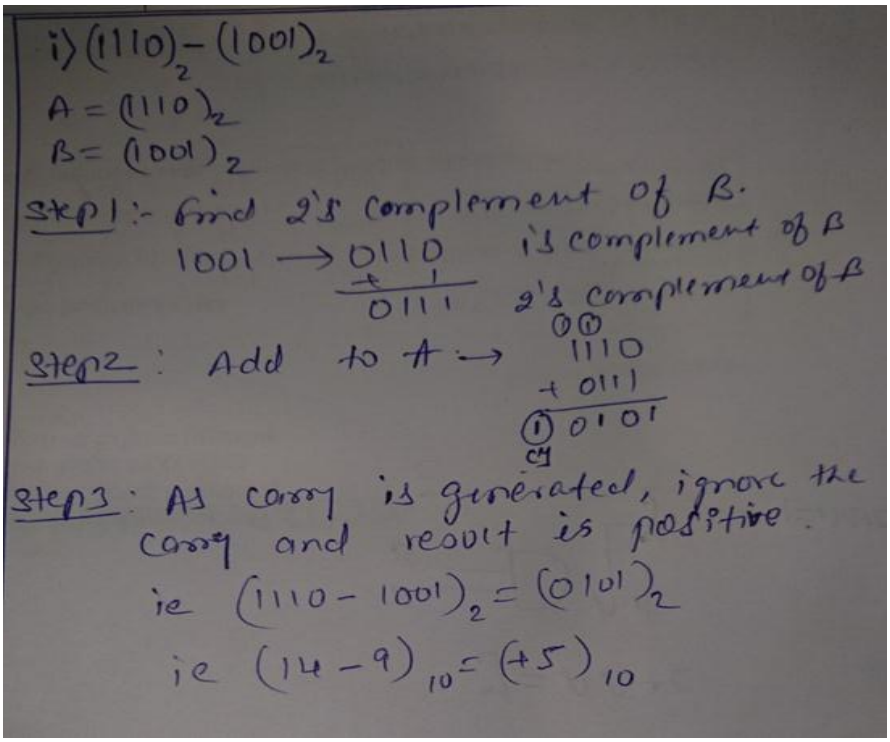
- If A and B both are connected to +Vcc, then both the diodes D1 & D2 will be reverse biased and do not conduct.
- Therefore diode D3 is forward biased and base current is supplied to transistor Q2 via R1 and D3.
- As Q2 conducts, the voltage at X will drop down and **Q3 will beOFF,** whereas voltage at Z (across R3) will increase **to turn ON Q4.**
- As Q4 goes into saturation, the output voltage Y will be pulled down to a low voltage, **Y=0.**

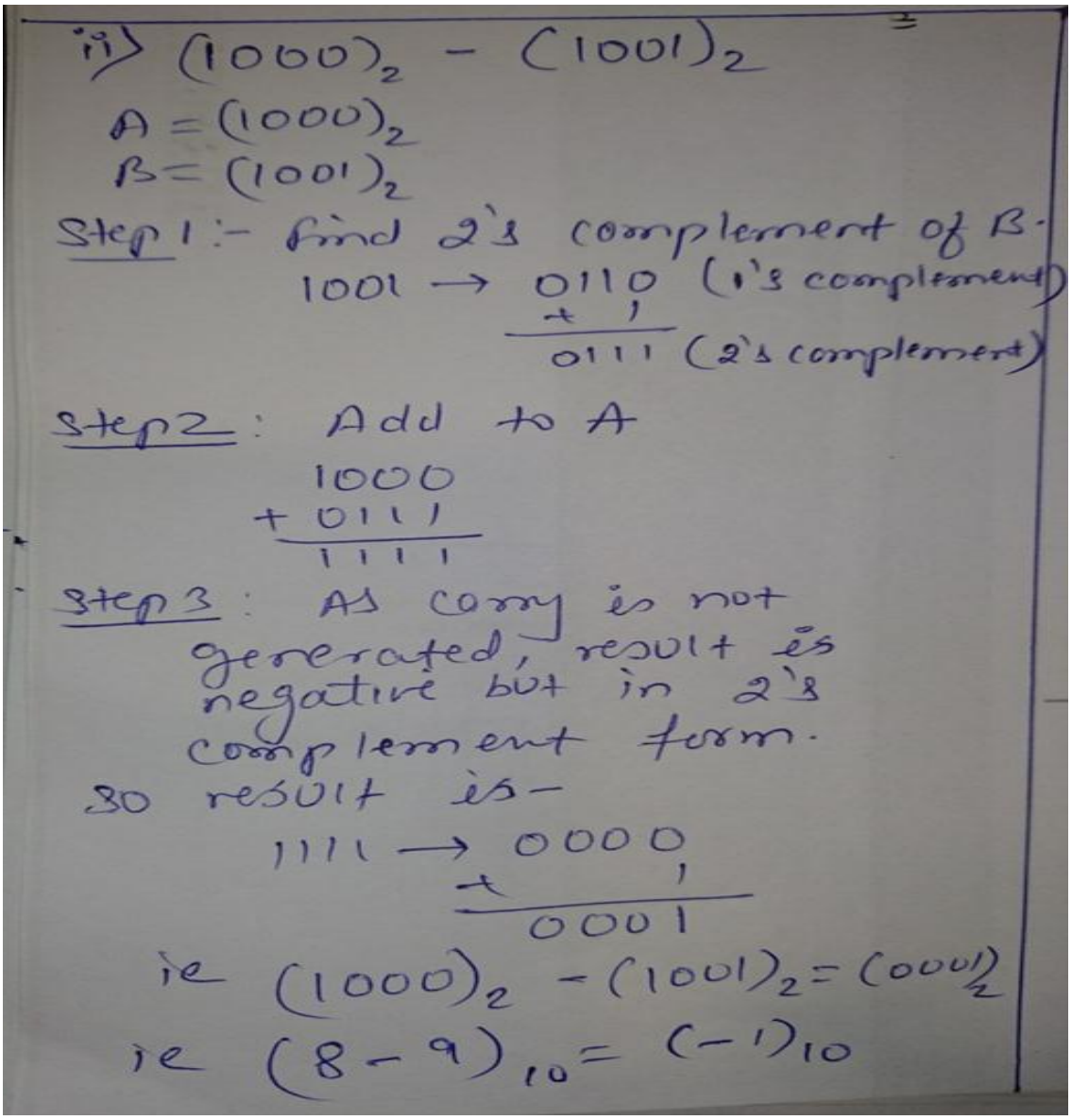
d) Subtract using 2's complement method

(i) $(1110)_2 - (1001)_2$

(ii) $(1000)_2 - (1001)_2$

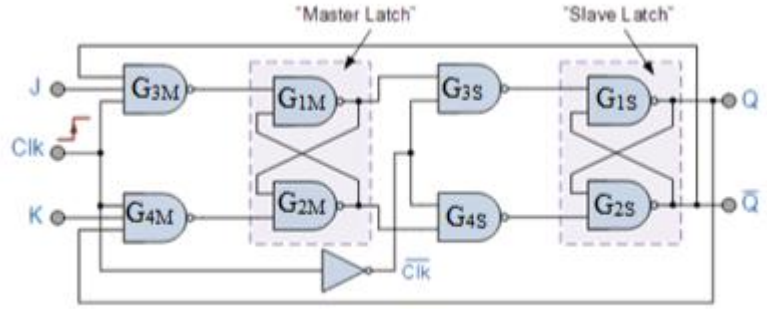
Ans:- (Each proper stepwise solving- 2 mks each)





e) Draw Master Salve JF FlipFlop and write its truth table.

Ans:- (Diagram- 2 mks, truth table- 2 mks)

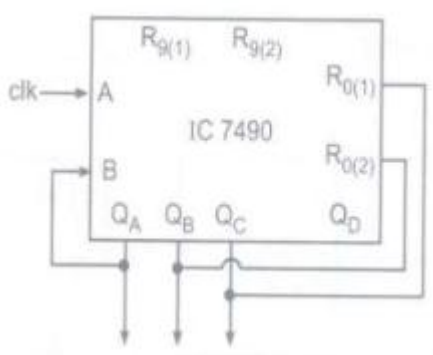


Truth Table

CLK	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q}n$

f) Design MOD-6 Counter using IC 7490 and write its truth table.

Ans:- (Diagram- 2 mks, Truth table- 2 mks)



To reset the counter after counting the first six states from 0 to 5, the counter outputs Q_c and Q_B should be connected to the reset inputs.

Truth Table

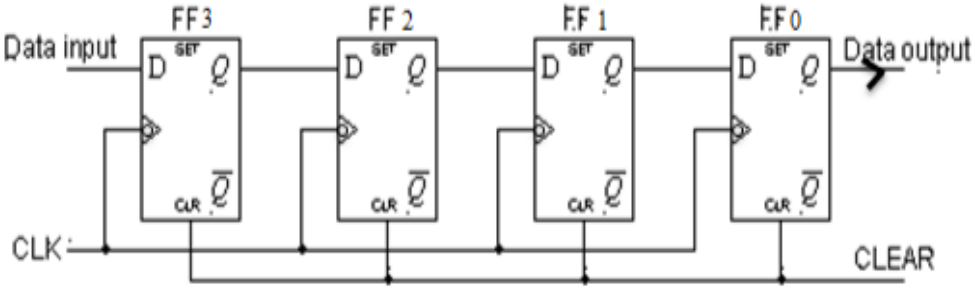
State	Q_C	Q_B	Q_A	Output Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	0	0	0	0

4. Attempt any FOUR of the following: 16

a) Describe working of SISO shift Register with proper circuit diagram.

Ans:- (Diagram- 2 mks, truth table 1 mks, describe/explain in short – 1 mks,waveform not compulsory, can be considered)

Diagram:-4 bit Serial in serial out shift register (Right shift)

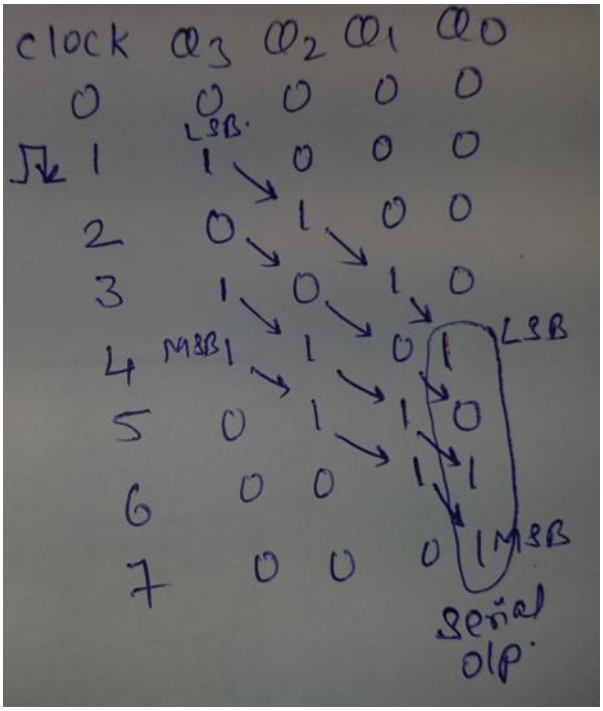


Description-As shown a 4 bit SISO shift register consists of 4 D flipflop , data is fed from first flipflop and on application of clock pulses the data is shifted from first flipflop to the last flipflop ,working as serial in and serial out shift register.

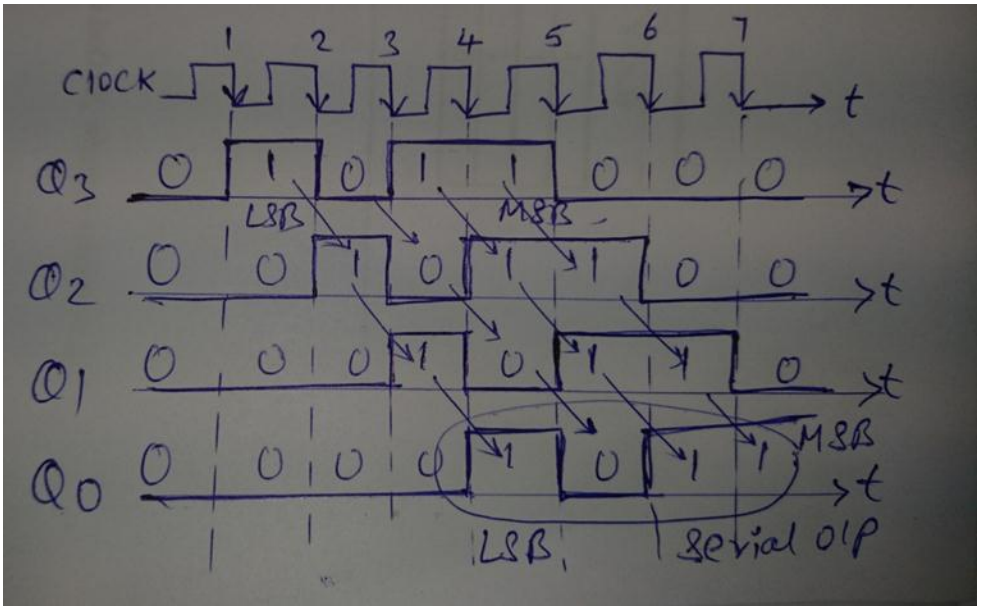
Let the data be -1101.

The truth table and timing diagram (optional) is as shown below-

Truth Table



Timing diagram-(optional)



b) Compare combinational and sequential circuit. (Four points)

Ans:- (Any 4 relevant comparison- 4 mks)

PARAMETERS	COMBINATIONAL CIRCUIT	SEQUENTIAL CIRCUIT
Definition	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
Need of Memory	No memory element required in the ckt	Memory element required to stored bit
Need of clock	Clock input not necessary	Clock input necessary
Examples	E.g. Adders, Subtractors ,Code converters, comparators etc.	E.g. Flip flop, Shift registers, counters etc,
Applications	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

c) Compare :

(i) Volatile with Non-Volatile memory.

(ii) SRAM with DRAM memory.

Ans:- Volatile with Non-Volatile memory (any 2 points-2 mks)

Sr No.	Parameter	Volatile	Non-volatile
1.	**Definition**	Information stored is lost if power is turned off	Information stored is not lost even if power goes off
2.	**Classification**	All RAMs	ROMs, EPROMs
3.	**Effect of power**	Stored information is retained only as long as power is ON	No effect of power on stored information
4.	**Application**	For temporary storage of data.	For permanent storage of data.
5.	**Devices used**	Volatile memory devices are mainly solid state devices	Nonvolatile memory can be sold state, magnetic or optical
6.	**Speed**	Volatile memory is very fast in data processing	Nonvolatile memory is slow in data processing as compared to volatile.

SRAM with DRAM memory (any 2 points- 2 mks)

SR. NO.	PARAMETER	STATIC RAM	DYNAMIC RAM
1.	**Components**	Flip-flops, using bipolar or MOS transistors are used as basic memory cell.	Flip flops using MOS transistors& parasitic capacitance are used.
2.	**Refreshing**	Not required	Required as charge leaks
3.	**Speed**	Access time is less hence these are faster memories.	Access time is more hence these are slower memories.

d) Explain working of single slope ADC with diagram.

Ans:- **[2 mks diagram;2 mks explaination]**

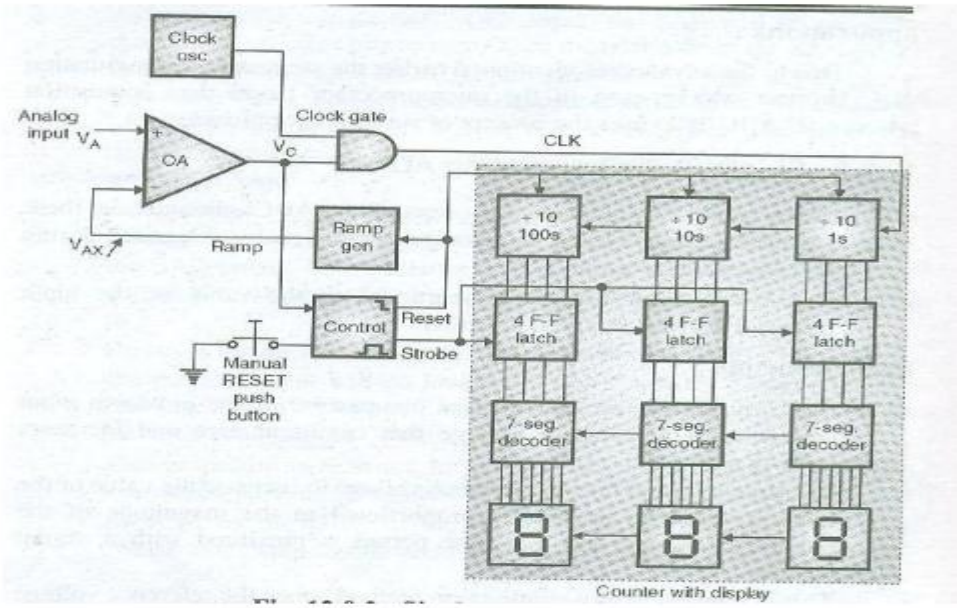


Fig: Single slope A/D converter

Operation:

Manual RESET, will reset ramp generator as well as counter.V_A has to be positive. RAMP begins at 0V.

As $V_{AX} < V_A, V_C = 1$ (HIGH). This will enable CLOCK gate allowing the CLK input, to be applied to the counter.

The ramp generator may be of two types.

(a) Using DAC : This will resemble with counter-ramp ADC.

(b) Using a sample integrator : For integrator, if V_i is constant, the output voltage is given by equation $V_O = (V_i / RC)$. Since V_i, R and C are all constants, this is the equation of a straight line that has a slope (V_i / RC).

As counter receives clock pulses, it will count up; and the RAMP continues upward.

RAMP voltage rises till it reaches to V_A input voltage.

At this point, time t_1, output $V_O = 0$(LOW) and it will disable CLOCK gate and counter cease to advance.

The negative transition of V_O, simultaneously generates a strobe signal in the CONTROL box that shifts the contents of the three decade counters into the three 4 FF latch circuit,

Shortly after that, a reset pulse is generated (time t_2), by the CONTROL box that resets the RAMP and clears the decade counter to all 0's (ZEROS) and another conversion cycle begins.

In the meantime the contents of the previous conversion are contained in the latches and are displayed on the seven segment display.

e) Identity the given circuit and explain its working . (Refer Figure No. 1)

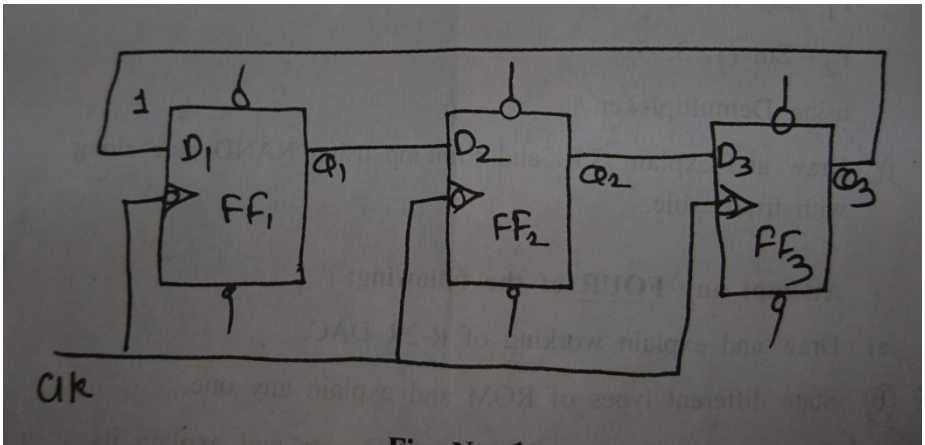
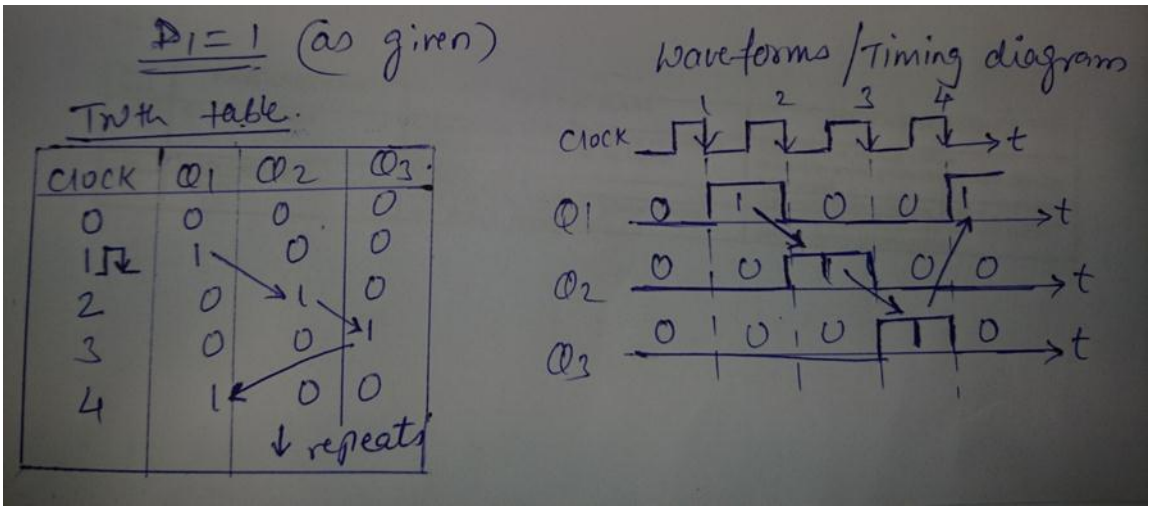


Fig. No. 1

Ans :- (Identification- 2 mks, operation with truth table as working – 2 mks)

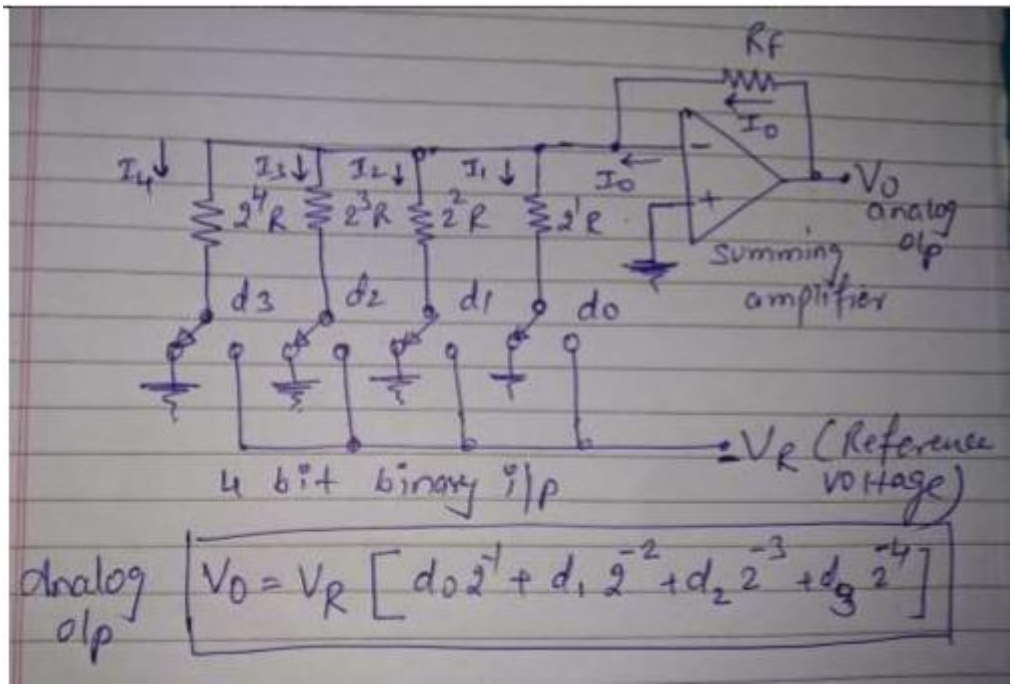
Identification- The given circuit is Ring Counter .

Operation- As shown D1=1, with clock pulses applied the data '1' shifts as shown in the truth table- (waveforms are optional, can be considered)



f) Draw and explain working of 4-bit Weighted Register DAC Circuit.

Ans:- (Diagram- 2 mks, explanation-2 mks)



Operation:

- Fig. above shows logic circuit of binary weighted resistor type DAC.
- It uses a network of binary weighted resistor and op-amp summing amplifier.
- The resistors are 2^1 R=2R, 2^2 R=4R,…. 2^n R are from the network of binary weighted resistors.
- There is n. number of electronically controlled switches used one per digit bit.

- They are SPDT type switches.
- The required output voltage equation
- $V_0 = V_R (d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots + d_n 2^{-n})$

Expression for output voltage:

$$V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}]$$

Where, V_0= Analog output voltage

$d_1, d_2 \ldots\ldots d_n$ are n bit digital input word with d_1 as MSB and d_n as LSB.

V_R= Reference voltage.

5. Attempt any FOUR of the following: 16

a) Compare TTL logic family with CMOS w.r.t. to

(i) Propagation delay.

(ii) Power dissipation

(iii) Fan-out.

(iv) Basic gate

Ans:- **[1 M for each point]**

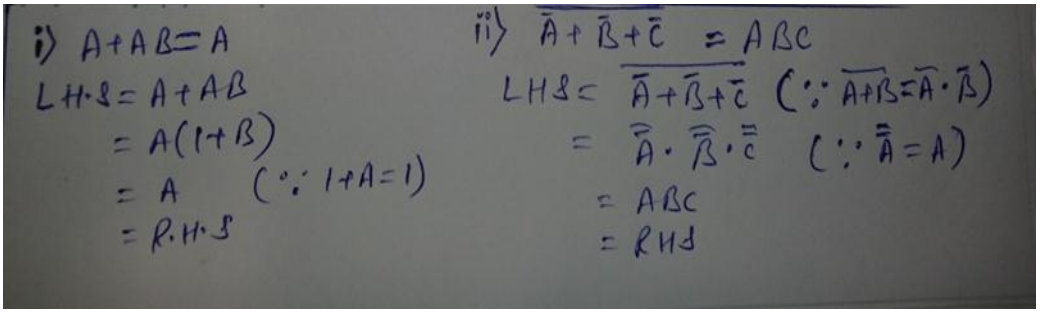
Parameters	CMOS	TTL
Propagation delay	105 nsec	10 nsec
Power dissipation per gate	0.1 mW	10 mW
Fan out	More than 50	10
Basic Gates	NAND/NOR	NAND

b) Prove :

(i) A + AB = A

(ii) A + B + C = ABC

Ans:- (Each proper solution – 2mks)

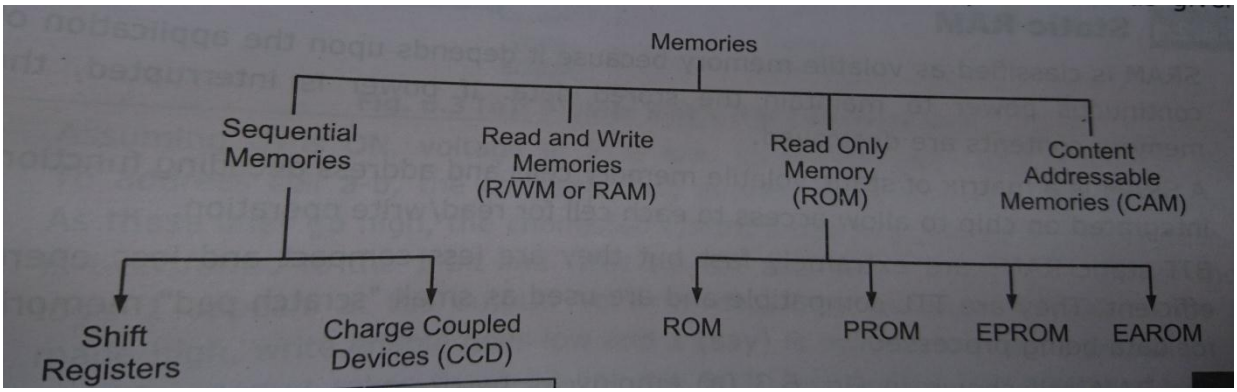


c) Classify memories and Identify the IC

(i) IC 2716

(ii) IC 7481

Ans:- (Classification- 2 mks, identification- 1 mks each)

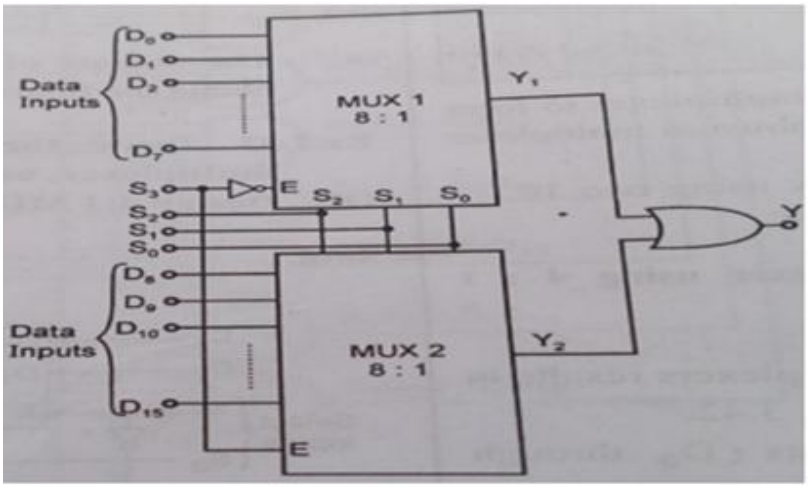


Identification

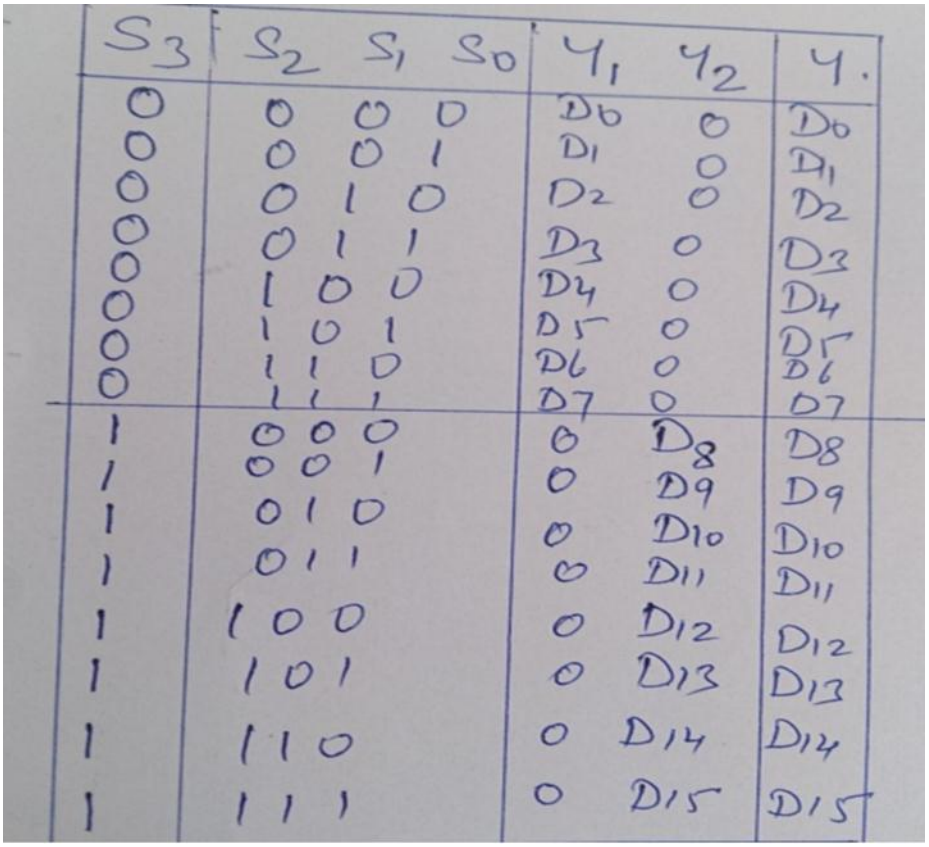
IC 2716- 16K bit, UV EEPROM
IC 7481-16 bit Bipolar RAM

d) Design and draw 16:1 MUX using 8:1 MUX (Multiplex).

Ans:- (Diagram- 2mks, truth table-2 mks)



Truth table

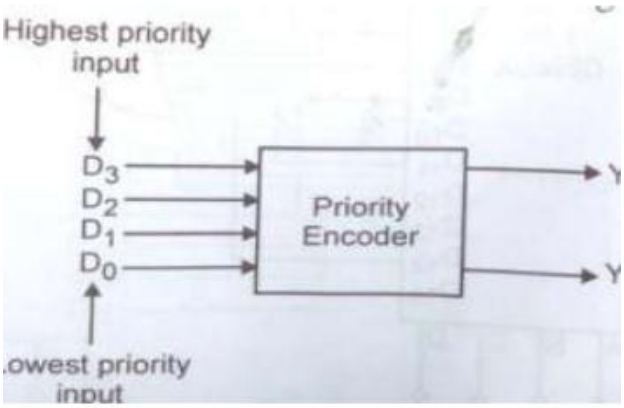


S_3	S_2	S_1	S_0	Y_1	Y_2	Y
0	0	0	0	D_0	0	D_0
0	0	0	1	D_1	0	D_1
0	0	1	0	D_2	0	D_2
0	0	1	1	D_3	0	D_3
0	1	0	0	D_4	0	D_4
0	1	0	1	D_5	0	D_5
0	1	1	0	D_6	0	D_6
0	1	1	1	D_7	0	D_7
1	0	0	0	0	D_8	D_8
1	0	0	1	0	D_9	D_9
1	0	1	0	0	D_{10}	D_{10}
1	0	1	1	0	D_{11}	D_{11}
1	1	0	0	0	D_{12}	D_{12}
1	1	0	1	0	D_{13}	D_{13}
1	1	1	0	0	D_{14}	D_{14}
1	1	1	1	0	D_{15}	D_{15}

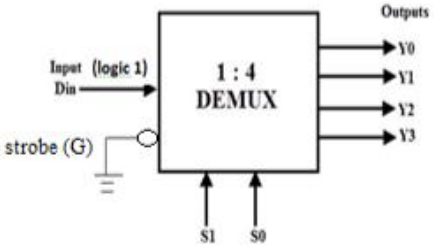
e) What is priority encodes? How is Demultiplex used as Decoder?

Ans:- (Priority encoder, diagram can be considered -2 mks, Demux as decoder-2mks
for diagram)

A priority encoder is a special type of encoder that responds to just one input accordance with some priority system among all those that may be applied simultaneously high. For two or more inputs are '1' at the same time, then input with highest priority will be considered.



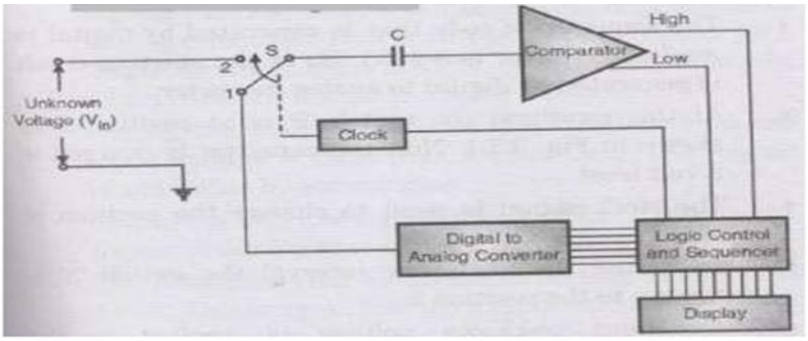
De-Mux used as Decoder:-



One of the applications of a De-Mux is that it can be used as a decoder.
Let us see how to operate a 1:4 De-Mux as a 2:4 Decoder.
The connections are to be made as shown in the figure above.
The data input Din is connected to logic 1 permanently. The two select (lines) inputs S_1, S_0 will act as the 2 input lines of the decoder & Y_0-Y_3 are the 4 output lines of the decoder.

f) Draw block diagram of successive approximation type ADC and write its advantages

Ans:- (Block diagram- 2 mks, 2 advantages- 2 mks)



Advantages (any 2)

1. High speed of conversion
2. Produce n bit of A to D conversion with only n clock pulses.
3. Constant conversion time.

6 . Attempt any FOUR of the following 16

a) Compare weighted resistor and R-2R methods of DAC.

Ans:- (Relevant 4 points- 4 mks)

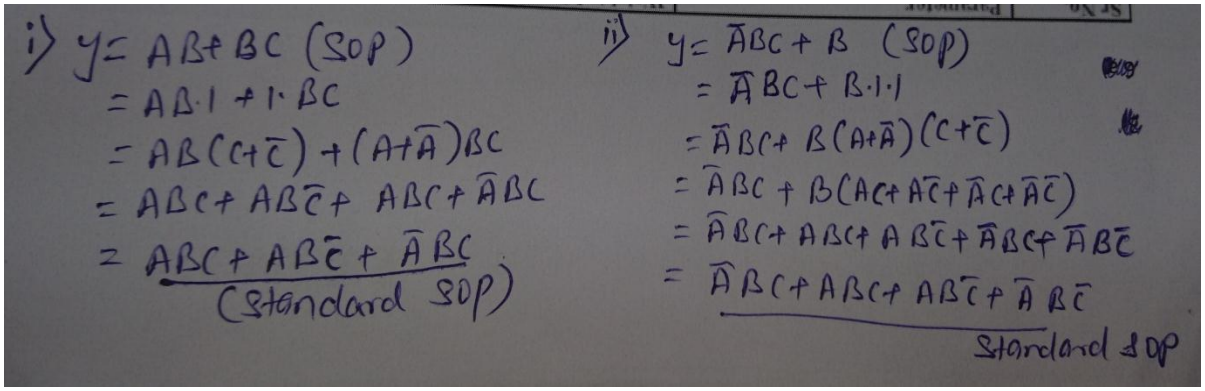
Sr No.	Parameter	Weighted Resistor	R-2R Ladder Network
1.	Simplicity	Simple	Slightly complicated
2.	Range of resistor values	Wide range is required	Resistors of only two values are required
3.	Number of resistors per bit	One	Two
4.	Ease of expansion	Not easy to expand for more number of bits	Easy to expand

b) Write std SOP equation of given logical equation.

(i) Y = AB + BC

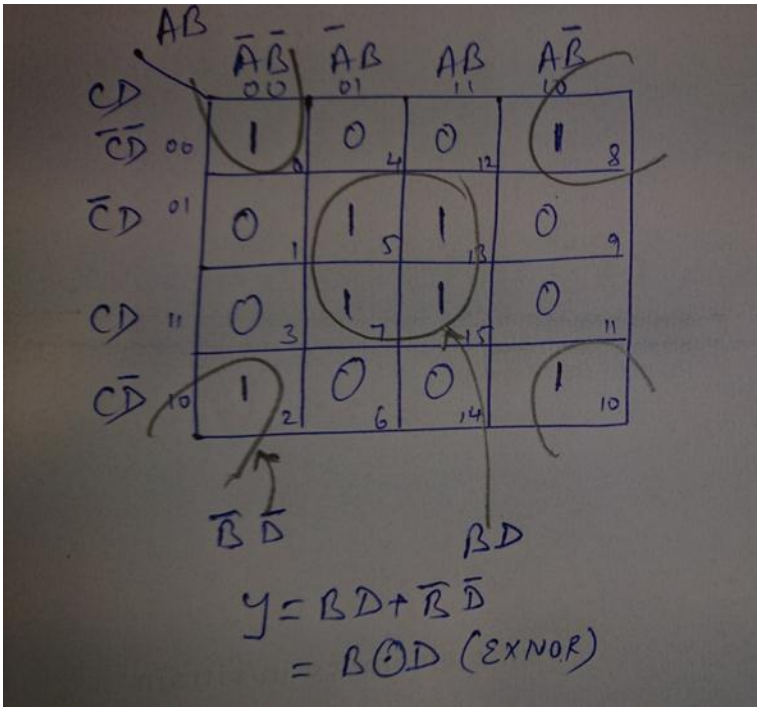
(ii) Y = ABC + B

Ans:-(Each conversion and proper answer -2 mks each)



c) Minimize y = Σm (0, 5, 2, 8, 7, 10, 15, 13) using k-map.

Ans:- (Proper K-map with correct minimized equation- 4 mks)



d) Write Advantages of MUX and DEMUX .State their applications.
Ans:- (2 advantages of MUX and DEMUX- 2 mks, 2 applications of MUX- 1 mks, 2 applications of DEMUX- 1 mks)

(Note – 2 advantages and 2 applications of MUX and DEMUX each can be given separately- 1 mks each)

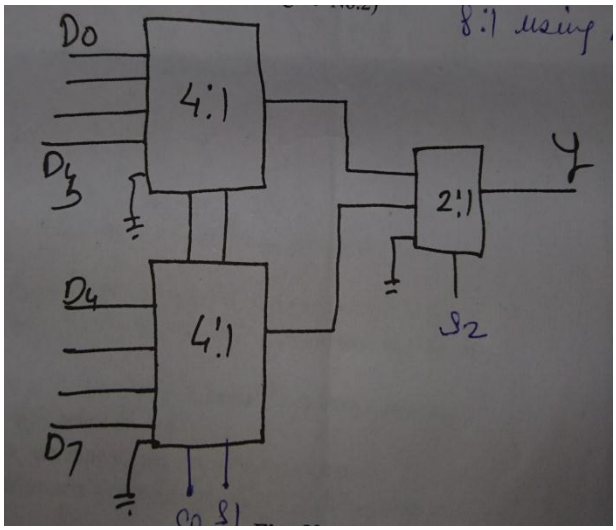
Advantages-

1. It reduces the number of wires.
2. So it reduces the circuit complexity and cost.
3. We can implement many combinational circuits using MUX.
4. It simplifies the logic design.
5. It does not need the k maps and simplification.

Applications-

1. Communication System
2. Computer Memory
3. Telephone Network
4. Transmission from the Computer System of a Satellite
5. TV Cable System

e) Identify the given circuit and write its truth table – Diagram below (Refer Figure No.2)



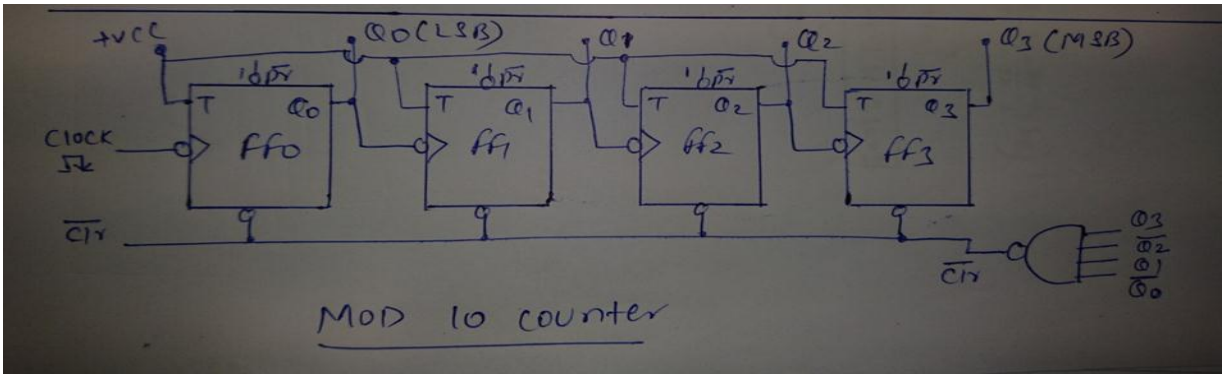
Ans:- (Identification- 2 mks, truth table-2 mks)

The given circuit is a MUX tree - 8:1 MUX using 4: 1 Mux .

Truth Table-

Select lines			O/P
S0	S1	S2	Y
0	0	0	D0
0	1	0	D1
1	0	0	D2
1	1	0	D3
0	0	1	D4
0	1	1	D5
1	0	1	D6
1	1	1	D7

f) (i) Draw circuit diagram of MOD – 10 counter using T-FF.
Ans:- (Proper detailed diagram-2 mks)



(ii) Identify the function of

1) IC – 0800
2) IC – 0890

Ans:- (Proper identification -1 mks each)

IC 0800 – 8 bit ADC IC
IC 0809- 8 bit DAC IC