Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1.a) Attempt any SIX of the following: (Marks 12)

i) **Name different operating region of BJT (any two 1M each)**

Ans:- The different operating regions are namely:

- Active Region
- Saturation Region
- Cut Off Region

ii) Define the term stability factor

Ans:- (Definition 2M, Formula is Optional)

Stability Factor-: It is defined as the rate of change of collector current with respect to reverse saturation current by keeping the common emitter current gain (β) and base current (I_B) as constant.

$$S = dI_C/dI_{Co}$$

iii) List advantages of transformer coupled amplifier (any two)

Ans:- (1M for each advantage)

1. It provides an excellent impedance matching between the two stages.
2. It provides a higher voltage gain than that of RC coupled amplifier.

iv) Define enhancement mode and depletion mode w.r.t. MOSFET.

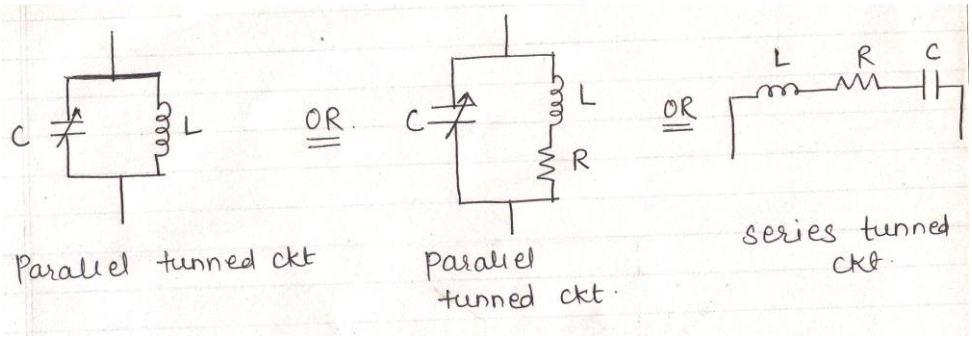
Ans:- **(Enhancement mode 1M , Depletion mode 1M)**

Enhancement mode: The MOSFET operates in this mode with the gate to source voltage is positive in N channel (for P channel V_{GS} is negative) For N-channel with increase in positive gate voltage, drain current starts enhancing.

Depletion mode: The MOSFET operates in this mode with the gate to source voltage is negative in N channel (for P-channel V_{GS} is positive). For N-channel with increase in negative gate voltage channel starts depleting.

v) Draw basic tuned circuit

Ans:-



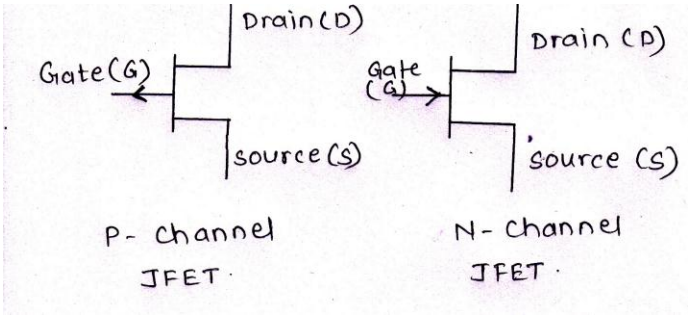
vi) List application of class A amplifier (any two)

Ans: - **(Each application 1M)**

1. It is used where distortionless output is required e.g. audio power amplifier.
2. It is used as voltage amplifier for audio, radio and video frequencies.

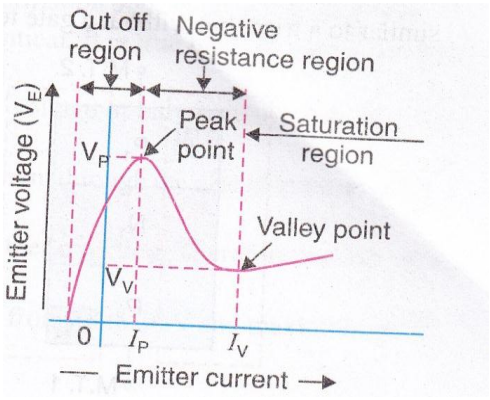
vii) Draw symbol of n-channel and p-channel JFET.

Ans: - **(Each symbol 1M)**



viii) Draw output characteristics of UJT.

Ans:-



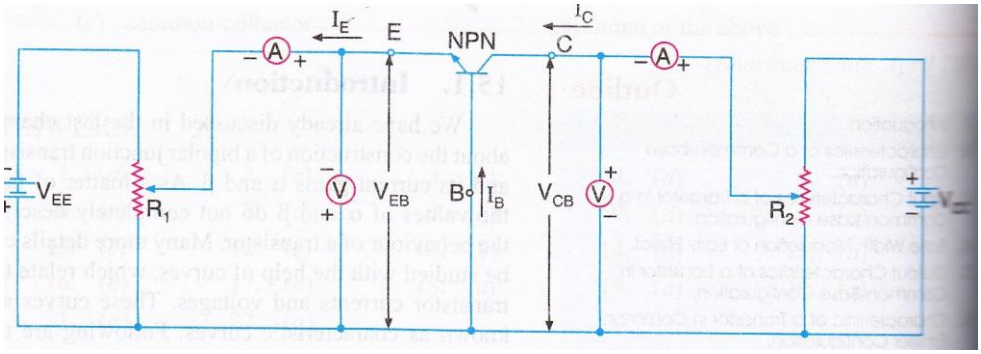
Q1.b) Attempt any TWO of the following: (8M)

i) Draw the ckt diagram for common base configuration and draw its output characteristics

Ans:-

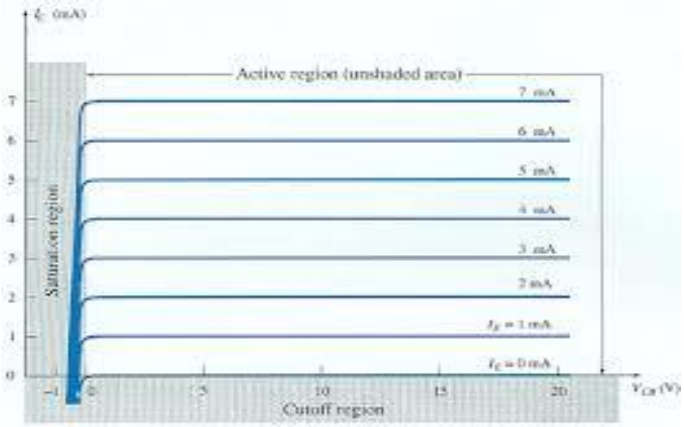
Circuit Diagram for Common base configuration

(2M Circuit diagram,2M Output Characteristics)



(Circuit diagram of PNP can be considered)

Common base configuration output characteristics



ii) Explain need of biasing. List any two methods of biasing.

Ans: - (2M Need of biasing, 1M each method of biasing)

For deciding the location of Q point (operating point)as per the application biasing is used.

E.g.: For faithful amplification Q is selected at the centre of load line by using biasing

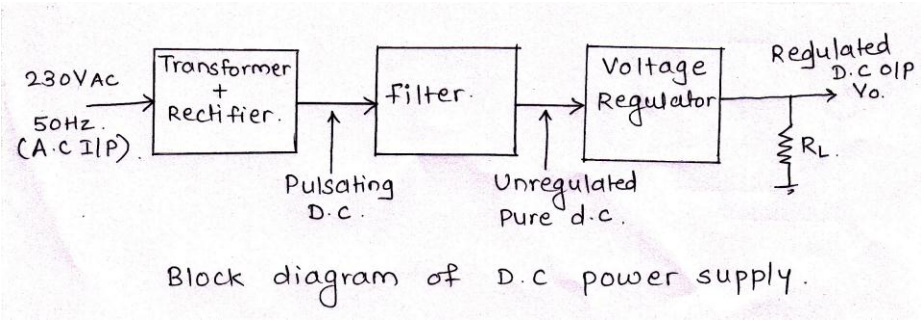
For switch Q point is selected on y-axis (saturation region) & x-axis (cut-off region).

Two Method of biasing: (any 2)

1. Base bias
2. Base bias with emitter feedback
3. Base bias with collector feedback
4. Voltage divider

iii) Draw block diagram of DC power supply and explain function of each block.

Ans:- (2M Block diagram,2M Explanation)



Block diagram of a regulated Dc power supply consist of the following blocks namely:

1) Transformer + Rectifier 2) Filter 3) Voltage regulator.

1. Transformer:- The AC main voltage is applied to a step down transformer. It reduces the amplitude of

ac voltage and applies it to a rectifier.

2. Rectifier: The rectifier is usually Centre tapped or bridge type full wave rectifier. It converts the ac

Voltage into a pulsating dc voltage.

3. Filter: The pulsating dc (or rectified ac) voltage contains large ripple. This voltage is applied to the

Filter circuit and it removes the ripple. The function of a filter is to remove the ripples to provide pure DC voltage at its output. This DC output voltage is not a steady DC voltage but it changes with the change in load current. It has poor load and line regulation. The voltage obtained so is the unregulated DC voltage.

4. Voltage Regulator: The unregulated DC voltage is applied to a voltage regulator makes this DC

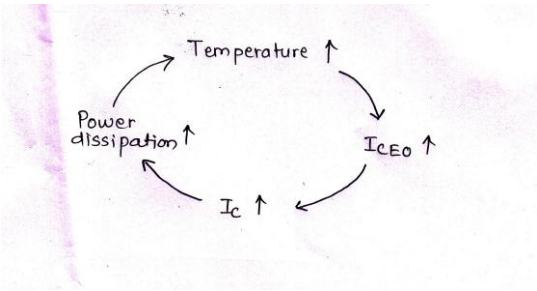
Voltage steady and independent of variation in load and mains AC voltage This improves the load and line regulation and provides the regulated DC voltage Across the load.

Q2) Attempt any FOUR of the following: (16M)

a) Explain thermal runway. How it should be avoided?

Ans: (Thermal Runaway 2M, to avoid Thermal runaway 2M)

Thermal Runaway



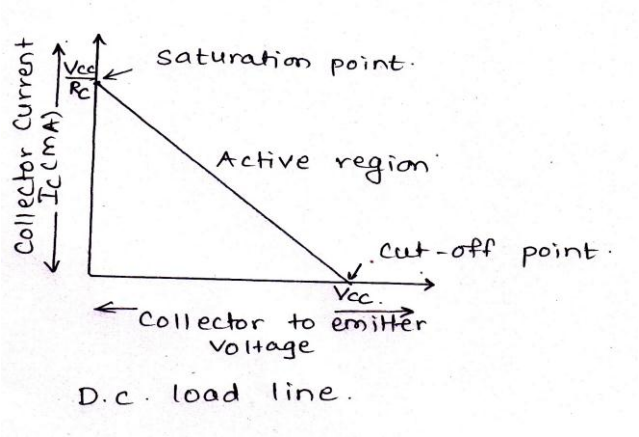
1. The reverse saturation current in semiconductor devices changes with temperature. The reverse saturation current approximately doubles for every 10^0 c rise in temperature.
2. As the leakage current of transistor increases, collector current (Ic) increases
3. The increase in power dissipation at collector base junction.
4. This in turn increases the collector base junction causing the collector current to further increase.
5. This process becomes cumulative. & it is possible that the ratings of the transistor are exceeded. If it happens, the device gets burnt out. This process is known as 'Thermal Runaway'.

Thermal runaway can be avoided by

1) Using stabilization circuitry
2) Heat sink

b) Draw D.C. load of common emitter amplifier and define Q.Point.

Ans:- **(2M diagram,2M definition)**

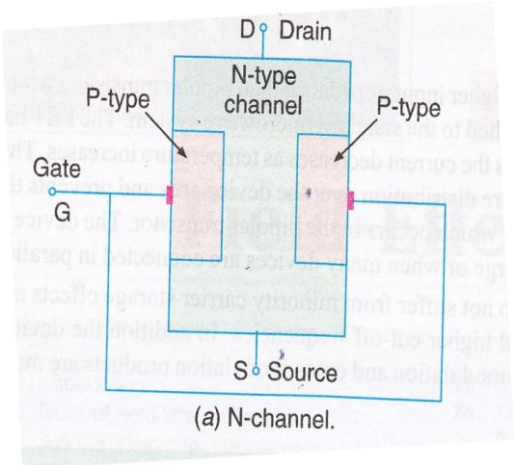


Q point:

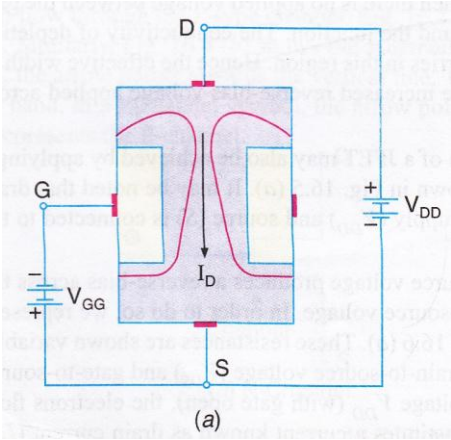
For proper operation of transistor, in any application, we set fixed levels of certain voltages & currents in a transistor. These values of currents & voltages define the point at which transistor operates. This point is called operating point. It is also known as quiescent point or Q point.

c) Draw construction and describe working of n-channel JFET with neat sketch.

Ans:- Construction Diagram: **(1M construction diagram,1M diagram,2M working)**



Working:



1) $V_{GS} = 0V$

When a voltage is applied between the drain & source with a D.C supply voltage (V_{DD}) with $V_{GS} = 0V$,the electrons flows from source to drain through the narrow channel existing between the depletion regions.

This constitutes drain current (I_D). The value of drain current is maximum when $V_{GS} = 0V$. This current is designated by the symbol I_{DSS}

2) When V_{GS} is negative

When V_{GS} is increased above zero, the reverse voltage across the gate source junction is increased. As a result depletion regions are widened. This reduces effective width of channel therefore controls the flow of drain current through the channel.

If V_{GS} increased further, two depletion regions touch each other. The drain current reduces to 0.The gate to source at which drain current reduces to 0 is called as pinch off voltage

d) Compare CB, CE, CC on basis of following points:

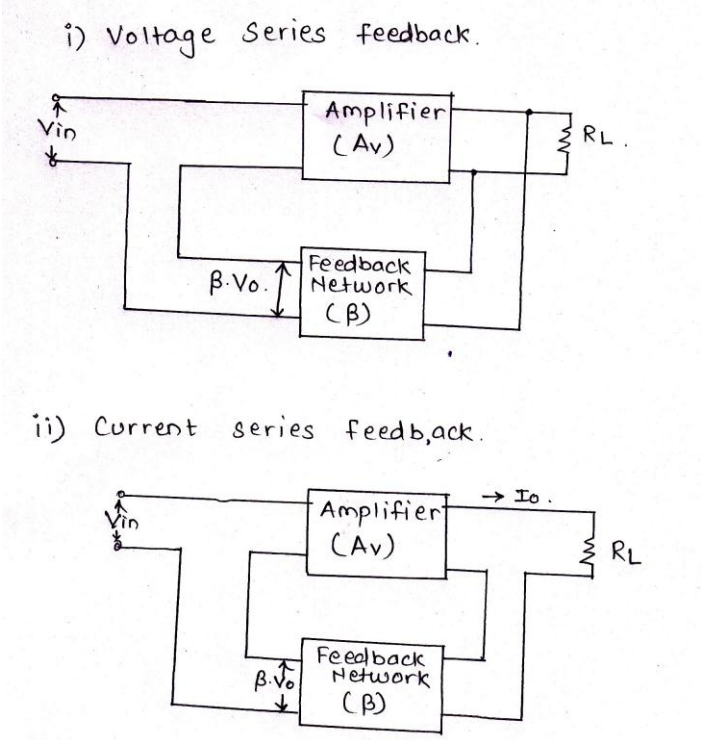
- Input resistance
- Output resistance
- Current gain
- Voltage gain

Ans:-
(1M each point)

Parameter	**CB**	**CE**	**CC**
Input Resistance	50Ω or (Low)	600 Ω to 4K Ω (Medium)	1M Ω or (High)
Output Resistance	500KΩ Or (High)	10K Ω to 50K Ω or (Medium)	50 Ω or (Low)
Current gain	$\alpha = I_c/I_E$ Or (nearly one)	$\beta = I_c/I_B$ Or (High)	$\Upsilon = I_E/I_B$ Or (very high)
Voltage gain	V_{BC}/V_{BE} or (High)	V_{CE}/V_{BE} or (Higher than CB)	V_{CE}/V_{BC} or (Nearly one)

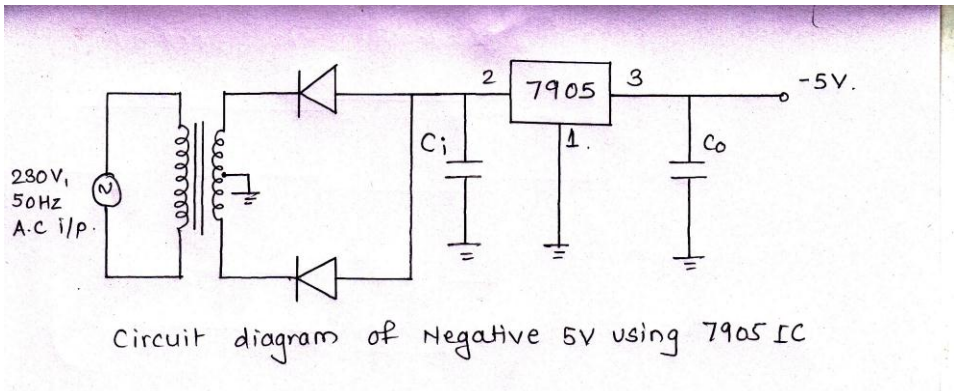
e) Draw block diagram of voltage series and current series feedback.

Ans:- **(2M for Each diagram)**



f) Draw the circuit diagram of negative 5 voltage using 7905 IC. Describe it's working.

Ans:- **(2M for diagram,2M for working)**



Working:

1. A full wave rectifies & capacitor Ci produces the unregulated negative D.C input to the regulator IC.
2. At the output of 7905 we get negative 5 V
3. The capacitor 'Ci' is connected between the input terminal and ground cancel out any inductive effect due to long distribution leads.
4. The output capacitor Co is used for improving the transient response of IC. This capacitor also helps in reducing the noise present at the output due to load variations.

Q3 Attempt any four of the following **(16M)**

a) In Common emitter configuration if β = 150 leakage current I_{CEO}= 100μA and base current is 0.5 mA determine Ic and IE.

Ans:

a.

Given data

$\beta = 150$

$I_{CEO} = 100\ \mu A$

$I_B = 0.5\ mA$

$I_C = ?$, $I_E = ?$

$I_C = \beta \cdot I_B + I_{CEO}$. —— 1Mark

$= 150 \times 0.5 \times 10^{-3} + 100 \times 10^{-6}$

$= 75 \times 10^{-3} + 0.1 \times 10^{-3}$

$I_C = 75.1\ mA$ —— 1 Mark

$I_E = I_C + I_B$ —— 1 Mark

$= 75.1 + 0.5$

$I_E = 75.6\ mA$ —— 1 Mark

b) Describe source self-bias method of FET with neat circuit diagram?

Ans: **Circuit Diagram:2M, Explanation: 2M)**

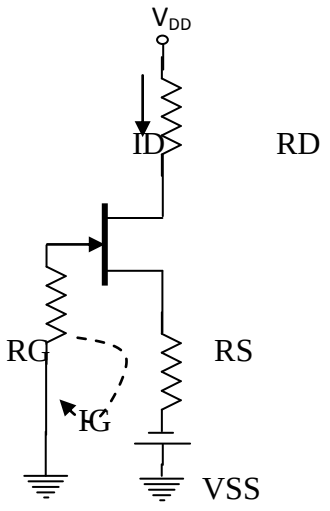


Fig shows the circuit of source biasing for JFET. FET gate is grounded via a resistor R_G. This type of biasing uses ± supply voltages as shown in fig. in this case the circuit behaves as a potential divider bias circuit with V_G equal to V_{SS}

D.C. analysis:-

From the circuit:-

For V_{GS} apply KVL as shown –

$- V_{GS} – I_D R_S + V_{SS} = 0$

$\therefore V_{SS} = V_{GS} + I_D R_S$

$$\therefore V_{GS} = V_{SS} - I_D R_S$$

Expression for V_{DS},

Apply KVL to the drain circuit

$V_{DD} – I_D R_D - V_{DS} – I_D R_S + V_{SS} =0$

$V_{DD} + V_{SS} = I_D (R_D + R_S) + V_{DS}$

$$V_{DS} = V_{DD} + V_{SS} – I_D (R_D + R_S)$$

The value of the drain current can be obtained by Shockley's equation. Thus the Q point of JFET amplifier using source biasing is given by.

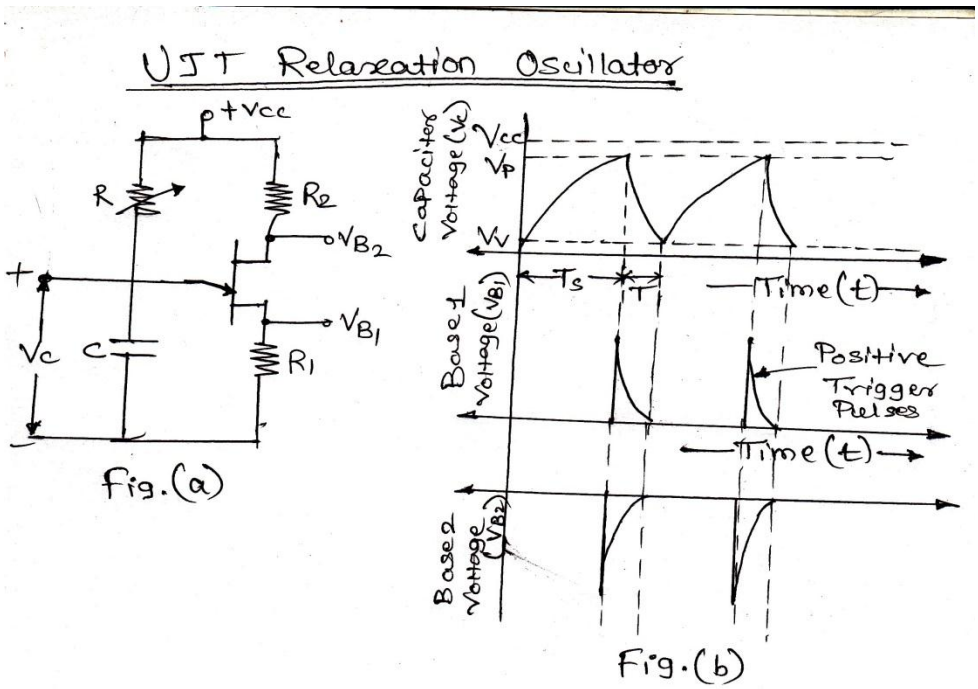
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{DS(off)}} \right)^2$$

$$V_{DS} = V_{DD} + V_{SS} – I_D (R_D + R_S)$$

c) Describe UJT as a relaxation oscillator with neat circuit diagram.

Ans: **(1m for circuit diagram, 1m for waveform and 2 m for explanation)**

Fig (a) below shows circuit diagram of UJT relaxation oscillator and Fig. (b) shows its waveforms.



Circuit Operation:

When the supply voltage VCC is switched ON, the capacitor C charges through resistor R till the capacitor voltage reaches the voltage level V_P which is called as *peak point voltage.*
At this voltage, the UJT turns ON; as a result of this capacitor C discharges rapidly through resistor R.
When the capacitor voltage drops level (called *valley-point voltage*) the UJT switches OFF, allowing capacitor C to charge again.
Because of charging and discharging of capacitor saw tooth waveforms are obtained at emitter terminal and positive trigger pulse is obtained at Base 1 and negative trigger pulses are obtained at base 2 as shown in Fig. (b)
The sweep period is given by the relation,

$$T = R.C.log_e \frac{1}{1-\eta}$$

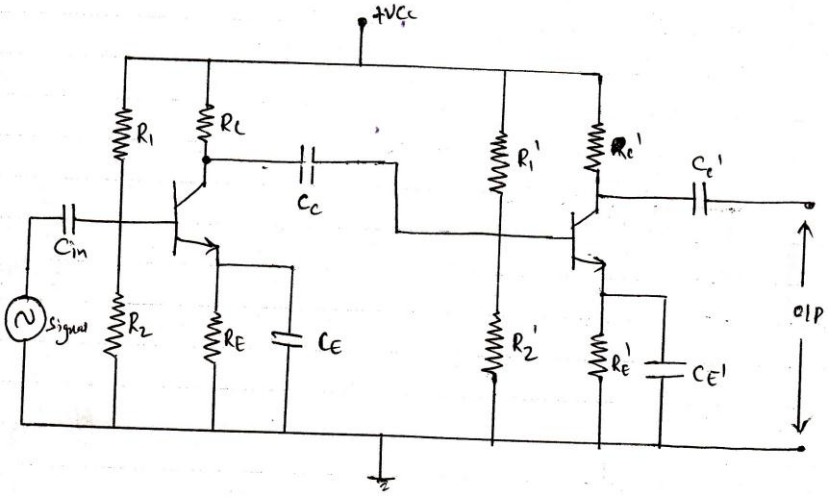
Where, η is intrinsic stand-off ratio
The sweep frequency can be varied by changing values of either R or C.

d) Draw the circuit diagram of two stage R-C coupled amplifier and describe it's working.

Ans: (**circuit diagram 2M**, **working 2M**)

R-C coupled amplifier -:

This is the most popular type of coupling method. It is usually employed for voltage amplification. Following fig shows two stage of an RC coupled amplifier.



A coupling capacitor Ce us used to connect the output of first stage to the base (i.e input) of the second stage and so on.

The resistance R1, R2 and Re form the biasing and stabilization network. The emitter be pass capacitor offers low reactance path to the signal. The coupling capacitor Ce transmits ac signal but blocks dc. This prevents dc interference between various stages and the shifting of operating point.

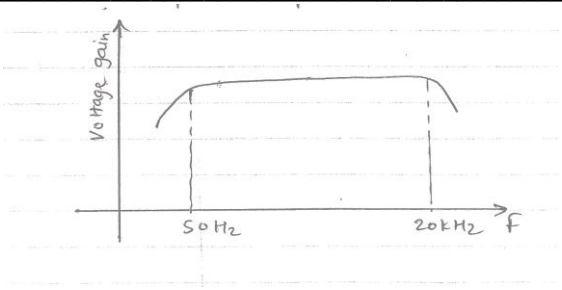
Operation:-

When ac signal is applied to the base of the first transistor, it appears in the amplified from across its collector load RC. Is given to base of next stage through coupling capacitor Cc.

The 2nd stage does further amplification of the signal. In this way the cascaded (in series) stage amplify and overall gain is considerably increased.

Frequency response-: **(Optional)**

Following fig. show frequency response of typical RC coupled amplifier.



From above frequency it is clear that bandwidth of RC coupled amplifer.is large. Voltage gain drops off at low (50 hz) and high (20 khz) frequencies. Whereas it is uniform over mid frequency range.(50 hz, to 20 khz)

e) Draw functional block diagram of IC723. Describe its working.

Ans: **(Block dig 2M, working 2M)**

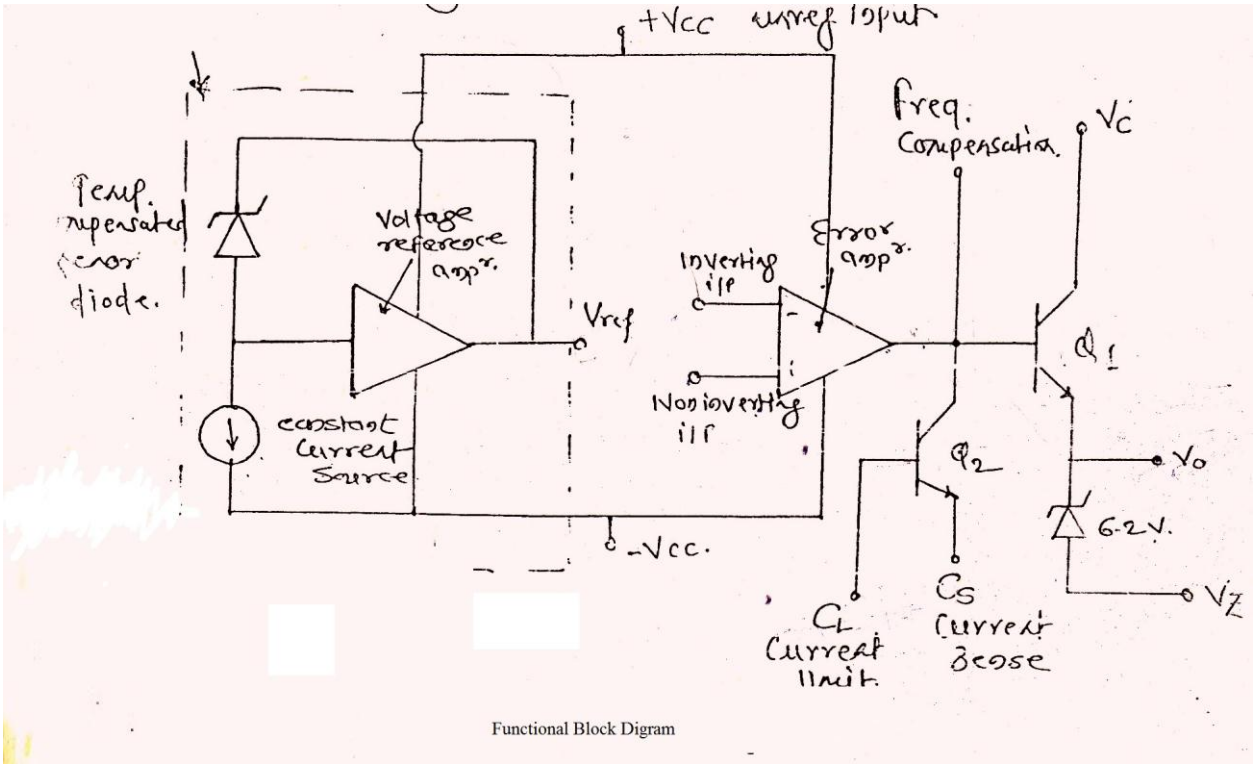


Fig shows block diagram of IC 723 regulator IC

1) It has two separate sections
   The zener diode, a current source and reference amplifier produces a fixed voltage of about 7 volts at terminal V reference.
2) The constant current source forces the zener diode to operate at fixed points so that the zener output a fixed voltage.
3) The other section of the IC consist of error amplifier, a series pass transistor Q_1 and the current limiting transistor.Q_2

4) Error amplifier compares a sample of the output voltage applied at inverting input terminal to the reference voltage Vreference applied at NI input terminal.
5) The output of error amplifier (error signal) controls the conduction of Q1
6) If due to some reason Vo increases then O/P voltage of error amplifier decreases. Therefore base drive to Q 1 become less, thus o/p voltage is brought back to its original value.

f) What is necessity of regulated power supply? define load and line regulation

Ans: **(Necessity 2M, Load regulation 1M, Line regulation 1M)**

Necessity of regulated power supply: The major disadvantage of a power supply is that the O/P voltage changes with the variations in the input voltage or The D.C O/P voltage of the rectifier also increase similarly, In many electronic applications, it is desired that the O/P voltage. Should remain constant regardless of the variations in the I/P voltage or load. In order to get ensure this; a voltage stabilizing device called voltage regulator is used.

- **Load Regulation:** The load regulation indicates the change in output voltage that will occur per unit change in load current.

Mathematically,

$$\textbf{Load Regulation} = \frac{V_{NL} - V_{FL}}{\Delta I_L}$$

The load regulation of voltage regulator is expressed in terms of µv/µA.
Where, V_{NL} *is no load output voltage*
V_{FL} *is full load voltage*
ΔI_L *is change in laod current*

- **Line regulation**: The line regulation rating of a voltage regulator indicates the change in output voltage that will occur per unit change in the input voltage.

$$\textbf{Line regulation} = \frac{V_L}{V_S}$$

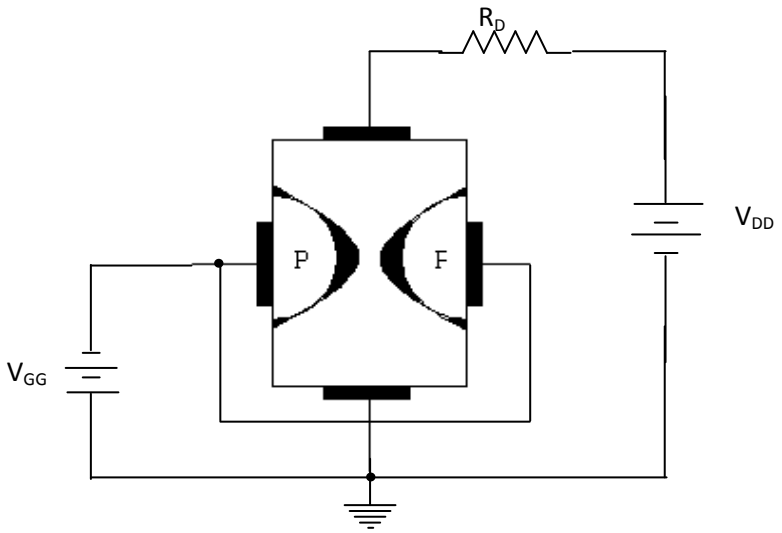
Where, ΔV_L is the change in output voltage in mV or µV
ΔV_S is the change in input voltage in volts.

(Note:- Formula for load & Line regulation is optional)

Q4 Attempt any four of the following. **(16M)**

a) Describe the working of n-channel JEET with diagram.

Ans: **(Diagram: 2M, working: 2M)**



Operation:

Fig. shows bias voltages applied to an n channel device. V_{DD} provided drain to source voltage & supplied a current from a drain to source. V_{GG} sets the reverse bias voltage between the gate & the source as shown.

The JFET is always operated with gate to source P-n junction reverse biased.

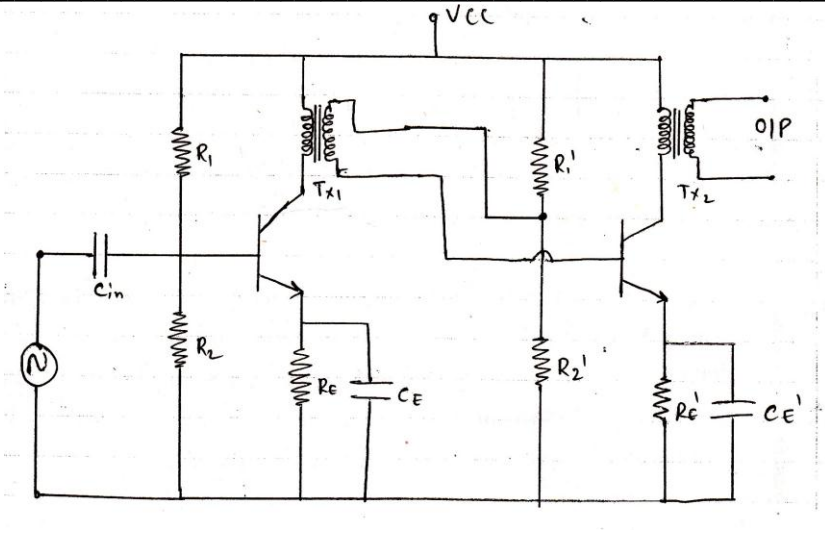
Reverse biasing of the gate – source junction produces a depletion region along the P-n junction, which extends into the n channel & thus increases its resistance by restricting the channel width.

The channel width and thus the channel resistance there by controlling the amount of drain current I_D

b) Describe transformer coupled amplifier with neat circuit diagram.

Ans: **(Diagram: 2M, working: 2M)**

Following Fig. shows the diagram for transformer coupled amplifier.



Transformer coupling is generally employed when the load is small. It is mostly used for power amplification. In above fig a coupling transformer is used to feed the output of one stage to the input of the next stage.

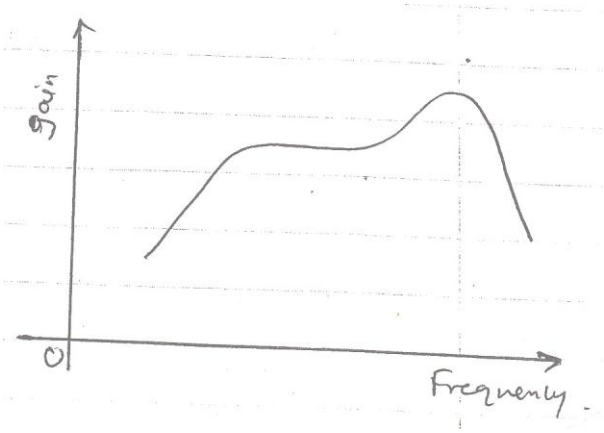
The Primary P of this transformer is made the collector load and its secondary S given input to the next stage.

Operation -:

When ac signal is applied to the base of first transistor, It appears in the amplified form across primary P of the coupling transformer. The voltage develop across primary is transferred to the input of the next stage by the transformer secondary as shown in above fig.. The second stage gives amplification in similar manner.

Frequency Response: (Optional)

The frequency response of transformer coupled amplifier is shown in following fig.

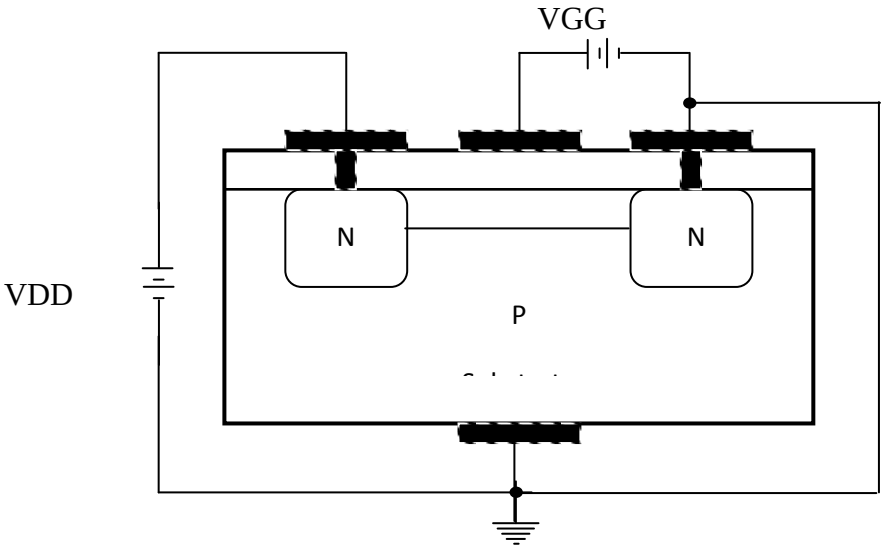


From the above graph it is clear that the frequency response is poor. i.e gain is constant only over a small range of frequency.

c) Describe working of D- MOSFET WITH neat diagrams.

Ans: **(Working diagram: 2M, Working: 2M)**

Circuit Operation:-



The gate to source voltage is set to zero volts by the direct connection from one terminal to the other. & voltage V_{DS} is applied across the drain to source terminals. This results the attraction by the free electrons of the n channel due to positive drain & I_{DSS} establish in the circuit.

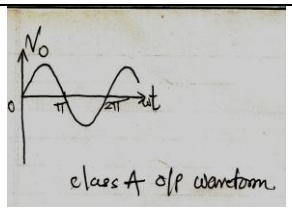
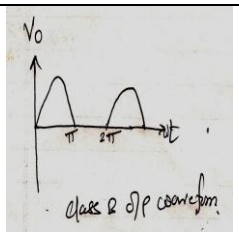
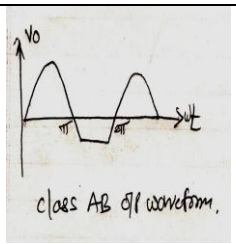
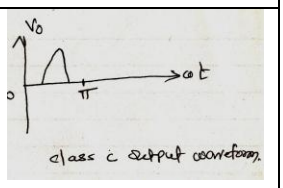
For negative voltage at gate, pressure electron towards P type substrate and attract holes toward insulated layer. Recombination occurs between electron & holes that will reduce the number of free electron in the channel for conduction. So drain current reduces. The more negative value at which drain current nearly equal to zero that voltage of V_{GS} is called cut off voltage.

Whereas, when gate is positive with respect to source then positive V_{GS} draws additional electrons from the P type substrate. Thus drain current (I_D) increases as increase in positive value.

d) Compare class A, Class B, Class AB and Class C amplifier W.R.T following points.

I. Position of operating Pt. on load line.
II. Efficiency
III. Conduction angle
IV. O/P waveform

Ans: **(1 Mark each point)**

Parameter	**Class A**	**Class B**	**Class AB**	**Class C**
Position of operating pt. on load line	Q point is at the centre of load line.	On X axis	Just above X axis.	Below X axis.
efficiency	lowest efficiency 25% to 50%	Above 78.5%	Between 50 to 78.5%	Above 95%
Conduction Angle	Conducts for (360^0) full cycle of input signal	(180^0) half cycle of input signal.	Greater than 180^0 and less than 360^0	Less than 180^0 of input signal.
O/P waveform				

e) Describe the working of single stage Class A amplifier with circuit diagram.

Ans: **(Circuit diagram: 2M, Working: 2M)**

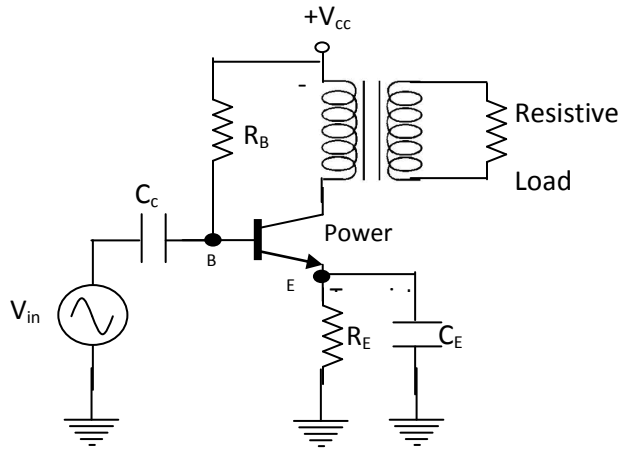
Note: series fed direct coupled class A Amplifier can also be consider

Transformer Coupled resistive load single stage class A power amplifier:-

(Single ended transformer coupled class A amplifier)

It is a large signal amplifier; it handles signals in the range of volts and transistor used is power transistor capable of operating in the range of few watts to 10 W. The beta (gain) of transistor is generally less than 100, Instead of connecting load directly here it is connected through output transformer so that impedance matching can take place and transfer maximum power to the load.

Circuit diagram:-

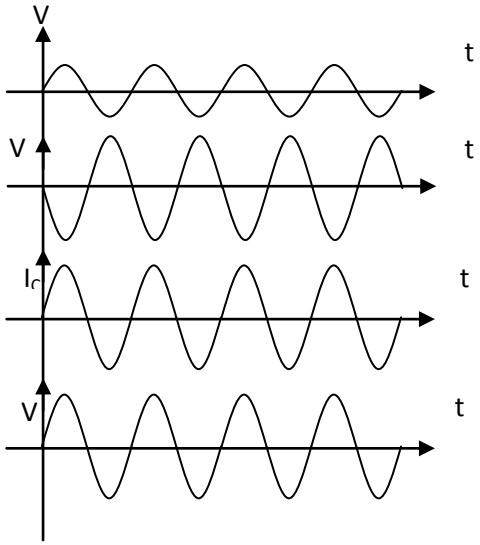


Circuit Operation:-

Fixed Biasing is provided by resistor R_B, R_e Stabilizes bias, Ce is bypass capacitor. Signal is fed between base and emitter through coupling capacitor C_c. Load in the collector of transistor is the output transformer used to match the low impedance of the load to the output impendence of amplifier.

For positive half cycle of the input signal BE junction is more forward biased due to this collector current Ic starts increasing. So that voltage is developed across primary winding of the transformer, polarities are as shown in above fig.

For negative half cycle, BE junction is less forward bias (reverse biasing increases) due to this collector current is also decreases and voltage polarity exactly opposite to the precious case. The output voltage, collector current waveforms are given as follows-



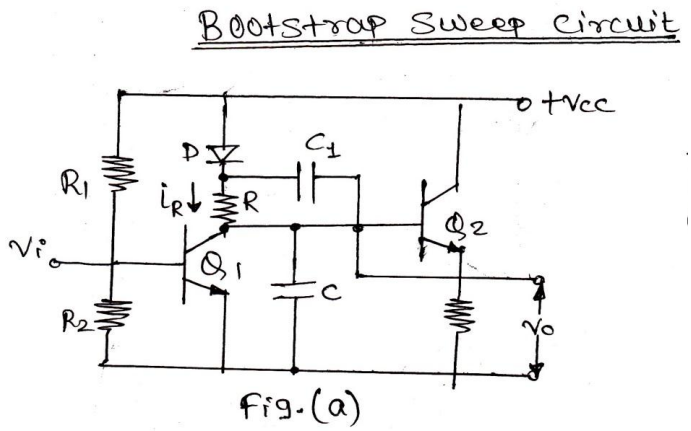
In class A amplifier, Q point is adjusted at the center of load line due to this output is obtained for full cycle (i.e. 360^0) of input signal as shown.

With respect to input I_C changes sinusoidal so input and collector current is in phase and V_{CE} is out of phase (i.e. 180^0).

f) Draw the working of Bootstrap time base generator with circuit diagram.

Ans**:** **(2 marks for circuit diagram, 2 mark for explanation)**

Fig. (a) Below shows a practical form of bootstrap circuit. Here transistor Q1 acts as a switch and transistor Q2 acts as an emitter follower (i.e. a unit gain amplifier).



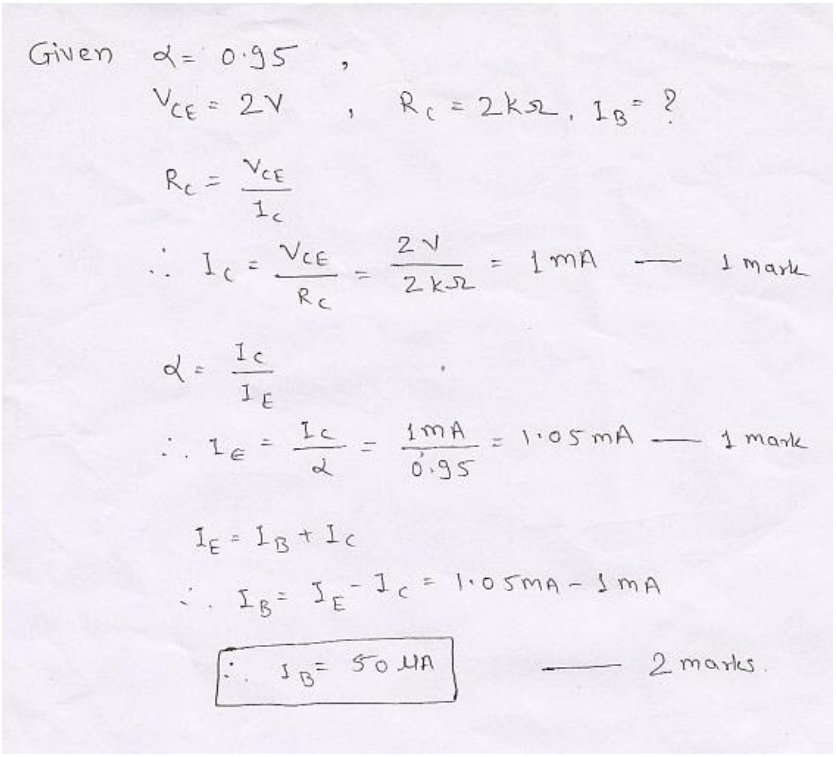
Circuit Operation:

Initially transistor Q1 is ON and Q2 is OFF. Therefore capacitor C1 is charged to VCC through the diode forward resistance (RF). At this instance output voltage is zero.
When negative pulse is applied to the base of transistor Q1, it turns OFF. Since Q2 is an emitter follower, therefore the output voltage V0 is same as base voltage of Q2.
Thus when Q1 turns OFF, the capacitor C1 starts charging this capacitor C through resistor (R). As a result of these both the base voltage of Q2 and output voltage begins to increase from zero.
As the output voltage increases diode D becomes reverse biased, because of the fact that the output voltage is coupled through the capacitor (C1) to the diode.
Since the value of capacitor (C1) is much larger than that of capacitor (C), therefore the voltage across capacitor (C1) practically remains constant.
Thus voltage drop across resistor (R) and hence current (I_R) remains constant, means capacitor C is charged with constant current.
This causes voltage across capacitor C (and hence the output voltage) to increase linearly with time.
The circuit pulls itself by its own bootstrap and hence it is known as bootstrap sweep circuit.

Q. 5 Attempt any FOUR of the following: (16 marks)

a) In common base connection α = 0.95 the voltage drop across resistance which is connected in collector is 2 V. Find base current if the value of resistance connected in collector is 2K.

Ans. -:



b) A phase shift oscillator has R = 220 KΩ, C= 500 pf calculate frequency of sine wave generator.

Ans. -: **(Formula 1 mark, Substitution 1 mark, Answer2 marks)**

Given data

R = 220κΩ

C= 500 PF

F_0=?

$$F_0 = \frac{1}{2\pi CR\sqrt{6}}$$

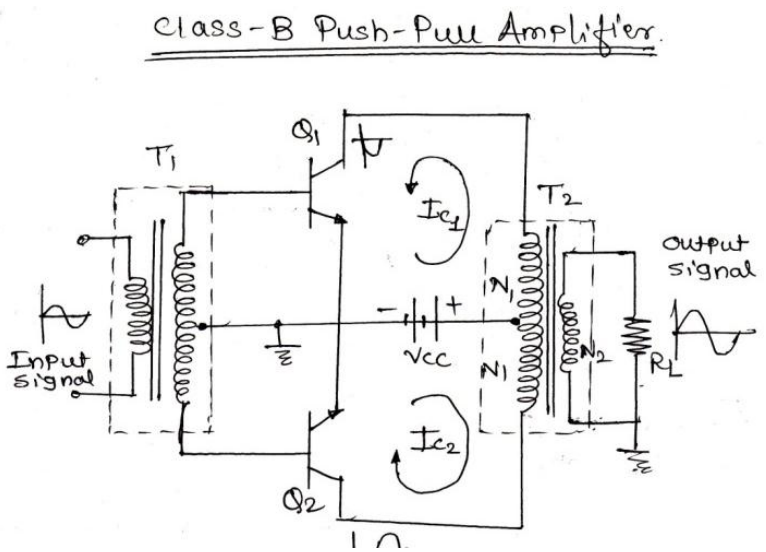
$$F_0 = \frac{1}{2\pi \times 500 \times 10^{-12} \times 220 \times 10^3\sqrt{6}}$$

= 590.6894 Hz

c) Describe Class B push pull amplifier with neat circuit diagram.

Ans. -: **(Diagram 2 marks, Explanation 2 marks)**

- In class B amplifier transistor conducts only for half cycle of input signal. This type of output signal gives large distortion.
- In order to avoid this we use two transistors connected in push-pull arrangement. One conducts in positive half cycle and other conducts in negative half cycle.
- Transistor T_1 is called as input transformer and is called phase splitter and produces two signals which are 180^0 out of phase with each other.
- Transistor T_2 is called output transformer and is required to couple the a.c. output signal from the collector to the load.



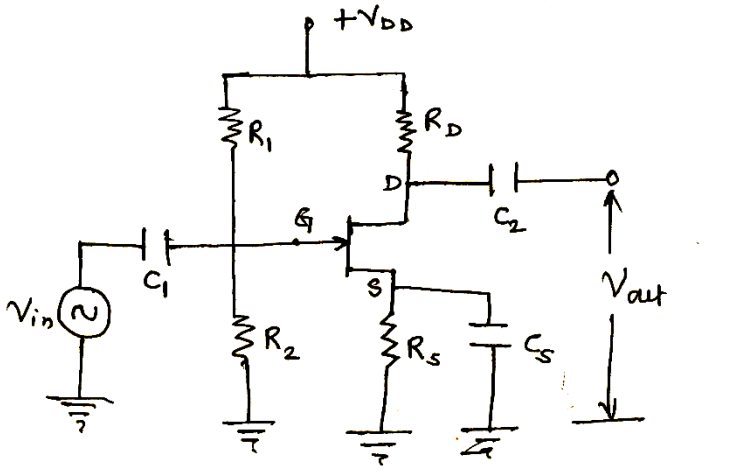
Working:

- When there is no input signal both the transistor Q_1 and Q_2 are cut-off. Hence no current is drawn from V_{CC} supply. Thus there is no power wasted in standby the power dissipation in both transistor is practically zero.
- During positive half cycle the base of Q_1 is positive and Q_2 is negative. As a result of this Q_1 conduct, while the transistor Q_2 is OFF. And at the output half cycle is obtained.
- During negative half cycle, Q_1 turns OFF and Q_2 conducts, and another half cycle is obtained at the output. At any instant only one transistor in the circuit is conducting. Each transistor handles one half of the input signal.
- Then output transformer joins these two halves and produces a full-sine wave in the load resistor.

d) Describe FET as an amplifier with circuit diagram.

Ans. -: **(Circuit diagram 2M, Explanation 2M)**

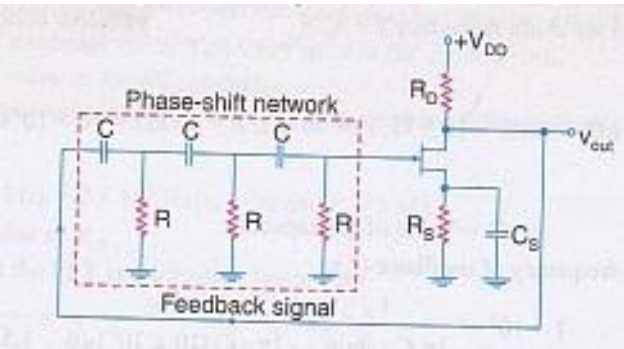
Operation: - When small a.c. signal is applied to the gate, its produces variation in the gate to source voltage. This produces variation in the drain current. As the gate to source voltage increases the current also increases. As the result of this voltage drop across R_D also increases. This causes the drain voltage to decreases. It means positive half cycle of the input voltage produces the negative half cycle of the output voltage.



Common Source FET amplifier

e) Draw the circuit diagram of RC phase shift oscillator and describe its working.

Ans. -: **(Diagram 2 marks, Explanation 2 marks)**



Working:-

Above fig. shows the circuit of a phase shift oscillator using FET. The circuit consists of a amplifier and feedback network.

The amplifier stage is self biased with a capacitor by passed source resistor (Rs) and drain bias resistor (R_D).

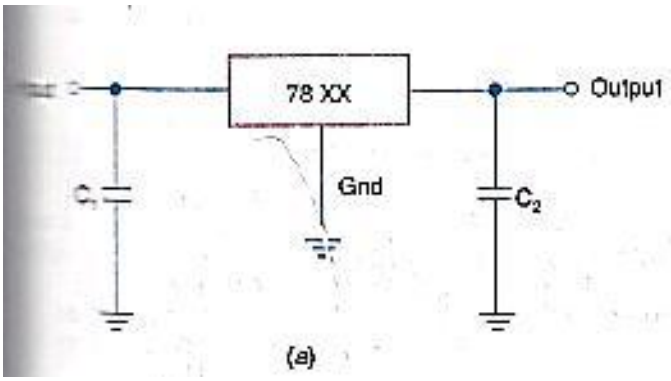
The feedback network consists of three identical RC sections. Each section produces a phase shift of 60^0. Therefore the net phase shift of the feedback network is 180^0 phase shift is provided by the amplifier circuit. Therefore the total phase shift between the input and the output circuit is 360^0 or 0^0.

When the circuit is energized by switching on the supply, the circuit starts oscillating. The oscillations may start due to minor variation in d.c. supply or inherent noise in the FET. The variation in the gate current is amplified in the drain circuit. Then it is feedback through the phase shift network and finally applied to the gate. To start oscillation $A_v\beta$ should be unity. The frequency of oscillations given by the relation

$$f = \frac{1}{2\pi CR\sqrt{6}}$$

f) Describe +ve voltage regulator using IC 78XX series.

Ans. -: **(Diagram 2 marks, Explanation 2 marks)**



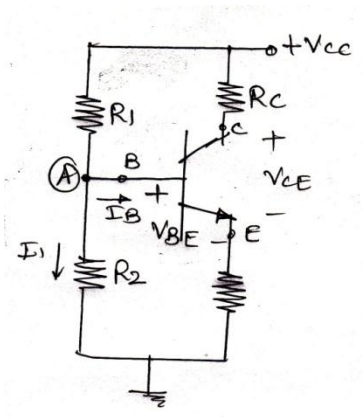
Explanation: 78XX series of IC regulators is representative of three terminal devices that are available with several fixed positive output voltages. It has three terminals labeled as input, output and ground. The last two digits (mark XX) in the part no. designate the input voltage. Above fig. shows a standard configuration of a fixed positive voltage IC regulator of 78XX series. The capacitor C_1 is required only if the power supply filter is located more than three inches from the IC regulator. The capacitor C_2 acts basically as a line filter to improve transient response.

Q. 6 Attempt any FOUR of the following: **(16M)**

a) Describe voltage divider biasing method in BJT with circuit diagram.

Ans. -: **(Circuit diagram 2 marks, Explanation 2 marks)**

- Fig. below shows the voltage divider.
- In this method two resistances R_1 and R_2 are connected across the supply voltage V_{CC} and provide biasing.
- The voltage drop across resistor R_2 forward biases the base emitter junction of transistor. The resistor R_E provides the d.c. stability.



(i) Collector Current (I_C) :-

$I_1 = \frac{V_{CC}}{R_1+R_2}$

∴ Voltage across resistance R_2 is

$V_2 = \left(\frac{V_{CC}}{R_1+R_2}\right) R_2$

Applying KVL to input loop,

$V_2 = V_{BE} + V_E$

OR $V_2 = V_{BE} + I_E R_E$

$I_E = \frac{V_2 - V_{BE}}{R_E}$

Since $I_E \simeq I_C$

$$I_{CQ} = \frac{V_2 - V_{BE}}{R_E} \quad \text{—— (1)}$$

(ii) To find Collector-Emitter Voltage (V_{CE}) :-

Applying KVL to the collector Side.

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$V_{CC} = I_C R_C + V_{CE} + I_C R_E \quad (\because I_E \simeq I_C)$

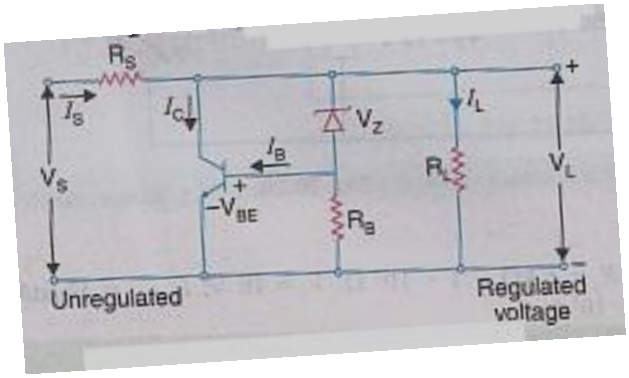
$V_{CC} = I_C (R_C + R_E) + V_{CE}$

∴ $$V_{CEQ} = V_{CC} - I_C (R_C + R_E) \quad \text{—— (2)}$$

Q Point = (V_{CEQ}, I_{CQ})

b) Describe the working of shunt voltage regulator using transistor with circuit diagram.

Ans. -: **(Circuit diagram 2 marks, Working 2 marks)**



Explanation:-

From the above circuit the load voltage is given by

$V_L = V_Z + V_{BE}$ Or $V_{BE} = V_L - V_z$ ..... (i)

Since the load voltage for a given zener diode is fixed, therefore any decrease or increase in load voltage will have a corresponding effect on the base to emitter voltage.

The unregulated input voltage increases, load voltage also increases. As a result of this from equation (i) above, we find that V_{BE} is also increases. And the base current increases. Due to this the collected

current also increases. This causes the input current (I_S) to increase, which in turn increases the voltage drop across series resistance (V_{RS}) . Consequently, the load voltage decreases. It is true because some of the voltage drop across series resistance (V_{RS}) and load voltage is equal to the input voltage at all times. i.e. $V_S = V_{RS} + V_L$ or $V_L = V_S - V_{RS}$

c) State Barkhausen criteria. List advantages of negative feedback over positive feedback (any two).

Ans. -: **(Barkhausen criteria: 2 Marks)**

Barkhausen criteria:

The two conditions for positive feedback or oscillations

1. Aνβ=1 i.e. loop gain must be 1
2. The net phase shift around loop equal to 360°or 0°

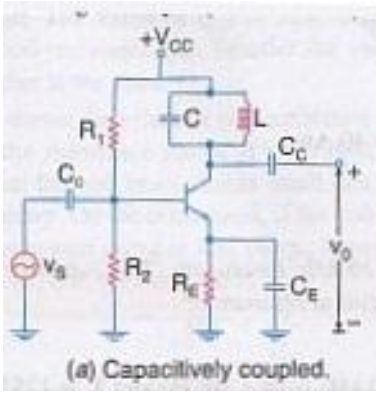
Advantages of negative feedback over positive feedback

(Any two advantages 1 Mark Each)

1. Bandwidth is increased.
2. Noise is decreased
3. Stability is increased
4. Less amplitude and harmonic distortion
5. Less frequency distortion.
6. Input and output resistance can be modified as desired.
7. Less phase distortion.

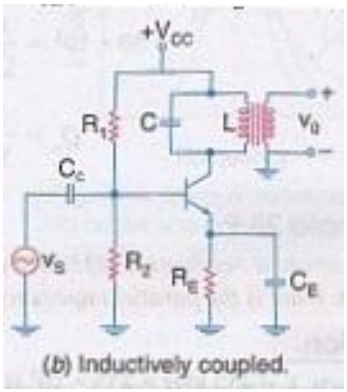
d) Describe the operating principle of single tuned amplifier with circuit diagram.

Ans. -: **(Diagram 2 marks, Operating principle 2 marks)**



(a) Capacitively coupled.

OR



(b) Inductively coupled.

Working:

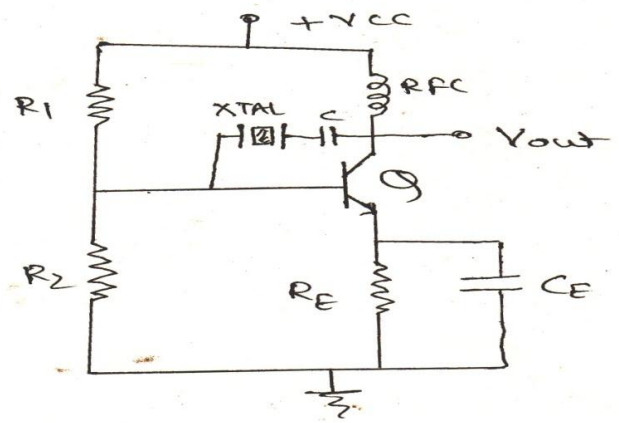
The working of tuned voltage amplifier may be understood by considering a radio frequency signal, to be amplified applied at the input of the amplifier. The resonant frequency of the tuned circuit is made equal to the frequency of the input signal by changing the value of capacitor (C) and inductor (L).when the frequency of the tuned circuit becomes equal to that of the input signal a large signal appears across the output terminals.

If the input signal is a complex wave (i.e. it contains many frequency components.) in that case the frequency with input frequency equal to the resonant frequency will be amplified. And all the other frequencies will be rejected by the tuned circuit.

Note -: In-place of BJT, FET also can be consider.

e) Describe the working principle of crystal oscillator with circuit diagram.

Ans. -: (**Circuit diagram 2 marks, working principle 2 marks)**



Working:-

Above fig shows the transistor pierce crystal oscillator. In this circuit, the crystal is connected as a series element in the feedback path from collector to the base.

The resistors R_1, R_2 and R_E provide voltage divider stabilized d.c. bias circuit. The capacitor C_E provides a. c. bypass of emitter resistor and RFC coil provides for d. c. bias. The coupling capacitor C has negligible impedance at the circuit operating frequency.

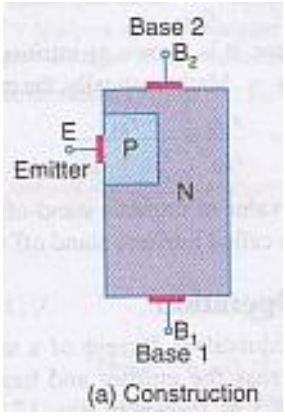
The circuit frequency of oscillation is set by the series resonant frequency of the crystal and its value is given by the relation

$$F_0 = 1/2\pi\sqrt{(LC_1)}$$

It may be noted that the changes in supply voltage, transistor device parameters etc have no effect on the circuit operating frequency, which is held stabilized by the crystal.

f) Draw construction and describe its working principle of UJT.

Ans. -: **(Construction 2m, working principle 2 m)**



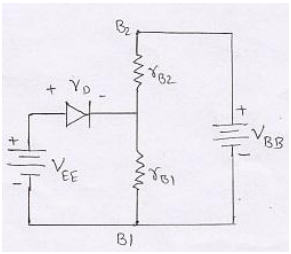


Fig. shows the equivalent circuit of a unijunction transistor with voltage source V_{EE} connected across emitter and base1 and V_{BB} connected across base1 and base2. Hence the diode is reversed biased by a voltage drop across the r_{B1} and its own barrier potential (V_D). Thus total reverse bias voltage across a diode is equal to sum of $\eta.V_{BB}$ and V_D.

As long as the V_{EE} is below the total reverse bias voltage (i.e. $\eta.V_{BB} + V_D$) across the diode, it remains reverse biased and there is no emitter current.

However if the V_{EE} voltage reaches or exceeds the value equal to ($\eta_{.BB} + V_D$), the diode conducts V_{EE}, which causes the diode to conduct, is called peak point voltage.

$V_P = \eta . V_{BB} + V_D$

When the emitter current begins to flow, the UJT is said to be fired, triggered or turned on.