Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1 a) Attempt any SIX of the following **(12M)**

i) Define

1) Instruction cycle

2) T- state

Ans: **(each definition 1M)**

Instruction cycle:

It is defined as the time required to complete the execution of an instruction. In 8085 instruction cycle may consist of 1-5 machine cycles or operations.

T- state:

It is defined as one subdivision of the operation or machine cycle performed in one clock cycle i.e 1 T state= 1/3 MHz = 333.33ns.

ii) What are stacks? list their use(any two)

Ans:

Stack- **(1 M)**

Stack is reserved area in RAM where contents of registers can be pushed & reserved in stack memory temporarily.

Use – (1M)

- Stack can be used to store the data of registers temporarily so that registers can be re-used efficiently.
- Program counter contents also are pushed to stack during execution of subroutine & interrupts service routine.

iii) List one example each of one byte, two byte and three byte type of instructions.

Ans: (any relevant instruction should be accessed.)

One byte- MOV A, B
Two byte- MVI A, 23h
Three byte STA 1234h

iv) Classify the data transfer techniques.

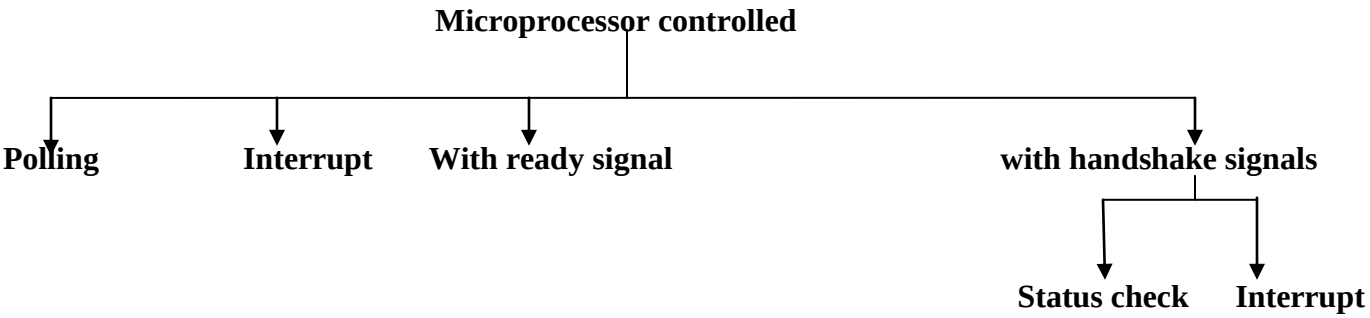
Ans:

Data transfer techniques

Serial
- **Synchronous**
- **Asynchronous**

Parallel

(DMA) device controlled



v) List any two features of 8255

Ans: Any two feature **(Each feature ---1M)**

- It has three 8 bit parallel ports
- It runs on two modes
  1) Input output with handshake signal
  2) Bit set reset mode
  - It requires +5V power supply

vi) What is a subroutine? List two related instruction while referring subroutine in main program.

Ans: **(Subroutine 1M, Instruction ½ M each)**

Subroutine

Set of instructions which need to be executed frequently are stored separately from main program is known as subroutine.

(Note: Any relevant definition should be given marks)

Instruction

- CALL addr of subroutine

e.g. CALL 2500h

- RET

vii) State the memory addressing capacity of 8085.

Ans:

No of addressing lines in 8085= 16 (1M)

2^{16} = 64 KB (1M)

64 KB memory addressing capacity

viii) Compare PUSH and POP instruction of 8085 microprocessor(any two)

Ans: **(each point 1 M)**

Sr no.	**PUSH**	**POP**
1	Register pair contents are stored in stack memory	Register pair contents are restored from stack memory to register pair specified in instruction
2	Program counter is decremented two times	Program counter is incremented two times.

Q1 b) Attempt any Two of the following **(8M)**

i) Compare between I/O and memory mapped I/O (any four points)

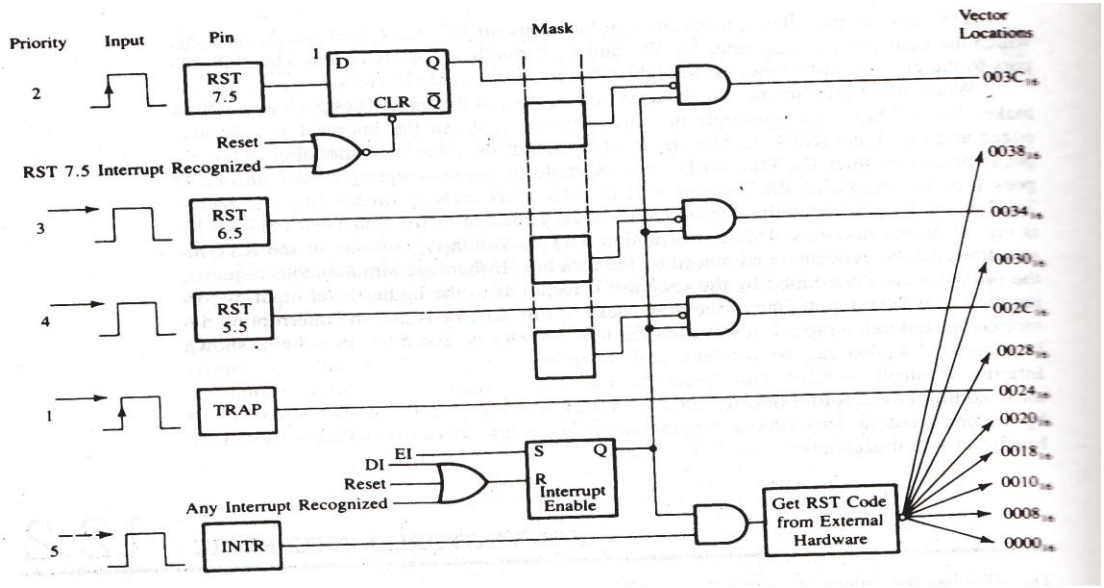
Ans: **(each Point 1 M)**

Characteristics	**Memory mapped**	**I/O mapped**
Device address	16 bit	8 Bit

Control signals for i/p /O/P	$\overline{MEMR}$/ $\overline{MEMW}$	$\overline{IOR}$ /$\overline{IOW}$
Instructions available	Memory related instruction STA; LDA ; STAX ; LDAX,MOV M,R ; ADD M ; SUB M ANA M etc.	In & Out
Data transfer	Between any register & I/O	Only between the I/O & the accumulator
Maximum no of i/o s possible	The memory map(64k) is shared between I/O s & system memory	The I/O map is independent of memory map; 256 input device can be connected.
Execution speed	12T- states (STA , LDA) 7T-states (MOV M,R)	10T - states
Hardware requirements	More hardware is needed to decode 16 bit address	Less- hardware is needed to decode 8bit address
Other features	Arithmetic or logical operations can be directly performed with I/O data	Not available.

ii) Draw the interrupts structure of 8085. Explain the vectored interrupts.

Ans: **(2M)**



Vectored interrupts (2M)

Interrupts which vector location i.e. starting address of interrupt service routine is pre-defined are known as vectored interrupts.

- These interrupts do not require $\overline{INTA}$ or any other acknowledge signal.
- TRAP & all RSTS are vectored interrupts

iii) State any four features of 8085

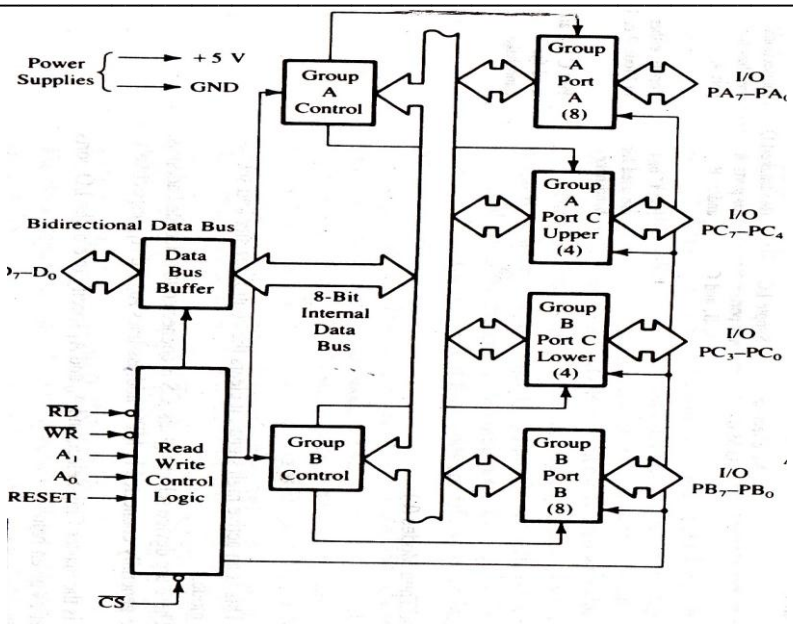
Ans: (each point 1 M)

- It has 8 bit data bus, 8bit ALU. So it is 8 bit microprocessor.
- It has 16 bit address bus.
- It can access 64 kb external memory.
- It requires +5v power supply.
- It requires 6 MHz crystal oscillator. 3 MHz is operating frequency.
- It offers 5 hardware interrupts & 8 software interrupts.
- It supports DMA feature using HOLD & HLDA Pins.
- Serial communication is possible through the pins SID & SOD.
- 2^8 = 256 input & output devices can be interfaced with 8085

Q2 **Attempt any Four of the following (16M)**

a) Draw the block diagram of 8255

Ans:



b) What are RST instructions? explain the following instruction

i) EI

ii) DI

iii) RIM

Ans: **(Each instruction 1M)**

RST – these are 1-byte call instructions that transfer the program execution to a specific location on page 004

There are 8 restart instructions in 8085, can be use as Software instruction in a program to transfer program execution to one of the 8 locations.

EI- (Enable interrupts)

It is 1-byte instruction which set the

- Interrupt enable Flip-flop & enables the interrupt process.
- System reset or an interrupt disables the interrupt process.

DI - (Disable interrupt)

It is 1 bite instruction which reset interrupt enable flip-flop & disables the interrupt

Rim – (read interrupt mask)

This is 1 byte multipurpose instruction used to read the status of interrupts 7.5, 6.5, & 5.5 and also to read serial data input bit

OR

Format

D7	D6	D5	D4	D3	D2	D1	D0
SID	I7	I6	I5	IE	7.5	6.5	55

c) Explain BSR mode of operation of 8255 in detail by giving a suitable example.
Ans:

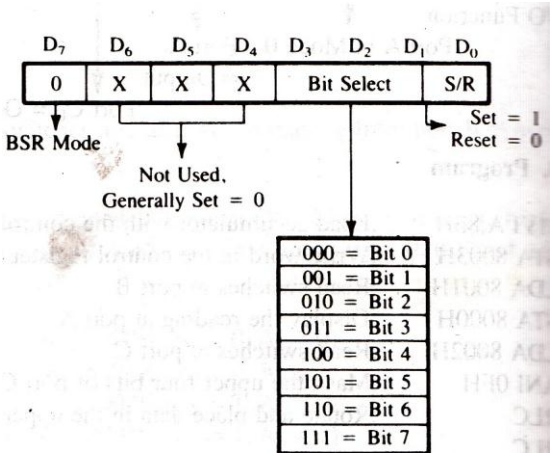
(Any relevant example 2M)

Assume we want to set bit 5th of port C

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	1

= 0BH

(Diagram 2 M)



d) Write an assembly language program for block of transfer of data(block – 4Nos 8Bits)
Ans: **(Program with suitable Comments 4 M)**

M VI C, 04h --------- Counter for no of blocks to be transferred
LXI B, C2000h ------ Initializing source address in BC pair
LXI H, D200h -------- Initializing destination address in HL pair

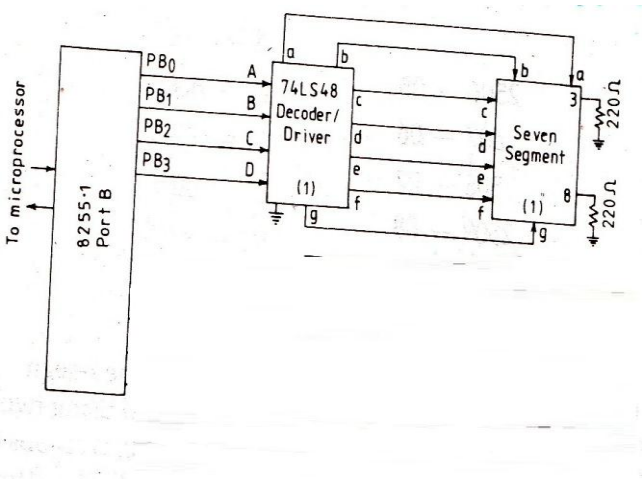
L1: LDAX B -------- Source address ----- (ACC)
MOV M, A ---------- (ACC) ----- Destination address
INX B ---------- Get next source address
INX H ---------- get next destination address
DCR C ---------- Decrement counter by 1
JNZ L1 ----------If counter ≠ 0 continue to transfer, else stop
HLT

e) Draw the interfacing diagram of8255 and seven segment display. Write assembly language program to display 0 to 9 digits

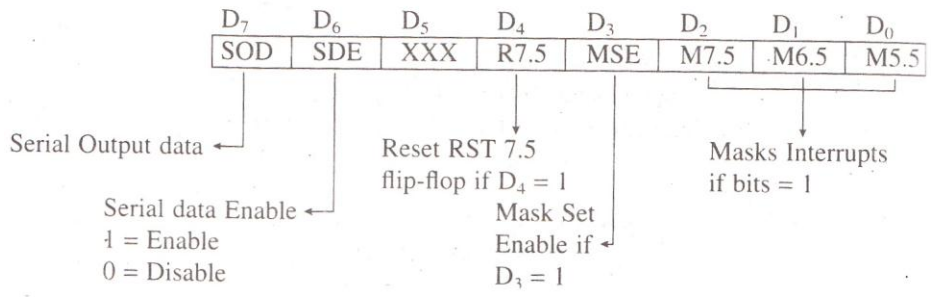
Ans: This Question has to be asked for 8marks but not for 4 marks. Students should be given marks for even logic of program. (2 M diagram, 2 M program)

Data stored at 2500H

Labels	*Mnemonics*	*Operands*	*Comments*
	MVI	A, 98 H	Get control word.
	OUT	03	Initialize ports.
ABOVE	LXI	H, 2500H	Get count.
	MOV	E, M	Count in register E.
LOOP	INX	H	
	MOV	A, M	Get next number.
	OUT	01	Output at Port B.
	MVI	B, 0F	
BEHIND	MVI	C, FF	
BACK	MVI	D, FF	
GO	DCR	D	Delay subroutine using
	JNZ	GO	3 registers.
	DCR	C	
	JNZ	BACK	
	DCR	B	
	JNZ	BEHIND	
	DCR	E	Decrement count.
	JNZ	LOOP	Go to LOOP to get next number
	JMP	ABOVE	Go to ABOVE to re-start.



f) Draw the SIM instruction word and explain the function of all bits in it.
Ans: (2 M diagram, 2 M program)

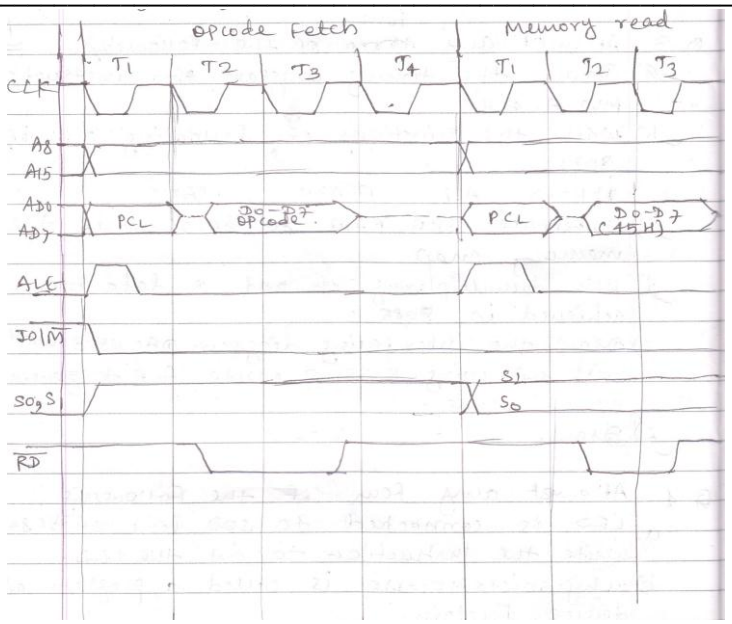


SOD – Serial Output Data: Bit D7 of the accumulator is latched into the SOD output line and made available to a serial peripheral if bit D6=1;
SDE- Serial Data Enable: If this bit=1, it enables the serial output. To implement serial output, this bit needs to be enabled.
XXX- Don't care
R7.5-Reset RST 7.5 if this bit=1, RST 7.5 flip-Flop is reset. This is an additional control to reset RST 7.5.
MSE- Mask Set Enable: if this bit is high, it enables the functions of bits D2, D1, D0. This id master control over all the interrupt masking bits. If this bit is low, bits D2, D1 and D0 do not have any effect on the masks.
M7.5-D2=0, RST 7.5 is enabled
=1, 7.5 is masked or disabled
M6.5-D1=0, RST 6.5 is enabled
=1, 6.5 is masked or disabled
M5.5-D0=0, RST 5.5 is enabled
=1, 5.5 is masked or disabled

Q3) Attempt any Four of the following: - (16 Marks)

a) Draw the timing diagram for instruction MVIA, 45H.

Ans :- (For correct diagram 4 M)



MVI A, 45H
This instruction requires two m/c cycle.
M_1- opcode Fetch- 4T states.
M_2- Memory Read- 3 states.

b) Write the functions of following pins of 8085.

- **HOLD**
- **ALE**
- **READY**
- **RESET**

Ans: - **(1 M for each pin function)**

- **HOLD:-**
  When another of the computer system requires address and data bus for data transfer, it sends **HOLD** signal to the Microprocessor.
  After receiving the **HOLD** signal, Microprocessor sends out **HLDA** signal to the device.
  Microprocessor leaves the control over the buses as soon as current machine cycle is completed.
- **ALE:-**
  It is address latch enable signal
  It goes high during first clock cycle of a machine cycle and enables the lower 8 bits of the address to be latched into the external latch.

- **READY:-**
  It is the signal sent by I/P or O/P device to the Microprocessor.
  This signal indicates that I/P or O/P device is ready to send or receive data.
  A slow i/p/o/p device is connected to Microprocessor through ready pin.

RESET:- (NOTE)

(There is no reset pin in Microprocessor . So explanation for both reset and $\overline{\text{Reset IN}}$ &Reset OUT is given. Marks should be given for any One)

RESET IN:-

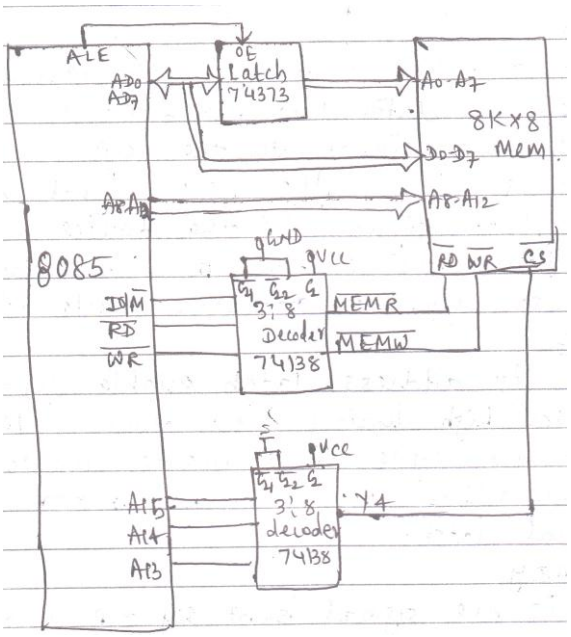
It resets the program counter to zero.

It also resets interrupts enable and **HLDA** Flip-flop.

It does not affect any other Flag or register, instruction register.

c) Interface 8KB RAM to 8085. State the memory map.

Ans **(3M-daig, 1M memory map)**

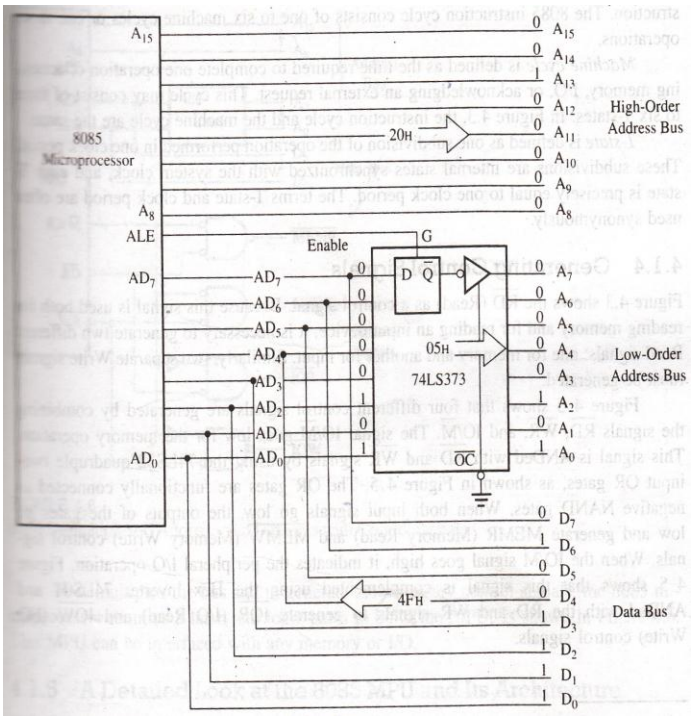


Memory Map:-

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000H	starting add
1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	9FFFH	ending add

d) How do multiplexing of address and data bus is achieved in 8085.

Ans: - (2 M diagram 2M explanation)



- Figure shows a schematic that uses a latch and the ALE signal to de multiplex the bus. The bus AD_7 – AD_0 is connected as the input to the latch 74LS373.
- The ALE signal is connected to the Enable (G) pin of the latch, and the output control (OC) signal of the latch is grounded.
- The ALE goes high during T_1. When the ALE is high, the latch is transparent; this means that the output changes according to input data.
- When the ALE goes low, the data byte is latched until the next ALE, and the output of the latch represents the low-order address bus A_7- A_0 after the latching operation.

e) Draw the interfacing diagram DAC 0800 with 8085 µ using 8255 and write ALP to generated square wave.

Ans:-

Program:-

Control word

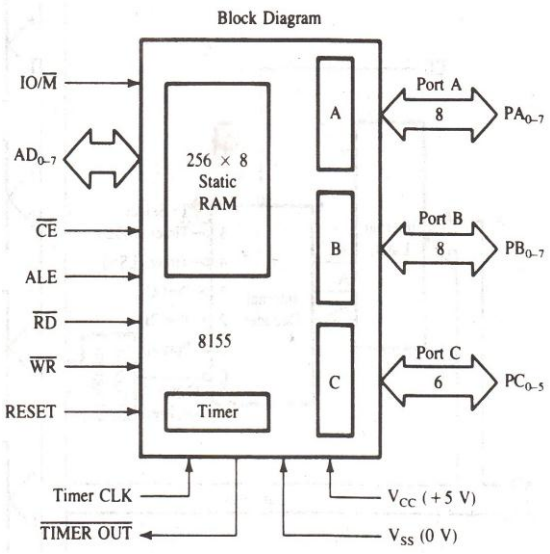
D7							D0
1	**MA_I**	**MA_D**	**PA**	**PC_U**	**MB**	**PB**	**PC_C**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**

=804

LABEL	MNEMONIC	OPERAND	COMMENTS
	MVIA	80H	**Initialize 8255**
	OUT	CWR	
	MVIA	00H	Out 00H to Port A and call delay to generate square wave.
	OUT	PORTA	
	CALL	DELAY	
UP	MVI	FFH	Out FFH to PA & call delay.
	OUT	PORTA	
	CALL	DELAY	
	JMP	UP	
DELAY	MVI C	85H	
	DCR	H	
	JNZ	BACK	
BACK	RET		

f) Draw block diagram of IC 8155.

Ans:-



Q4) Attempt any Four of the following:- **(16 Marks)**

a) LED is connected to SOD line of 8085. Write instructions to turn ON the LED

Ans: - **(Format 2M, Program 2M)**

SIM instruction is used to output data from accumulator to SOD pin.

Format of SIM

D7	D6	D5	D4	D3	D2	D1	D0

D7 is the data to be transmitted

D6 is SDE Serial data enable

To turn ON LED

MVI A ,C0H

SIM

b) Why microprocessor is called programmable device? Explain.

Answer:-

- Microprocessor has got instruction set of different addressing modes Using.
- These instructions task can be performed by microprocessor

- Microprocessor can be connected to programmable peripheral ICs like 8155, 8255 since they can share control bus, data bus and address bus. Also same instruction set can be used to interface applications using 8085 through 8255
- Microprocessor consists of general purpose registers and ALU using which contents can be altered, modified and manipulated using instructions
- Microprocessor can transmit and receive data serially through the pins SID and SOD using instructions.

c) Draw the instruction format of instruction. Describe with one example.

Ans : - (Format 2M, Example 2M)

Each instruction of 8085 is divided into two parts

i) **Opcode:** operation to be performed.

ii) **Operand:** data on which operation to be performed.

Example: MVI A, 20H

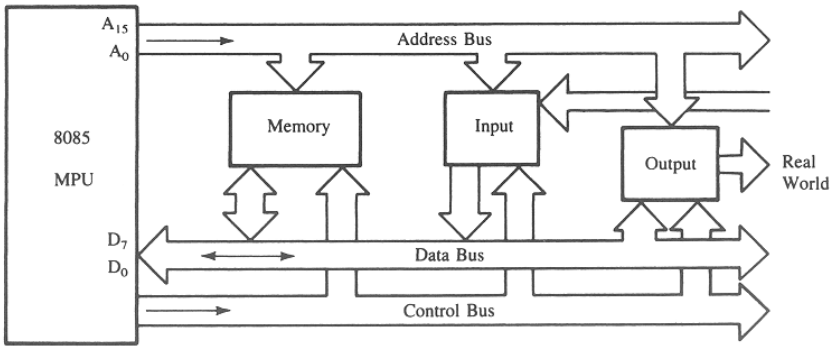
Opcode:-MVI –move immediately

Operand:-a, 20H data 20H into accumulator

(**Note:-**any relevant example should be given mark)

d) Draw the organization of Microprocessor based system and show the bus structure.

Ans:-



e) State any four features of 8155.

Ans :- (Each feature 1M)

- It includes 256 bytes of R/W memory.
- It includes two 8-bit & one 6-bit I/O port.
- It includes 14-bit timer which can produce square wave & pulses.
- It requires +5V power supply**.**

f) Write an assembly language program to add 8-bit numbers available in memory location from 2500H to 2509H.

Ans:- **(Program with comments 4 M)**

MNEMONIC	OPERAND	COMMENTS
MVI C	**OA**	**Set the counter for no.of numbers to be added.**
LXI H	**2500h**	**Set initial address**
SUB A		**Reset accumulator**
MOV A	**M**	**Move 1st no. to accumulator**
L1:INX H		**Get next no.**
ADD M		**Add 1st & 2nd no.**
DCR C		**Decrement Counter**
JNZ L1		**If counter is not zero continue addition, else go down**
INX H		
MOV M	**A**	**Store result in next memory location**

Q 5 Attempt any Four of the following: **(16M)**

a) Draw interfacing of 32 kb EPROM and 16 KB RAM to 8085. State the memory map

Ans:

1) Given 32 kb EPROM **(1M)**

- No of address lines = 15

2) 16 kb RAM

- No of address line = 14

Memory map (Abstruse decoding) **(1M)**

EPROM

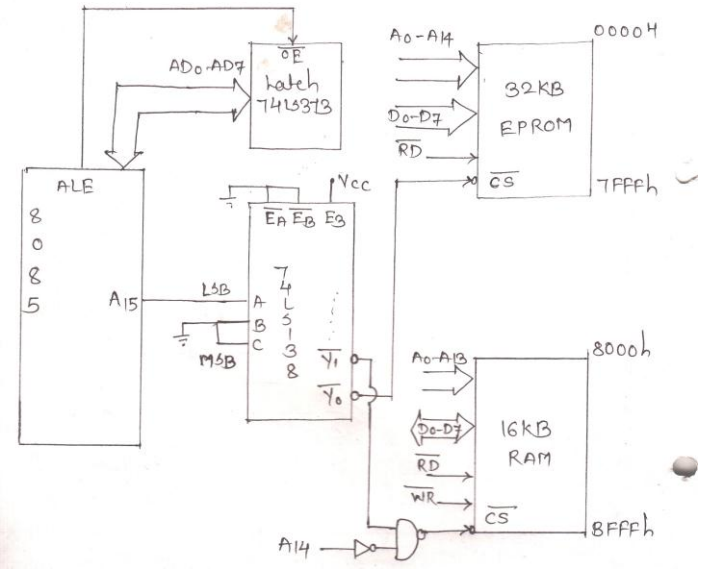
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Starting address = 0000H end address = 7FFFH

RAM

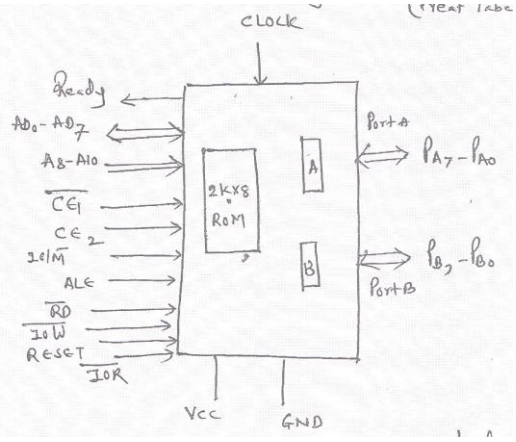
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Standing address = 8000H end address = BFFFH.



b) Draw the block diagram of 8355.

Ans:



c) What is meant by memory interfacing? State signals of microprocessor used for

i) RAM

ii) ROM memory interfacing

Ans: (Memory interfacing 2M, 1M RAM signal, 1M ROM signal)

Memory Interfacing

Memories provide storage area for both programs and data. The CPU executes the instruction stored in the memory & can store result in the Memory so memories can be attached or connected with microprocessor through system buses i.e. address bus, data bus and control bus known as memory interfacing.

Signal used for RAM & ROM

RAM	ROM
Chip select	Chip select
Read	Read / output enable
Write	
Data pins/ lines	Data pins / lines
Address Lines	Address Lines

d) Write the any four advantages of subroutines.

Ans: (Any Four – 1 Mark each)

Advantages of subroutines

1. Large programs are lined into modules.
2. Different modules of programs in the form of subroutine are written, tested and debugs separately.
3. It improves the efficiency or the program by reducing errors.
4. Repeated group of instruction are written into the subroutines are called whenever required in the main program.
5. It save memory space and reduce time, size of program.
6. It reduces the time of market.

e) How the basic control signals are generated in 8085?

Ans: **(Identification of signals 1M, Tables 3M)**

The basic control signals are generated using IO/M with S1, S0 Status Signals as follows.

Machine Cycle	**IO/M**	**S1**	**S0**	**Control Signal**
SP Code Fetch	0	1	1	$\overline{RD}$
Memory Read	0	1	0	$\overline{RD}$
Memory Write	0	0	1	$\overline{WR}$
I/O Read	1	1	0	$\overline{RD}$
I/O Write	1	0	1	$\overline{WR}$
Interrupt Acknowledge	1	1	1	$\overline{INTA}$
Halt	2	0	0	-
Hold/ Reset	2	X	X	-

f) Write an assembly language program to arrange the data available in memory location from 2000H to 2009H in descending order.

Ans: **(Program 4M, Student may use different logic)**

```
        MVI D, 0A      Ten byte data counter array length.

NEXT:   LXIB 2000H     Array initialization
        MVI E, 09H – Pass counter
Back :  LDAX B
        MOV L,A        L←  First number
        INX B          increment array Pointer
        LDAX B         A ←second number
        CMP L          Compare 'A'  & 'L' ('I' & 'A' no )
        JC Skip        'A' < 'L'    CF = 1

        DC X B
        STAX B
        INX B          Exchange the II & I number
```

```
        MOV A, L        and number and  store on array
        STAX B


    Skip : DCR E ----- Decrement counter
           JNZ  Back
           DCR D
           JNZ NEXT
           HLT
```

OR

```
           MVI D, OA
Next:      LXI H, 2000
           MVI C, 09
Up:        MOV A, M
           INX H
           CMP M
           JNC Skip
           MOV BM
           MIN M A
           DCX H
           MOV M, B
           INX H
Skip:      DCR C
           JNZ Up
           DCR D
           JNZ Next
           HCT
```

Q6 Attempt any four of the following: (16M)

a) Write the timer modes of 8155 and explain any one with the timing diagram.

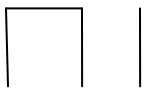
Ans: (2M for mode list 2M description of mode with timing diagram)

8155 timer has four modes

1) Mode 0 – Single square wave cycle
2) Mode 1 – Continuous square wave
3) Mode 2- single pulse on terminal count
4) Mode 3 – Continuous pulse at the end of terminal count

Mode 0 M_2 M_1 = 0 N = Count

In this mode the timer output remains high for half the count and row for remaining half of the counter



N/ 2 N/2

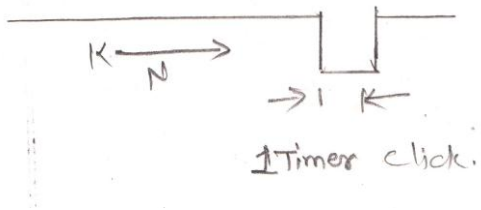
Mode 1 M_2 =0 M_1=0

N/2 N/2 N/2 N/2 N/2

In this mode timer O/P remains high for half and Low for half the period are repeated to generate the continuous square wave. The count is automatic reloaded.

Mode 2

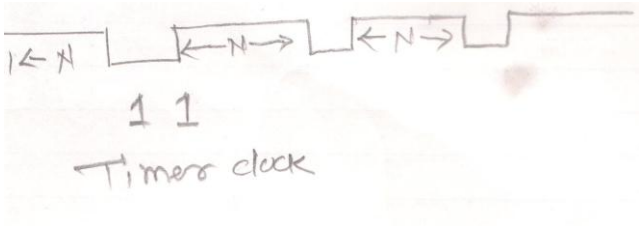
M_2= 1 M $_1$ = 0



This mode generates single clock pulse with variable on time. The pulse width is a function of clock frequency.

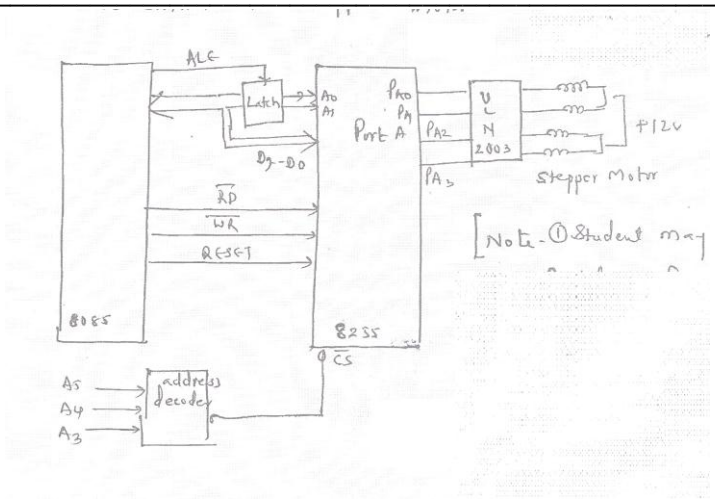
Mode 3 M_2 = 1 M_1 = 1

This mode generates pulse of the end of terminal count & repeated as shown in timing diagram



b) Draw a diagram to interface stepper motor to 8085 microprocceor using 8255 PPL. Write an 8085 assembly language program to control the stepper motor.
Ans: (2M for interfacing, 2 m for Program)

(Note 1 Student may use any port lines form PA, PB or PC
2. Motor driver transistor logic may be used
3. Program continues rotation; clockwise student may assume suitable data for program)



Look table
C100 – 0AH
C101 – 09H
C102 – 05H
C103- 06H

input for stepper motor 8255 CWR -8011 – all port in O/P & motor

Program

Label	Mnemonics	Comments
	LX1 SP D0004	
	MV1 A, 804 OUT CWR	8255 initialization
AGAIN :	LXI H, C100	Lookup table
	MV 1 B , 04H	Step counter for I/P
UP:	MOV A,M	
	OUT Port A	
	CALL DELAY	
	INH X	
	DCR B	
	JNZ UP	
	JMP AGAIN	
DELAY:	LXI D, FFFFH	
GO:	DCX D	
	MOV A,E	
	ORA D	
	JNZ GO	
	RE T	

c) List the addressing modes of 8085 microprocessor. Given example of one instruction for each addressing mode and explain it.

Ans: (any four modes with example 1* 4 =4 M)

1) Immediate addressing –
   MVI A, 99H
   A ← 99H
   The operand is the part of instruction
2) Register addressing mode :
   The operand is available in register 'B'
   e.g MOV A, B
   (A← B)
   ADD A, B
   (A←A+B)
3) Direct addressing : the address of operand is directly specified in the instruction
   Eg. LDA 2000H A← (20004)2w0h- direct address of
   STA 200H A → (2000H) Operand
   LHLD 2000H
   SHLD 2000H

4) Indirect addressing mode: The address of the operand is available in register pair and register pair is the part of instruction.

E g. LDAX B A← (BC)
STAX B A → (BC) } Address of operant is available in BC register Pair

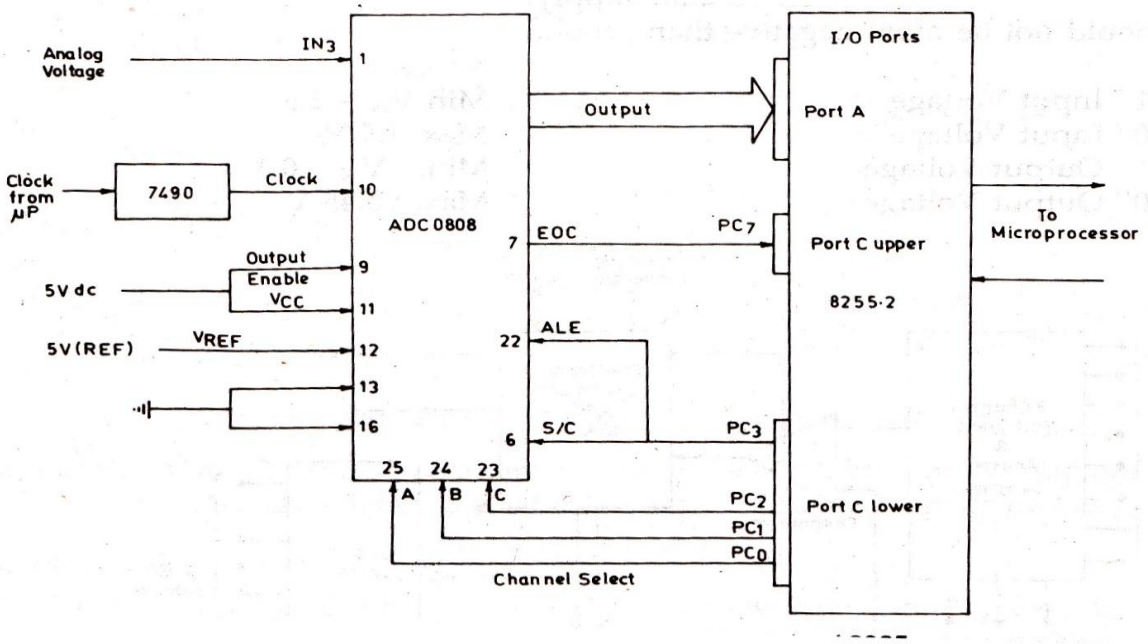
5) Implied address / Inherent: The operand is defined in opcode itself.
6) Eg. CMA - A← $\overline{A}$
   RAL Rotate Accumulator left

d) Draw the interfacing of 8 bit ADC 0808 with microprocessor 8085 write a program to read the input from channel and store at address.

Ans: (2 M interface, 2 M program)

(Note -: interfacing parts student may select any part for O/P & I/P)

8255 – PA –IP CWR for 8255 = 984
PC Upper I/P channel – INO = 0
PC lower –O/P : ABC of ADC =000



Program

Program :-

Label	Mnemonics	operands	Comments
	MVI	A, 98	Initialise I/o ports of 8255.
	OUT	0B	
	MVI	A, 03	Switch on MUX. channel IN3
	OUT	0A	
	MVI	A, 0B	Start of conversion pulse without affecting mux. channel
	OUT	0A	
	MVI	A, 03	
	OUT	0A	Read EOC signal
READ :	IN	0A	
	RAL		
	JNC	READ	Is conversion over ? No, jump to READ.
	IN	08	Read digital o/p of ADC
	STA	FC50 H	Store the result.
	HLT		

e) Explain how information is exchanged between program counter and stack pointer. What are the contents of stack pointer register when a subroutine is called?

Ans: (2M for SPHL & PCHL 2M description subroutine flow)

There is no such instruction to read the stack pointer. However the program counter PC is HL loaded with HL register by instruction 'PCHL' and the stack pointer is loaded with 'HL' register by instruction 'SPHL'

When subroutine is called the content of 'PC' is stored on stack & returned when submitting returns in the main program. The stack pointer hold the address of stack memory containing the information of main program address, content of registered pushed on stack etc.

f) Write the execution flow in steps for instruction CC 2200H.

Ans: (Instruction 1M, 3 M for step)

CC 2200H. Call on carry if carry flag sets CY = 1 then subroutine called form memory location 2200H.

Carry flag set CY= 1

1) Saves the content of program counter
2) Address of next instruction on stack
3) Decrements stack pointer register by two
4) Jumps to memory location '2200H'by loading 'PC' with 2200H.