MODEL ANSWER

SUMMER– 17 EXAMINATION

Subject Title: Microprocessor Subject Code: **17443**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. A) Attempt any SIX: 12

a) What are fetching and execution operations of microprocessor?

Ans :- (Proper valid reason- 2 mks)

Since the code and data is in external memory the microprocessor requires fetch and execute operations .Fetch operations can be for both code and data. Fetching code gets code into instruction decoder and fetching data puts data into internal register. Execution is done only for code after decoding instruction

b) Why it is necessary to multiplex data an address bus in 8085?

Ans:- (Proper valid reason- 2 mks)

Since only 40 pins were available due to limitation of IC technology and various functions need to be implemented address and data bus wee multiplexed to save the number of pins for other functions.

c) State the number of machine cycles and T-states required for the following instructions.
i) LDA 2500 H ii) SUBM

Ans:- (Each answer- 1 mks)

i) LDA is 3 bytes instruction will requires 1 opcode fetch machine (4T states) cycle followed by 3 memory read machine cycles each 3T states hence 13 states.

ii) SUB M is 1 byte instruction. It requires 1 opcode fetch (4T) and 1 memory read machine cycle and hence 7T states.

d) What is the necessity for interrupts controller?

Ans:- (Proper valied reason- 2 mks)

Since microprocessor have limited numbers of pins to serve external interrupts we require interrupt controller IC such as 8259 to expand the total number on interrupts that can be served by programming their priorities along with their masking requirements.

e) Define: Machine cycle.

Ans:- (proper definition – 2 mks)

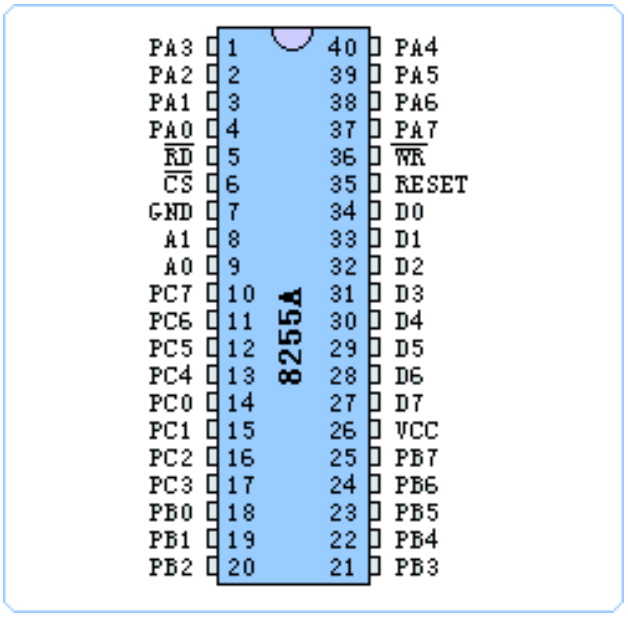
Machine cycle: It is defined as the time required to complete one operation of accessing memory, I/O, or acknowledging an external request.

4 types of machine cycles: (optional)

1. Op-code fetch
2. Memory read
3. Memory write
4. I/O read
5. I/O write

f) Draw pin configuration of 8255 A.

Ans:- (Proper pin diagram- 2 mks)



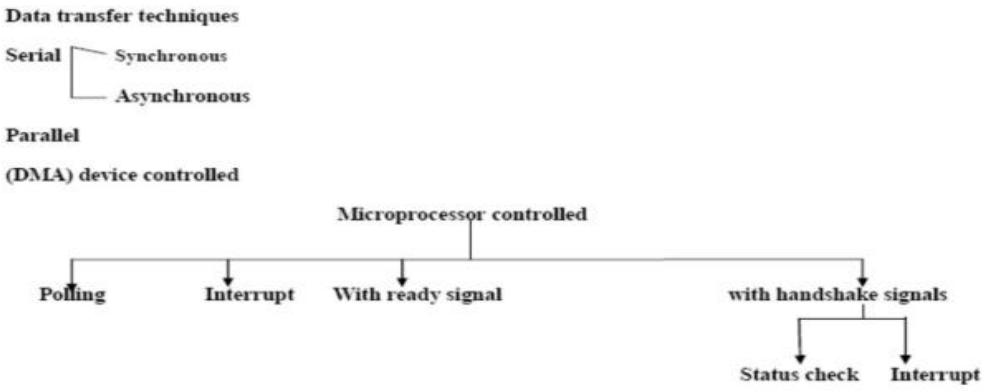
g) How the port 'C' is divided in Group A and Group B of 8255?

Ans:- (relevant answer-2 mks)

Port C has one 8-bit output latch and one 8-bit input buffer. Port C can be divided into two 4-bit ports using handshake mode. Each 4-bit port contains a 4-bit latch.
Group A: Higher four bits of Port C i.e. PC_4-PC_7 are used by Port A for handshaking signals and called as Port c upper, PC_U
Group B: Lower bits of Port C i.e. PC_0-PC_3 are used by Port B for handshaking signals and called as a Port C lower , PC_L

h) Classify the data transfer techniques.

Ans:-(Properclassification-

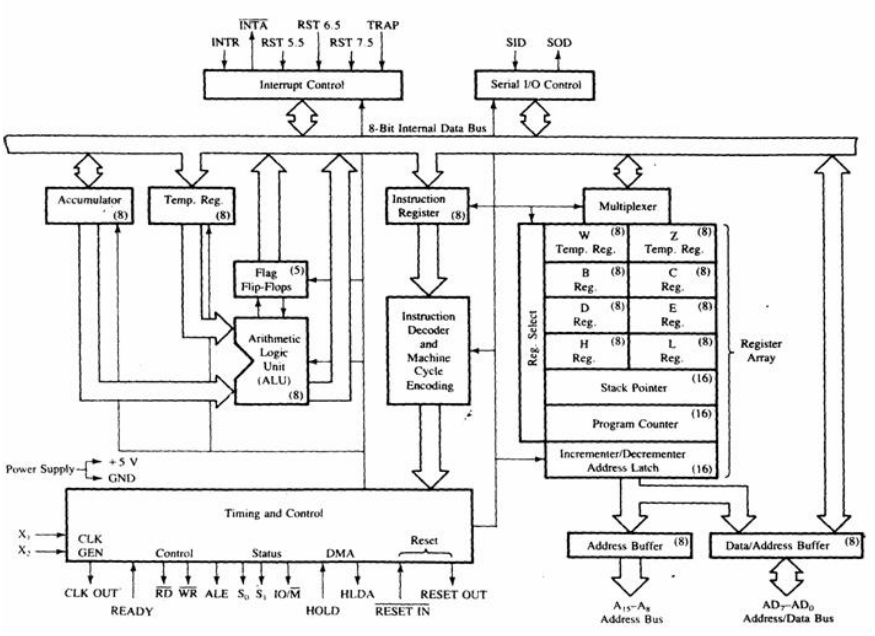


2mmks)

B) Attempt any TWO: 8

a) Draw the architecture diagram of 8085 microprocessor.

Ans:- (Proper complete diagram- 4 mks)



b) Write a program to get square of number 08H and the result must be in BCD format. Store the result into HL. Register pair.

Ans:- (Proper program with comments – 4 mks)

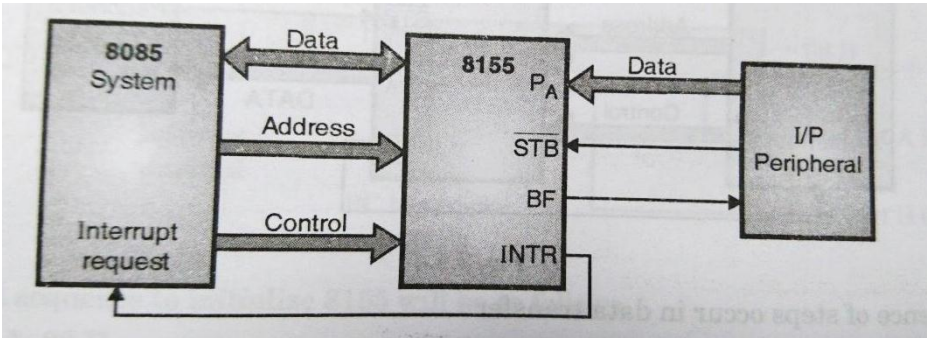
assume data 08H in memory location C050H

```
LXI H, C050H        ; loading pointer in HL pair
XRA A               ; clearing A
MOV C, M            ; transfer data 08 from memory to  C
UP: ADD  A          ; add C to A
DCR C               ; decrement counter
JNZ UP              ; check completion of C times addition
DAA                 ; adjust content of A in BCD
MOV L, A            ; move content in L
XRA A               ; clear A
MOV H, A            ; move content in H
HLT
```

c) Define handshake signals. Draw interfacing of 8155 port A in input mode with handshake signals.

Ans:- (Definition- 1 mks, interfacing -3 mks)

Handshake signals- Auxiliary signals required to transfer data asynchronously to processor are known as handshaking signals example buffer full (BF) and strobe (STB) in 8255.



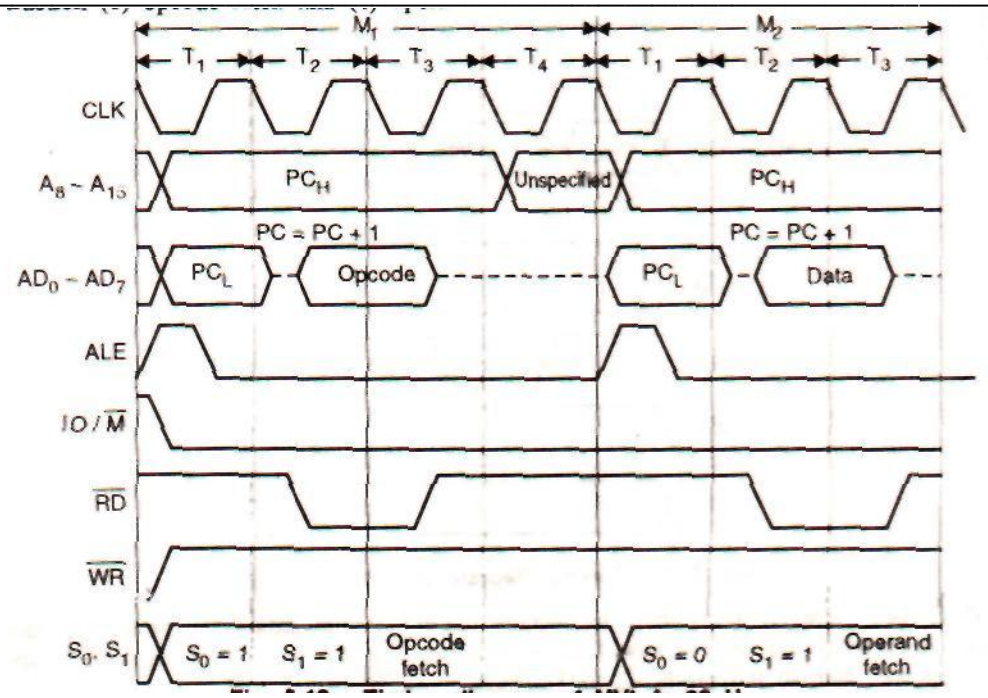
8155 input mode with handshake signals

2. Attempt any FOUR: 16

a) Draw the timing diagram of the instruction MVI A, 08H.

Ans:-(Timing diagram- 3 mks, explanation- 1 mks)

MVI A, 08H timing diagram consists of 2 machine cycles opcode fetch 4T states followed by memory read 3T states.



:-

b) Describe the functions of the following blocks of 8085 microprocessor.
I) General purpose register , II) Arithmetic logic unit.

Ans:-(Each function -2 mks)

i) General purpose register- Consists of various general purpose registers used for arithmetic and logical operations. It also contains PC (program counter) to keep track of the next instruction to be fetched from memory. SP (stack pointer) keeps the track of the stack implemented. Address incrementer/ decrementer latch is used to increment and decrement address as required.

ii) Arithmetic logic unit (ALU) 8 bit- Performs arithmetic and logical operation on the incoming data as per the instruction Performs arithmetic and logical operation on the incoming data as per the instruction decoded in the instruction decoder. Data is taken from the temporary register and accumulator. Result is stored as per the instruction decoded. Status of the result is given in the flag flip/flop.

c) What is subroutine? List any two advantages of subroutine. State any two instructions related to subroutine.

Ans:-Definition- 1 mks, any 2 advantages- 2 mks, any 2 instructions- 1mks)

In 8085 microprocessor a subroutine is a separate program written aside from main program, this program is basically the program which requires to be executed several times in the main program. The microprocessor can call subroutine any time using CALL instruction, after the subroutine is executed the subroutine hands over the program to main program using RET instruction.

Advantages of subroutines

1. Large programs are lined into modules.
2. Different modules of programs in the form of subroutine are written, tested and debugs separately.
3. It improves the efficiency or the program by reducing errors.
4. Repeated group of instruction are written into the subroutines are called whenever required in the main program.
5. It save memory space and reduce time, size of program.
6. It reduces the time of market.

Two instructions related to subroutine

1. RET
2. Jump
3. CALL

d) How SOD and SID pins can be used as a single bit output and input port respectively?

Ans:-(Each function-2 mks)

SOD (Serial Output data): When SIM instruction is executed, the content of MSB of accumulator is transferred to SOD pin. The instruction SIM is necessary to output data serially from the SOD line. It can be interpreted for serial output.

INSTRUCTIONS:

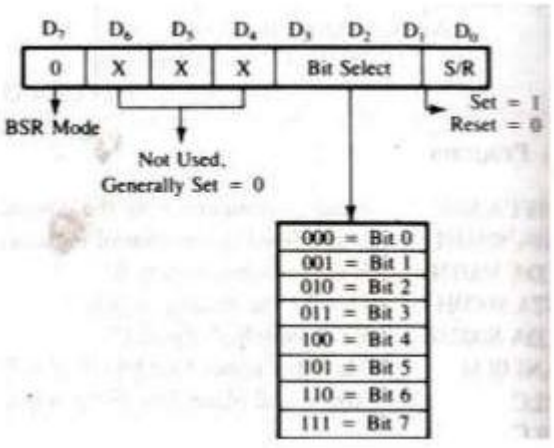
```
MVI A,80H        ;Set D7 in the accumulator = 1
RAR              ;Set D6 = 1 and bring Carry into D7
SIM              ;Output D7
```

SID (Serial Input data): When RIM instruction is executed, the content of SID pin is loaded into MSB of Accumulator. Instruction RIM is used to input serial data through the SID line. Instruction RIM can be interpreted for serial I/O. In the context of serial I/O, instruction RIM is similar to instruction IN, except RIM reads only one bit and places it in the accumulator at D7.

e) What is BSR mode of 8255? Write control word to set PC3 bit.

Ans:- (BSR- 1 mks, control word- 2 mks, CW to set PC3- 1 mks)

BSR- Is the bit set reset mode of 8255



MODIFY TO SET PC3

D7	D6	D5	D4	D3	D2	D1	D0
0	x	x	X	0	1	1	1

07H

MOV A, 07H

OUT CWR

f) Explain DMA controlled data transfer technique.

Ans:- (Need – 2 mks, diagram- 2 mks)

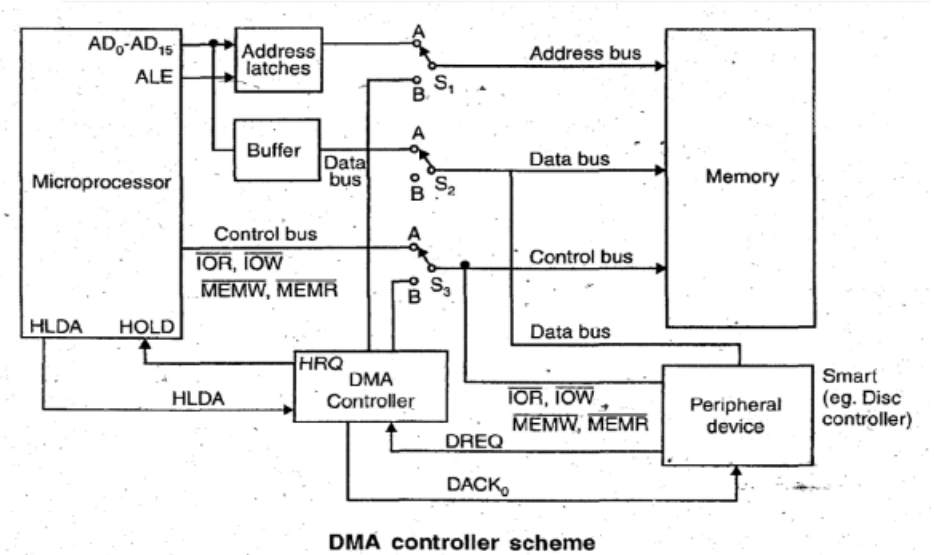
Need: In situation in which the microprocessor controlled data transfer is too slow, the DMA is generally used. E.g. data transfer between a floppy disk & R/W memory of the system.

In this data transfer method, the data transfer operation is carried out by the DMA controller which is another master in the microprocessor based system.

The data is transferred directly between I/O device and memory and data transfer is controlled by either I/O device or DMA controller.

Microprocessor does not participate in this data transfer method.

Whenever there is request from the I/O device, then DMA controller takes the control of all system buses i.e. address bus, data bus and control bus and perform data transfer operation directly between I/O device and memory.



DMA controller scheme

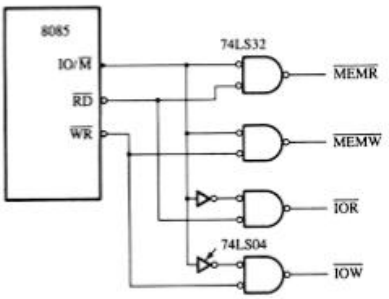
OR

3. Attempt any FOUR: 16

a) With the help of diagram, explain how control signals are generated in 8085.

Ans:- (Diagram- 2 mks, table- 2 mks)

The basic control signals are generated using IO/M with S1, S0 Status Signals as follows.



Machine Cycle	IO/M	S1	S0	Control Signal
SP Code Fetch	0	1	1	$\overline{RD}$
Memory Read	0	1	0	$\overline{RD}$
Memory Write	0	0	1	$\overline{WR}$
I/O Read	1	1	0	$\overline{RD}$
I/O Write	1	0	1	$\overline{WR}$
Interrupt Acknowledge	1	1	1	$\overline{INTA}$
Halt	2	0	0	-
Hold/ Reset	2	X	X	-

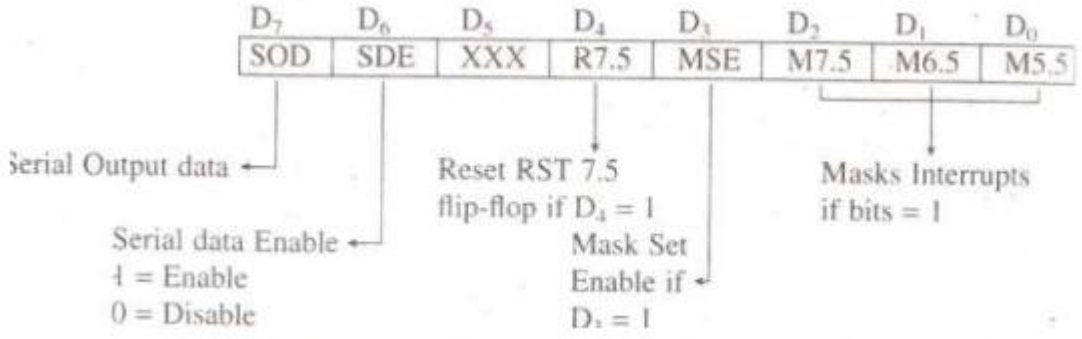
b) Write a program to add 98H and 9AH. The number 98H is in the memory location 2501 and 9AH is in 2502 H and the results are to be stored in 2503 and 2504 H.

Ans:- (Proper relevant program with comment – 4 mks)

```
LXI H, 2501H          ; Load pointer in HL pair
MOV A, M              ; transfer data 98H to A
INX H                 ; increment pointer
ADD M                 ; add data 9AH to A
JNC DOWN              ; check for carry
INX H                 ; increment pointer
MOV M, A              ; move result in 2503H
XRA A                 ; clear A
ORI 01H               ; set LSB of A for carry
DOWN: INX H           ; increment A
MOV M, A              ; transfer carry to 2504H as LSB
HLT
```

c) Draw and explain the format of SIM instruction.

Ans:- (diagram- 2 mks, explanation- 2mks)



Explanation-

SOD – Serial Output Data: Bit D7 of the accumulator is latched into the SOD output line and made available to a serial peripheral if bit D6=1;
SDE- Serial Data Enable: If this bit=1, it enables the serial output. To implement serial output, this bit needs to be enabled.
XXX- Don't care
R7.5-Reset RST 7.5 if this bit=1, RST 7.5 flip-Flop is reset. This is an additional control to reset RST 7.5.
MSE- Mask Set Enable: if this bit is high, it enables the functions of bits D2, D1, D0. This id master control over all the interrupt masking bits. If this bit is low, bits D2, D1 and D0 do not have any effect on the masks.
M7.5-D2=0, RST 7.5 is enabled
=1, 7.5 is masked or disabled
M6.5-D1=0, RST 6.5 is enabled
=1, 6.5 is masked or disabled
M5.5-D0=0, RST 5.5 is enabled
=1, 5.5 is masked or disabled

d) State what is memory mapped I/O? State its features (any two points).

Ans:- (Definition- 2 mks, any 2 features- 2 mks)

It is technique of interfacing I/O devices with microprocessor. I/O devices are identified as memory devices since I/O devices are selected when IO/M# pin is low.

Features:

i) I/O have 16 bit addresses.

ii)I/O devices can be accessed with memory based instructions such as LDAX.

e) Compare features of 8155 and 8255 (any two points).

Ans:- (any two relevant points – 4 mks)

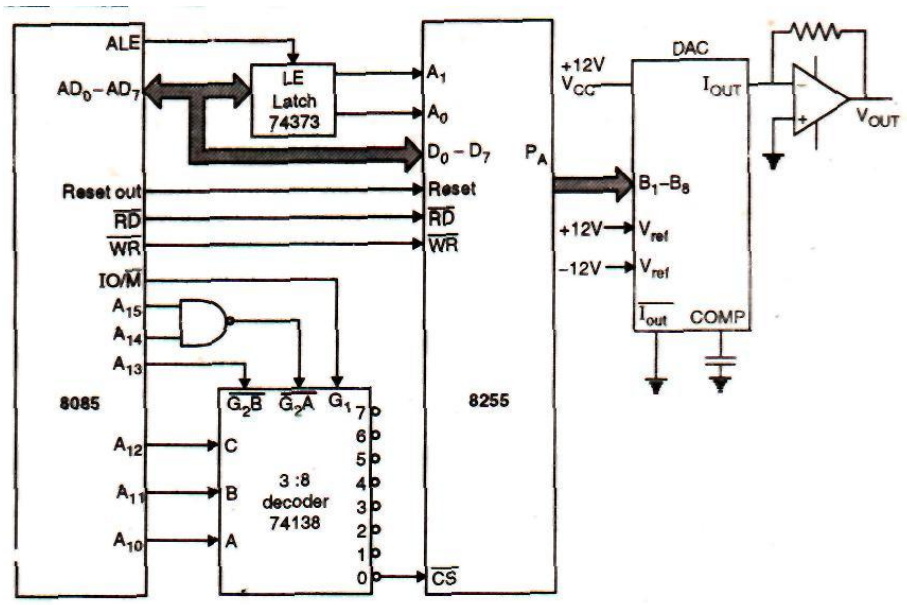
Sr. No.	8255	8155
1.	Three 8 bit I/O Ports i.e. Port A, Port B	Two 8 bit I/0 ports i.e. Port A, Port B and one
2.	No timer	Inbuilt 13 bit timer
3.	Separate data bus D_0-D_7 and address lines	Multiplexed AD_0-AD_7 bus
4.	IO/M, ALE signals are not available.	IO/M, ALE signals are available
5.	No memory	Inbuilt 256 byte of RAM

f) Draw and explain the interface diagram of DAC with 8085 microprocessor.

Ans:-(Diagram- 2 mks, explanation- 2 mks)

Explanation- DAC is interfaced to microprocessor through 8255 interface requires

1) Data bus of 8255 port A to be connected to the data bus of DAC.
2) Reference supply voltage of +12V and -12V
3) O/P is current proportional to input data bits.
4) I to V convertor using OPAM is implemented to obtain analog voltage.
5) Compensation capacitor is used at COMP input.



4. Attempt any FOUR: 16

a) State any eight features of 8085.

Ans:-(any 8 features- 4 mks)

It has 8 bit data bus, 8bit ALU. So it is 8 bit microprocessor.

- It has 16 bit address bus.
- It can access 64 kb external memory.
- It requires +5v power supply.
- It requires 6 MHz crystal oscillator. 3 MHz is operating frequency.
- It offers 5 hardware interrupts & 8 software interrupts.
- It supports DMA feature using HOLD & HLDA Pins.
- Serial communication is possible through the pins SID & SOD.

b) With examples describe ant four addressing modes of 8085.

Ans:- (Any four addressing modes with example- 4 mks)

ADDRESSING MODES OF 8085 INSTRUCTIONS

The ways in which the data is presented to an 8085 instruction is termed as its addressing modes

1) Immediate addressing mode: Data is directly given in an instruction itself. Data byte is immediate byte to opcode byte. Usually it leads to 2 byte instruction (8 bit data)/3 byte instruction (16 bit data).
MVI A, 02H LXI B, C050H

2) Register addressing mode: Data is transferred from one register (source register) to other register (destination register).Data in source register is maintained. Usually it leads to 1 byte instruction.
MOV A, B

3) Direct addressing mode: Address of data is directly given in an instruction itself. Address bytes are immediate byte to opcode byte. Usually it leads to 3 byte instruction.
LDA CO50H

4) Indirect addressing mode: Address of data is indirectly given in a register pair. Concerned register pair is mentioned in the instruction .Usually it leads to 1 byte instruction
LDAX D

c) Write a subroutine for 8085 to generate time delay of 100 µ sec (assume 320 nsec clock cycle).

Ans:- (proper program – 4 mks)

MVI C , N ; 7T states

BACK: DCR C ; 4T states

JNZ BACK 10/7T states

General delay equation for above code

Total T states=18+ 14(N-1)

Total T states required 100µs/320nsec =312.5=313 approx

Calculate N for 313 T states

313= 18+14(N-1)

N=22

MVI C , 16H

BACK: DCR C

JNZ BACK

d) Draw the block diagram of 8355.

Ans:- (Block diagram – 4 mks)

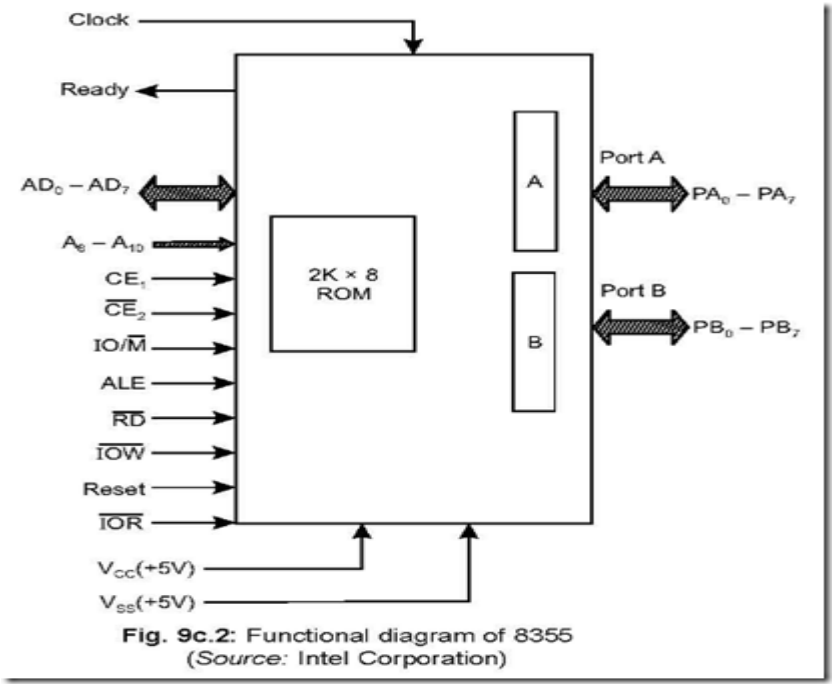


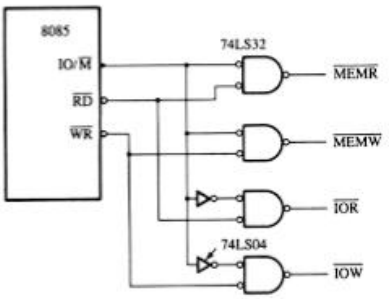
Fig. 9c.2: Functional diagram of 8355
(*Source:* Intel Corporation)

e) Which control signals are necessary in the memory mapped I/O? Explain.

Ans:- (Need – 2 mks, diagram- 2 mks)

In memory mapped I/Os I/O devices are mapped as if they are memory locations having 16 bit addresses. They use same control signals that are used by memory. They can be differentiated from memory only by the address.

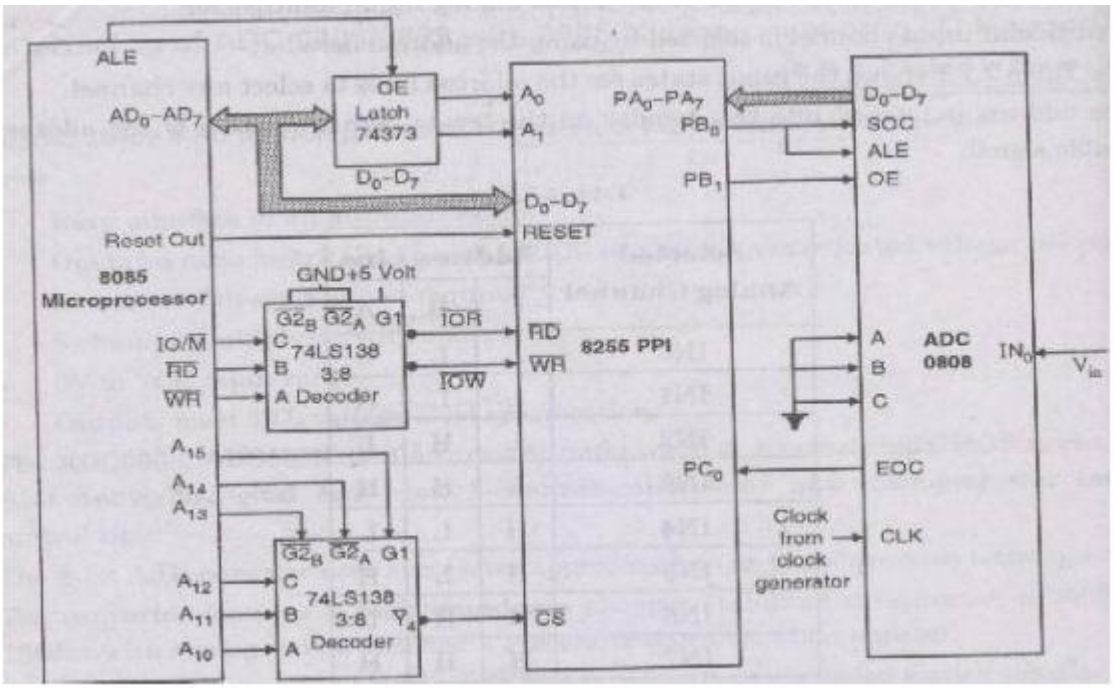
The basic control signals are generated using IO/M with S1, S0 Status Signals as follows.



As shown in above diagram memory mapped I/Os will use MEMR AND MEMW (both active low)

f) Interface the ADC to 8085 and write assembly language program to convert analog data to digital data.

Ans:- (Diagram- 2 mks, program- 2 mks)



Program- 8255 PORT ADDRESSESS

PORT A-90H

PORT-B -91H

PORT C -92H

CWR-93H

CWR CONFIGURATION

PORT A INPUT

PORT B OUTPUT

PORT C INPUT

1	0	0	1	X	0	0	1

91H

```
MVI A, 91H                    ; configure ports
OUT   93H                     ; A input, B output, C input
MVI A, 01H                    ; generate SOC high pulse
OUT   91H
XRA A                         ; generate SOC low pulse
OUT 91H
UP: IN 92H                    ; check for EOC
ANI 01H;
JZ UP;
MVI A, 02H                    ; generate OE
OUT  91H
IN 90H                        ; read data in port A
RET
```

5. Attempt any FOUR: 16

a) Describe any two conditional CALL and any two conditional JUMP instructions.

Ans:- (2 conditional call description – 2 mks, 2 unconditional call description – 2 mks)

In conditional CALL instruction, when the condition is true, then a CALL at NEW address is made. If condition is false then it will not have a CALL and will proceed for next instruction after it. Different conditional CALL instructions available:

1) CC- Call, if carry flag is set.
2) CNC - Call, if carry flag is reset.
3) CP - Call, if positive i.e. sign flag is reset.
4) CM - Call, if minus i.e. sign flag is set.
5) CPE - Call, if parity even i.e. parity flag is set.
6) CPO - Call, if parity odd i.e. parity flag is reset.
7) CZ - Call, if zero flag is set.
8) CNZ - Call, if zero flag is reset.

There is no call on auxiliary carry flag.

Conditional Jump instruction - The jmp instruction transfers execution control to a different point in the instruction stream; records no return information.

1) JC- Jump, if carry flag is set.
2) JNC - Jump , if carry flag is reset.
3) JP - Jump, if positive i.e. sign flag is reset.

4) JM - Jump, if minus i.e. sign flag is set.
5) JPE – Jump, if parity even i.e. parity flag is set.
6) JPO – Jump, if parity odd i.e. parity flag is reset.
7) JZ - Jump , if zero flag is set.
8) JNZ – Jump, if zero flag is reset.

b) Write the assemble language program to arrange the data available in memory location from 2000 H to 2009. H in descending order.

Ans:- (Proper program with comment—4 mks)

```
MVI D, 09H                  ; Load try counter
UP2: LXI H, 2000H           ; Load pointer to start of data
MOV C, D                    ; Load loop counter through try counter
UP1: MOV A, M               ; Load first data
INX H                       ; increment pointer
MOV B, M                    ; load next data
CMP B
JNC DOWN                    ; check whether upper number is small or big
MOV M, A                    ;exchange in memory if upper number is small
DCX H;
MOV M, B;
INX H;
DOWN: DCR C;
JNZ UP1;
DCR D;
JNZ UP2;

HLT
```

c) Describe vectored interrupts of 8085.

Ans:-(Table – 2 mks, explanation- 2 mks)

Vectored interrupts are interrupts , after its execution , the program execution is transferred to a particular vector location.

Interrupts which vector location i.e. starting address of interrupt service routine is pre-defined are known as vectored interrupts.

- These interrupts do not require $\overline{\text{INTA}}$ or any other acknowledge signal.
- TRAP & all RSTS are vectored interrupts

Interrupt	Priority	Vector Address
TRAP	1	0024H
RST 7.5	2	003CH
RST 6.5	3	0034H
RST 5.5	4	002CH
INTR	5	---------

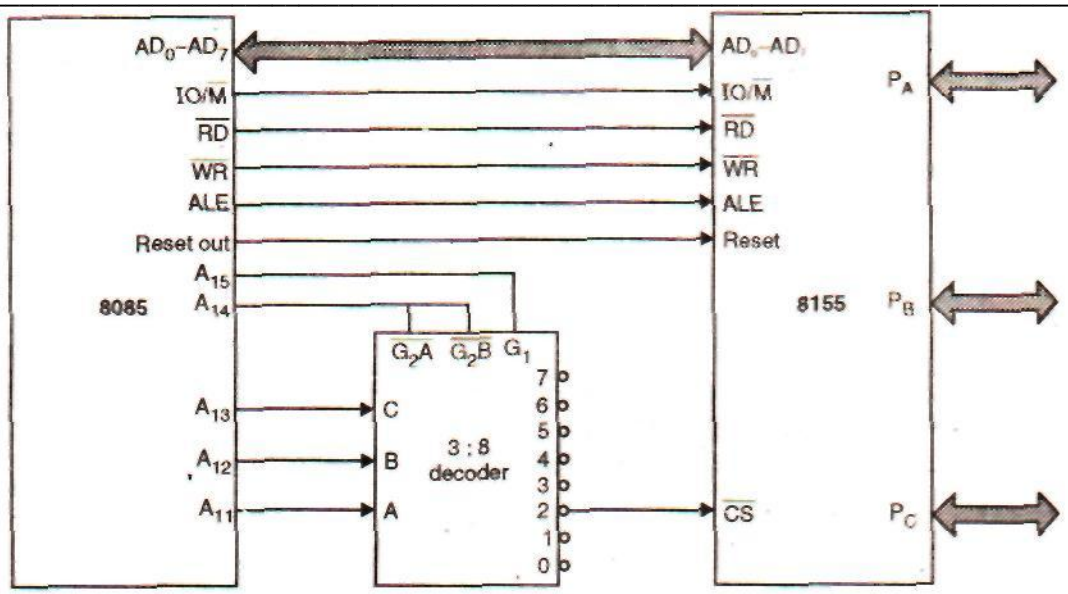
d) Compare I/O mapped I/O and memory mapped I/O (any four points).

Ans:- (Relevant four comparison- 4 mks)

Parameters	Memory mapped I/O	I/O mapped I/O
Device address	16 bit	8 Bit
Control signals for i/p /O/P	MEMR/ MEMW	IOR /IOW
Instructions available	Memory related instruction STA; LDA ; STAX ; LDAX,MOV M,R ; ADD M ; SUB M ANA M etc.	In & Out
Data transfer	Between any register & I/O	Only between the I/O & the accumulator
Maximum no of i/o s possible	The memory map(64k) is shared between I/O s & system memory	The I/O map is independent of memory map; 256 input device can be connected.
Execution speed	12T- states (STA , LDA) 7T-states (MOV M,R)	10T - states
Hardware requirements	More hardware is needed to decode 16 bit address	Less- hardware is needed to decode 8bit address
Other features	Arithmetic or logical operations can be directly performed with I/O data	Not available.

e) Draw the neat labeled minimum system using 8085, 8155.

Ans:- (Proper relevant diagram – 4 mks)



f) Write timer mode of 8155 and explain any one with timing diagram.

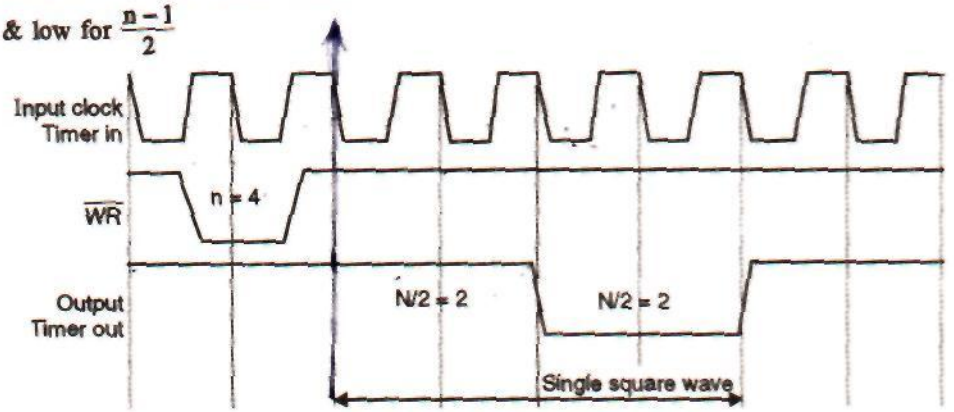
Ans:- (4 modes- 2 mks, explain any one- 2 mks)

8155 timer has four modes

1) Mode 0 – Single square wave cycle
2) Mode 1 – Continuous square wave
3) Mode 2- single pulse on terminal count
4) Mode 3 – Continuous pulse at the end of terminal count

M_2	M_1	
0	0	Mode 0 - Single square wave.
0	1	Mode 1 - Square wave.
1	0	Mode 2 - Single pulse on TC
1	1	Mode 3 - Pulse every TC

Mode 0 : Single square wave : In this mode, timer gives only one cycle of square wave, the output remains high for 1/2 count & remains low for 1/2 count. If the count is odd it remains high for $\frac{n+1}{2}$ & low for $\frac{n-1}{2}$



6. Attempt any FOUR: 16

a) Write the functions of following pins of 8085: HOLD, ALE, READY and reset.

Ans:- (Each function- 1 mks)

HOLD: HOLD pin is used by DMA to request microprocessor for release of bus for direct memory access. Upon receiving this signal microprocessor tristates its bus. Now bus is available for DMA.

ALE: It is used to signal latch to latch the address so that multiplexed bus is made available for incoming data.

Ready : This pin is input to microprocessor from wait state generator. Low on this pin indicates microprocessor to introduce wait state i.e. addition of one more T state for the response of slower device.

RESET: This pin is input to microprocessor. Low on this pin will suspend all the activities of microprocessor and it restarts fetching instructions from address 0000h

b) Write a program to transfer a block of data. The data is stored in memory from C550H to C55FH. The data is to be stored from C570H to C57FH in reverse order.

Ans:- (Proper program with comments- 4 mks)

```
MVI C, 0FH          ; Initialize count
LXI D, C550H        ; load pointer in DE register pair
LXI H C57FH         ; load pointer in HL register pair
UP: LDAX D
MOV M, A
INX D
DCX H
DCR C
JNZ UP
RET
```

c) Explain what operation will take place when the following instructions are executed.

j) PUSH ii) POP

iii) CALL iv) RETURN

Ans:- (Each 1 mks)

I) PUSH R_P

This instruction transfers the content of mentioned register pair on to the stack. This is done in following steps

- The SP is decremented by 1
- Contents of the higher part of register pair are transferred to the location pointed by SP.
- The SP is again decremented by 1
- Contents of the lower part of register pair are transferred to the location pointed by SP.

II) POP R_P

This instruction transfers the content of stack to mentioned register pair. This is done in following steps

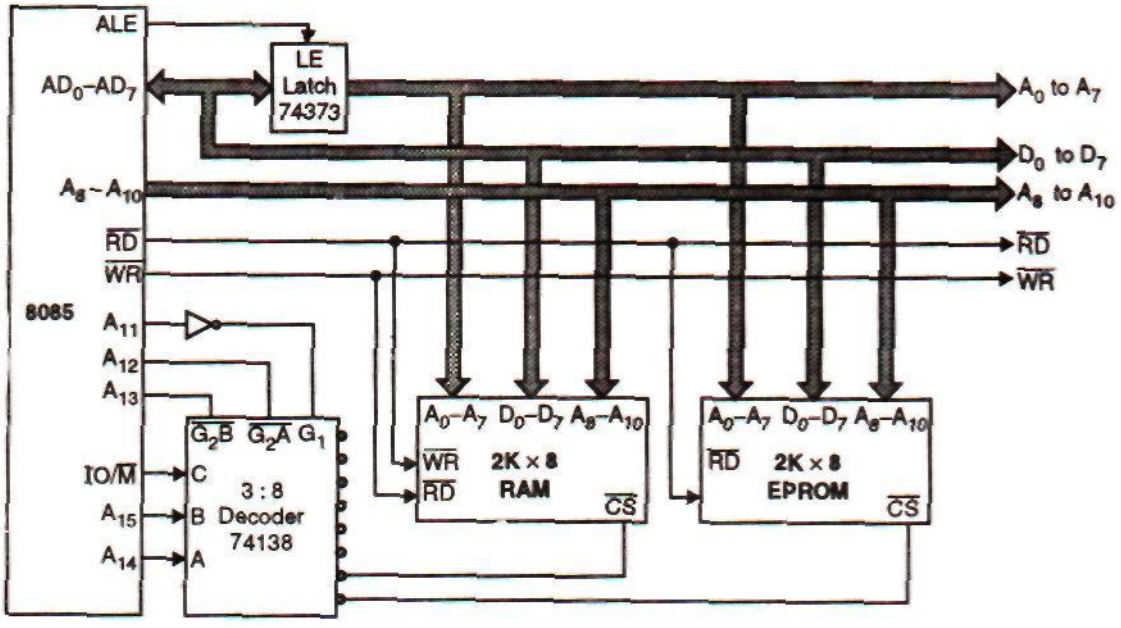
- Content of stack pointed by SP is transferred to lower order register from mentioned register pair.
- The SP is incremented by 1
- Content of stack pointed by SP is transferred to higher order register from mentioned register pair.
- The SP is incremented by 1

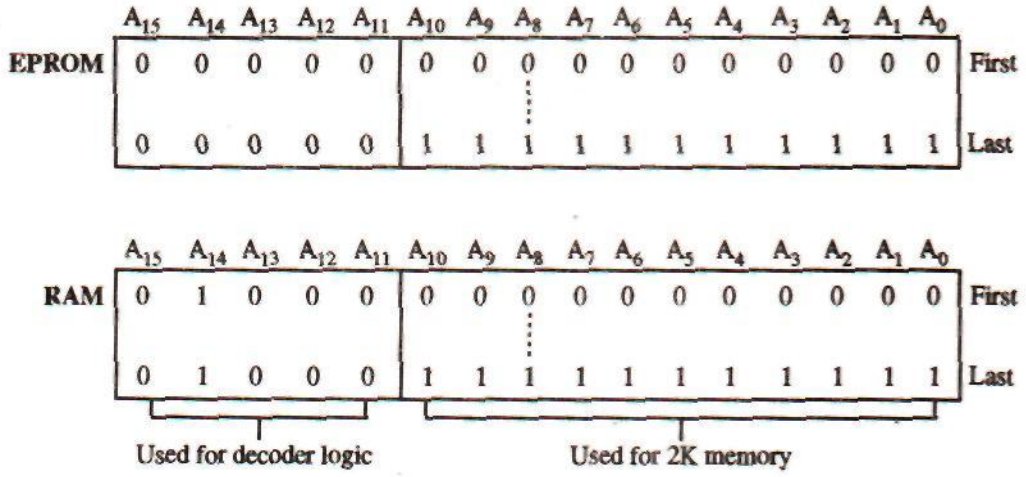
II) CALL: CALL instruction will transfer the control of program to target address i.e. enter the subroutine and store the return address on the stack.

iv) RETURN: This instruction will retrieve the return address from the stack and control will return back to main program.

d) Draw the diagram showing interface of 2 kbyte RAM and EPROM chips with 8085 microprocessor. State the memory map.

Ans:-(Diagram- 2 mks, memory map- 2 mks)





e) State different operating modes of 8255. Explain mode-2 in detail.

Ans:- (3 modes- 1 mks, explain mode 2- 1 mks for diagram, explanation- 2 mks)

8255 ports can operate in 3 different modes

1. mode 0 (group port A,B) simple I/O
2. mode1(group A,B) handshaking I/O and
3. mode2 bidirection(group A only)2 can poerate

Mode 2 is for group A for generating handshaking signals both for transmitting and receiving data .Following handshaking signal are generated as per shown in diagram.

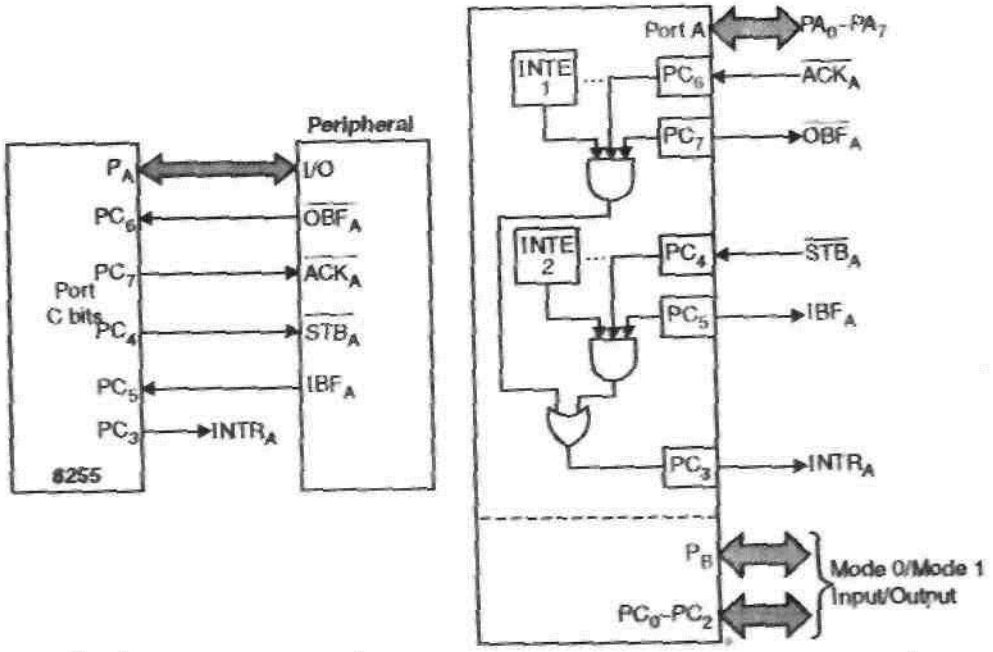
ACK_K(active low,input, PC6):This signal is used to acknowledge that the data is read from the port.

OBF_A(active low ,output, PC7): This signal is enabled when microprocessor write data into port.

STB_A(active low, input, PC4):This signal indicates that the data is written to the port.

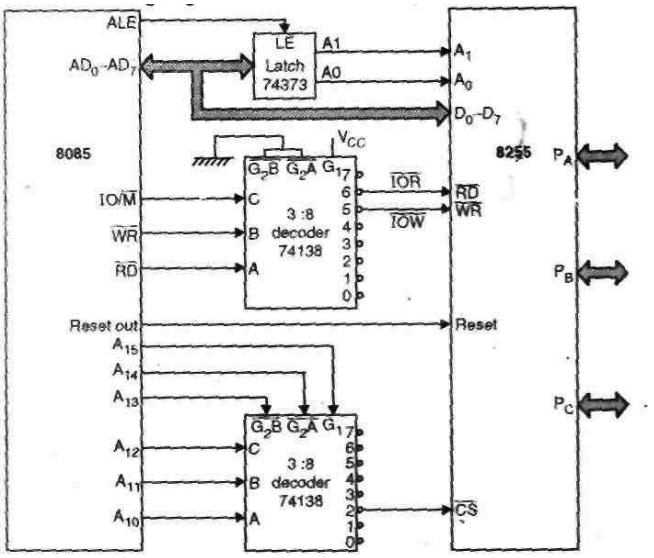
IBF_A(active high; output, PC5):This signal is enabled when data is available in port.

$INTR_A$(active high output,PC3):This signal is request to microprocessor for service i.e to read data from the port.



f) Draw interfacing of 8255 with 8085 microprocessor and explain it.

Ans:- (Diagram- 2 mks, explanation-2 mks)



Above diagram shows 8255 interfaced with 8085 in I/O mapped I/O mode. Address of various ports and CWR are also derived. 8255 requires demultiplexed address and data bus

Control signals are derived through 74138.Resetout of microprocessor is connected to reset of 8255. CS is generated again through 74138.

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_1	A_0		
1	0	0	0	1	0	0	0	= 88 H	Port A
1	0	0	0	1	0	0	1	= 89 H	Port B
1	0	0	0	1	0	1	0	= 8A H	Port C
1	0	0	0	1	0	1	1	= 8B H	Control word Register