Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

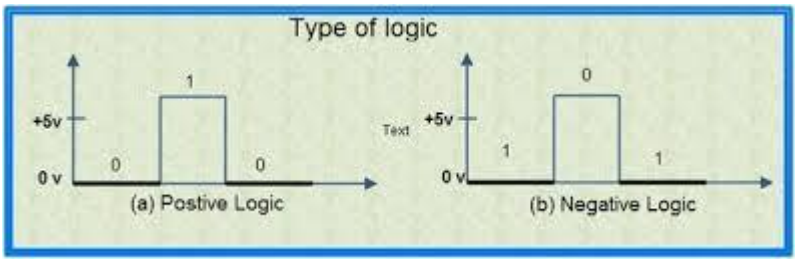
Q.1.

a) Attempt any six of the following: 12

i. What is positive logic and negative logic in digital system?
(Each for 1M)

Positive logic: A"LOW" voltage level represent "logic 0" state and a comparatively "HIGH" output voltage level represents "logic 1" state.

Negative logic:
A"LOW" voltage level represents "logic 1" state and a comparatively "HIGH" output voltage level represents "logic 0" state.



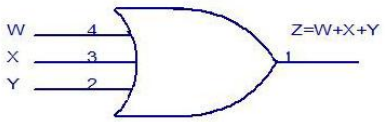
ii. Define fan in and noise margin.
(Each for 1M)

Fan in:
The number of inputs of a logic gate can handle.

Noise margin
A quantitative measure of noise margin is called as noise margin.

iii. Draw symbol and truth table of 3 input OR gate.
(Symbol 1M and truth table 1M)

3 Input OR Gate



TRUTH TABLE

INPUTS			OUTPUT
W	X	Y	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

iv. State De Morgan's theorem.
(Any one theorem 2M)
Theorem 1: $\overline{A+B} = \bar{A}.\bar{B}$

The theorem state that the, complement of a sum is equal to product of complements

Theorem 2: $\overline{\boldsymbol{A.B}} = \overline{\boldsymbol{A}} + \overline{\boldsymbol{B}}$
This theorem states that, the complement of a product is equal to addition of the complements.

v. Convert the following: (2M)
a*)** $(\mathbf{156})_{BCD} \rightarrow (?)_{BCD}$ ***and $(?)_2$

$(156)_{10} = (?)_{BCD}$ & $(?)_2$

2	156	0
2	78	0
2	39	1
2	19	1
2	9	1
2	4	0
2	2	0
	1	

1 → 0001
5 → 0101
6 → 0110

$(156)_{10} = (0001\ 0101\ 0110)_{BCD}$

$(156)_{10} = (10011100)_2$

vi. List any four Boolean laws.

(Any 4 – ½ M each)

OR Laws	AND Laws	Associative Law	Commutative Law	Distributive Law
A+0=A	A.1=A	(A.B)C=A.(B.C)	A.B=B.A	A.B+A.C=A(B+C)
A+1=1	A.0=0	(A +B)+C= A+ (B+C)	A+B=B+A	(A+B)(A+C)=A+BC
A+A=A	A.A=A			
A+$\bar{A}$=1	A.$\bar{A}$=0			

vii. Define encoder. Write the number of IC used as decimal to BCD encoder.
(Definition 1M, Number 1M)

Encoder is a combinational circuit which is designed to accept an n i/p digital word & converts it into m bit another digital word.

IC 74147-Decimal to BCD encoder

viii. Define any two specification of ADC.
(Any two specification of ADC 2M)

- **Analog input voltage**: This is the maximum allowable input voltage range
- **Input impedance**: Its value ranges from 1 kΩ to 1 MΩ depending upon the type of A/D converter. Input capacitance is in the range of tens of pF.
- **Linearity**: is conventionally equal to the deviation of the performance of the converter from a best straight line.
- **Accuracy**: the accuracy of the A/D converter depends upon the accuracy of maximum deviation of the digital output from the ideal linear line.
- **Monotoxicity**: In response to a continuously increasing input signal the output of an A/D converter should not at any point decrease or skip one or more codes. This is called the monotoxicity of A/D converter.
- **Resolution** is define as the maximum number of digital output codes. This is same as that of a DAC **Resolution= 2^n**

Resolution is defined as the ratio of change in the value of the input analog voltage V_A, required to change the digital output by 1 LSB.

Resolution= $\frac{V_{FS}}{2^n-1}$

Conversion Time:

It is the total time required to convert the analog input signal into a corresponding digital output.

Quantization Error:

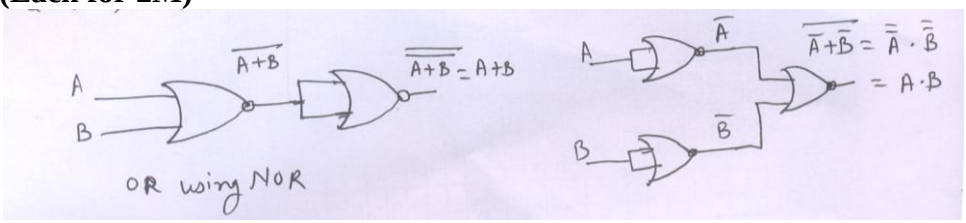
- This approximation process is called as quantization and the error due to the quantization process is called as quantization error.

b) Attempt any two: 8

i. Compare TTL and CMOS logic family on the basis of propagation delay, power dissipation, fan out and components used.
(Each for 1M)

Parameter	**TTL**	**CMOS**
Propagation Delay	10ns	70ns
Noise Margin	Moderate	High
Fan Out	10	20 - 50
Component use	Transistor and resistors	n-channel MOSFET p-channel MOSFET

ii. Design OR and AND gate using NOR gate only.
(Each for 2M)



iii. Perform the following binary subtraction using 2's complement:

1. $(54)_{10} - (33)_{10} = ?$ (2M)

1) $(54)_{10} - (33)_{10} = ?$

2	54	0
2	27	1
2	13	1
2	6	0
2	3	1
	1	

2	33	1
2	16	0
2	8	0
2	4	0
2	2	0
	1	

$(54)_{10} = (110110)_2$ $(33)_{10} = (100001)_2$

2's complement of $(33)_{10} = (100001)_2$

```
  011110
+     1
--------
  011111

  110110
+ 011111
--------
 1010101
```

Discard carry,
As final carry is generated ans. is positive
& in true form, $(10101)_2$

2. $(48)_{10} - (68)_{10} = ?$ **(2M)**

2) $(48)_{10} - (68)_{10} =$

2	48	0
2	24	0
2	12	0
2	6	0
2	3	1
	1	

2	68	0
2	34	0
2	17	1
2	8	0
2	4	0
2	2	0
	1	

$(48)_{10} = (110000)_2$ $(68)_{10} = (1000100)_2$

2's complement of $(1000100)_2$

$$\begin{array}{r} 0111011 \\ \quad\quad\quad 1 \\ \hline \textcircled{1}111100 \end{array}$$

$$\begin{array}{r} 0110000 \\ +0111100 \\ \hline \boxed{0}1101100 \end{array}$$

No carry – the result is negative & in its 2's complimnd form.

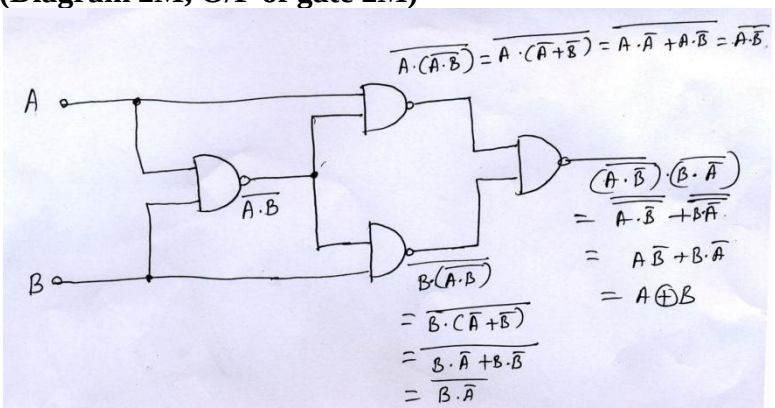
To convert ans. in true form

$$\begin{array}{r} 1101100 \\ - \quad\quad 1 \\ \hline 1101011 \end{array}$$

Taking 1's complimnd $-(0010100)_2 = -(20)_{10}$

Q.2. Attempt any 4: **16**

a) Draw X-OR gate using NAND gate only. Also write O/P of each gate. (Diagram 2M, O/P of gate 2M)



$\overline{A\cdot(\overline{A\cdot B})} = \overline{A\cdot(\overline{A}+\overline{B})} = \overline{A\cdot\overline{A}+A\cdot\overline{B}} = \overline{A\cdot\overline{B}}$

$= \overline{B\cdot(\overline{A}+\overline{B})}$

$= \overline{B\cdot\overline{A}+B\cdot\overline{B}}$

$= \overline{B\cdot\overline{A}}$

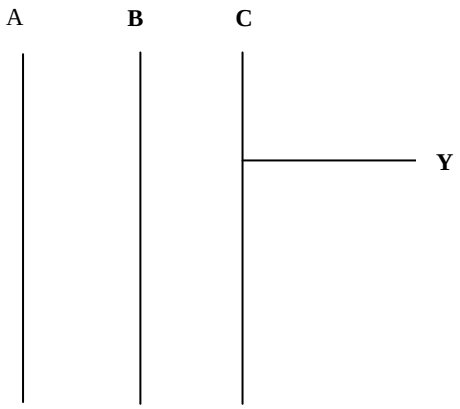
$= \overline{A\cdot\overline{B}}+\overline{B\cdot\overline{A}}$

$= A\overline{B}+B\cdot\overline{A}$

$= A \oplus B$

b) Simplify the following equation using Boolean laws and realize it using basic gate only. $Y = ABC + A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}\,C$
(Solution 2M, Gate 2M)
Solution

$Y = ABC + A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}\,C$
$Y = A(BC + \bar{B}C) + \bar{A}(BC + \bar{B}C)$
$Y = (A + \bar{A})(BC + \bar{B}C)$ ……. $A + \bar{A} = 1$
$Y = (1)(C(B + \bar{B}))$ ……. $B + \bar{B} = 1$
$Y = C$



c) Perform the following BCD arithmetic:
1. $(630)_{10} + (468)_{10}$ =?
2. $(245)_{10} + (186)_{10}$ =?

1. $(630)_{10} + (468)_{10}$ =? **(2M)**

1) $(630)_{10} + (468)_{10}$

630 → 0110 0011 0000
+ 468 → 0100 0110 1000
1010 1001 1000
Invalid BCD, Valid BCD, Valid BCD

For correction, add 6

1010 1001 1000
+ 0110 0000 0000
1 0000 1001 1000
↓ ↓ ↓ ↓
1 0 9 8

$(630)_{10} + (468)_{10} = (1098)_{10}$

2. $(245)_{10} + (186)_{10} = ?$ **(2M)**

2) $(245)_{10} + (186)_{10} =$

245 → 0010 0100 0101
+ 186 → 0001 1000 0110
0011 1100 1011
valid BCD, invalid BCD, invalid BCD

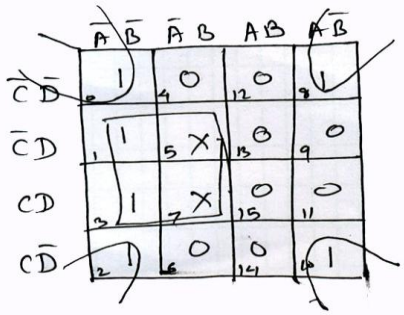
For correction, add 6 in invalid BCD

0011 1100 1011
+ 0000 0110 0110
0100 0011 0001
↓ ↓ ↓
4 3 1

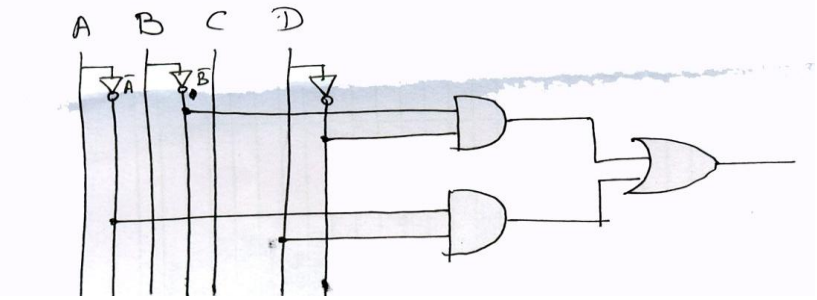
$\therefore (245)_{10} + (186)_{10} = (431)_{10}$

d) Simplify the following equation using k-map and realize it using logic gates.
$Y = \sum m(0,1,2,3,8,10) + \sum d(5,7)$ **(4M)**

$Y = \sum m(0,1,2,3,8,10) + \sum d(5,7)$



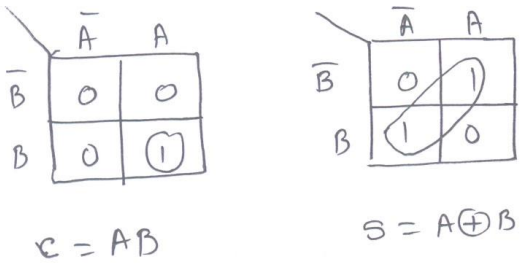
$Y = \bar{B}\bar{D} + \bar{A}D$

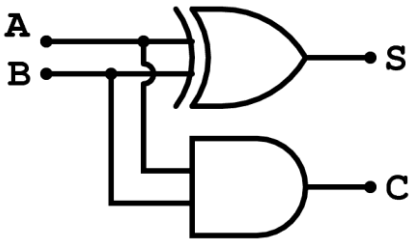


e) Design Half adder using k-map and basic gates.
(Truth Table 2M, k-map 1M, basic gates 1M)

Truth Table

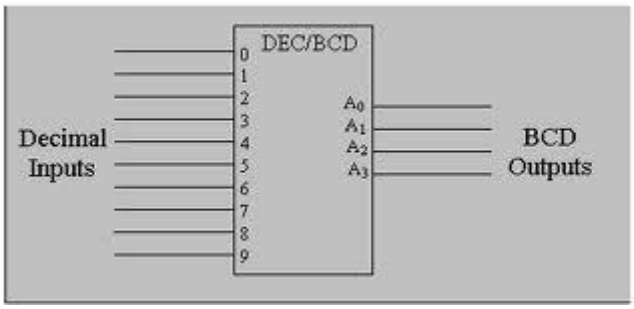
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0





f) Draw diagram of decimal to BCD encoder and write its truth table.

Decimal to BCD encoder: (2M)



Truth table: (2M)

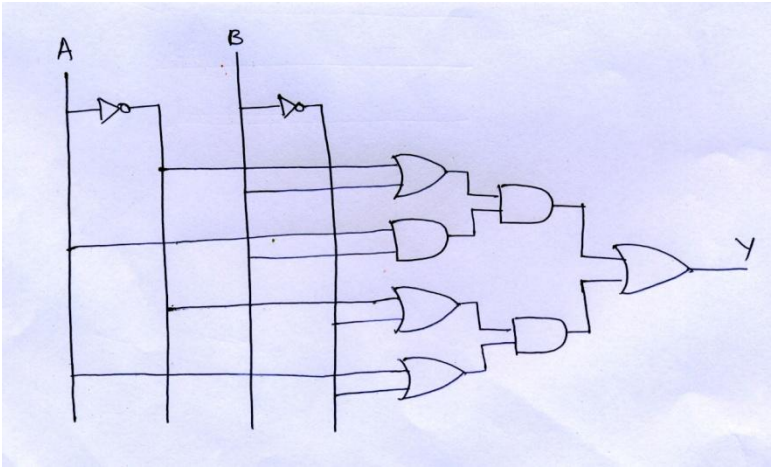
Input										Output			
D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

Q.3. Attempt any four: **16**

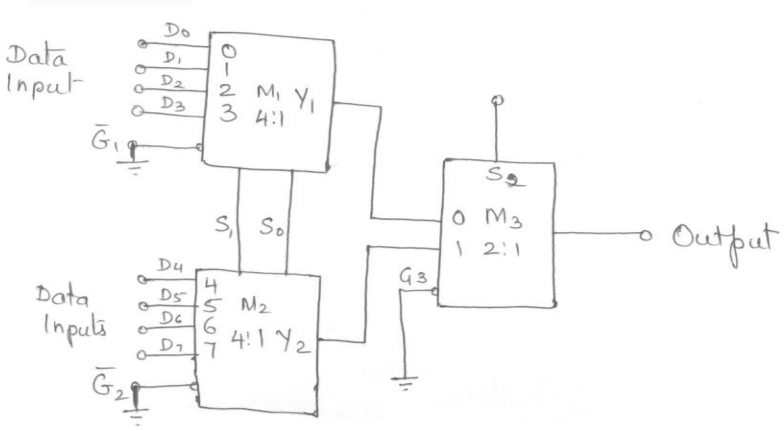
a) Simplify using De Morgan's theorem and realize it using basic gates. (Simplification 2M; Diagram 2M)

$$Y = \overline{(A\bar{B} + \bar{A}\bar{B})(AB + \bar{A}B)}$$

$$= \overline{(A\bar{B} + \bar{A}\bar{B})} + \overline{(AB + \bar{A}B)}$$
$$= (\overline{A\bar{B}}.\overline{\bar{A}\bar{B}}) + (\overline{AB}\,.\,\overline{\bar{A}B})$$
$$= (\bar{A} + B).(AB) + (\bar{A} + \bar{B})(A + \bar{B})$$



b) Design 8:1, MUX using 2:1 MUX and 4:1 MUX.
(Diagram 4M)

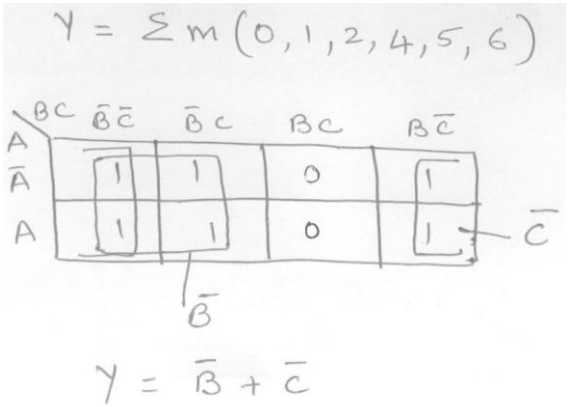


c) Minimize the following equation using k-map.

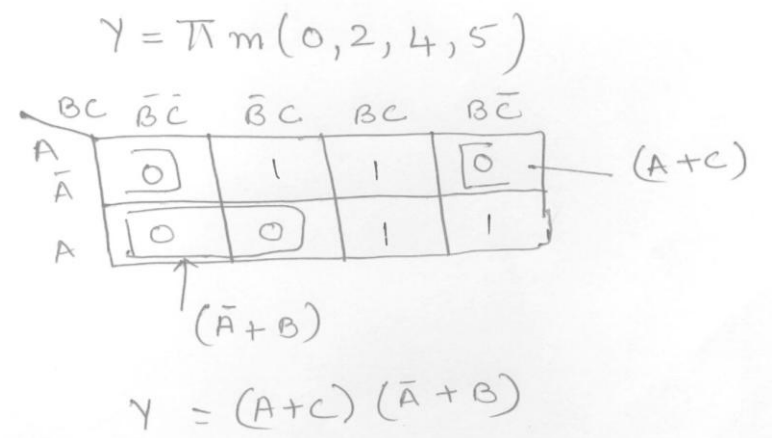
1. $Y = \sum m(0, 1, 2, 4, 5, 6)$
2. $Y = \Pi\, m(0, 2, 4, 5)$.

(Each for 2M)

1. $Y = \sum m(0, 1, 2, 4, 5, 6)$



2. $Y = \Pi\, m(0, 2, 4, 5)$.



d) Design 1:8 De Mux using basic gates.
(Truth Table 2M, circuit diagram 2M)

Depending on the combination of the select inputs S_2 S_1 S_0 the data input D_{in} is connected to one of the eight outputs.

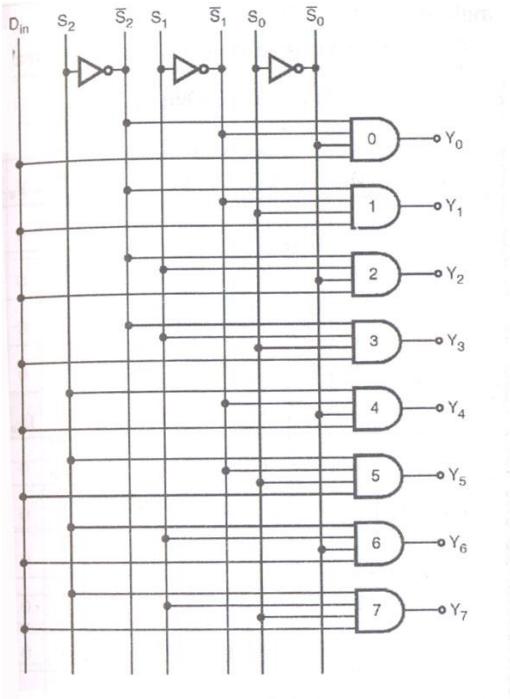
For example if S_2 S_1 S_0=1 1 0 then D_{in} is connected to output Y_6.

The truth Table

Enable	Select			Outputs							
E	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	×	×	×	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	D_{in}
1	0	0	1	0	0	0	0	0	0	D_{in}	0
1	0	1	0	0	0	0	0	0	D_{in}	0	0
1	0	1	1	0	0	0	0	D_{in}	0	0	0
1	1	0	0	0	0	0	D_{in}	0	0	0	0
1	1	0	1	0	0	D_{in}	0	0	0	0	0
1	1	1	0	0	D_{in}	0	0	0	0	0	0
1	1	1	1	D_{in}	0	0	0	0	0	0	0

Truth table for 1 : 8 demux

The circuit diagram of 1:8 demultiplexer



Logic circuit of a 1 : 8 demultiplexer

The circuit diagram of 1:8 demultiplexer

e) Explain different triggering method used in f.f.

(2 marks each)

Triggering is classified in to two types
1. Level Triggered
2. Edge Triggered

1. **Level triggering**:

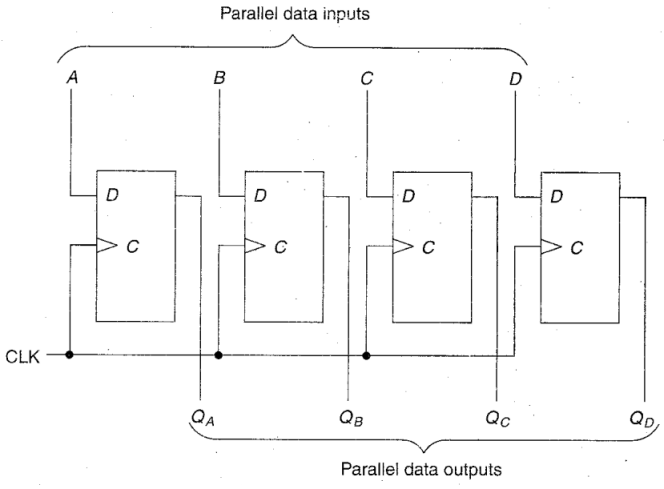
The latch or flip-flop circuits which respond to their inputs, only if their enable input (E) or clock input held at an active HIGH or LOW level are called as level triggered latches or flip flops. **Positive level triggered:** If the outputs of S-R flip flop response to the input changes, for its clock input at high (1), level then it is called as the positive level triggered S-R flip flop.

Negative level triggered FF: If the outputs of an S-R flip-flop respond to the input changes, for its clock input at low (0) level, then it is called as the negative level triggered S-R flip-flop.

2. Edge Triggering:

The flip-flop which changes their outputs only corresponding to the positive or negative edge of the clock input are called as edge triggered flip-flops. **Types of edge triggered flip-flops:** There are two types of edge triggered flip flops: **Positive edge triggered flip flops**: Positive edge triggered flip flops, will allow its outputs to change only at the instants corresponding to the rising edges of clock (or positive spikes). Its outputs will not respond to change in inputs at any other instant of time. **Negative edge triggered flip flops**: Negative edge triggered flip-flops will respond only to the going edges (or spikes) of the clock.

f) Explain working PIPO with neat logic diagram and timing diagram.
(Consider 2bit and 3bit also diagram 2M, explanation 2M)

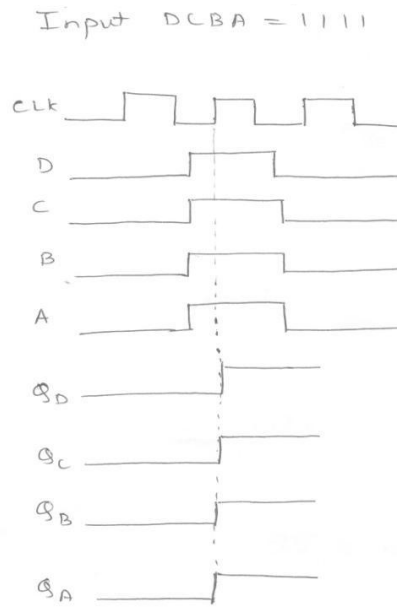


Working: In Parallel In-Parallel out Shift register, the data bits are entered simultaneously into their respective stages on parallel lines. The output data bits are also available on parallel lines. Immediately following the simultaneous entry of all data bits, the bits appear in the parallel outputs.

Truth Table

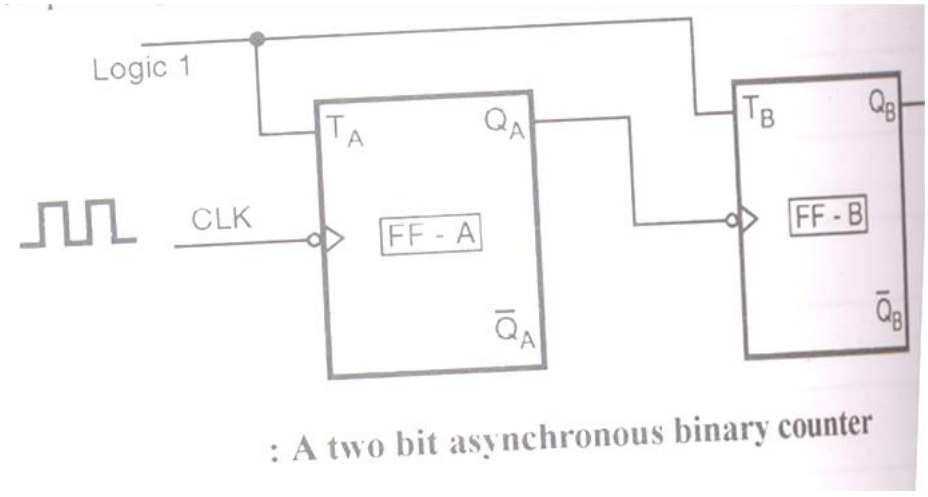
Inputs	Outputs			
ABCD	QA	QB	Qc	QD
1111	1	1	1	1

Timing diagram



Q.4. Attempt any four: 16

a) Explain working of 2 bit asynchronous counter with the help of neat diagram, truth table and timing diagram.
(Correct diagram using any other type of flip flop and its explanation may also be considered)
(Diagram2M; explanation 2M)



: A two bit asynchronous binary counter

Figure shows the logical diagram of a 2-bit ripple up counter. The number of flip flop used is 2. Thus the number of bits will always be equal to the number of flip-flops. A 4 bit counter will use four flip flops.

The toggle (t) flip flops are being used. But we can use the JK flip-flop also with J and K connected permanently to logic 1.
External clock is applied to the clock input of flip flop A an Q_A output is applied to the clock input of the next flip flop i.e. FF-B.

Initially let both the flip flop be in reset condition

$$\therefore Q_B Q_A = 00 - - - - initially$$

On the first negative going clock edge:

As soon as the first falling edge of the clock hits FF-A, it will toggle as TA=1. Hence Q_A will be equal to 1.
Q_A is connected to clock input of FF-B. Since Q_A has change from 0 to 1, it is treated as the positive clock edge by FF-B. There is no change in QB because FF-B is a negative edge triggered FF.
Hence after the first clock pulse the counter outputs are

$$\therefore Q_B Q_A = 01 - - - - After\ a\ first\ CLK\ pulse.$$

At the second falling edge at clock:

On the arrival of second falling clock edge FF-A toggles again to make Q_A=1.
This change in Q_A from 1 to 0 acts as a negative clock edge for FF-B. so it will also toggle, and Q_B will become 1
Hence after the second clock pulse the counter outputs are

$$\therefore Q_B Q_A = 10 - - - After\ a\ second\ CLK\ pulse$$

Note that both the outputs are changing their states. But both the changes do not take place simultaneously. Q_A will change first from 1 to 0 and then Q_B will change first from 0 to 1. This is due to the propagation delay of FF-A. so both flip-flops will never get triggered at the same instant. Therefore the counter is called as an asynchronous counter.

At the third falling edge at clock:

On arrival of the third falling edge, FF-A toggles again and Q_A become 1 from 0.since this is a positive going change, FF-B does not respond to it and remains inactive. So Q_B does not change and continues to be equal to 1.

$$\therefore Q_B Q_A = 11 - - - After\ a\ third\ CLK\ pulse$$

At the forth negative clock edge:

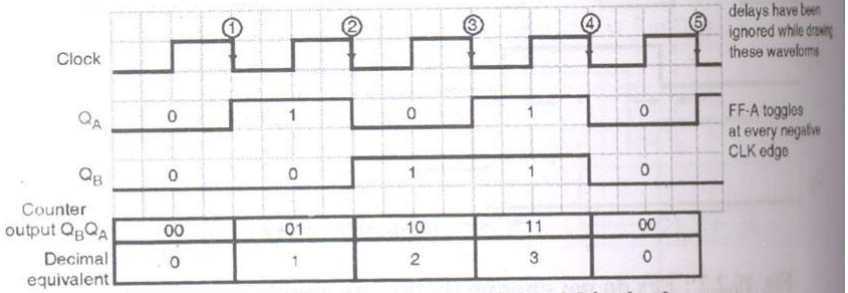
- On the 4th falling clock edge, FF-A toggles and Q_A change from 1 to 0.
- This negative change in Q_A acts as clock pulse for FF-B. Hence it toggles to change Q_B from 1 to 0.

$$\therefore Q_B Q_A = 00 - - - After\ a\ fourth\ CLK\ pulse$$

So the counter has reached the original state. The operation will now repeat.
Table summarizes the operation of the counter and fig shows the timing waveforms.

Table : Summary of operation of a 2-bit binary ripple counter

Clock	Counter outputs Q_B (MSB)	Counter outputs Q_A (LSB)	State number	Decimal equivalent of counter output
Initially	0	0	–	0
1st (↓)	0	1	1	1
2nd (↓)	1	0	2	2
3rd (↓)	1	1	3	3
4th (↓)	0	0	4	0

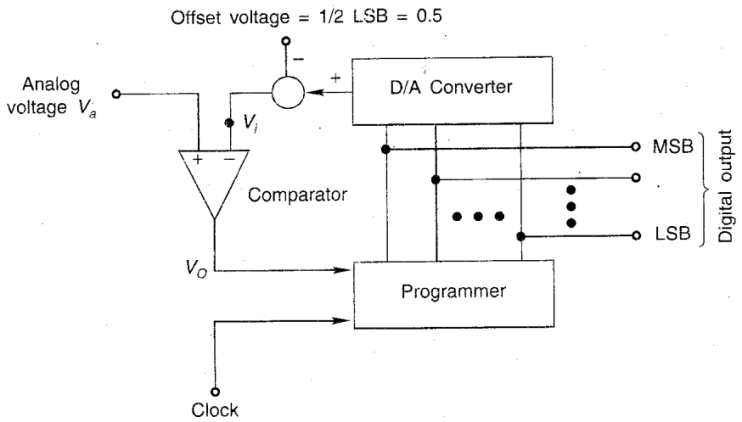


: Timing diagram for a 2 bit ripple counter

b) Explain successive approximation type ADC with neat diagram.

(Diagram2M; explanation 2M)

Block diagram



Working: The comparator serves the function of the scale, the output of which is used for setting/ resetting the bits at the output of the programmer. This output is converted into

equivalent analog voltage from which offset is subtracted and then applied to the inverting input terminal of the comparator. The outputs of the programmer will change only when the clock pulse is present. To start the conversion, the programmer sets the MSB to 1 and all other bits to 0. This is converted into analog voltage by the DAC and the comparator compares it with the analog input voltage. If the analog input voltage Va >= Vi, the output voltage of the comparator is HIGH, which sets the next bit also. On the other hand if Va <= Vi, Then the output of the comparator is LOW which resets the MSB and sets the next bit. Thus a 1 is tried in each bit of DAC until the binary equivalent of analog input voltage is obtained.

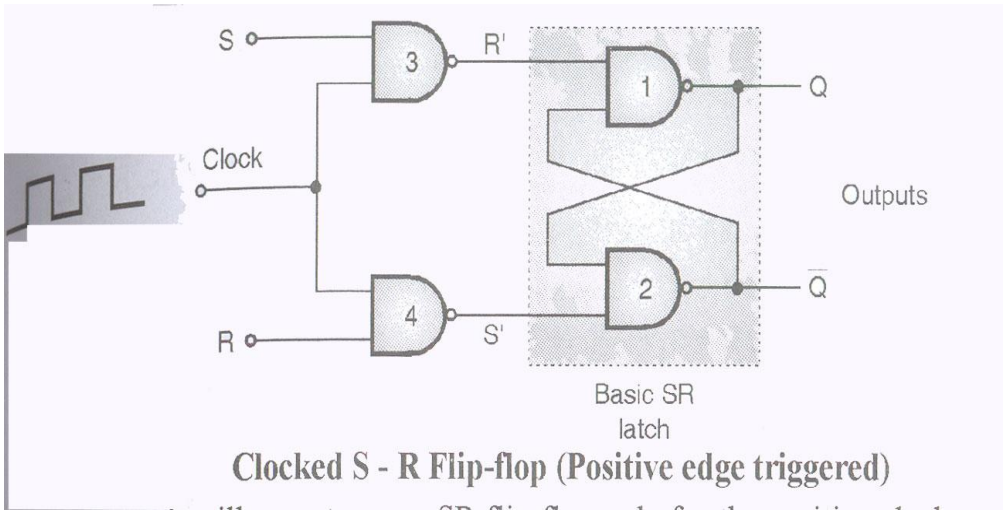
c) Describe working of SR ff using NAND gates only

(Diagram 2M, Truth Table 2M)
(Either positive edge triggered or negative edge triggered flip flop should be considered)
(Truth table with only for 4 conditions should also be awarded full marks)

The clocked SR flip flop is an edge triggered SR flip flop. It can be of two types.

1. **Positive edge triggered**
2. **Negative edge triggered.**

Positive edge triggered SR Flip Flop:



Clocked S - R Flip-flop (Positive edge triggered)

The positive edge triggered S-R flip Flop. It is also called as clocked SR FF.
This circuit will operate as an SR flip flop only for the positive clock edge but there is no change in output id clock=0 or even for the negative going clock edge.

Operation:

Case I: S=X, R=X, clock=0

- Since clock =0, the outputs of NAND gates 3 and 4 will be forced to be 1 irrespective of the values of S and R. that means R'= S'=1 these are the inputs of the latch.
- Hence the outputs of basic SR F/F i.e. Q and $\overline{Q}$ will not change in the output of the clocked SR flip flop.

Case II: S=X, R=X, clock=1(high level)

As this flip flop does respond not respond to levels applied at the clock input, the outputs Q and $\bar{Q}$ will not change. So $Q_{n+1} = Q_n \; and \; \bar{Q}_{n+1} = \bar{Q}_n$

Case III: S= R=0: No Change

- If S=R=0 then outputs of NND gates 3 and 4 are force to become 1.
- Hence R' and S' both will be equal to 1. Since S' and R' are the inputs of the basic S-R flip flop using NAND gates, there will be no change in the state of outputs.

Case IV: S=0 R=1, $clock \uparrow$

- Now S=0, R=1 and a positive edge is applied to the clock input.
- Since S=0, output of NAND -3 i.e. R'=1. And as R=1 and clock =1 the output of NAND-4 i.e. S'=0. Hence $\bar{Q}_{n+1} = 0 \; and \; \bar{Q}_{n+1} = 1$. This is the reset condition.

Case V: S=1 R=0, $clock = \uparrow$

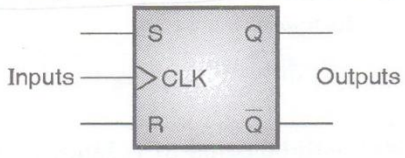
- Now S=1, R=0 and a positive going edge is applied to the clock input.
- Output of NAND 3 i.e. R'=0 and output of NAND 4 i.e. S' =1
- Hence output of SR flip flop is $Q_{n+1} = 1 and \; \bar{Q}_{n+1} = 0$
- This is the reset condition.

Case VI: S=1 R=1, $clock = \uparrow$

- As S=1, R=1 and clock=1, the outputs of NAND gates 3 and 4 both are 0. i.e. S'=R'=0.
- Hence the "Race" condition will occur in the basic SR flip-flop.
- The symbol of positive edge triggered SR flip flop is as shown in figure and the truth table.

Inputs			Outputs		Remark
CLK	S	R	Q_{n+1}	$\bar{Q}_{n+1}$	
0	×	×	Q_n	$\bar{Q}_n$	No change (NC)
1	×	×	Q_n	$\bar{Q}_n$	No change (NC)
↓	×	×	Q_n	$\bar{Q}_n$	No change (NC)
↑	0	0	Q_n	$\bar{Q}_n$	No change (NC)
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	Race	Race	Avoid

↓ = Negative edge of clock, ↑ = Positive edge of clock



- Note that for clock input to be at negative or positive levels as the edge triggered flip flop does not respond. Similarly it does not respond to negative edge of the clock.
- The flip flop will respond only to the positive edge of clock.
- With positive edge of the clock, the SR flip flop behaves in the following way:

$S = R = 0 \rightarrow$ No change in output

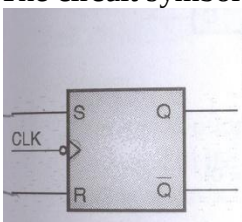
$S = 0, R = 1 \rightarrow Q_{n+1} = 0, \bar{Q}_{n+1} = 1$ Reset condition

$S = 1, R = 0 \rightarrow Q_{n+1} = 1, \bar{Q}_{n+1} = 0$ Set condition

$S = R = 1 \rightarrow$ Race condition.

Negative Edge Triggered S-R Flip Flop:

- The internal circuit (with NAND gates) of the negative edge triggered S-R flip flop is exactly same as that for the positive edge triggered one.
- The differentiator circuit is slightly modified in order to enable the flip flop for the negative (falling) edges of the clock input.
- The circuit symbol of the negative edge triggered S-R flip flop and its truth table.



(C-590)**Fig. 5.6.3 : Circuit symbol of negative edge triggered SR FF**

↑ = Positive edge of clock
↓ = Negative edge of clock

Inputs			Outputs		State	
CLK	S	R	Q_{n+1}	$\bar{Q}_{n+1}$		
0	×	×	Q_n	$\bar{Q}_n$	No change (NC)	FF is disabled
1	×	×	Q_n	$\bar{Q}_n$	No change (NC)	
↑	×	×	Q_n	$\bar{Q}_n$	No change (NC)	
↓	0	0	Q_n	$\bar{Q}_n$	No change (NC)	FF responds only to negative edges
↓	0	1	0	1	Reset	
↓	1	0	1	0	Set	
↓	1	1	Race	Race	Avoid	

d) What is race around condition? How to eliminate it?
(Explanation of condition 2M, Elimination 2 M)

Race around Condition

The Race Around condition occurs when J=K=1 i.e. when the FF is in the toggle mode.

Elimination of Race around Condition

Race around condition can be avoided using

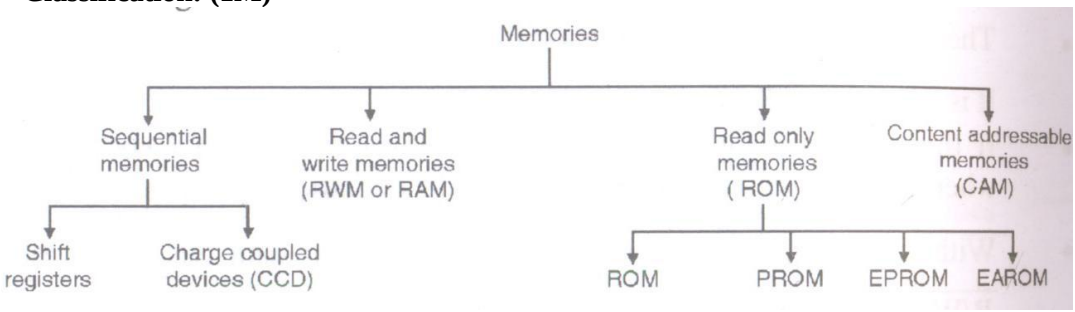
- Master Slave Flip Flop.
- Edge Triggered Flip Flop

e) Define memory. Give classification of memory. Compare PROM and EPROM (any 2).

Definition: (1M)

The sub system of digital processing system which provides the storage facilities is referred as memory. A flip flop is a one bit memory cell.

Classification: (1M)



(Any two point 2M)

PROM	**EPROM**
PROM stands for Programmable Read Only Memory	EPROM Erasable Programmable Read Only Memory
PROM can be programs only once	EPROM can be programmed and erased electrically
PROM chip is available without any data storage	EPROM chip is available with data storage.
PROM is suitable for storage of data which is of permanent nature	EPROM is suitable for storage of data which require changes.

f) What is the need of data converters? List specifications of DAC.

Need of data converters: (2 M)

It is often necessary that before processing the analog data, by a digital system, it should be changed to an equivalent digital form. Similarly, after processing the data, it may be desirable that the final result obtained in the digital form be converted back to the analog form. Therefore, data converters are necessary in digital systems.

A combinational digital circuit which converts the one form of data into the other or vice versa is called as data converter.

List any four specifications of DAC.

(Any 4 specification – 1/2 mark each specification) (2 M)

1. Resolution
2. Accuracy
3. Linearity
4. Temperature sensitivity
5. Settling time
6. Speed
7. Long term Drift
8. Supply rejection

Q.5. Attempt any four: **16**

a) Convert the following:

1. $(366.54)_8 \longrightarrow (?)_{10} and$
2. $(2015.32)_{10} \rightarrow (?)_{16}$

(Each for 2M)

1) $(366.54)_8 \rightarrow (?)_{10}$

$366 \rightarrow 3\times8^2 + 6\times8^1 + 6\times8^0$

$= 192 + 48 + 6$

$= (246)_{10}$

$0.54 \rightarrow$

$0.54 \times 8 = 4.32 \rightarrow 4$

$0.32 \times 8 = 2.56 \rightarrow 2$

$0.56 \times 8 = 4.48 \rightarrow 4$

$\therefore (366.54)_8 = (246.424)_{10}$

2) $(2015.32)_{10} \rightarrow (?)_{16}$

16 | 2015	15	F
16 | 125	13	D
16 | 7	7	
0		

$(7DF)_{16}$

$0.32 \rightarrow$

$0.32 \times 16 = 5.12 \rightarrow 5$

$0.12 \times 16 = 1.92 \rightarrow 1$

$0.92 \times 16 = 14.72 \rightarrow E$

$(.51E)_{16}$

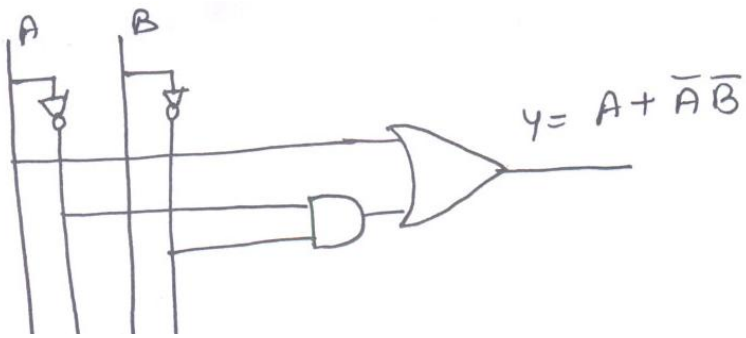
$\therefore (2015.32)_{10} = (7DF.51E)_{16}$

b) Compare combinational logic circuit and sequential logic circuit (any 4 pts)
(Any 4 pts 4M)

Combinational logic	**Sequential logic**
The combinational logic circuit consists of logic gate only	Sequential logic circuit consists of combinational logic circuit along with memory for storage of information
It operation depend upon present input and does not required history of inputs	It operation depend upon present input as well as last state of input and output which are stored in memory.
Easy to design due to lack of memory.	Difficult to design due to presence of memory.
Faster in speed as all inputs are primary inputs are applies simultaneously	Slower in speed because of secondary inputs
E.g. Encoders, decoders, multiplexer, demultiplexer etc	E.g. counters, shift registers flip-flop etc

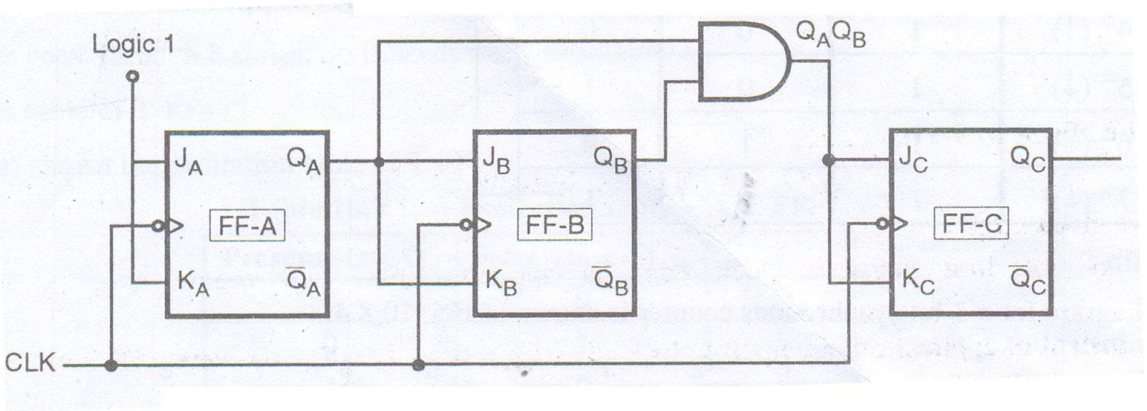
c) Simplify the following and realize it.
(Simplification 2M, Diagram 2M)

$$Y = A + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C} + ABC + \overline{A}\overline{B}$$
$$= A(1 + BC) + \overline{A}\overline{B}(c + \overline{C} + 1)$$
$$= A + \overline{A}\overline{B}$$



d) Explain working of 3 bit synchronous counter with the help of neat logic diagram, timing diagram and truth table.

(2 M Logical Diagram, 1 M Explanation, 1 M Timing Diagram)



Operation:

Initially all the FFs are in their reset state. $Q_c\ Q_B Q_A = 000$

1st Clock pulse:

- FF-A toggles and Q_A becomes 0.But since Q_A =0 at the instant of application of 1st falling clock edge, J_B=K_B=0 and Q_B does not change state ∴ $Q_B\ remains\ 0$.
- Similarly Q_C also does not change state ∴ $Q_C = 0$.

$$Q_A Q_B Q_C = 001 \ldots\ldots\ldots after\ 1st\ clock\ pulse$$

2nd Clock pulse:

- FF-A toggles and Q_A becomes 0.
- But at the instant of application of 2nd falling clock edge Q_A was equal to 1.Hence, J_B=K_B=1. Hence FF-B will toggle and Q_B becomes 1.
- Output of AND gate is 0 at the instant of negative clock edge. So J_C= K_C =0. Hence Q_C remains 0.

$$\therefore Q_A Q_B Q_C = 010 \ldots\ldots\ldots after\ 2nd\ clock\ pulse$$

3rd clock pulse:

- After the 3rd clock pulse, the output are $Q_CQ_BQ_A$=011

4th clock pulse:

- Note that Q_B =Q_A= 1. Hence output of and gate= 1 and J_C=K_C=1, at the instant of application of 4th negative edge of the clock.
- Hence on application of this clock pulse, FF-C will toggle and Q_C changes from 0 to 1.
- FF-A toggles as usual and Q_A becomes 0.
- Since Q_A was equal to 1 earlier, FF-B will also toggle to make Q_B=0.

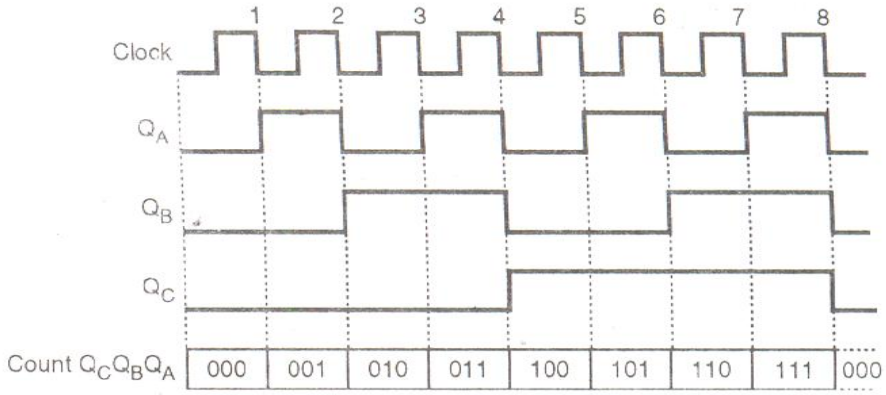
$$\therefore Q_CQ_BQ_A = 100 \quad \ldots\ldots\ldots After\ the\ 4th\ clock\ pulse$$

- Thus the counting progresses.
- After the 7th clock pulse the output is 111 and after the 8th clock pulse, all the flip-flops toggle and change their outputs to 0. Hence $Q_CQ_BQ_A$=000 after the 8th pulse and the operation repeats.

Clock	Q_C	Q_B	Q_A
0	0	0	0
1st (↓)	0	0	1
2nd (↓)	0	1	0
3rd (↓)	0	1	1
4th (↓)	1	0	0
5th (↓)	1	0	1
6th (↓)	1	1	0
7th (↓)	1	1	1

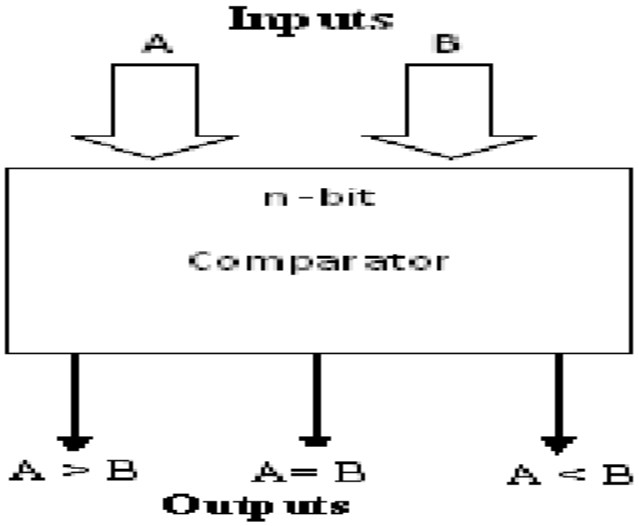
On 8th pulse counter returns to the all 0 state

Timing Diagram



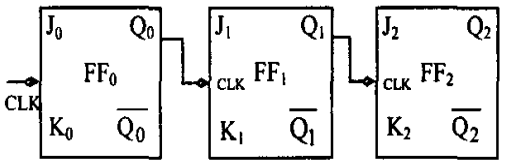
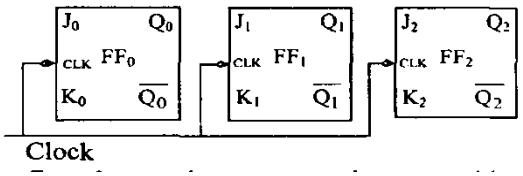
e) Describe block diagram of digital comparator and write truth table of 2 bit comparator.

- Digital comparator is a combinational circuit which compares two numbers, A and B; and evaluates their relative magnitudes.
- The outcome of the comparison is given by three binary variables which indicate whether
- A = B or A > B or A < B.
- Depending on the result of comparison one of these outputs will go high.



Inputs				Outputs		
A1	A0	B1	B0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

f) Compare synchronous and asynchronous counter. (any four points)
(any four points 4M)

SR. No.	Asynchronous Counter	Synchronous Counter
1.	In an Asynchronous Counter the output of one Flip Flop acts as the clock Input of the next Flip Flop.	In a Synchronous Counter all the Flip Flop's are Connected to a common clock signal.
2.	Speed is Low	Speed is High
3.	Only J K or T Flip Flop can be used to construct Asynchronous Counter	Synchronous Counter can be designed using JK,RS,T and D FlipFlop.
4.	Problem of Glitch arises	Problem of Lockout
5.	Only serial count either up or down is possible.	Random and serial counting is possible.
6.	Settling time is more	Settling time is less
7.	Also called as serial counter	Also called as Parallel Counter
8.		

Q.6. Attempt any Two:

a)

i. Convert the following SOP equation into standard SOP equation.
$\boldsymbol{Y = AB + \bar{A}B + A\bar{B}\bar{C}.}$

Solution: (2M)

$$Y = AB + \bar{A}B + A\bar{B}\bar{C}$$

$$Y = AB(C + \bar{C}) + \bar{A}B(C + \bar{C}) + A\bar{B}\bar{C}$$

$$Y = ABC + AB\bar{C} + \bar{A}BC + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

ii. List any four applications of multiplexer and implement the following logic expression using 16:1 MUX.

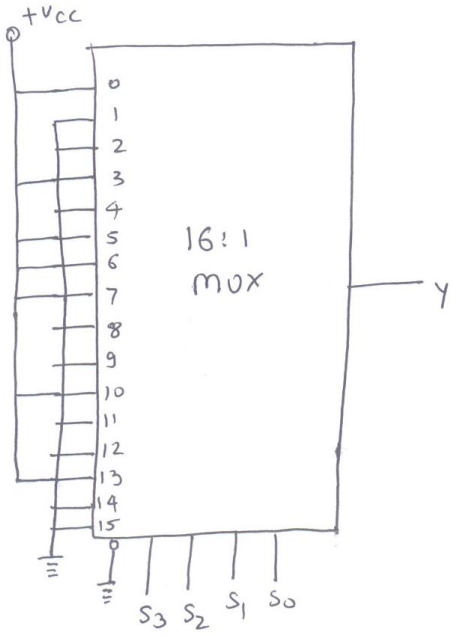
$$Y = \sum m(0, 3, 5, 6, 7, 10, 13)$$

Applications: (2M)

1. Digital computer
2. Microprocessor
3. Data converters
4. Digital system**s**

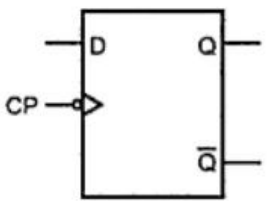
Expression using 16:1 MUX.

$Y = \sum m(0, 3, 5, 6, 7, 10, 13)$ **(4M)**



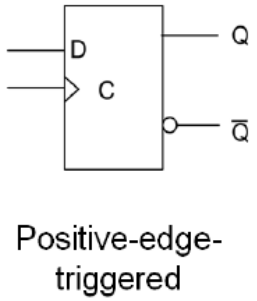
b)

i. Draw symbol and truth table of negative edge triggered D. FF and positive edge triggered JK FF. (2M)
(1M each)
Negative edge triggered D. FF



CP	D	Q_{n+1}
↓	0	0
↓	1	1
0	X	Q_n

Positive edge triggered JK FF



Positive-edge-triggered

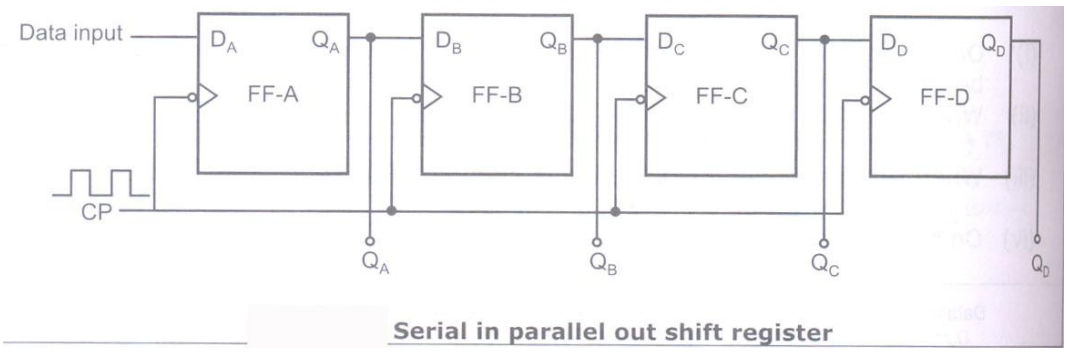
CLK	Data inputs		Output
	J_n	K_n	Q_{n+1}
↑	0	0	Q_n
↑	0	1	0
↑	1	0	1
↑	1	1	$\overline{Q}_n$

ii. What is modulus of counter? Show the method to determine the no. of flip flops for a mod-52 counter.
(Modulus 2M; MOD 52 counter 2M)

Modulus of a counter is the no. of different states through which the counter progress during its operation. It indicates the no. of states in the counter; pulses to be counted are applied to counter. The circuit comes back to its starting state after counting N pluses in the case of modulus N counter.

MOD 52 counter
No. Of flip flops= no of bits of count of the counter
$(52)_{10}=(?)_2$
$52=(110100)_2$
Therefore no. of flip flops required for mod 52 is 6 flip flops

iii. Draw only logic diagram of SIPO. (2M)
(Any other correct logic diagram should be given due credit)



Serial in parallel out shift register

c)

i. A DAC has a full scale analog O/P of 10V and accepts 4 binary bits as i/ps. Find the voltage corresponding to each analog step.

Solution: (4M)

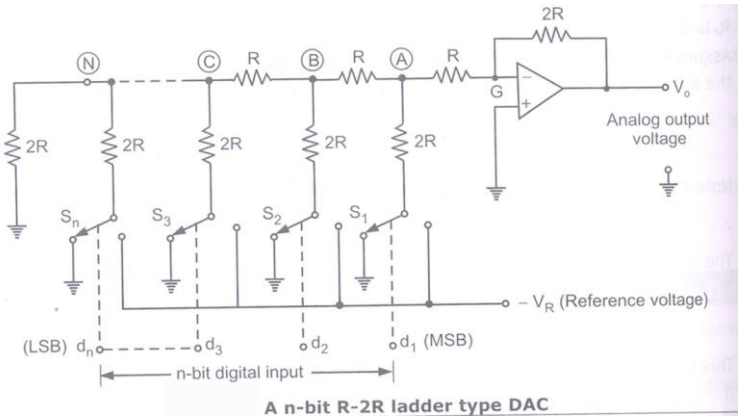
Full scale analog o/p =10V
4bit i/p
1111=10V
Analog o/p=K(digital i/p)
10=K X 15
K=0.666

Analog o/p for
0000=0V
0001=0.666V
0010=1.333V
0011=1.998V
0100=2.664V
0101=3.33V
0110=3.996V
0111=4.662V
1000=5.328V
1001=5.994V
1010=6.667V
1011=7.326V
1100=7.992V
1101=8.658V
1110=9.324V
1111=10V

ii. Describe working of R-2R Ladder type DAC. (4M)

- The binary ladder network largely overcomes the problem of the weighted resistor network.
- This type of circuit also has a resistive network to produce binary weighted currents but uses only two values of resistor, namely R and 2R.
- It uses a ladder network containing series-parallel combination of two resistors of value R and 2R.

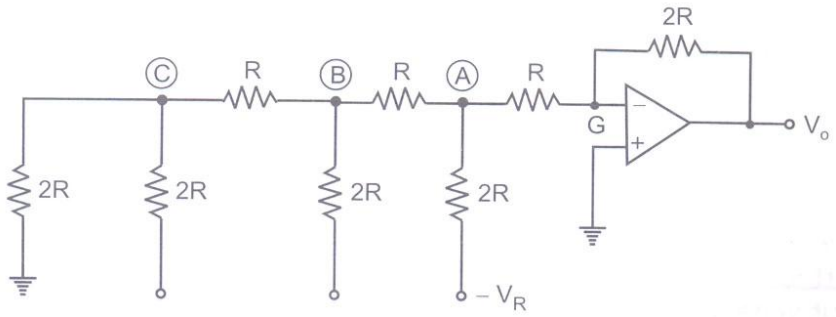
- Figure shows the circuit diagram of a binary ladder type D/A converter with sets of identical resistors R and 2R.

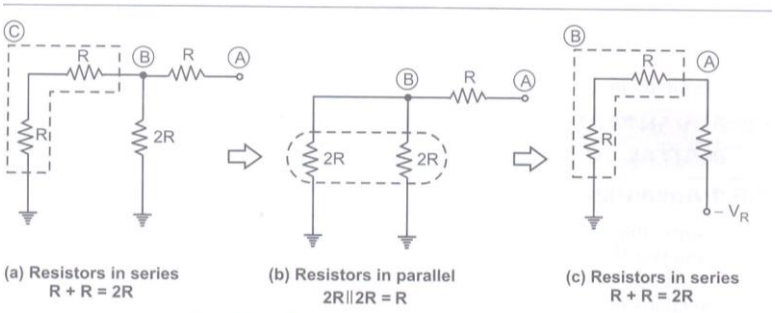


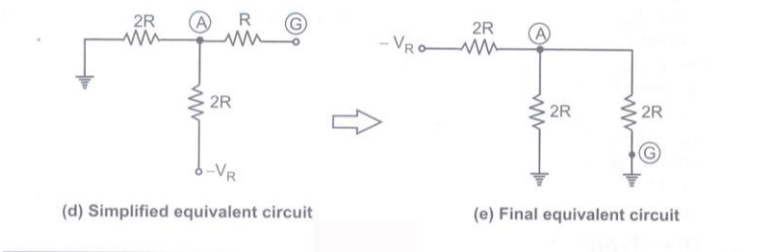
A n-bit R-2R ladder type DAC

- It consists of a R-2R ladder network and op-amp inverting amplifier.
- The value of resistor R can be between 2.5 K Ω.
- The resistor 2R can either be connected to the reference voltage ($-V_R$) line or grounded through controlled switched $S_1,S_2,S_3,\ldots S_n$.

The simplified circuit of a 3-bit (d1,d2,d3 =100) binary ladder type DAC is shoen in fig this simplified circuit is further reduced to the equivalent circuit shown in fig. the equivalent resistance to the left of node (A) in fig is only 2R and the node G is at virtual ground potential.





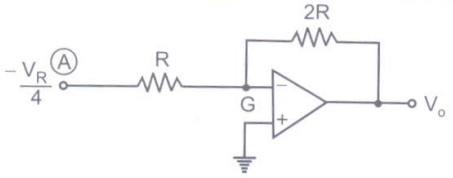


- As the two resistors R and 2R are in parallel with each other, their parallel combination result in a resistance of 2R/3.

The voltage at the node (A) is given by

$$V_A = \frac{\frac{2R}{3}}{\left[2R + \left(\frac{2R}{3}\right)\right]} \times (-V_R)$$

$$V_A = \frac{\frac{2R}{3}}{\frac{8R}{3}} \times (-V_R) = -\frac{V_R}{4}$$



The output voltage of an op-amp inverting amplifier is given by

$$V_0 = -\left(\frac{R_F}{R}\right) V_i = -\left(\frac{2R}{R}\right) \times \left(\frac{-V_R}{4}\right)$$

$$= +\frac{V_R}{2}$$

For a digital input of $d_1\ d_2\ d_3 = 100$, the analog output produced is $\frac{V_R}{2}$.