MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION
(Autonomous)
(ISO/IEC - 27001 - 2005 Certified)

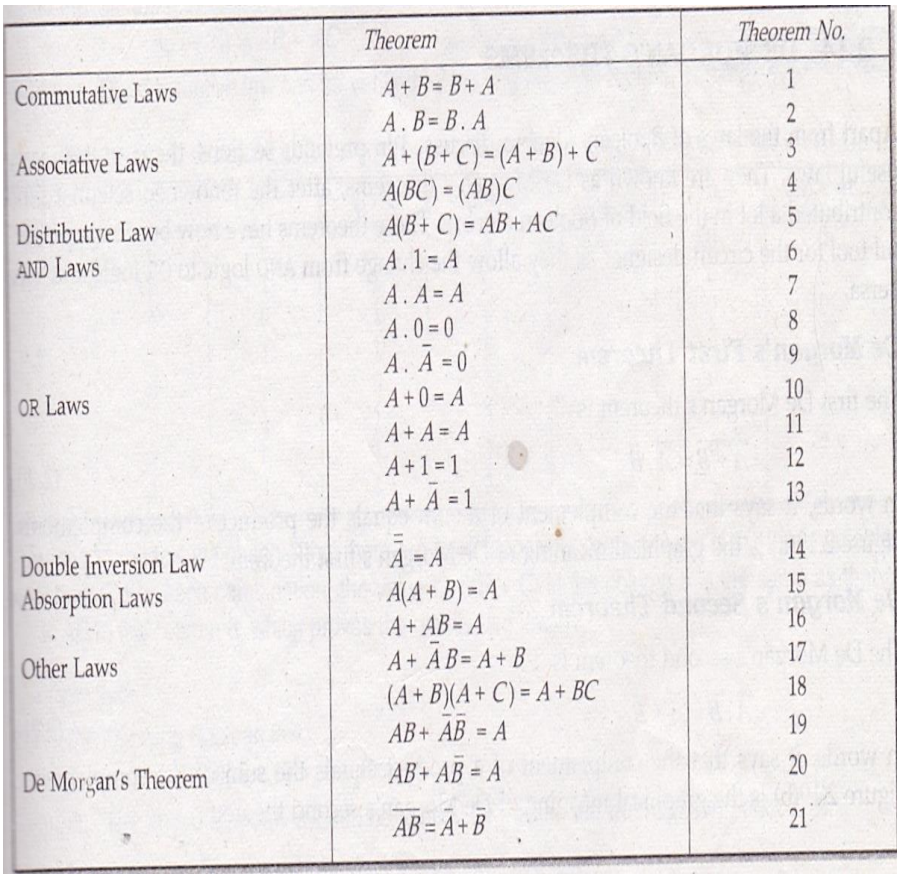
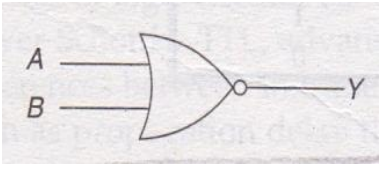
WINTER – 2016 EXAMINATION

Model Answer **Subject Code:** **17333**

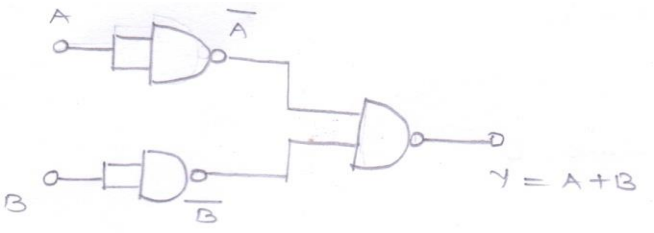
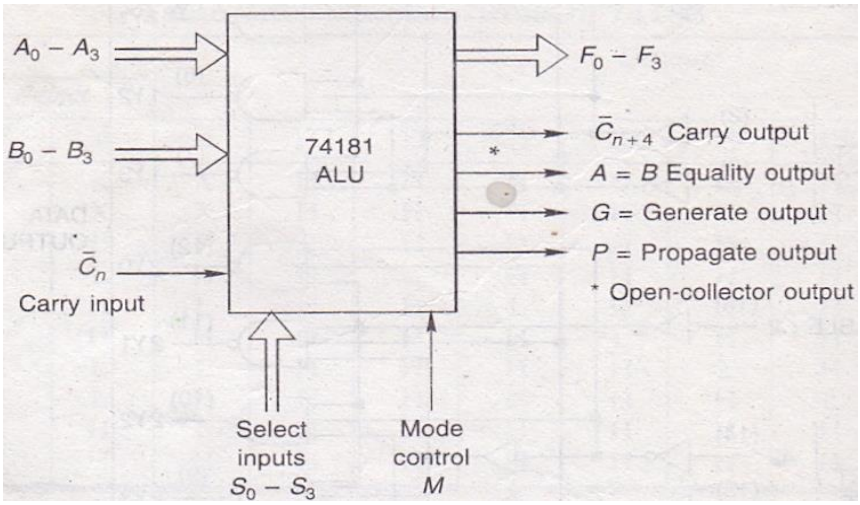
Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

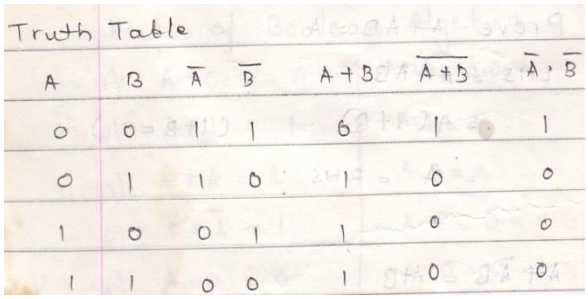
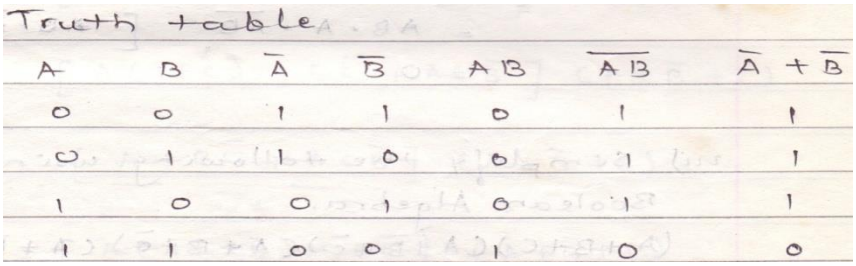
Q.No.	Sub Q.N.	Answer	Marking Scheme
1.	**a)**	**Attempt any six of the following:**	**12**
	i)	**Define w.r.t. digital IC's** **1) Nosie Immunity** **2) Propagation delay.**	***2M***
	Ans.	**1) Noise Immunity**: The ability of a digital circuit to tolerate noise signals is called as noise immunity of a circuit. **2) Propagation delay:** Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.	***Noise Immunity 1M*** ***Propagation delay 1M***
	ii)	**State advantages of digital systems (any 4).**	***2M***
	Ans.	**Advantages of digital systems:** • The devices used in digital systems generally operate in one of the two states, known as ON and OFF resulting in a very simple operation. • A large number of ICs are available for performing various operations. These are highly reliable, accurate, small in size and the speed of operation is very high. A number of programmable. ICs are also available. • The effect of fluctuations in the characteristics of the components,	***Any four advantages 1/2M each***

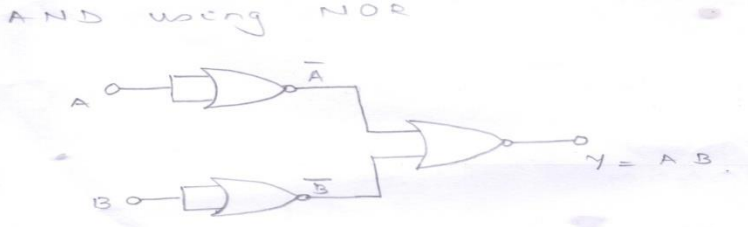
		ageing of components, temperature, and noise etc. is very small in digital systems. • Digital systems have capability of memory which makes these circuits highly suitable for computers, calculators, watches, telephones etc.	
	iii) Ans.	**State any 4 Boolean laws.** **Boolean laws:** 	***2M*** ***Any 4 Boolean laws 1/2M each***
	iv) Ans.	**Draw symbol and truth table of NoR gate.** **Symbol of NOR gate:** 	***2M*** ***Symbol of NOR gate 1M***

	Theorem	Theorem No.
Commutative Laws	$A + B = B + A$	1
	$A \cdot B = B \cdot A$	2
Associative Laws	$A + (B + C) = (A + B) + C$	3
	$A(BC) = (AB)C$	4
Distributive Law	$A(B + C) = AB + AC$	5
AND Laws	$A \cdot 1 = A$	6
	$A \cdot A = A$	7
	$A \cdot 0 = 0$	8
	$A \cdot \bar{A} = 0$	9
OR Laws	$A + 0 = A$	10
	$A + A = A$	11
	$A + 1 = 1$	12
	$A + \bar{A} = 1$	13
Double Inversion Law	$\bar{\bar{A}} = A$	14
Absorption Laws	$A(A + B) = A$	15
	$A + AB = A$	16
Other Laws	$A + \bar{A}B = A + B$	17
	$(A + B)(A + C) = A + BC$	18
	$AB + \bar{A}\bar{B} = A$	19
De Morgan's Theorem	$AB + A\bar{B} = A$	20
	$\overline{AB} = \bar{A} + \bar{B}$	21

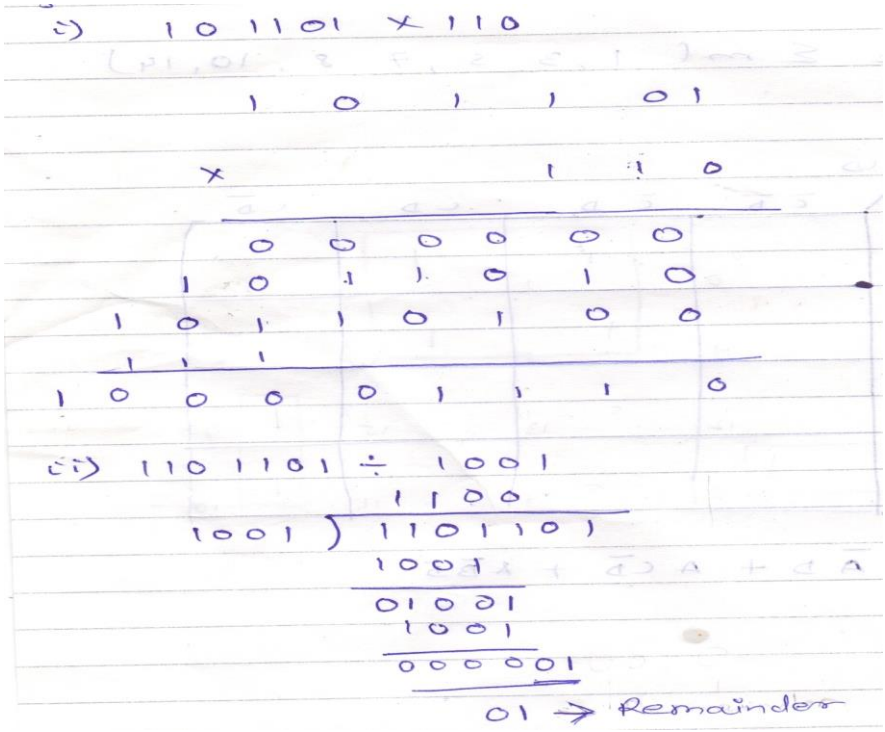
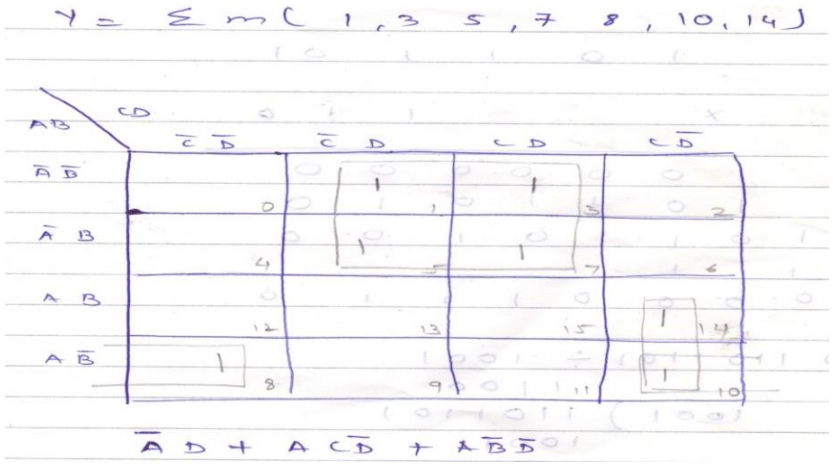
		Truth table of NOR gate: Inputs: A, B; Output: Y 0 0 1 0 1 0 1 0 0 1 1 0	***Truth table of NOR gate 1M***
	v) Ans.	**Convert the following:** **$(AB8C)_{16}$ = ( )$_2$** $(AB8C)_{16}$ = (1010 1011 1000 1100)$_2$	***2M*** ***2M***
	vi) Ans.	**Derive OR gate using NAND gates only.**  **$\overline{\overline{A}.\overline{B}}$** **$= \overline{\overline{A}} + \overline{\overline{B}}$** **= A + B**	***2M*** ***2M***
	vii) Ans.	**Draw the functional block diagram of ALU 74181.**  **Block diagram of ALU 74181**	***2M*** ***Correct diagram 2M***
	viii) Ans.	**Define the following w.r.t. to DAC.** **1) Resolution** **2) Conversion time** **1) Resolution:** This is the smallest possible change in output voltage as a fraction or percentage of the full scale output range. **OR**	***2M*** ***1M***

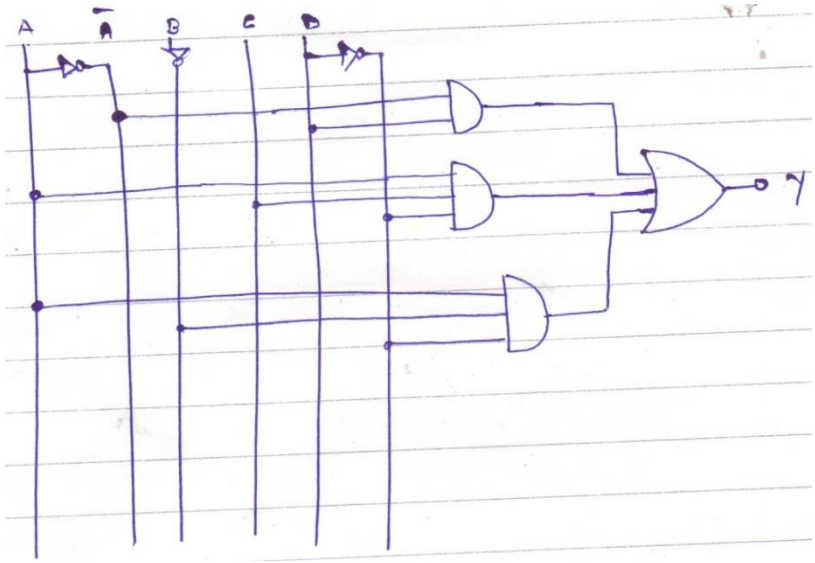
		The number of bits accepted at the input can itself be used as the resolution. For example, an 8-bit D/A converter has an 8-bit resolution. **2) Conversion time:** Total time required to convert analog input signal into corresponding digital output.	 ***1M***
1.	**b)**	**Attempt any two of following:**	**8**
	i)	**Subtract using 2's complement method** **1) $(10110)_2 - (10001)_2$** **2) $(1101)_2 - (11010)_2$**	***4M***
	Ans.	**1) $(10110)_2 - (10001)_2$:** Step1: obtain 1's complement of $(10001)_2$ 1's complement of 1 0 0 0 1 is 0 1 1 1 0 2's complement is 0 1 1 1 0 + 1 2's complement 0 1 1 1 1 Step 2: Add 10110 & 2's complement obtained in step1 1 0 1 1 0 0 1 1 1 1 1 1 1 carry → 1 0 0 1 0 1 Hence carry is 1 Answer is in positive form. Discarding carry **$(10110)_2 - (10001)_2$: $(00101)_2$**	***2M***
		2) $(1101)_2 - (11010)_2$: Make no. of bits equal 01101-11010 Step 1: Find 2's complement of $(11010)_2$ 1's complement of 1 1 0 1 0 is 0 0 1 01 2's complement is 0 0 1 0 1 + 1 2's complement 0 0 1 1 0 Step 2: Add $(01101)_2$ & 2's complement of (11010) from step 1. 0 1 1 0 1 0 0 1 1 0 1 1 carry → 0 1 0 0 1 1	***2M***

		Final carry is 0. Hence answer is in negative form & in 2's complement form. ∴ 2's complement of 1 0 0 1 1 1's complement 0 1 1 0 1 + 1 2's complement is $(0\ 1\ 1\ 0\ 1)_2$ **Result= $(-01101)_2$**	
	ii) Ans.	**State and prove Demorgan's theorems.** **De Morgan's first law:** "Complement of the sum of variables is equal to the product of complement of the variables" $\overline{A+B} = \overline{A}.\overline{B}$ Proof by perfect Induction method Truth Table:  **De Morgan'ssecond law: "**Complement of the product of variables is equal to the sum of complement of variables" $\overline{AB} = \overline{A}+\overline{B}$ Truth Table: 	***4M*** ***1M*** ***1M*** ***1M*** ***1M***
	iii)	**Convert the following:** **1) $(498.25)_{16}$ = ( )$_{10}$** **2) $(10110101)_2$ = ( )$_{16}$** **3) $(B689D)_{16}$ = ( )$_8$** **4) $(110110111)_2$ = ( )$_{10}$**	***4M***

	Ans.	1) $(498.25)_{16} = (\quad)_{10}$ $498.25 = 4\times16^2 + 9\times16^1 + 8\times16^0 + 2\times16^{-1} + 5\times16^{-2}$ $1024 + 144 + 8 + 0.125 + 0.0195$ $= 1176.145$ 2) $(1.01110101)_2 = (\quad)_{16}$ $1011\ 0101 = (B\ 5)_{16}$ 3) $(B\ 6\ 8\ 9\ D)_{16} = (\quad)_8$ $(B\ 6\ 8\ 9\ D)_{16} = 1011\ 0110\ 1000\ 1001\ 1101$ $010\ 110\ 110\ 100\ 010\ 011\ 101$ $(2\ 6\ 6\ 4\ 2\ 3\ 5)_8$ $= (2664235)_8$ 4) $(110\ 110\ 111)_2 = (\quad)_{10}$ $(110\ 110\ 111)_2 = 1\times2^8 + 1\times2^7 + 0\times2^6 + 1\times2^5 + 1\times2^4 + 0\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0$ $= 439$	***1M for each bit***
2.	**a)** Ans.	**Attempt any four of the following:** **Derive AND gate and OR gate using NOR gates only.** AND using NOR  $\overline{\bar{A} + \bar{B}}$ $= \bar{\bar{A}} \cdot \bar{\bar{B}}$ $= A \cdot B$ OR using NOR  	**16** ***4M*** ***2M*** ***2M***

	b)	**Simplify the following Boolean expressions using Boolean laws:**	***4M***
		i) $\overline{(A\bar{B} + \bar{A}\bar{B})(AB + \bar{A}B)}$	
		ii) $\bar{A}B + ABD + A\bar{B}C\bar{D} + BC$	
	Ans.	**i)**	
		$\overline{(A\bar{B} + \bar{A}\bar{B})(AB + \bar{A}B)}$ $= \overline{(A\bar{B} + \bar{A}\bar{B})} + \overline{(AB + \bar{A}B)}$ $= (\overline{A\bar{B}} \cdot \overline{\bar{A}\bar{B}}) + (\overline{AB} \cdot \overline{\bar{A}B})$ $= (\bar{A} + B) \cdot (A + B) + (\bar{A} + \bar{B}) \cdot (A + \bar{B})$ $= A\bar{A} + \bar{A}B + AB + BB + A\bar{A} + \bar{A}\bar{B} + A\bar{B}$ $= \bar{A}B + AB + B + \bar{A}\bar{B} + A\bar{B} + \bar{B}$ $= B(\bar{A} + A + 1) + \bar{B}(\bar{A} + A + 1)$ $= (B + \bar{B})(\bar{A} + A + 1)$ $= 1$	***2M***
		ii)	
		$\bar{A}B + ABD + A\bar{B}C\bar{D} + BC$ $\bar{A}B + ABD + A\bar{B}C\bar{D} + ABC + \bar{A}BC$ $\bar{A}B + AC(B + \bar{B}\bar{D}) + ABD$ $B(\bar{A} + AD) + AC(B + \bar{D})$ $B(\bar{A} + D) + AC(B + \bar{D})$ $\bar{A}B + BD + ABC + AC\bar{D}$ $B(\bar{A} + AC) + BD + AC\bar{D}$ $B(\bar{A} + C) + BD + AC\bar{D}$ $Y = \bar{A}B + BC + BD + AC\bar{D}$	***2M***

	c) Ans.	**Perform the following binary operations.** **i) 101101 X 110** **ii) 1101101 ÷ 1001**  	***4M*** ***2M*** ***2M***
	d) Ans.	**Minimize the following Boolean expression using K-map.** **Y = ∑ m (1, 3, 5, 7, 8, 10, 14)** **Draw the logical diagram using basic gates.**  	***4M*** ***K-map 1M*** ***Simplification 2M***



Logical diagram 1M

e) Ans.

Design a half adder circuit using k-map.

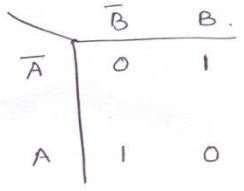
Half adder: A logic circuit for the addition of two one-bit numbers is referred to as a half-adder. The addition process a reproduced in truth table form in Table. Here, A and B are the two inputs and S(SUM) and C (CARRY) are the two outputs

Table: Truth table of a half-adder

Inputs		*Outputs*	
A	*B*	*S*	*C*
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table 1M

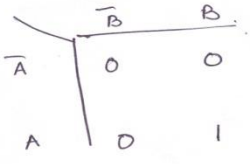
K-map for Sum



$Y = \bar{A}B + A\bar{B}$
Sum

$Y = A \oplus B$.

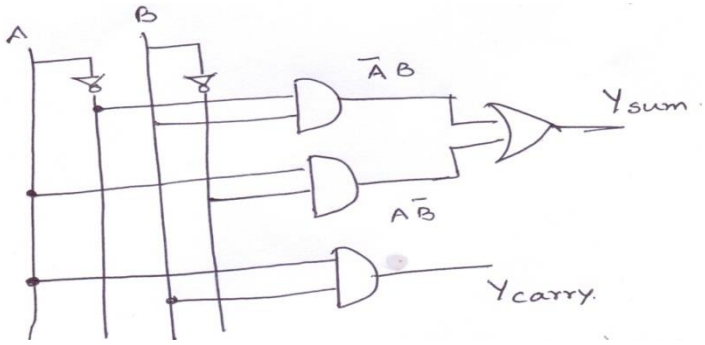
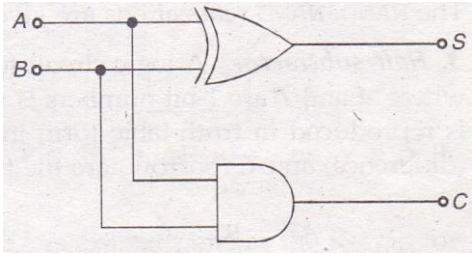
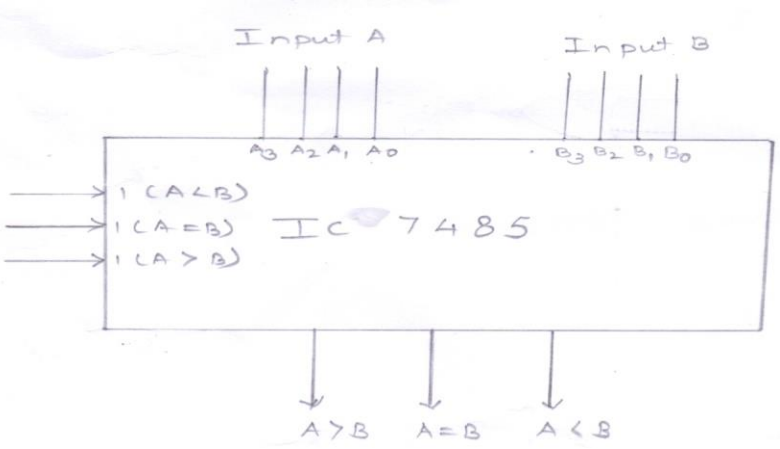
K-map for Carry.



$Y = AB$.
carry.

K-maps for sum 1M

k-map for carry 1M

		 OR circuit diagram with universal gates may also be given marks OR 	***Logical diagram 1M***
	f) Ans.	**Draw block diagram of digital comparator IC 7485 and explain with the help of truth table.** **Block diagram of digital comparator IC 7485:** 	***4M*** ***Block diagram 2M***

Function Table of 7485:

Comparing inputs A, B	Cascading inputs A > B	Cascading inputs A = B	Cascading inputs A < B	Outputs A > B	Outputs A = B	Outputs A < B
A > B	×	×	×	1	0	0
A = B	1	0	0	1	0	0
	×	1	×	0	1	0
	0	0	1	0	0	1
	0	0	0	1	0	1
	1	0	1	0	0	0
A < B	×	×	×	0	0	1

Truth table 1M

Explanation of Function table of IC 7485:

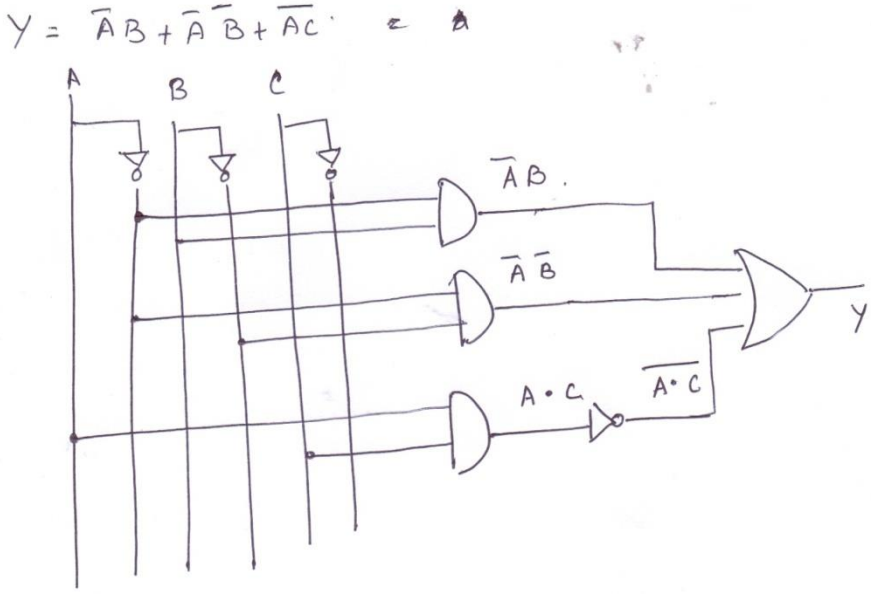
1. For comparing inputs A>B, irrespective of the cascading input, the output will be A>B.
2. For comparing inputs A=B, the output depends on the cascading inputs.
   a. If cascading inputs are A>B then output will be A>B.
   b. If cascading inputs are A=B then output will be A=B.
   c. If cascading inputs are A<B then output will be A<B.
3. For comparing inputs A<B, irrespective of the cascading input, the output will be A<B.

Explanation 1M

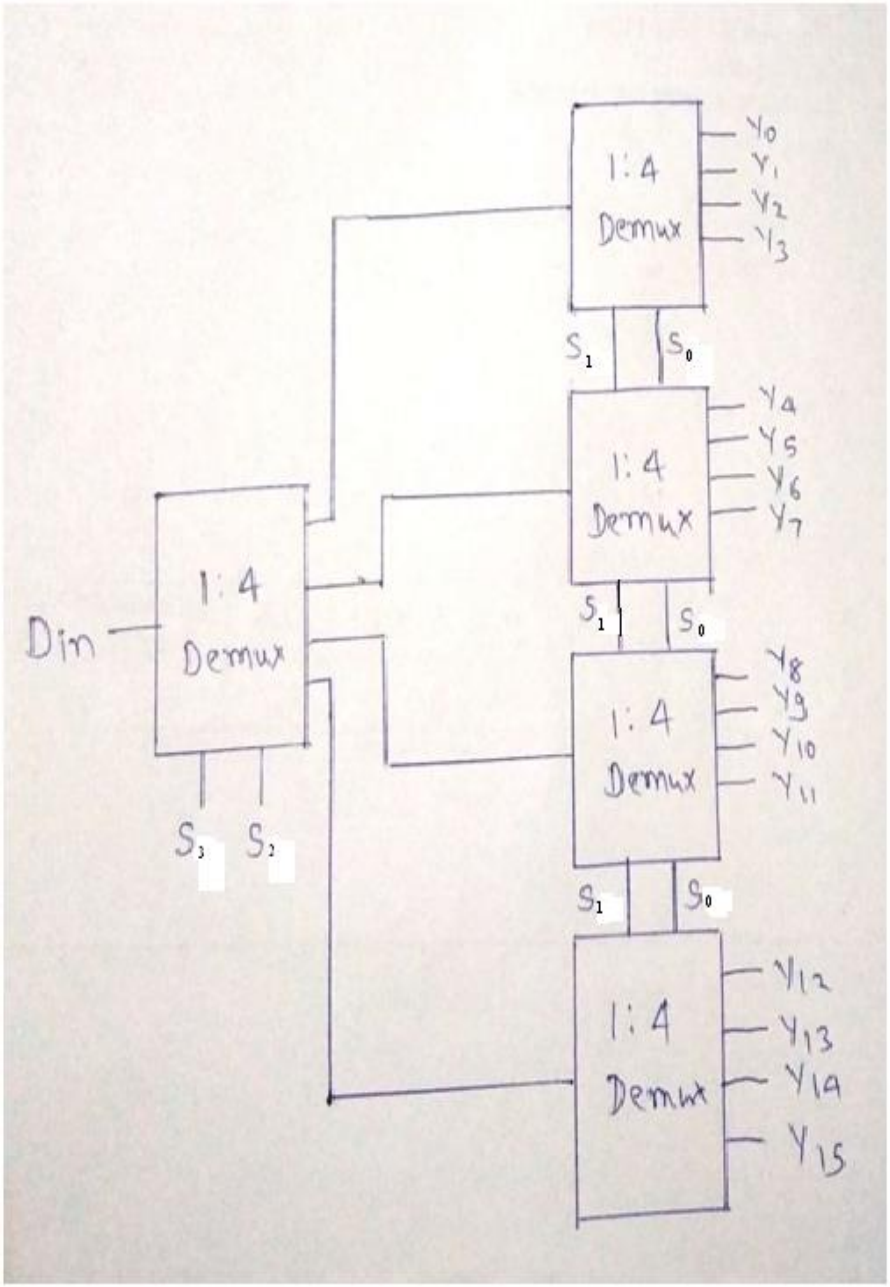
3. **Attempt any four of the following:** **16**

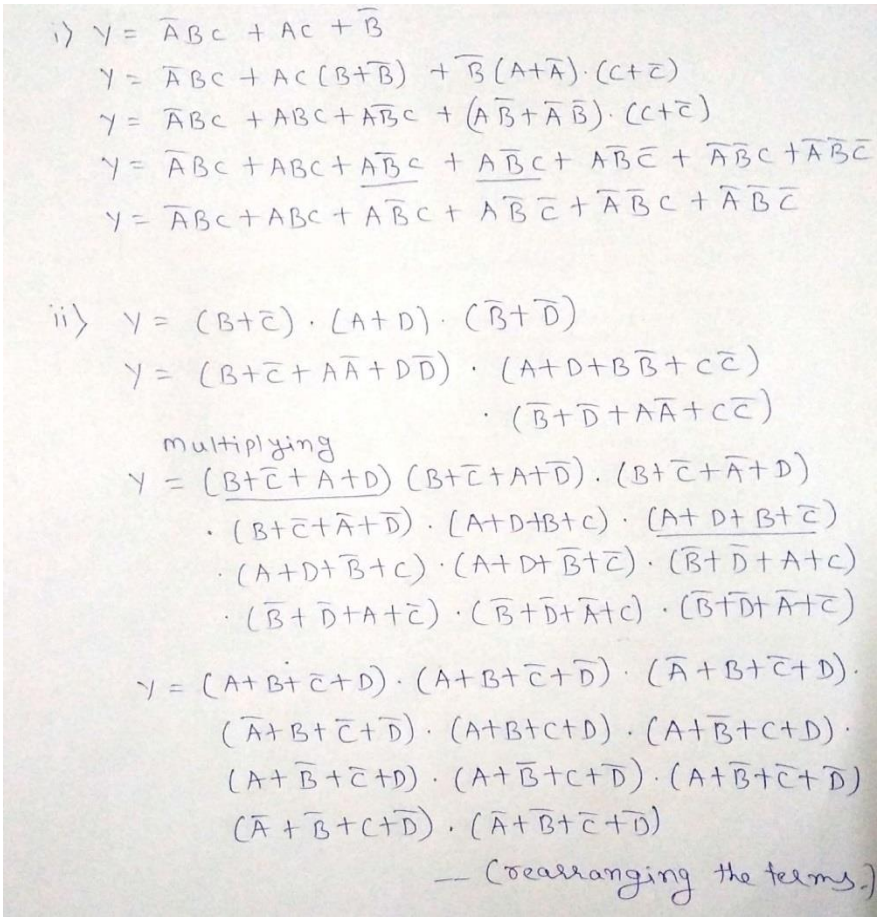
a) **Implement the logical expression using basic gates.** ***4M***

Ans. **$Y = \bar{A}B + \bar{A}\bar{B} + \bar{A}\bar{C}$**



Simplification: 2M, Implementation: 2M

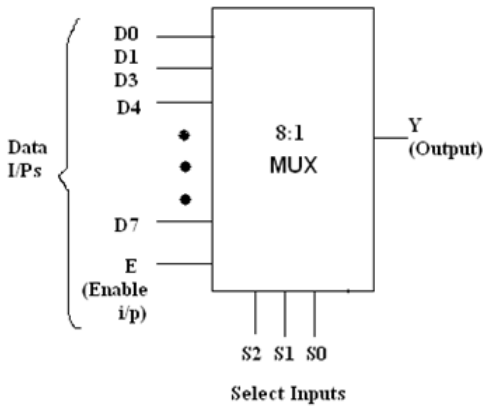
	b) Ans.	**Design 1:16 demultiplexer using only 1:4 demultiplexers.** 	***4M*** ***Design: 4M***
	c) Ans.	**Convert the following expression into its standard forms.** **i) $Y = \bar{A}BC + AC + \bar{B}$** **ii) $Y = (B + \bar{C}) \bullet (A + D) \bullet (\bar{B} + \bar{D})$**	***4M***



Each correct conversion: 2M

d) Ans.

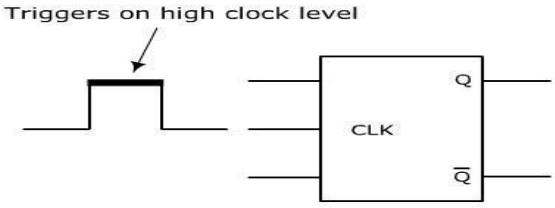
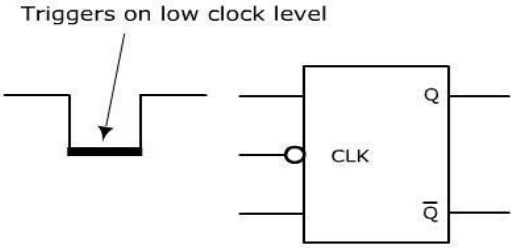
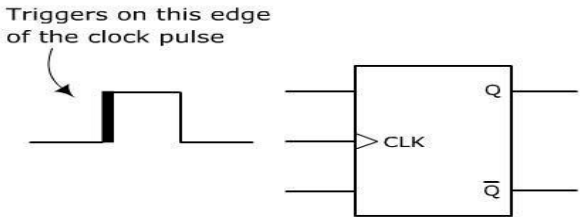
Draw logic diagram of 8:1 multiplexer. Write it's truth table.

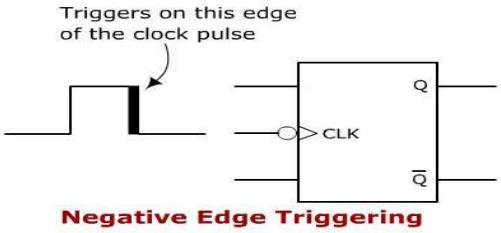
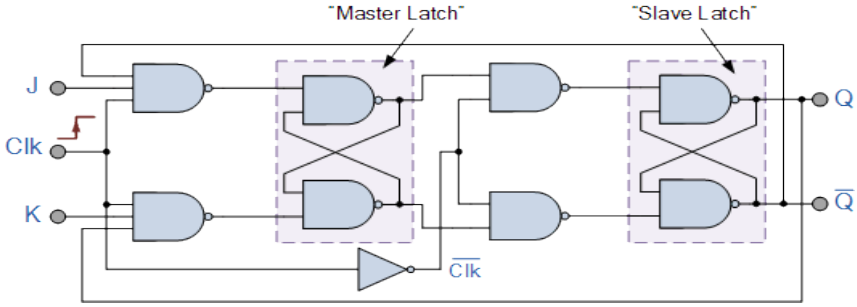


Enable	Select Inputs			Output
E	S2	S1	S0	Y
0	×	×	×	0
1	0	0	0	D0
1	0	0	1	D1
1	0	1	0	D2
1	0	1	1	D3
1	0	0	0	D4
1	0	0	1	D5
1	0	1	0	D6
1	0	1	1	D7

4M

Diagram : 2M, Truth Table: 2M

	e) Ans.	**Explain different triggering methods.** There are four types of pulse-triggering methods: 1.**Positive (High) Level Triggering:** When a flip flop is required to respond at its HIGH state a HIGH level triggering method is used. It is mainly identified from the straight lead from the clock input. Take a look at the symbolic representation shown below.  High Level Triggering 2. **Negative (Low) Level Triggering:** When a flip flop is required to respond at its LOW state, a LOW level triggering method is used. It is mainly identified from the clock input lead along with a low state indicator bubble. Take a look at the symbolic representation shown below.  Low Level Triggering 3. **Positive Edge Triggering:** When a flip flop is required to respond at a LOW to HIGH transition state, POSITIVE edge triggering method is used. It is mainly identified from the clock input lead along with a triangle. Take a look at the symbolic representation shown below.  Positive Edge Triggering	***4M*** ***Four triggering Method: 1M each***

		4. Negative Edge Triggering: When a flip flop is required to respond during the HIGH to LOW transition state, a NEGATIVE edge triggering method is used. It is mainly identified from the clock input lead along with a low-state indicator and a triangle.  Negative Edge Triggering	
	f) Ans.	**Explain Master-Slave JK flip-flop with neat diagram.** Master-Slave JK Flip-flop: It is two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from Q and Q from the "Slave" flip-flop are fed back to the inputs of the "Master" with the outputs of the "Master" flip flop being connected to the two inputs of the "Slave" flip flop.  The input signals J and K are connected to the gated "master" SR flip flop which "locks" the input condition while the clock (Clk) input is "HIGH" at logic level "1". As the clock input of the "slave" flip flop is the inverse (complement) of the "master" clock input, the "slave" SR flip flop does not toggle. The outputs from the "master" flip flop are only "seen" by the gated "slave" flip flop when the clock input goes "LOW" to logic level "0". When the clock is "LOW", the outputs from the "master" flip flop are latched and any additional changes to its inputs are ignored. The gated "slave" flip flop now responds to the state of its inputs passed over by the "master" section.	***4M*** ***Diagram : 2M*** ***Explanation: 2M***

Then on the "Low-to-High" transition of the clock pulse the inputs of the "master" flip flop are fed through to the gated inputs of the "slave" flip flop and on the "High-to-Low" transition the same inputs are reflected on the output of the "slave" making this type of flip flop edge or pulse-triggered.

Then, the circuit accepts input data when the clock signal is "HIGH", and passes the data to the output on the falling-edge of the clock signal.

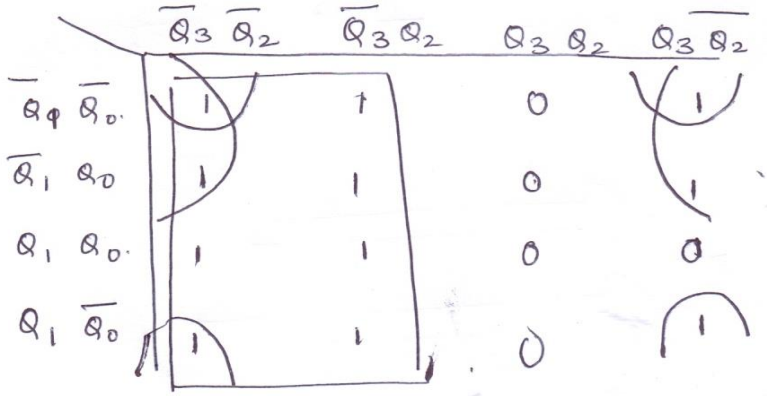
4. **Attempt any four of the following:** **16**

a) **Draw the logical diagram of MOD -11 counter and describe its operation with truth table.** ***4M***

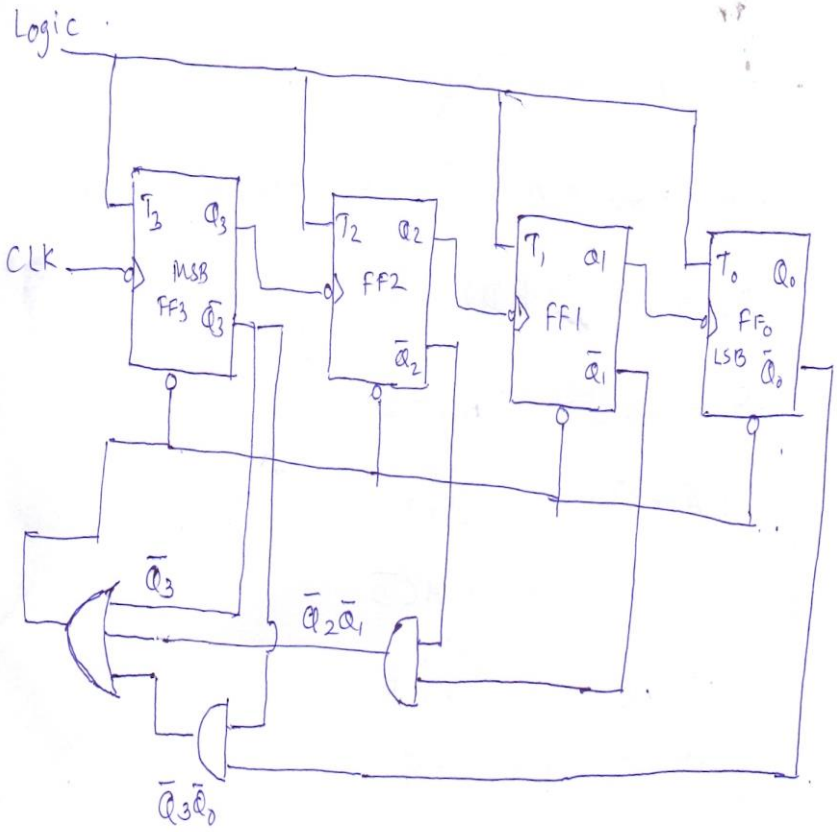
Ans. For designing Mod-11 Counter 4 Flip-Flops (4 bits) will be required.
Mod-11 Counter Truth Table

Clock Count	Output bit Pattern				Decimal Value
	Q_3	Q_2	Q_1	Q_0	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	1	0	1	0	10
12	Counter Resets its Outputs back to Zero				

Designing: 2M, Operation: 2M



$$Y = \bar{Q}_3 + \bar{Q}_1\bar{Q}_2 + \bar{Q}_3\bar{Q}_0$$



	b) Ans.	**State any four specification of ADC** **Resolution:** The resolution refers to the finest minimum change in the signal which is accepted for conversion and it is decided with respect to number of bits. It is given as 1/2n, where n is the number of bits in the digital output word. As it is clear, that the resolution can be improved by increasing the number of bits or the number of bits representing the given analog input voltage. Resolution can also be defined as the ratio of change in the value of input voltage V_i, needed to change the digital output by 1 LSB. It is given as $\text{Resolution} = V_{iFS} / (2^n - 1)$ Where 'V_{iFS}' is the full-scale input voltage. 'n' is the number of output bits. **Quantization error:** If the binary output bit combination is such that for all the values of input voltage V_i between any two voltage levels, there is a unavoidable uncertainty about the exact value of Vi when the outputis a particular binary combination. This uncertainty is termed as quantization error. It is given as, $Q_E = V_{iFS} / 2(2^n - 1)$ Where 'V_{iFS}' is the full-scale input voltage 'n' is the number of output bits. **Linearity Error:** It is defined as the measure of variation in voltage step size. It indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as fraction of LSB. **DNL (Differential Non-Linearity) Error:** The analog input levels that trigger any two successive output codes should differ by 1 LSB. Any deviation from this 1 LSB value is called as DNL error. **INL (Integral Non-Linearity Error:** The deviation of characteristics of an ADC due to missing codes causes INL error. The maximum deviation of the code from its ideal value after nulling the offset and	***4M*** ***Any 4 Specific ations: 1M each***

gain errors is called as Integral Non-Linearity Error.

Input Voltage Range: It is the range of voltage that an A/D converter can accept as its input without causing any overflow in its digital output.

c) Ans.

Describe the function of preset and clear terminals in JK flipflop. Write truth table of it. *4M*

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{PR}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	X	X
1	1	↓	0	0	Q_0	$\overline{Q}_0$
1	1	↓	1	0	1	0
1	1	↓	0	1	0	1
1	1	↓	1	1	Toggle	
1	1	1	X	X	Q_0	$\overline{Q}_0$

Truth table: 2M

The function of preset and clear in J-K flip flop can be seen in the below.

1. When preset input is low (Since active low signal), the output of the flip-flop is set to 1, independent of clock pulse.
2. When Clear input is low (since active low signal), the output of the flip-flop is reset to 0, independent of clock pulse.
3. If both preset and clear is low at the same time, the o/p of flip flop states becomes X. (Don't Care)
4. If both preset and clear is high at the same time, the o/p of flip flop is controlled by clock and JK inputs.

Functions: 2M

d) Ans.

Draw the neat diagram of clocked SR flip flop using NAND gates. Write truth table. *4M*

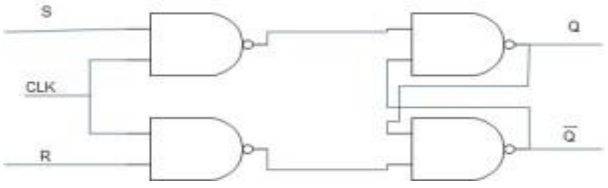


Fig: Clocked SR Flip-Flop using NAND

Diagram : 2M

The table belo summarizes above explained working of SR Flip Flop designed with the help of a NAND gates

$\bar{S}$	$\bar{R}$	Q	State
1	1	Previous State	No change
1	0	0	Reset
0	1	1	Set
0	0	?	Forbidden

Truth table: 2M

e) Ans.

Differentiate between RAM and ROM – (any four points) ***4M***

RAM	ROM
Random Access Memory or RAM is a form of data storage that can be accessed randomly at any time, in any order and from any physical location, allowing quick access and manipulation	Read-only memory or ROM is also a form of data storage that cannot be easily altered or reprogrammed. Stores instructions that are not necessary for re-booting up to make the computer operate when it is switched off. They are hardwired
RAM allows the computer to read data quickly to run applications. It allows reading and writing.	ROM stores the program required to initially boot the computer. It only allows reading.
RAM is volatile i.e. its contents are lost when the device is powered off.	It is non-volatile i.e. its contents are retained even when the device is powered off.
The two main types of RAM are static RAM and dynamic RAM.	The types of ROM include PROM, EPROM and EEPROM.

Any 4 points: 1M each

f) Ans.

Draw the circuit diagram of weighted resister type D to A converter. Describe the working. ***4M***

Weighted Resistor:

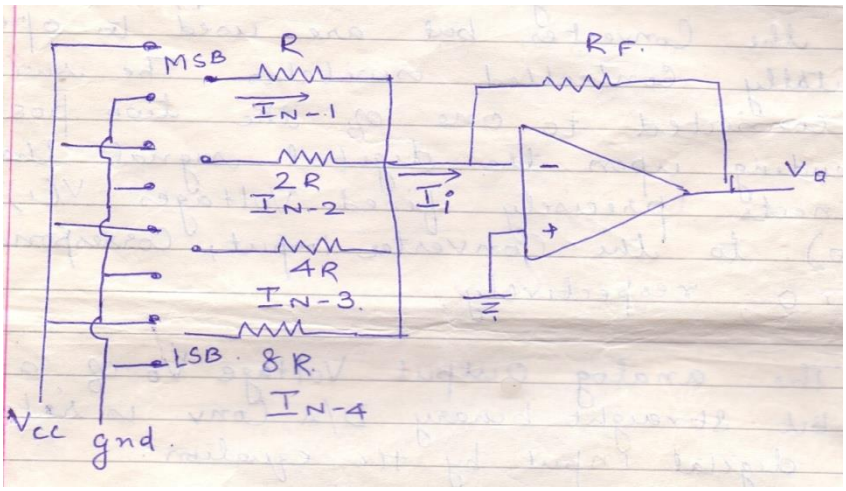
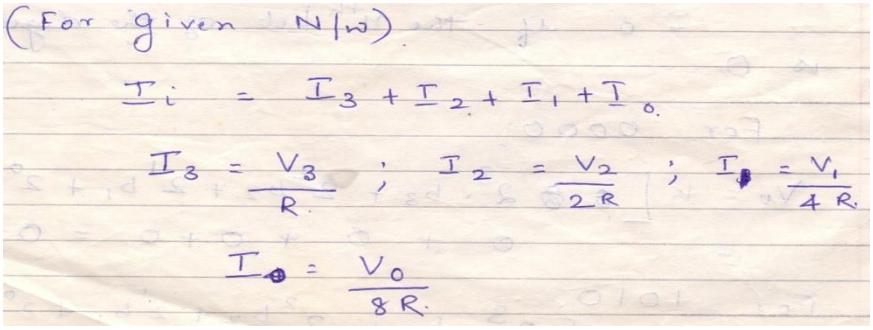


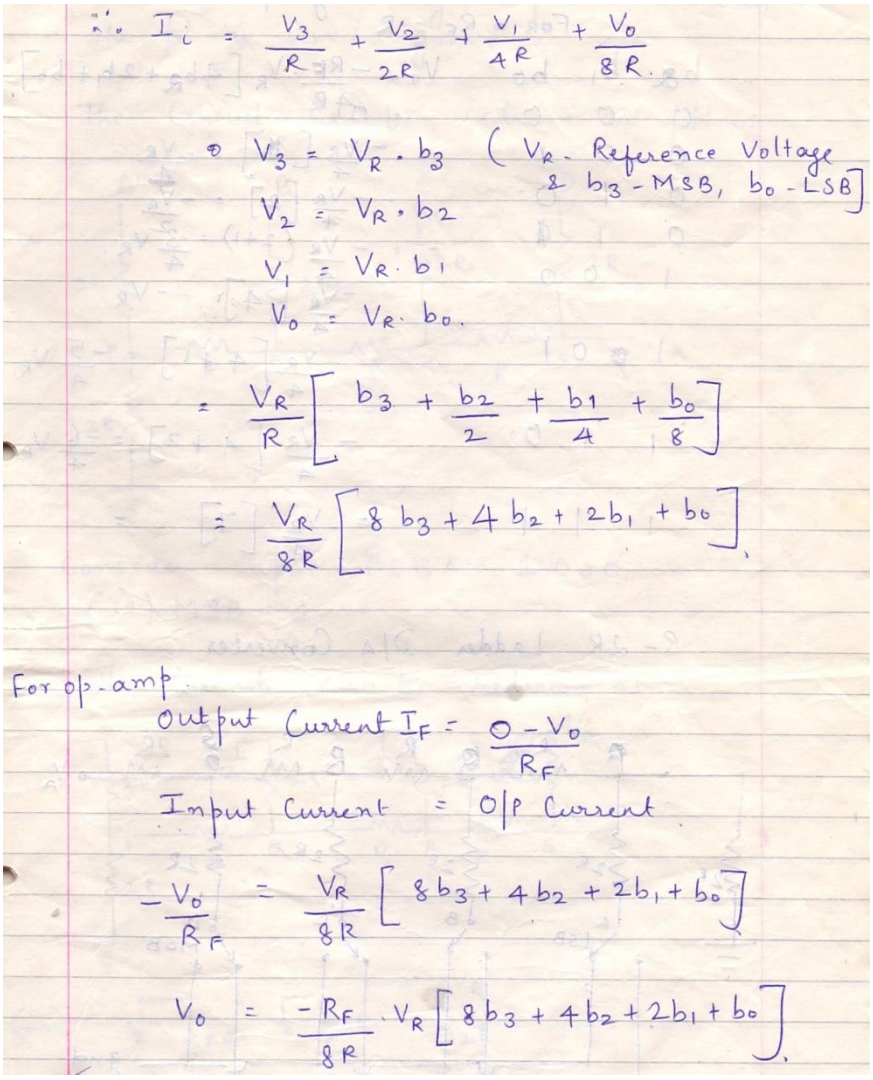
Diagram : 2M

Let us assume an N-bit straight binary input to a resistor network as shown.

$I_i = I_{N-1} + I_{N-2} + I_{N+3} + \ldots\ldots\ldots + I_2 + I_1 + I_0$

Description: 2M





$\therefore I_i = \frac{V_3}{R} + \frac{V_2}{2R} + \frac{V_1}{4R} + \frac{V_0}{8R}$

$\therefore V_3 = V_R \cdot b_3$ (V_R - Reference Voltage & b_3 - MSB, b_0 - LSB]

$V_2 = V_R \cdot b_2$

$V_1 = V_R \cdot b_1$

$V_0 = V_R \cdot b_0$.

$= \frac{V_R}{R}\left[b_3 + \frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8} \right]$

$= \frac{V_R}{8R}\left[8b_3 + 4b_2 + 2b_1 + b_0 \right]$.

For op-amp.

Output Current $I_F = \frac{0 - V_0}{R_F}$

Input Current = O/P Current

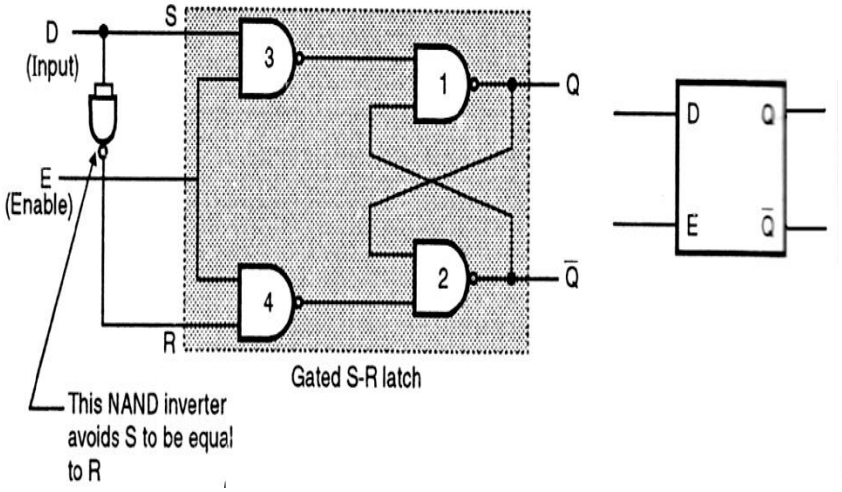
$-\frac{V_0}{R_F} = \frac{V_R}{8R}\left[8b_3 + 4b_2 + 2b_1 + b_0 \right]$

$V_0 = \frac{-R_F}{8R} \cdot V_R \left[8b_3 + 4b_2 + 2b_1 + b_0 \right]$.

5.	**a)**	**Attempt any four of the following:** **Perform the following BCD arithmetic** **i) $(78)_{BCD} + (59)_{BCD}$** **ii) $(86)_{BCD} + (36)_{BCD}$**	**16** ***4M***
	Ans.	**i) $(78)_{BCD} + (59)_{BCD}$:**	

		i) $(78)_{BCD} + (59)_{BCD}$ $(78)_{BCD} = 0111\ \ 1000$ $(59)_{BCD} = 0101\ \ 1001$ $1101\ \ 1\,0001$ Invalid BCD — valid BCD with cy=1 ∴ Convert Invalid to valid by adding $(6)_{BCD}$ i.e. (0110) $1101\ \ 0001$ $+\ 0110\ \ 0110$ $0001\ \ 0011\ \ 0111$ 1 3 7 ∴ $(78)_{BCD} + (59)_{BCD} = (137)_{BCD}$	*2M*
		ii) $(86)_{BCD} + (36)_{BCD}$: Method I:- Using 9's complement method:— Step i) obtain 9's complement of $(36)_{BCD}$ ⇒ Substract each digit from 9 ∴ 99 − 36 = (63) = 9's complement of 36 Step ii) Add $(86)_{BCD}$ to 9's complement of 36 $(86)_{BCD} = 1000\ \ 0110$ $(63) = 0110\ \ 0011$ $1110\ \ 1001$ Invalid BCD — valid BCD Step iii) Add $(6)_{BCD}$ to Invalid BCD $1110\ \ 1001$ $+\ 0110\ \ 0000$ $1\ 0100\ \ 1001 = (49)_{BCD}$ End around cy Step iv) Add end around carry 49 + 1 = $(50)_{BCD}$	*2M*

		OR Method 2) Using 10's complement method Step i) obtain 10's Complement of $(36)_{BCD}$ → obtain 9's complement → add 1 to 9's complement 9's complement = 99 − 36 = 63 63 + 1 10's comp = (64) Step ii) Add $(86)_{BCD}$ to 10's complement of $(36)_{BCD}$ $\therefore (86)_{BCD} = 1000\ 0110$ (64) + 0110 0100 1110 1010 Invalid BCD, Invalid BCD Step iii) Convert Invalid to valid by adding $(6)_{BCD}$ 1110 1010 + 0110 0110 1 0100 10000 discard 5 0 $\therefore (86)_{BCD} - (36)_{BCD} = (50)_{BCD}$	
	b) Ans.	**Draw the logic diagram of D. flipflop using NAND gates. Write its truth table.**	***4M***



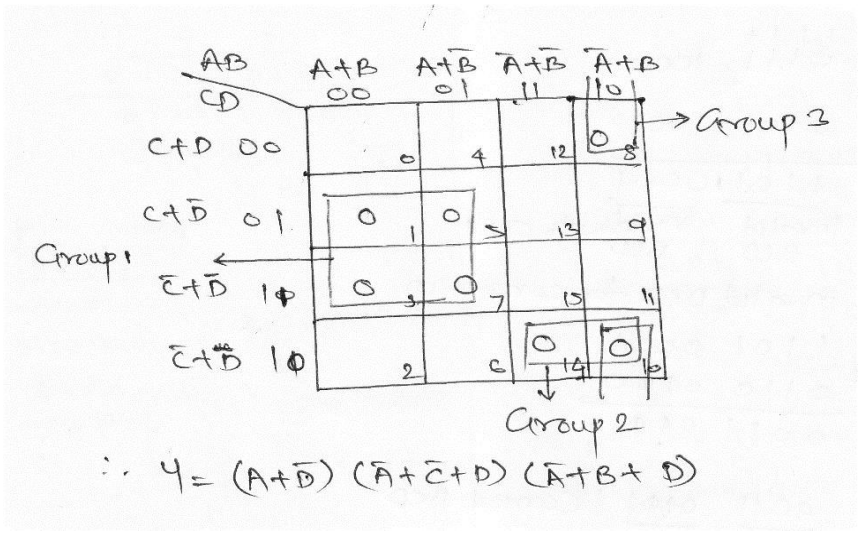
Input Dn	Output Qn+1
0	0
1	1

Logical diagram 2M

Truth table 2M

c) Ans.

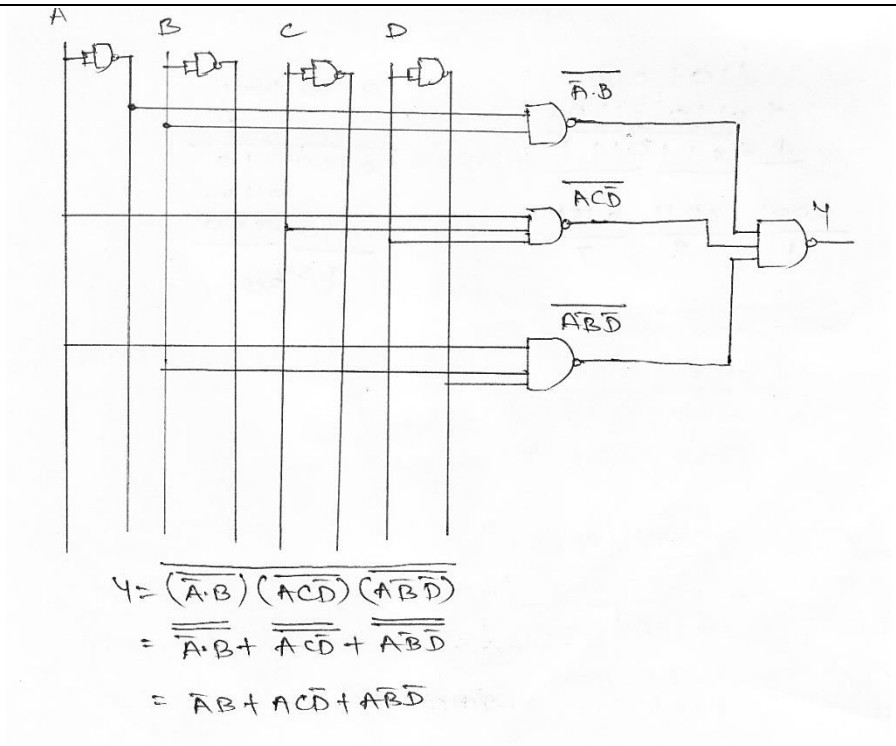
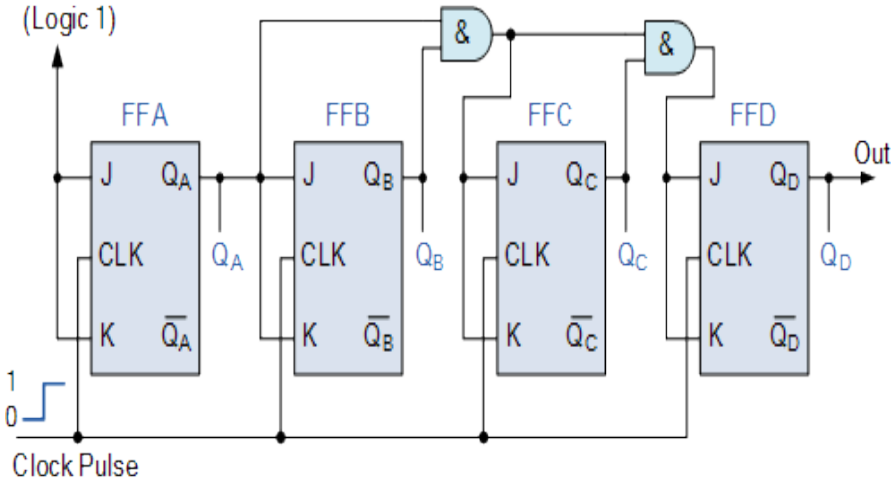
Reduce the following expression using k-map and implement it using NAND gates.
Y = ∏ M (1, 3, 5, 7, 8, 10, 14)

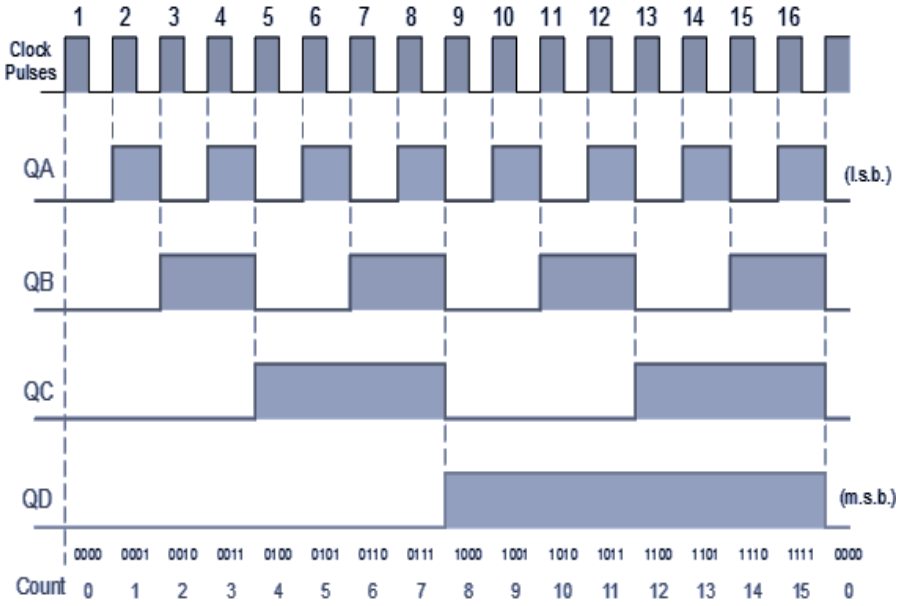


4M

1M for K-map

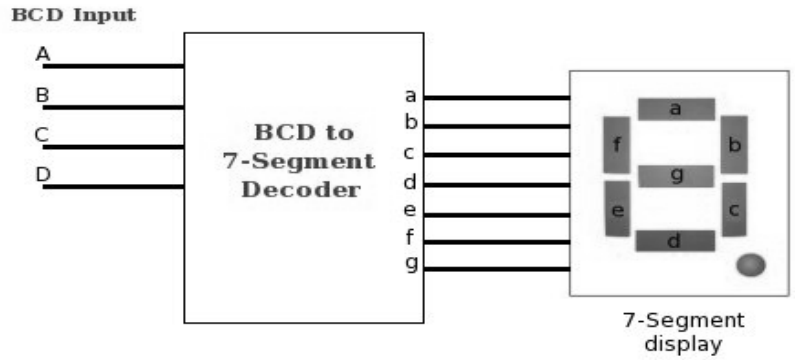
Expression 2M

			***Logical diagram 1M***
	d) Ans.	**Design 4-bit asynchronous up counter and describe its operation.**  It can be seen above, that the external clock pulses (pulses to be counted) are fed directly to each of J-K flip-flops in the counter chain and that both the J and K inputs are all tied together in toggle mode, but only in the first flip-flop, flip-flop FFA(LSB) are they connected	***4M*** ***Logical diagram 2M*** ***Explanation 1M***

		HIGH, logic "1" allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse. The J and K inputs of flip-flop FFB are connected directly to the output Q_A of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage. If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are "HIGH" we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time. Then as there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.  	***Timing diagram 1M***

e) **Draw the block diagram of BCD to 7-segement decoder. Write its truth table.** — *4M*

Ans.



Circuit diagram 2M

Binary Inputs				Decoder Outputs							7-Segment Display Outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9

Truth table 2M

f) **Draw the block diagram of SISO shift register and describe its operation.** — *4M*

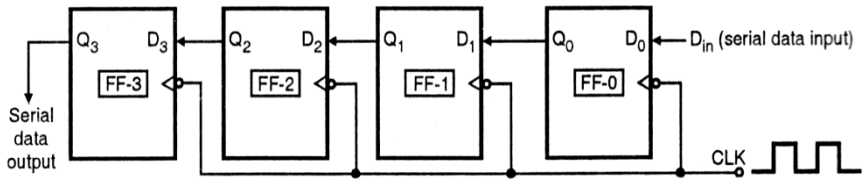
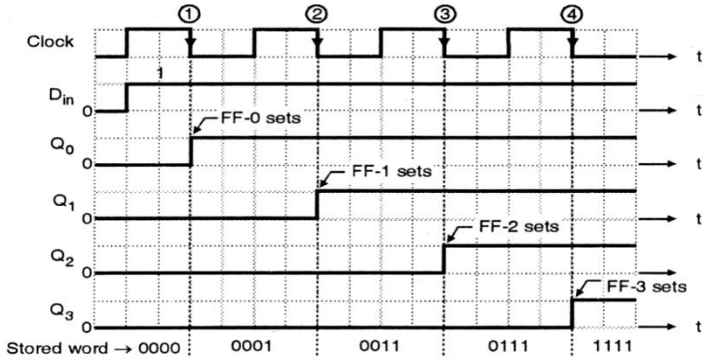
Ans.

The diagram shows four flip-flops connected to form a SERIAL IN, SERIAL OUT shift register. Upon the arrival of a clock pulse, data at the D input of each flip-flop is transferred to its Q output. At the start, the contents of the register can be set to zero by means of the CLEAR line.

If a 1 is applied to the input of the first flip-flop, then upon the arrival of the first clock pulse, this 1 is transferred to the output of flip-flop 1 (input of flip-flop 2).

After four clock pulses this 1 will be at the output of flip-flop 4. In

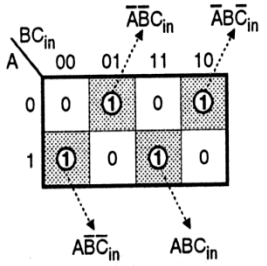
Explanation 1M

		this manner, a four bit number can be stored in the register. After four more clock pulses, this data will be shifted out of the register. Shift Left:   	***Logical diagram 2M*** ***Timing diagram 1M***
6.	**a) i)** Ans.	**Attempt any two of the following:** **State any two applications of counters.** • In digital clock. • In the frequency counters. • In time measurement. • In digital voltmeters. • In the frequency divider circuits.	**16** ***2M*** ***Any 2 applications 1M each***
	ii) Ans.	**Design full adder circuit using K-map. Implement using logic gates.** In Half adder there is no provision to add the carry generated by lower bits while adding present inputs that is when multibit addition is performed. Hence a third input is added and this circuit is used to add A_n, $B_n$and C_{n-1} where A_n, B_n are present state inputs and C_{n-1} is the last state output that is previous carry. This circuit is known as Full Adder	***6M*** ***Definition 1M***

An	Bn	Cn-1	Sum Sn	Carry Cn
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table 1M

For the sum output



(a) : K-map for sum output

K-map sum 1M

Expression for sum output

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + AB\bar{C}_{in} + A\bar{B}\bar{C}_{in}$$

$$S = C_{in}(\bar{A}\bar{B} + AB) + \bar{C}_{in}(\bar{A}B + A\bar{B})$$

EX-NOR EX-OR

$$\therefore S = C_{in}(\overline{A \oplus B}) + \bar{C}_{in}(A \oplus B)$$

Let $X = A \oplus B$

$$\therefore S = C_{in}\bar{X} + \bar{C}_{in}X = C_{in} \oplus X$$

$$\therefore S = C_{in} \oplus (A \oplus B)$$

But $A\bar{B} + \bar{A}B = A \oplus B$

$$\therefore S = C_{in} \oplus A \oplus B$$

For carry output

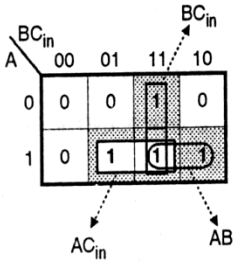


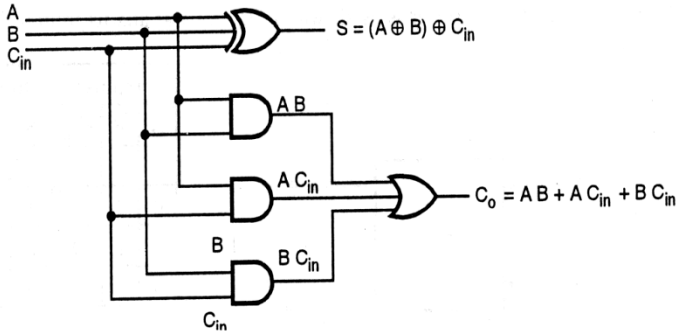
Fig. 6.3.6(b) : K-map for carry output

k-map carry 1M

Expression for carry output

$$C_o = AB + AC_{in} + BC_{in}$$

Logic diagram for full adder :



Logical circuit 2M

6. b) i) Ans.

Differentiate combinational and sequential logic circuits (2pts). *2M*

Sr. No.	Combinational circuits	Sequential circuits
1	In combinational circuits, the output variables depends on the combinational of input variables.	In sequential circuits, the output variables depends upon the present inputs as well as on the past output.
2	Memory unit is not required in these circuits.	Memory unit is required in these circuits to store the previous output.
3	These circuits are faster in speed because the delay between the input and output is due to the propogation delay.	Sequential circuits are slower than the combinational circuits.
4	These are easy to design.	These are complex in designing.
5	Ex: Parallel Adder.	Ex: Serial Adder.

Any 2 points 1M each

ii) Ans.

State the applications of shift registers. *2M*

- For temporary data storage.
- For multiplication and division.
- Parallel to serial converter.
- Ring counter.

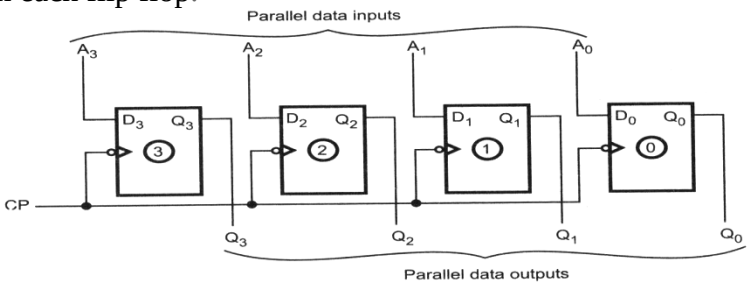
Any 2 applications 1M each

iii) Ans.

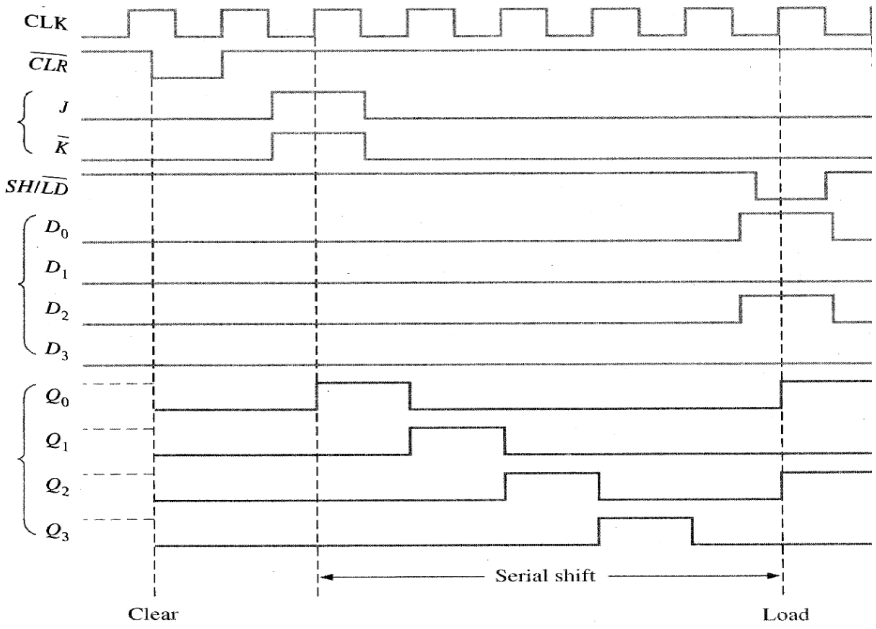
Draw the block diagram of 4-bit PIPO shift register and explain its working with timing diagram. *4M*

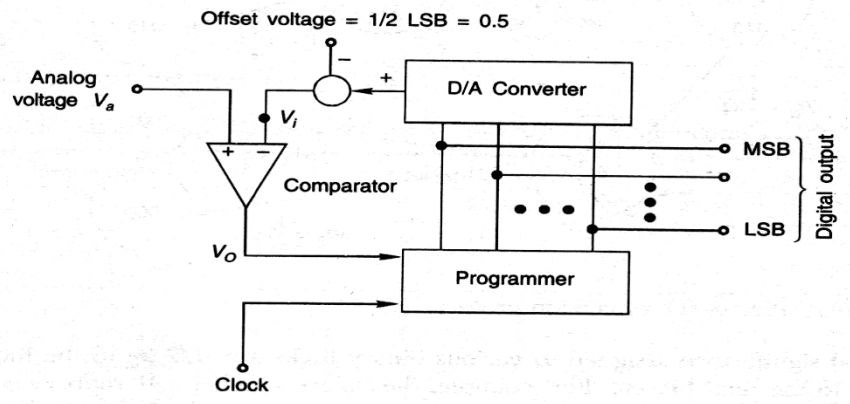
In this register, the input is given in parallel and the output also collected in parallel. The clear (CLR) signal and clock signals are connected to all the 4 flip flops. Data is given as input separately for each flip flop and in the same way, output also collected individually from each flip flop.

Explanation 1M



Logical diagram 2M

			***Timing diagram 1M***
6.	**c) i)** Ans.	**Describe specification of DAC.** **1. <u>Resolution</u>:** This is the smallest possible change in output voltage as a fraction or % of the full scale output range. The resolution can be given as: Resolution = 2^n *OR* Resolution is also defined as "the ratio of change in analog output voltage resulting from a change in 1 LSB at the digital input. Resolution = $\frac{V_{FS}}{2^n - 1}$ **2. <u>Linearity</u>:** In a D/A converter, equal increments in the numerical significance of the digital input should result in equal increments in the analog output voltage. In an actual circuit, the input-output relationship is not linear. This is due to the error in resistor values and voltages across the switches. The linearity of a converter is a measure of precision with which linear I-O relationship is satisfied. **3. <u>Accuracy</u>:** The accuracy of a D/A converter is a measure of the difference between the actual output voltage and the expected output	***4M*** ***Any 4 1M each***

		voltage. It is specified as a % of full-scale or maximum output voltage. **4. Settling time:** When the digital input to a D/A converter changes, the analog output voltage does not change abruptly. The time required for the analog output to settle to within LSB of the final value after a change in the digital input is usually specified by the manufacturers & is called as settling time. **5. Temperature Sensitivity**: The analog output voltage for any fixed digital input varies with temperature. This is due to the temperature sensitivities of the reference voltage source, resistors, OP AMP etc.	
	ii) Ans.	**Describe the working of successive approximation type A to D converter with neat diagram.** The successive approximation A/D converter is as shown in fig. An analog voltage (V_a) is constantly compared with voltage Vi, using a comparator. The output produced by comparator (V_o) is applied to an electronic Programmer.  ❖ If $V_a=V_i$, then $V_o=0$ & then no conversion is required. The programmer displays the value of Vi in the form of digital O/P. ❖ But if $V_a \neq V_i$, then the O/P is changed by the programmer. ➢ If $V_a > V_i$, then value of V_i is increased by 50% of earlier value. ➢ But if $V_a < V_i$, then value of V_i is decreased by 50% of earlier value. This new value is converted into analog form, by D/A converter so as to compare it with V_a again. This procedure is repeated till we get $V_a=V_i$. As the value of V_i is changed successively, this method is called as successive-approximation A/D converter.	***4M*** ***Explanation 2M*** ***Diagram 2M***