MODEL ANSWER

SUMMER - 2017 EXAMINATION

Subject: Digital Techniques **Subject Code:** **17333**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

<table>
<tr><th>Q. No.</th><th>Sub Q.N.</th><th>Answer</th><th>Marking Scheme</th></tr>
<tr><td>1.</td><td>A)
i)
Ans.</td><td>Attempt any six:
Draw truth table for NAND and NOR gates.
Truth table of NAND and NOR gates:
NANDNOR
<table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table><table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table></td><td>6x2=12
2M

Each 1M</td></tr>
<tr><td></td><td>ii)

Ans.</td><td>Compare analog signal with digital signal according to nature/shape of signals and application.<table><tr><th></th><th>Analog Signal</th><th>Digital Signal</th></tr><tr><td>Shape of signal</td><td>Continuous in time. Can have any value in a limited range</td><td>Continuous in time. Can have only two possible values</td></tr><tr><td></td><td>Denoted by sine waves</td><td>Denoted by square waves</td></tr></table></td><td>2M

1M each</td></tr>
</table>

Applications	Amplifiers, Operational Amplifiers, telephones	Logic gates, microcontrollers, Computers	

iii) Ans.

State any two Boolean laws with expression. **2M**

Boolean laws:

A + 1 = 1
A + 0 = A
A . 1 = A
A . 0 = 0
A + A = A
A . A = A
A+B = B+A
A.B = B.A
(A + B) + C = A + (B + C)
(A B) C = A (B C)
A (B + C) = A B + A C
A + (B C) = (A + B) (A + C)

Any 2 1M each

iv) Ans.

Perform "BCD addition" for (2375) + (4933) = ? **2M**

2375	0010	0011	0111	0101
+				
4933	0100	1001	0011	0011
	---	---	---	---
	0110	1100	1010	1000
+		0110	0110	
	---	---	---	---
	0110	**1**0010	**1**0000	1000

Adding carry to the next four bit group

	0110	0010	0000	1000
+	0001	0001		
	---	---	---	---
	0111	0011	0000	1000
	7	3	0	8

Correct 2M

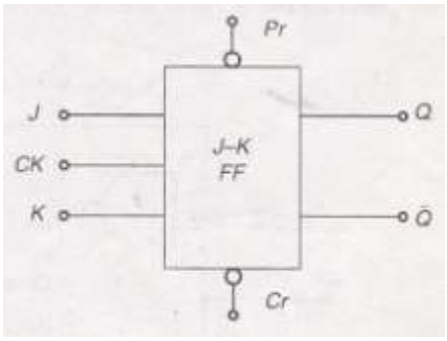
v) Ans.

State the difference between Half and Full adder. **2M**

Half adder is a circuit that adds 2 binary bits.
A full adder is a circuit the adds 3 bits (2 bits along with carry)

Each 1M

	vi) Ans.	**Write any four applications of counter.** **Applications of counters:** 1. Frequency counters 2. Digital clocks 3. Analog to digital convertors. 4. With some changes in their design, counters can be used as frequency divider circuits. The frequency divider circuit is that which divides the input frequency exactly by '2'. 5. In time measurement. That means calculating time in timers such as electronic devices like ovens and washing machines. 6. We can design digital triangular wave generator by using counters.	**2M** ***Any four ½M each***
	vii) Ans.	**State application of MUX and De-MUX.** **Application of MUX:** 1. Implementing multi output combinational logic circuit 2. Multiplexer allow the process of transmitting different type of data such as audio, video at the same time using a single transmission line. 3. In telephone network, multiple audio signals are integrated on a single line for transmission with the help of multiplexers. 5. Multiplexers are used to implement huge amount of memory into the computer, at the same time reduces the number of copper lines required to connect the memory to other parts of the computer circuit. 6. Multiplexer can be used for the transmission of data signals from the computer system of a satellite or spacecraft to the ground system using the GPS (Global Positioning System) satellites. **Application of De-MUX:** 1. Decoder 2. Demultiplexer is used to connect a single source to multiple destinations. 3. In an ALU circuit, the output of ALU can be stored in multiple registers or storage units with the help of demultiplexer. 4. Serial data from the incoming serial data stream is given as data input to the demultiplexer at the regular intervals.	**2M** ***Any two application 1M each***
	viii) Ans.	**Draw symbol of J-K flip-flop and write its truth table.** **Symbol of flip-flop:**	**2M**



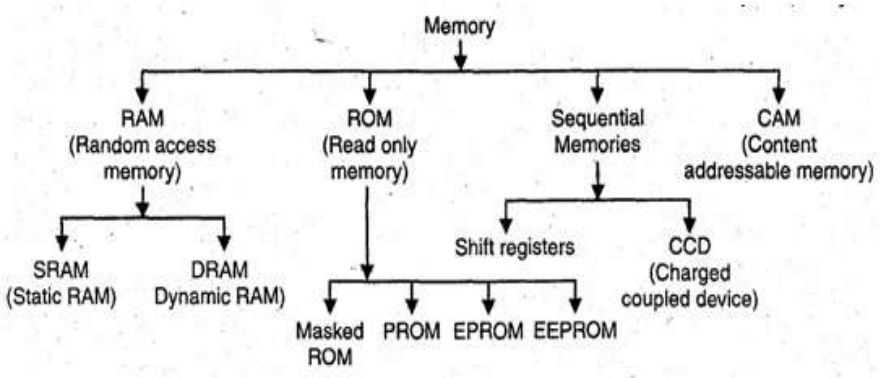
1M J_K flip-flop

Truth Table:

Inputs		Output
J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q_n}$

Truth Table 1M

1.	**(B) i)**	**Attempt any two:** **List types of digital to analog converters and state specifications of ADC (any four).**	**4x2=8** **4M**
	Ans.	**Types of Digital to Analog converters and specifications** 1. Weighted resistor D to A converter 2. R – 2R D to A converter	***Types 2M***
		Specifications of ADC: 1. Resolution 2. Accuracy 3. Conversion time 4. Linearity 5. Analog input voltage 6. Format of digital output	***Any four specifications ½ M each***
	ii)	**Describe classification of memories.**	**4M**
	Ans.	**Classification of Memories:**	



Classification of Memories 1M

Random Access Memories (RWM or RAM)
In this type of memory the memory locations are organized in such a way that any memory location requires equal time for writing or reading. RAMs can be static or dynamic and can be fabricated using bipolar or Unipolar technologies.

Description 3M

Read Only Memories (ROM)
These memories are meant only for reading the information from it. The process of entering information is done outside the system where it is used. This type of memory is used to store fixed tables of functions etc. These memories are further classified on the basis of technique employed in storing information into the memory or their erasable properties.
These are

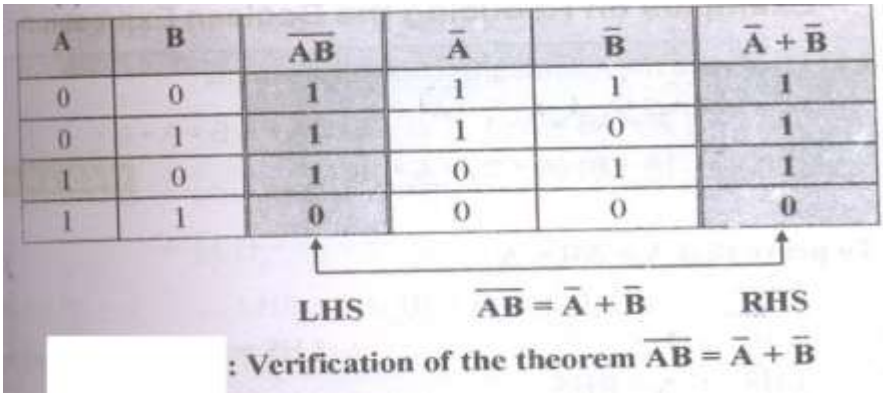
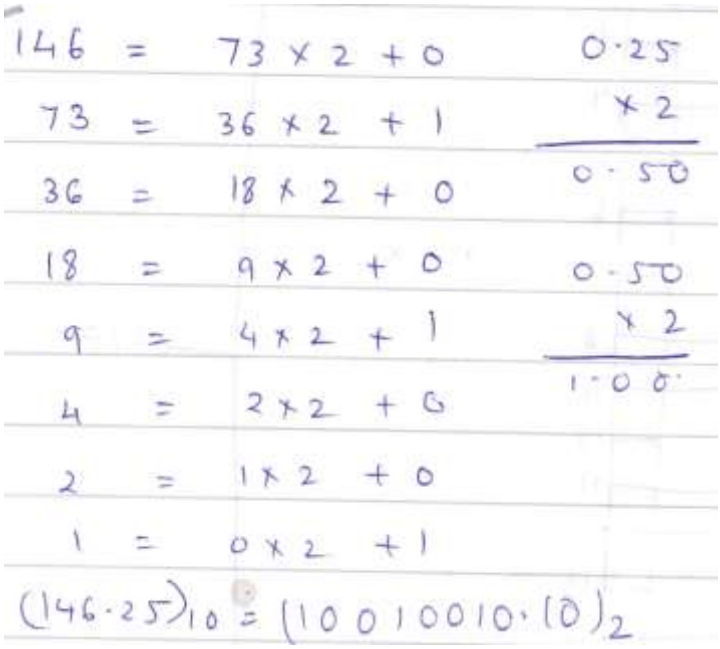
1. ROM (Read Only Memory)
2. PROM (Programmable Read Only Memory)
3. EPROM (Erasable Programmable Read Only Memory)
4. EEPROM (Electrically Erasable PROM)

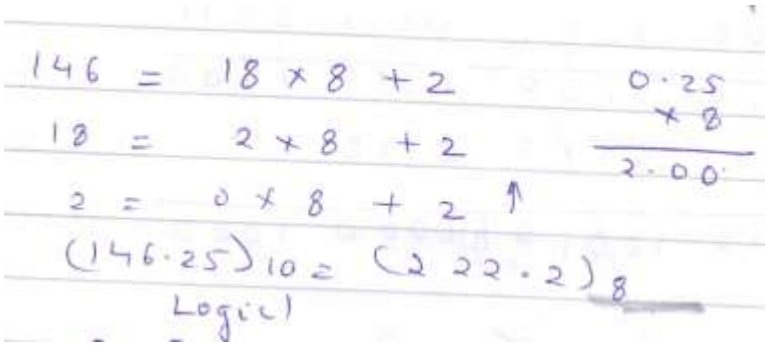
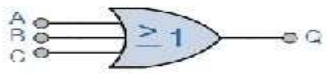
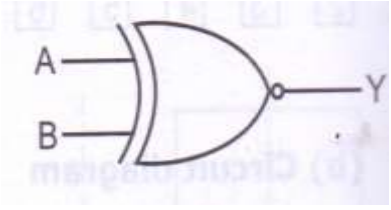
Programmable ROM (PROM)
It can be programmed by the user. It can be programmed only once after which its contents are permanently fixed as ROM. To write data into a PROM a PROM programmer or PROM burner is used. At the time of manufacturing a blank PROM, the data is entirely made up of 1's. The PROM programmer writes data into the PROM by applying high voltage pulses which are not encountered during normal operation. Once the PROM has been programmed in this way, its

		contents can never be changed. Hence PROMs are also known as One-time programmable ROMs. **Erasable PROM (EPROM)** It can be programmed again and again. Once programmed the EPROM is a non-volatile memory that holds stored data indefinitely. EPROM can be erased by exposure to strong ultraviolet light for about 20 minutes or longer. The programming is done with EPROM programmer which is a separate unit. EPROMs are identified by the presence of a transparent quartz window, which permits ultraviolet light during erasing. **Electrically Erasable PROM (EEPROM)** It is non-volatile memory which allows its entire contents or selected locations to be erased and rewritten. EEPROM need not be removed from the circuit to erased and reprogrammed.	
	iii) Ans.	**State and explain De-morgan theorems.** Verification of the second theorem : $\overline{A+B} = \bar{A} \cdot \bar{B}$ Truth table to verify De-Morgan's second theorem **Theorem1**: It state that the, complement of a sum is equal to product of complement **Theorem2:** It states that, the complement of a product is equal to sum of the complements.	**4M** ***Explanation 4M***

A	B	$\overline{A+B}$	$\bar{A}$	$\bar{B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

LHS $\overline{A+B} = \bar{A} \cdot \bar{B}$ RHS

		 : Verification of the theorem $\overline{AB} = \bar{A} + \bar{B}$	
2.	**a)** Ans.	**Attempt any four:** **Convert following number into its equivalent = $(146.25)_{10}$** **i) Binary number:** **ii) Octal number respectively.** **i) Binary number:** 	**4x4=16** **4M** ***2M***

		ii) Octal number:  	***2M***
	b) Ans.	**Draw symbol and truth table for (i) 3 i/p OR gate (ii) 2 i/p EX-NOR gate.** **(i) 3 i/p OR gate:** Symbol  3-input OR Gate Truth Table C B A Q 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1 1 **(ii) 2 i/p EX-NOR gate.** Truth Table Inputs: A, B — Output: Y = $\overline{A \oplus B}$ 0 0 1 0 1 0 1 0 0 1 1 1  	**4M** ***3 i/p OR gate 2M*** ***2 i/p EX-NOR gate 2M***

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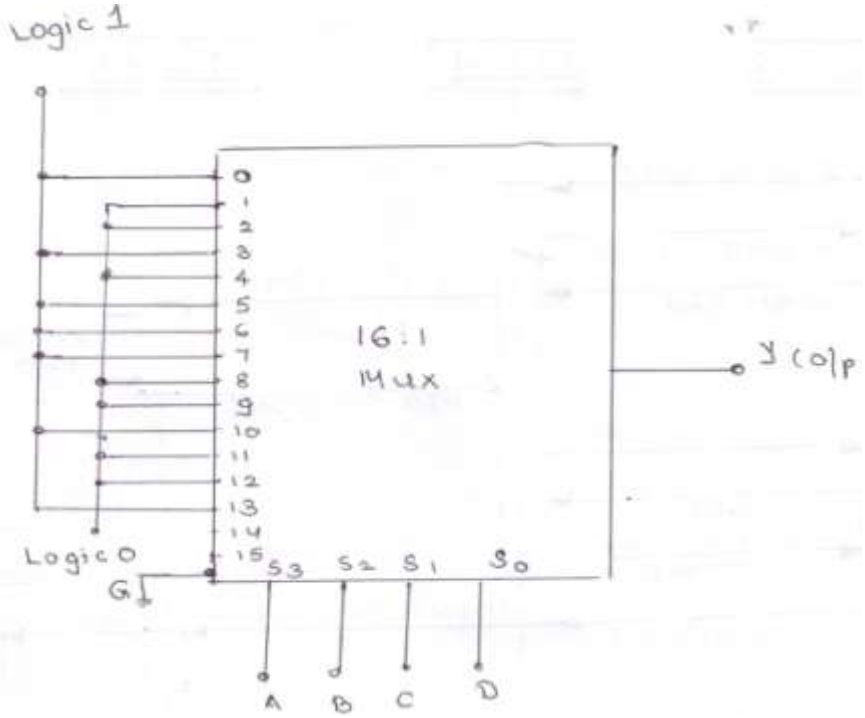
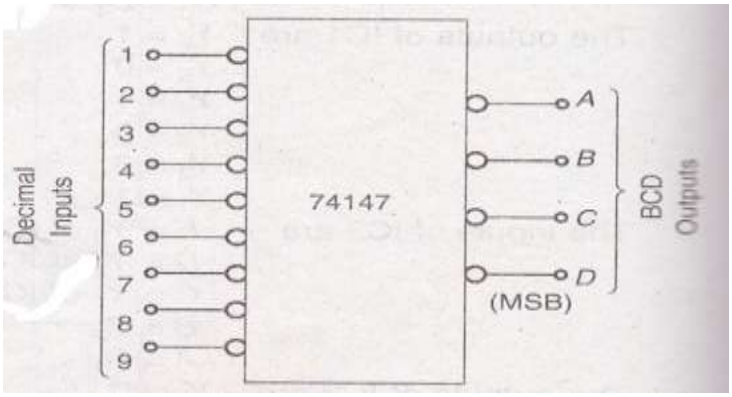
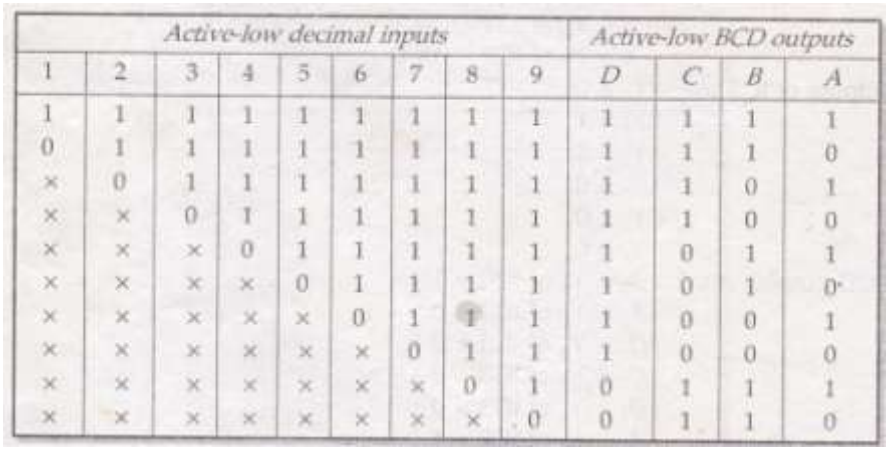
	c) Ans.	**Implement the following logic expression using 16 : 1 MUX Y = ∑ m (0, 3, 5, 6, 7, 10, 13).**  	**4M** ***4M***
	d) Ans.	**Draw block diagram of decimal to BCD encoder and write its truth table.**  **Block Diagram of Decimal to BCD encoder**	**4M** ***Diagram 2M***



Active-low decimal inputs									Active-low BCD outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0
×	0	1	1	1	1	1	1	1	1	1	0	1
×	×	0	1	1	1	1	1	1	1	1	0	0
×	×	×	0	1	1	1	1	1	1	0	1	1
×	×	×	×	0	1	1	1	1	1	0	1	0
×	×	×	×	×	0	1	1	1	1	0	0	1
×	×	×	×	×	×	0	1	1	1	0	0	0
×	×	×	×	×	×	×	0	1	0	1	1	1
×	×	×	×	×	×	×	×	0	0	1	1	0

Truth Table

Truth table 2M

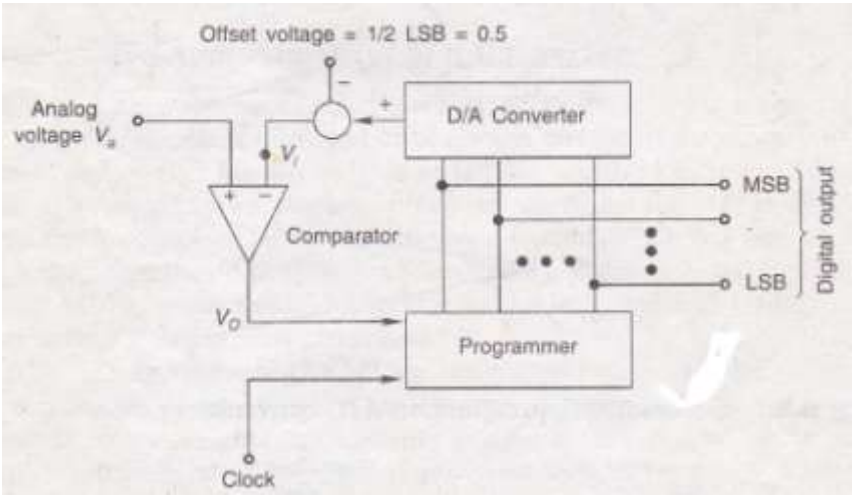
e) Ans. **Compare combinational and sequential circuits (four points).** **4M**

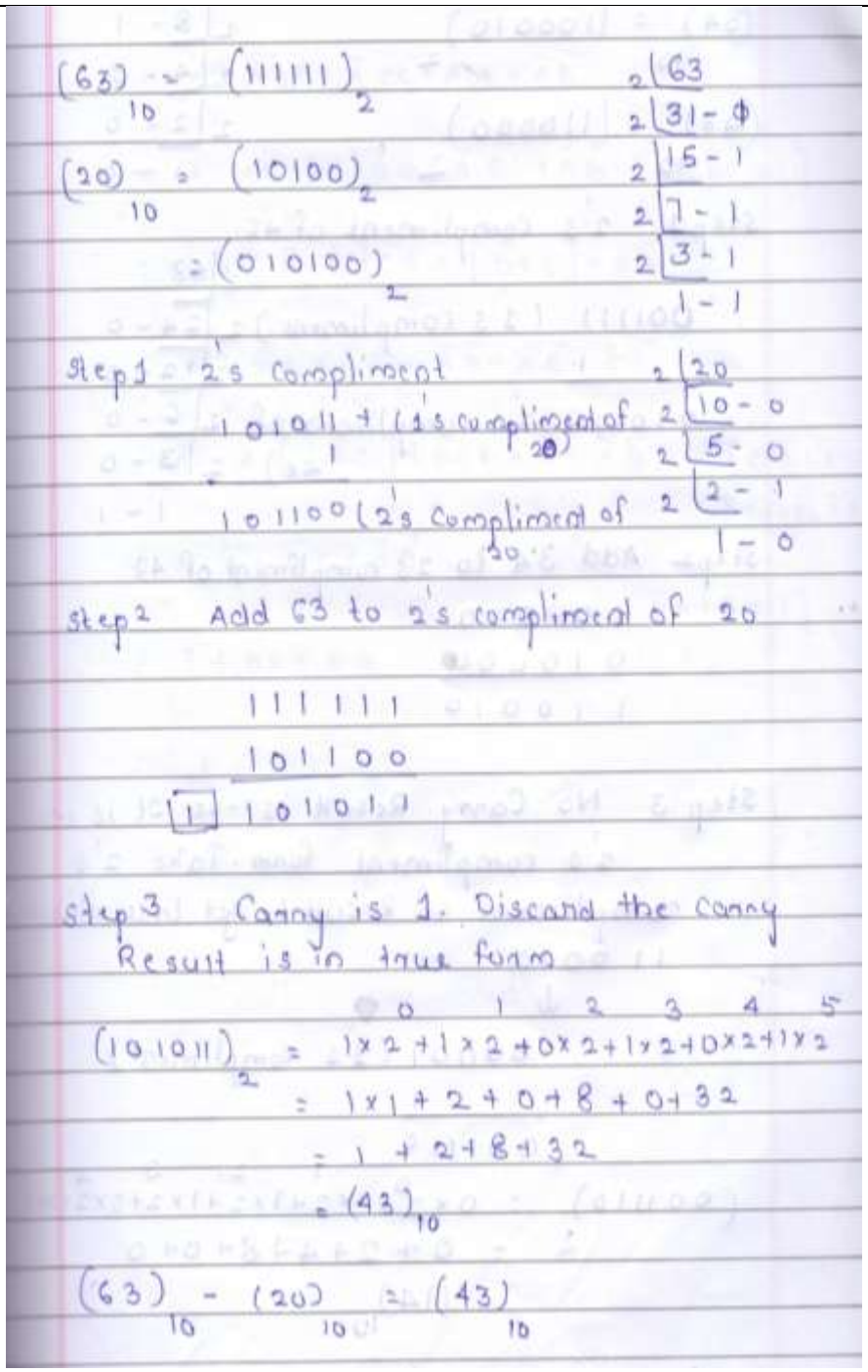
Combinational Logic Circuits	Sequential Logic Circuits
Output is a function of the present inputs (Time Independent Logic)	Output is a function of clock, present inputs and the previous states of the system.
Do not have the ability to store data (state).	Have memory to store the present states that is sent as control input (enable) for the next operation.
Logic gates are the elementary building blocks.	Flip flops (binary storage device) are the elementary building unit.
Independent of clock and hence does not require triggering to operate.	Clocked (Triggered for operation with electronic pulses).
Used mainly for Arithmetic and Boolean operations.	Used for storing data (and hence used in RAM).
It does not require any feedback. It simply outputs the input according to the logic designed.	It involves feedback from output to input that is stored in the memory for the next operation.

Any four points 1M each

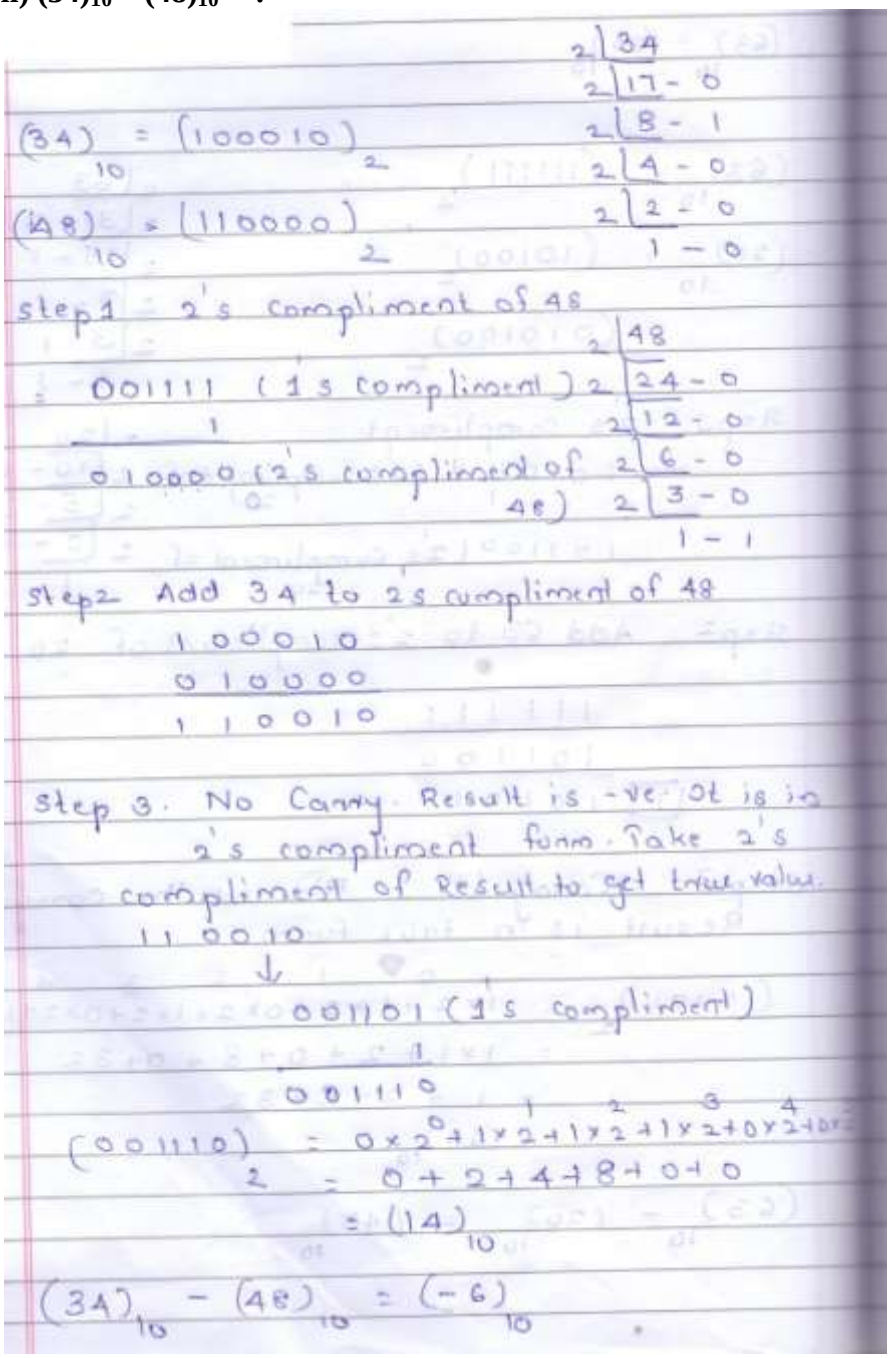
f) Ans. **Draw circuit diagram of successive approximation type ADC and explain its working.** **4M**

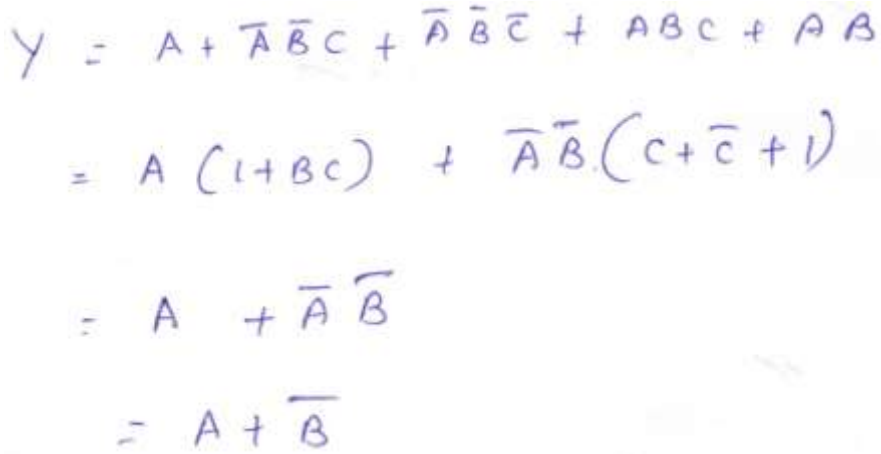
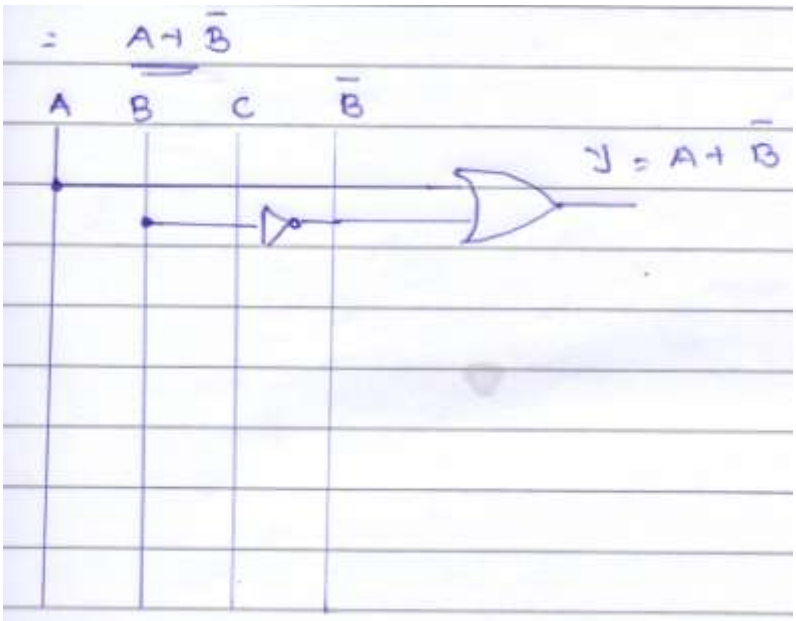
The comparator serves the function of the scale, the output of which is

		used for setting resetting the bits at the output of the programmer/ This output is converted into equivalent analog voltage from which the offset voltage is subtracted and then applied to the inverting input terminal of the comparator. It should be noted that the offset weight was added on the side of the unknown weight, and therefore, it is to be subtracted from the known weight side for getting the equivalent effect. The outputs of the programmer will change only when the clock pulse is present. To start conversion, the programmer sets the MSB to 1 and all other bits to 0. This is converted into analog signal by the D/A converter and the comparator compares it with the analog input voltage. If the analog input voltage $V_a \geq V_i$, the output voltage V_O of the comparator is HIGH which sets the next bit also. On the other hand, if $V_a < V_i$, then $V_O$is LOW which resets the MSB and sets the next bit. Thus, a 1 is tried in each bit of the D/A converter until the binary equivalent of the analog input voltage is obtained.  **Successive-approximation A/D converter.**	***Explanation 2M*** ***Diagram 2M***
3.	**a)** Ans.	**Attempt any four:** **Perform binary subtraction using 2's complements of following:** **i) $(63)_{10} - (20)_{10}$** **ii) $(34)_{10} - (48)_{10}$ = ?** **i) $(63)_{10} - (20)_{10}$:**	**4x4=16** **4M**

			***2M***

(63)10 = (111111)2
(20)10 = (10100)2
= (010100)2
Step 1 2's Complement
10101 + (1's complement of 20)
1
101100 (2's Complement of 20
Step 2 Add 63 to 2's complement of 20
111111
101100
1 101011
Step 3 Carry is 1. Discard the carry
Result is in true form
(101011)2 = 1×2+1×2+0×2+1×2+0×2+1×2
= 1×1+2+0+8+0+32
= 1+2+8+32
= (43)10
(63)10 - (20)10 = (43)10

		ii) $(34)_{10} - (48)_{10}$ = ?  $(34)_{10} = (100010)_2$ $(48)_{10} = (110000)_2$ step 1 2's compliment of 48 001111 (1's compliment) + 1 010000 (2's compliment of 48) step 2 Add 34 to 2's compliment of 48 100010 010000 110010 step 3. No Carry. Result is -ve. It is in 2's compliment form. Take 2's compliment of Result to get true value. 110010 ↓ 001101 (1's compliment) + 1 001110 $(001110)_2 = 0\times2^0+1\times2^1+1\times2^2+1\times2^3+0\times2^4+0\times2^5$ $= 0+2+4+8+0+0$ $= (14)_{10}$ $(34)_{10} - (48)_{10} = (-6)_{10}$	***2M***

	b) Ans.	**Simplify the following and realize it $Y = A + \bar{A}\bar{B}C + \bar{A}\,\bar{B}\bar{C} + ABC + \bar{A}\bar{B}$**  	**4M** ***2M*** ***2M***
	c) Ans.	**Explain full adder with logic diagram and its truth table and proper expressions.** It is a combinational circuit which performs the arithmetic sum of three input bits. It consists of 03 inputs and two outputs.	**4M**

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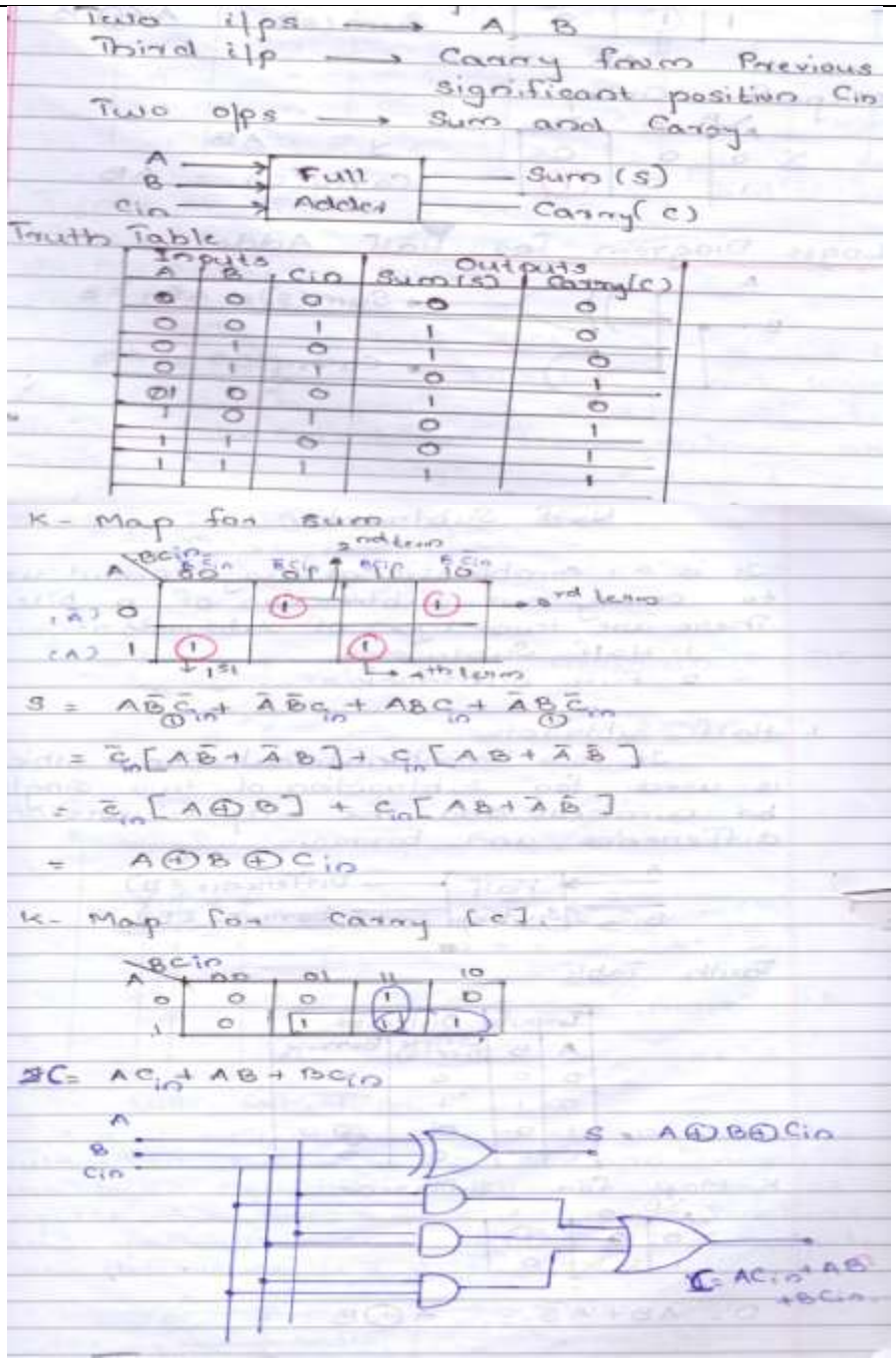
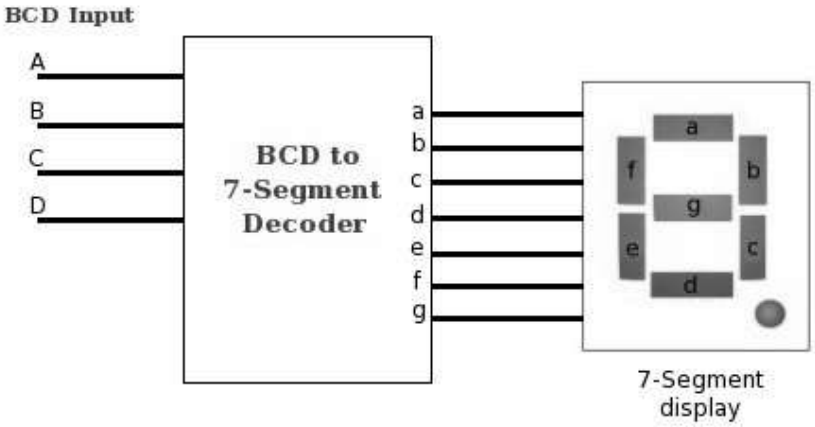


Explanation & Truth table 1M

k-map + expression 2M

Logic diagram 1M

	d) Ans.	**Draw diagram of BCD to segment decoder using IC 7447 with truth table.**	**4M**

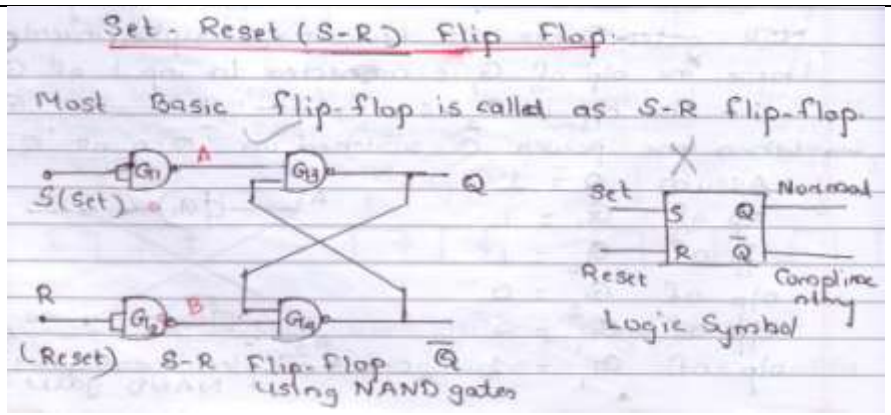


Circuit diagram 2M

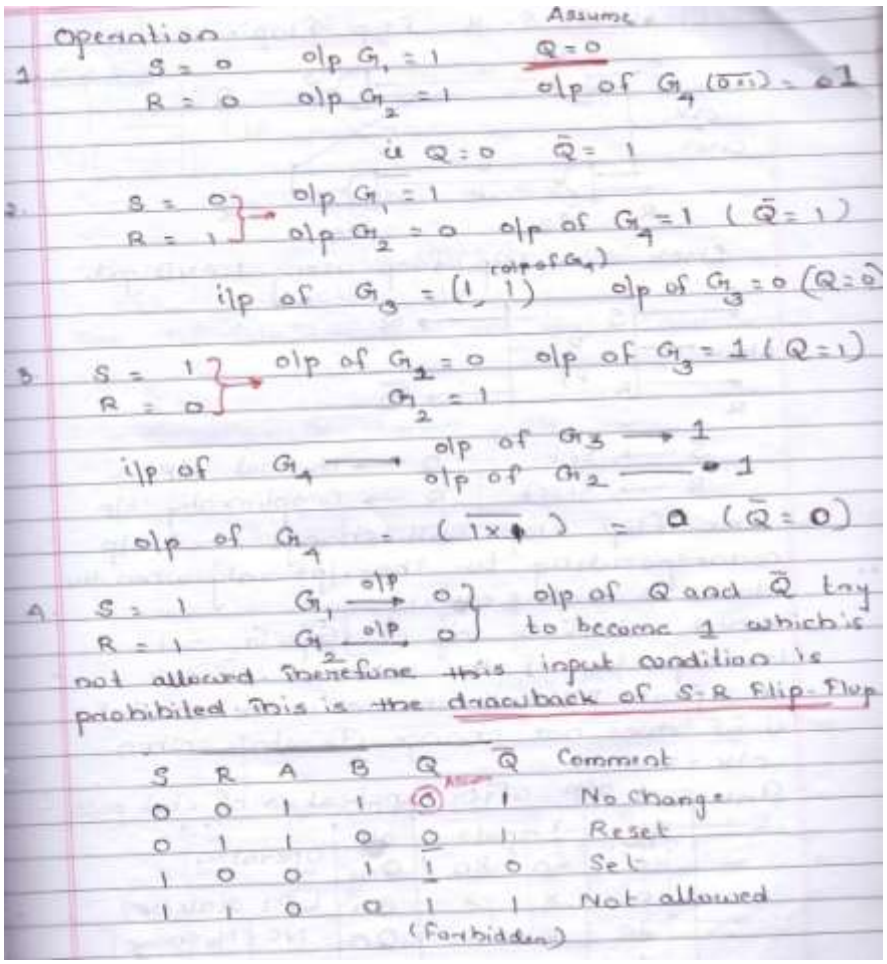
Binary Inputs				Decoder Outputs							7-Segment Display Outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9

Truth Table 2M

	e) Ans.	**Describe the operation of RS Flip Flop using NAND gates only.** **(*(Note: Consider the working of Clocked RS Flip Flop also)***	**4M**

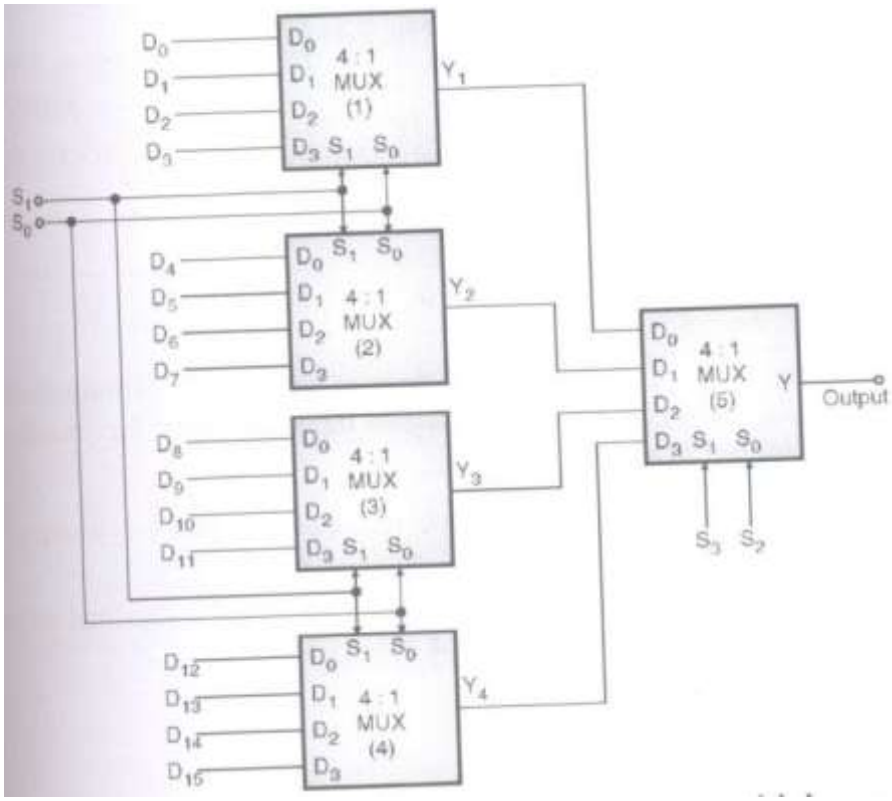
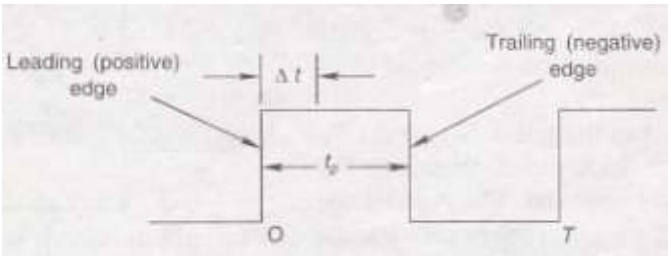


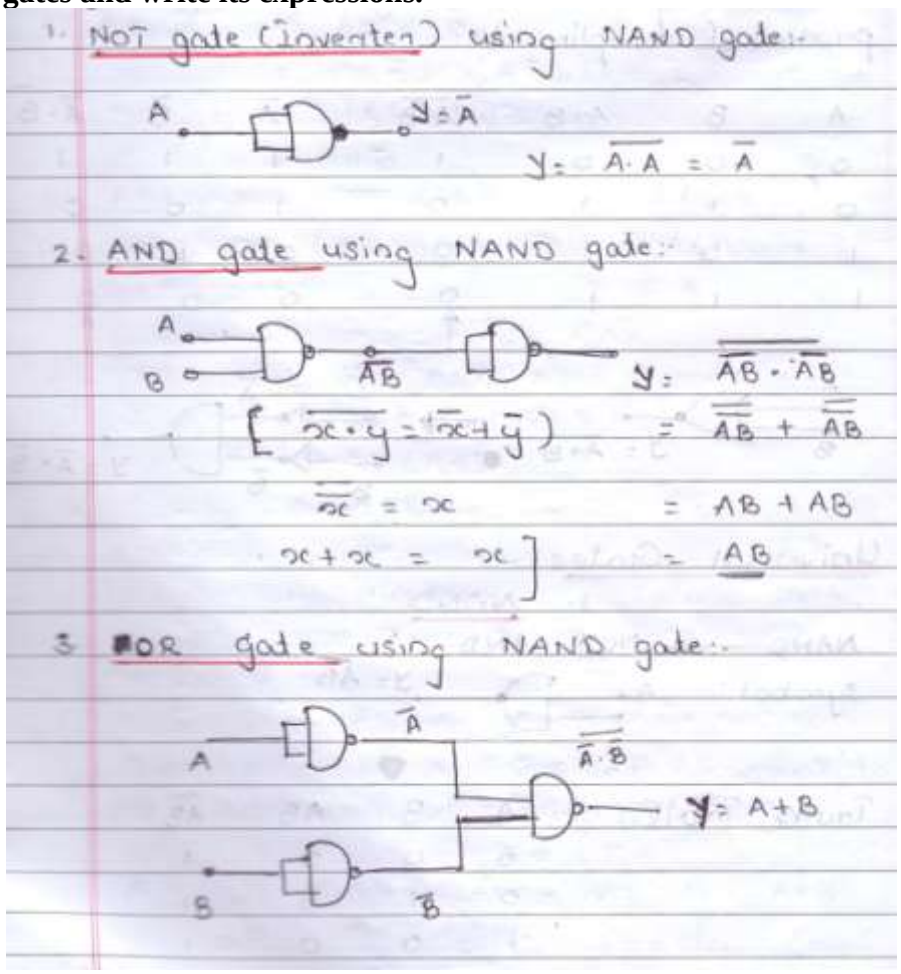
2M Diagram

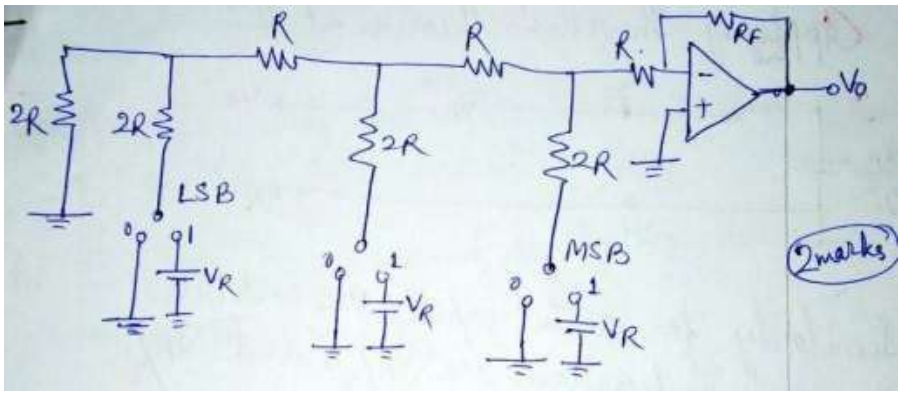
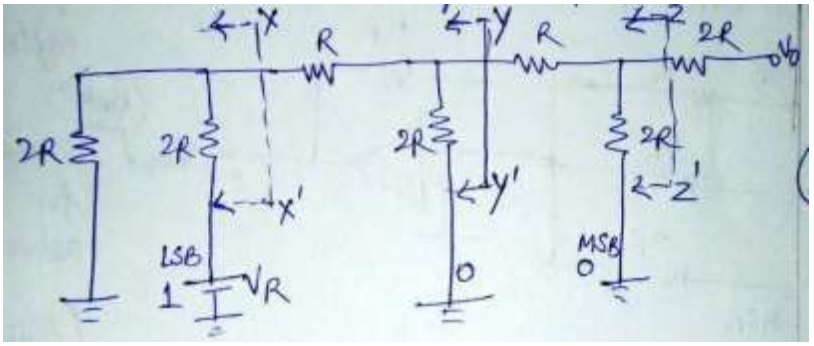
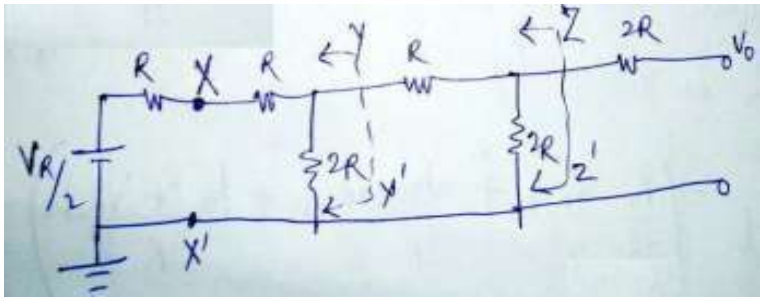


2M Explanation

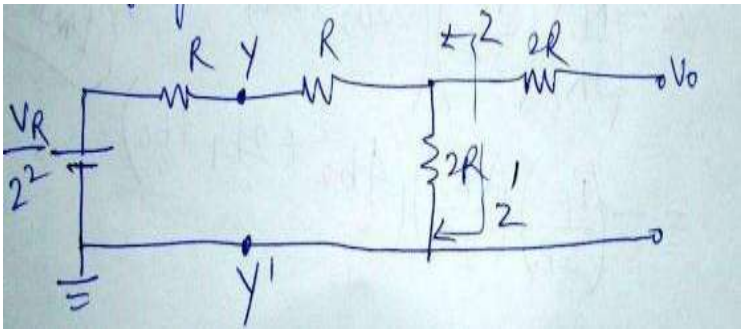
	f) Ans.	**State advantages and disadvantages of (i) Ramp type ADC (ii) Dual slope type ADC.** **(i) Ramp type ADC:** **Advantages of Ramp type ADC:** 1. It is very simple in construction. 2. It is easy to design. 3. It is last expensive. 4. Its speed can be adjusted by adjusting the clock frequency 5. It is faster than a dual slope ADC. **Disadvantages of Ramp type ADC:** 1. It is comparatively very slow. 2. The conversion time does not remain constant. 3. The conversion time can be as long as clock cycle period for high input voltages. 4. It needs longer conversion time. **(ii) Dual slope type ADC:** **Advantages of Dual slope type ADC::** 1. It is simple and relatively inexpensive. 2. It has high conversion accuracy. 3. It is more stable and of low cost. 4. It is not affected by time, temperature and input voltage. 5. It does not require crystal oscillator for stability. 6. It is less sensitive to noise. **Disadvantages of Dual slope type ADC:** 1. It has large conversion time as compared to any other ADC. 2. It has very low speed of conversion.	**4M** ***Any two advantages and disadvantages of Ramp type ADC each 1M*** ***Any two advantages and disadvantages of Dual slope type ADC each 1M***
4.	**a)** Ans.	**Attempt any four:** **Construct 16:1 multiplexer using 4:1 multiplexer. Draw diagram.**	**4x4=16** **4M**

			***Correct implementation 4M***
	b) Ans.	**What is race around condition? How can it be overcome?** In J-K Flip Flop, when the I/p J = 1 & K = 1then the O/p of J-K flip flop is Q_n compliments of previous O/p. Let Q = 0 & clock pulse is applied as  At a time interval Δt, the O/p will change to $\overline{Q_n}$ that means the O/p now is Q = 1.Now we have J =1, K = 1 & Q = 1. After another time interval Δt, the O/p will again change from 1 to 0	**4M** ***Explanation 4M***

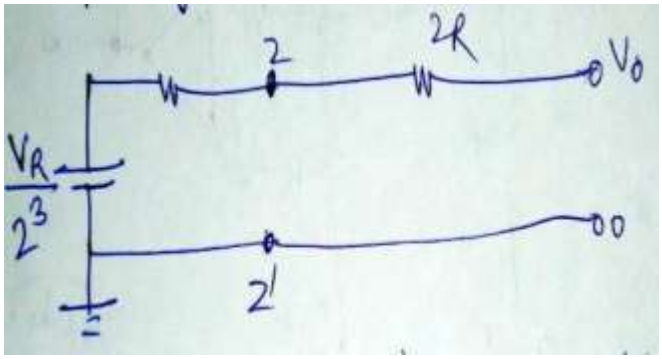
		($\overline{Q_n}$) due to feedback connection. Thus the O/p oscillates back and forth between 0 to 1 for the duration of the clock pulse. (1K = 1) Hence at the end of the clock pulse, when C/k=0, the value of a Q O/p is uncertain. This situation is called as race around condition. This race around condition can be avoided by using Master Slave I-K flip flop. A Master Slave J-K flip flop is a cascade of two J-K flip flop. The feedback from the output of second flip flop is given to the input of first flip-flop as shown in fig.	
	c) ANS.	**Draw AND, OR, NOT logic gates using any one of the universal gates and write its expressions.**  	**4M** ***Correct expressions 4M***

	d) Ans.	**Draw R-2R ladder digital to analog converter and explain its working.** R -2R ladder DAC uses two resistors R & 2R. The input is applied through digitally controlled switches.  For example if the digital input is 001  Applying Thevenins theorem at XX′  	**4M** ***Circuit diagram 2M*** ***Description 2M***

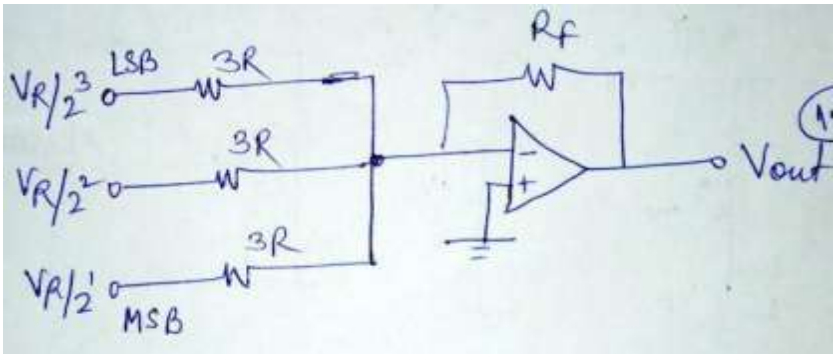
Applying Thevenins theorem at yy´



Applying Thevenins theorem at zz´



Similarly for digital input 010 and 100 the equivalent voltages are $VR/2^2$
And $VR/2^1$
respectively. The equivalent resistance is 3R in each case. So the simplified circuit of 3bit R-2R ladder DAC is



The analog output voltage for a given digital input is given by

$V_{out} = -((R_F/3R)\ V_R \times b_0/2^3 + R_F/3R\ V_R \times b_1/2^2 + R_F/3R\ V_R \times b_2/2^1)$

$= -(R_F/3R)(V_R/2^3)(2^2b_2 + 2^1b_1 + 2^0b_0)$

$= -(R_F/3R)(V_R/2^3)(4b_2 + 2b_1 + b_0)$

e) Ans.

Describe following number systems with respect to their base/radix, digits/symbols and its example. (i) Octal number (ii) Hexadecimal number. **4M**

Binary	Base/ Radix	Digits/symbols	Example
Octal number	8	0, 1, 2, 3, 4, 5, 6, 7	$(3567.25)_8$
Hexadecimal number	16	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, f	$(3FA9.56)_{16}$

Each 2M

f) Ans.

What is modulus counter? Design MOD-7 counter using IC 7490. **4M**

Modulus of a counter. Number of states through which the counter passes during its operation.

A flip flop has 02 states. Thus the group of 'N' flip flops will have 2^n states. This means it is possible to make a module 2^n counter using 'n' flip-flops.

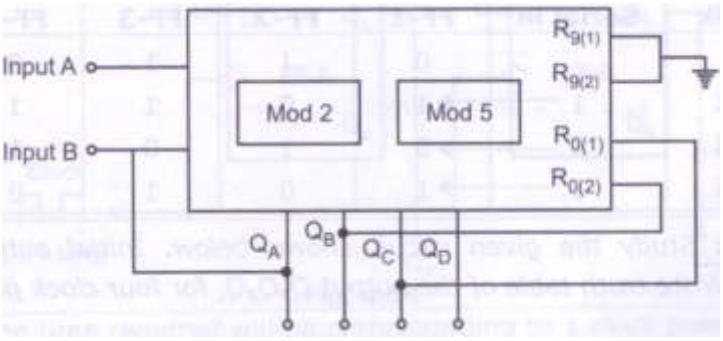
However it is desired to have a module m counter the no. of FF's required is determined by the following equation.

$m \leq 2^N$

N – Minimum value of N which satisfies the equation.

Explanation 4M

State	clk	Q_C	Q_B	Q_A
Initially 1	↓	0	0	0
2	↓	0	0	1
3	↓	0	1	0
4	↓	0	1	1
5	↓	1	0	0
6	↓	1	0	1
7	↓	1	1	0



5. **a)** Ans.

Attempt any four: **4x4=16**

Compare CMOS and TTL Logic families. **4M**

Sr No.	Parameters	TTL	CMOS
1	Basic gates	NAND	NOR or NAND
2	Fan-in	8	10
3	Fan-out	10	>50
4	Power dissipation per gate	10mW	0.01mW
5	Noise margin (immunity)	0.4V good	5V (excellent)
6	Propagation delay	10 ns	70 ns
7	Speed-power product	100	0.7
8	Clock rate for flip-flop	35 MHz	10 MHz
9	Available function	Very large	Large
10	Packing Density	Lower	Larger
11	Cost	Low	Very low.

Any 4 points 1M each

b) Ans.

Draw and explain working of Hex to Binary encoder with truth table. **4M**

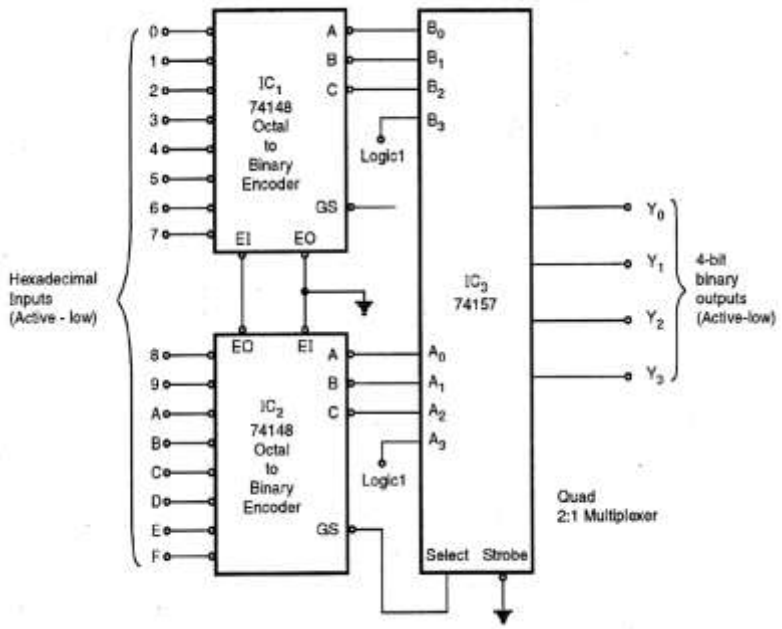
Hexadecimal to Binary Encoder can be constructed by using two octal to binary encoder IC 74148. The lower 8-bits are applied to inputs of IC-1 where as higher 8-bits are applied to inputs of IC-2. The enable inputs are so connected that only one IC is enabled at a time. To achieve this EO of the IC-2 is connected to EI of IC-1. The binary outputs of both these ICs are applied as inputs to IC 74157 which is a Quad 2:1 multiplexer.

GS output of IC 74148 is connected to select input of 74157. GS o/p will go low when one of its input is active. The low signal at select

Explanation 1M

input of 74157 will select A input and produce a binary number.
But is GS is high then a high signal at the select input of 74157 will select B input and produce the binary output.

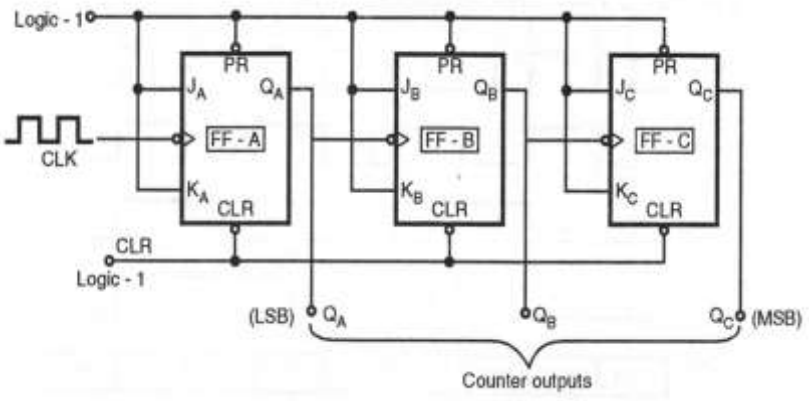
Inputs									Outputs				
$\overline{EI}$	$\overline{I_0}$	$\overline{I_1}$	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	$\overline{GS}$	$\overline{EO}$
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	X	0	1	1	1	1	1	1	1	1	0	0	1
0	X	X	0	1	1	1	1	1	1	0	1	0	1
0	X	X	X	0	1	1	1	1	1	0	0	0	1
0	X	X	X	X	0	1	1	1	0	1	1	0	1
0	X	X	X	X	X	0	1	1	0	1	0	0	1
0	X	X	X	X	X	X	0	1	0	0	1	0	1
0	X	X	X	X	X	X	X	0	0	0	0	0	1



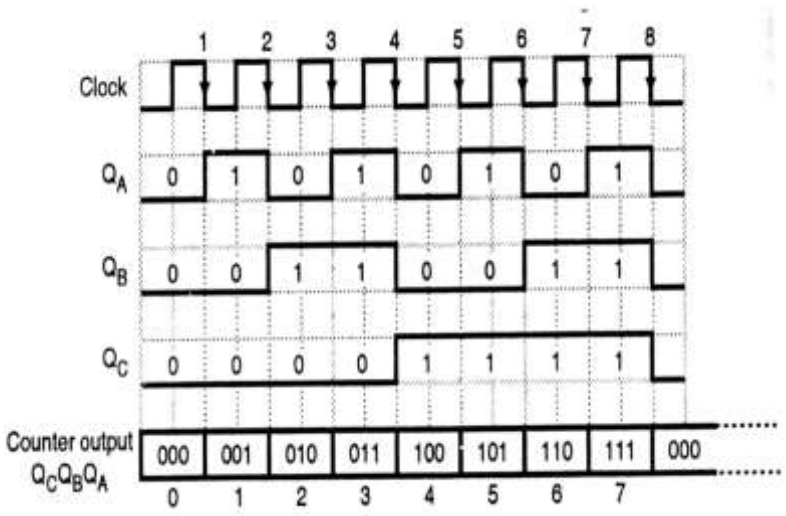
Truth table 1M

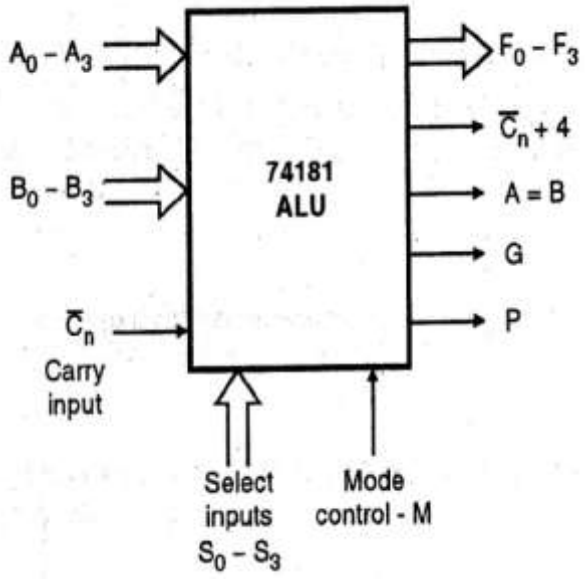
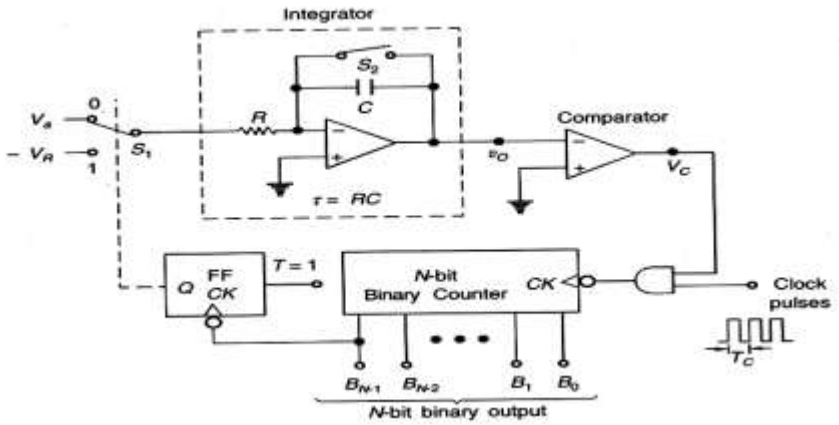
Diagram 2M

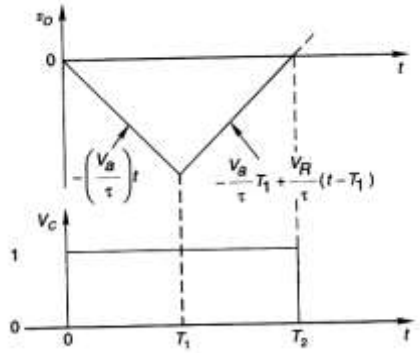
	c) Ans.	**Explain the operation 3-bit asynchronous counter with diagram.** The number of states in 3-bit counter is 8 that require 3 flip-flops and QA, QB and QC are the output of the flip-flops. The output QA of the least significant F/F changes for every clock pulse. This can achieved by using the T-type F/F with TA=1. The output QB makes a transition from 0-1 or 1-0 whenever QA changes from 1 to 0. Therefore if QA is connected to the clock input of next T-type F/F FF1 with TB=1, QB goes from 1-0. Similarly QC makes a transition whenever QB goes from 1-0 and this is achieved by connecting QB to the clock input of the most significant FF2 and TC=1.	**4M** ***Count sequence + wavefo rm: 2M*** ***Diagra m 2M***



COUNT-UP Mode			
States	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

			
	d) Ans.	**Draw labeled block diagram of 74181 ALU.** A combinational circuit used for performing ALU operations is as shown: The block diagram of 74181 ALU is as shown. The various inputs and output control lines are: 1. A and B: 4-bit binary data input. 2. $\overline{C}_n$: Carry input. 3. $\overline{C}_{n+4}$: Carry output. 4. F: 4-bit Binary data output. 5. G: Carry Generate output. 6. P: Carry propagate output. 7. A = B: Logic 1 on this line indicates A = B. G and P outputs are used when more than one 74181 are cascaded along with 74182 Look ahead Carry Generator circuit to make arithmetic operations faster. Select inputs are used to select the specific operations out of the available. Mode control (M) is used to select between the operations. ❖ M = 0: Arithmetic Operations. ❖ M = 1: Logical Operations. $\overline{C}_{n+4}$ is used for subtraction operation which indicates the sign of output. Logic 0 indicates positive result and logic 1 indicates result is negative and in its 2's complement form.	**4M**

			***Block diagram 4M***
	e) Ans.	**Draw circuit diagram and explain working principle of dual- slope type ADC.** The block diagram of this method is shown in Fig. It has 4 major blocks: an integrator, comparator, a binary counter & a switch driver. 	**4M** ***Diagram 2M***



Explanation 2M

The conversion process begins at t = O with the switch S1 in position 0, hence connecting the analog voltage Va to the input of the integrator.

The integrator output is Vo = $-\frac{1}{\tau}\int_0^t Vadt = -\frac{Va}{\tau}t$

This results in HIGH Vc, thus enabling the AND gate & the clock pulses reach the clock (CK) input terminal of the counter which was initially clear.

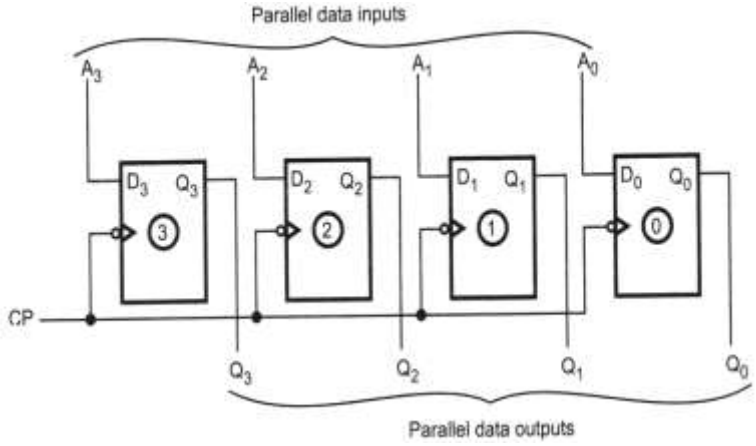
The counter counts from 00 ... 00 to 111 … 11 when (2^N–1) clock pulses are applied. At the next clock pulse (2^Nth) the counter is cleared & Q becomes 1. This controls the state of S1 which now moves to position 1 at T1, thereby connecting $-V_R$ to the input of the integrator. The output of the integrator now starts to move in the positive direction. The counter continues to count until Vo< O. As soon as Vo goes positive at T2, Vo goes LOW disabling the AND gate. The counter will stop counting in the absence of the clock pulses.

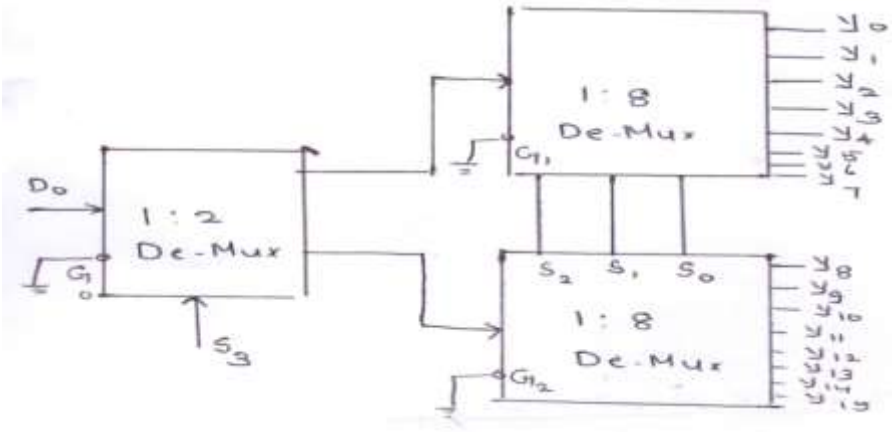
Advantages:

1. The analog input is independent of R, C and T. thus drifts in any of the components affects T1 and T2 in same proportion and ADC output remains unaffected.
2. Dual Slope ADC is capable of rejecting noise and hum.
3. Low cost.
4. Accuracy of ADC can be order of 0.05% suitable for many applications.

Dis-Advantages:

1. The conversion time of this device is more than other ADC.

	f) Ans.	**Draw proper labeled diagram of parallel in parallel out (4 bit) shift register and explain its working.**  The four bit binary input A3- A0 is applied to the data inputs D3 to D0 respectively of the four flip flops. As soon as the negative clock edge is applied the input binary bits will be loaded into the flip flops simultaneously. The loaded bits will appear simultaneously at the output side, only one clock pulse is essential to load all the bits.	**4M** ***Diagram 2M*** ***Explanation 2M***
6.	**a)** Ans.	**Attempt any two:** **Reduce following Boolean expression using laws and theory of Boolean algebra.** i) $A + BC = (A + B)(A + C)$. ii) $Y = (A + \bar{B})(\bar{A} + B)(A + B)$. **1.** $A + BC = (A + B)(A + C)$ $LHS = (A + B)(A + C)$ $(A + B)(A + C) = A(A + C) + B(A + C)$ $= A.A + AC + AB + AC$ $= A + AC + AB + BC$ $= A(1 + C + B) + BC$ $= A + BC = RHS$	**8x2=16** **8M** ***4M***

		2. $Y=(A+\bar{B})(\bar{A}+B)(A+B)$ $=[A(\bar{A}+B)+B(\bar{A}+B)](A+C)$ $=[A.\bar{A}+AB+\bar{A}B+B.B](A+C)$ $=[0+AB+\bar{A}B+B](A+C)$ $=[B(A+\bar{A})+B](A+C)$ $=(B.1+B)(A+C)$ $=(B+B)(A+C)$ $=B(A+C)$	***4M***
	b) Ans.	**i) Implement 1 : 16 demultiplexer using 1 : 8 demultiplexer.**  **Truth table** 1:8 Demux–1 is selected 1:8 Demux–2 is selected	**4M** ***2M Diagram*** ***2M Truth table***

S_3	S_2	S_1	S_0	Selected output
0	0	0	0	Y_0
0	0	0	1	Y_1
0	0	1	0	Y_2
0	0	1	1	Y_3
0	1	0	0	Y_4
0	1	0	1	Y_5
0	1	1	0	Y_6
0	1	1	1	Y_7
1	0	0	0	Y_8
1	0	0	1	Y_9
1	0	1	0	Y_{10}
1	0	1	1	Y_{11}
1	1	0	0	Y_{12}
1	1	0	1	Y_{13}
1	1	1	0	Y_{14}
1	1	1	1	Y_{15}

b) Ans.

ii) Explain working of full substractor with circuit diagram. **4M**

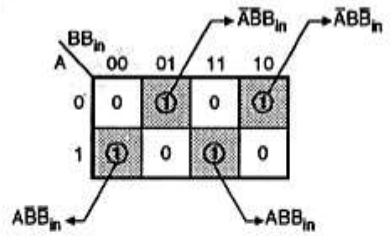
A full substractor is used for performing multibit substraction where the borrow from the previous bit position is available. This circuit has three inputs An (minuend), Bn (subtrahend) and Bn-1 (borrow from previous stage) and two outputs Difference (Dn) and Borrow (Cn).

Explanation 2M

An	Bn	Bn-1	Difference Dn	Carry Cn
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

For difference output

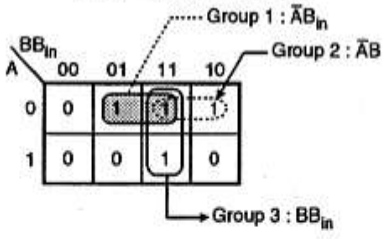
$\therefore D = \bar{A}\,\bar{B}\,B_{in} + \bar{A}B\bar{B}_{in} + A\bar{B}\bar{B}_{in} + ABB_{in}$



(a) K-map for D

For Borrow output

$\therefore B_o = \bar{A}B_{in} + \bar{A}B + BB_{in}$



(b) K-map for B_o

Fig.

Simplification for difference output :

$$D = \bar{A}\,\bar{B}\,B_{in} + \bar{A}B\bar{B}_{in} + A\bar{B}\bar{B}_{in} + ABB_{in}$$

$$= B_{in}\underbrace{(\bar{A}\,\bar{B} + AB)}_{\text{EX-NOR}} + \bar{B}_{in}\underbrace{(A\bar{B} + \bar{A}B)}_{\text{EX-OR}}$$

$$\therefore D = B_{in}\overline{(A \oplus B)} + \bar{B}_{in}(A \oplus B)$$

Let $A \oplus B = C$,

$$\therefore D = B_{in}\bar{C} + \bar{B}_{in}C = B_{in} \oplus C$$

$$\therefore D = B_{in} \oplus A \oplus B$$

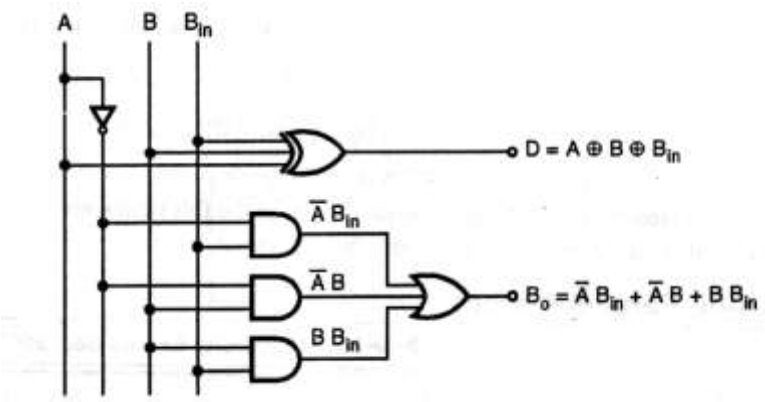


Diagram 2M

c) Ans.

i) Compare synchronous and asynchronous counter. **2M**

Sr No: .	Synchronous Counter	Asynchronous Counter
1.	All flip flops are triggered with same clock.	Different clock is applied to different flip flops.
2.	It is faster	It is slower.
3.	Deign is complex.	Design is relatively easy.
4.	Decoding errors are not present.	Decoding errors are present.
5.	Any required sequence can be designed.	only

Any 4 points 2M

c) Ans.

ii) Design a mod-10 synchronous counter. **6M**
(Note: **other relevant flip flop can be used)**
Number of desired states = 10
Number of flip flops required= 4 [$2^n = m$]
Use JK flip Flop

6M

Counter State				Flip flop inputs							
Q3	Q2	Q1	Q0	JO	KO	J1	K1	J2	K2	J3	K3
0	0	0	0	1	X	0	X	0	X	0	X
0	0	0	1	X	1	1	X	0	X	0	X
0	0	1	0	1	X	X	0	0	X	0	X
0	0	1	1	X	1	X	1	1	X	0	X
0	1	0	0	1	X	0	X	X	0	0	X
0	1	0	1	X	1	1	X	X	0	0	X
0	1	1	0	1	X	X	0	X	0	0	X
0	1	1	1	X	1	X	1	X	1	1	X
1	0	0	0	1	X	0	X	0	X	X	0
1	0	0	1	X	1	0	X	0	X	X	1
0	0	0	0								

Draw the k maps for the respective inputs in terms of ouputs

1. J0 =1

	Q3Q2	Q3 Q2	Q3 Q2	Q3 Q2
Q1Q0	1	1	X	1
Q1 Q0	X	X	X	X
Q1 Q0	X	X	X	X
Q1 Q0	1	1	X	X

2. K0 = 1

	Q3Q2	Q3 Q2	Q3 Q2	Q3 Q2
Q1Q0	X	X	X	X
Q1 Q0	1	1	X	1
Q1 Q0	1	1	X	X
Q1 Q0	X	X	X	X

3. J1= Q0 Q3

	Q3Q2	Q3 Q2	Q3 Q2	Q3 Q2
Q1Q0	0	0	X	0
Q1 Q0	1	1	X	0
Q1 Q0	X	X	X	X
Q1 Q0	X	X	X	X

4. K1= Q0

	Q3Q2	Q3 Q2	Q3 Q2	Q3 Q2
Q1Q0	X	X	X	X
Q1 Q0	X	X	X	X
Q1 Q0	1	1	X	X
Q1 Q0	0	0	X	X

5. J2=Q0Q1

	Q3Q2	Q3 Q2	Q3 Q2	Q3 Q2
Q1Q0	0	X	X	0
Q1 Q0	0	X	X	0
Q1 Q0	1	X	X	X
Q1 Q0	0	X	X	X

6. K2=Q0Q1

	Q3Q2	Q3 Q2	Q3 Q2	Q3 Q2
Q1Q0	X	0	X	X
Q1 Q0	X	0	X	X
Q1 Q0	X	1	X	X
Q1 Q0	X	0	X	X

7. J3=Q0Q1Q2

	Q3Q2	Q3 Q2	Q3 Q2	Q3 Q2
Q1Q0	0	0	X	X
Q1 Q0	0	0	X	X
Q1 Q0	0	1	X	X
Q1 Q0	0	0	X	X

8. K3=Q0

	Q3Q2	Q3 Q2	Q3 Q2	Q3 Q2
Q1Q0	X	X	X	0
Q1 Q0	X	X	X	1
Q1 Q0	X	X	X	X
Q1 Q0	X	X	X	X

MODEL ANSWER

SUMMER - 2017 EXAMINATION

Subject: Digital Techniques **Subject Code:** **17333**