MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION
(Autonomous)
(ISO/IEC - 27001 - 2005 Certified)

Summer 2016– EXAMINATIONS

Subject Code: **17321** **Model Answer**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. Attempt any ten of the following: 20

a) Write the four specifications of Zener diode.

Ans:- (any 4 specifications- 2 mks)-

1. Zener Voltage
2. Maximum Zener current
3. Power dissipation
4. Operating temperature
5. Dynamic Resistance

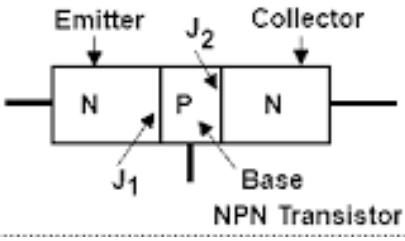
b) State the applications of LED.

Ans:- (Any 2 – 2 mks)

1) 7 segment Displays
2) Indicators
3) Dot matrix display
4) Decorations
5) Opto couplers in optical fibres

c) Draw construction of bipolar junction transistor give size and doping concentration of each region.

Ans:- (construction- 1 mks, size – ½ mks , doping ½ mks)



NPN Transistor

The doping concentration is high for emitter region , moderate for collector region and very low doping for base region.

Size- Collector is having largest size, then the emitter and the thinnest is the base region.

d) Define line regulation and load regulation.

Ans:- (1 mark for each definition)

Load Regulation - It is defined as the change in output voltage when the load current is changed from zero (no load) to maximum (full load) value.
Mathematically it is expressed as,

$$\% \text{ Load Regulation} = \frac{(V_{NL} - V_{FL}) \times 100}{V_{FL}}$$

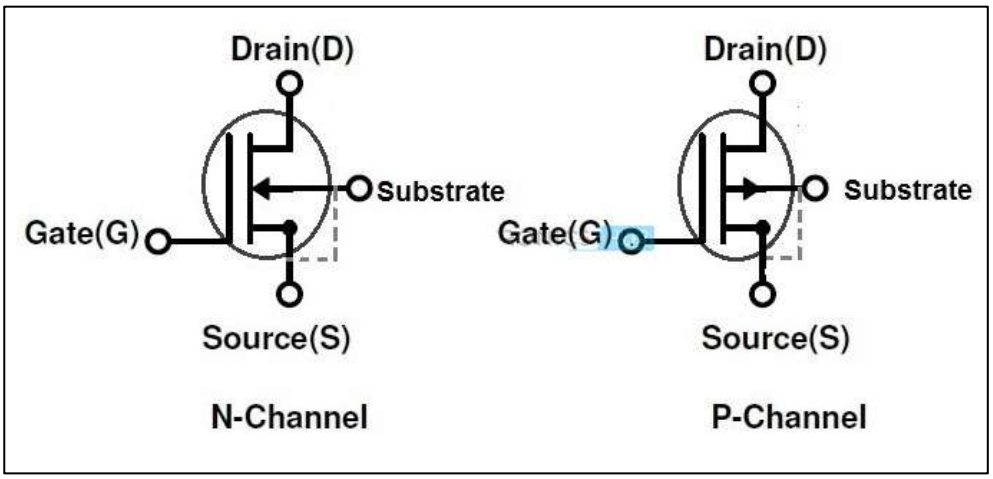
With Vin= Constant
Where VNL = No load voltage (IL = 0)
VFL = Full load voltage (IL = IL Max)

Line Regulation: It is defined as the change in output voltage due to change in input voltage with load RL constant (IL constant)
Therefore

$$\% \text{ Line Regulation} = \frac{(V_{LH} - V_{LL}) \times 100}{V_{normal}}$$

VLH = Load voltage with high line voltage
VLL = Load voltage with low line voltage
Vnormal= normal line voltage

e) Draw symbol of D-MOSFET (n-channel and p-channel).
Ans.: (1 mark each)



f) State the concept of cross-over distortion.
Ans: (Proper concept 2 marks)

When a transistor is operated in Class-B and signal is applied. The collector current does not flow until the base voltage (V_{BE}) overcomes. The knee voltage (i.e. 0.7 V for Si and 0.3 V for Ge). The result is that there is no output across the

load for the period during which the base signal is less than the knee voltage. This leads to cross-over distortion.

g) State typical values of knee voltage for silicon and germanium P-N junction.
Ans:- (1 mark each)

The value of Knee voltage is

Si diode-0.7 V and Ge Diode- 0.3 V

h) State the applications of FET (any four).
Ans:- (Any 4- 2 mks)

1) High frequency Switch
2) Oscillator
3) Amplifier
4) Isolator
5) Radio transmitter and receiver
6) TV transmitter and receiver
7) Voltage Variable Resistor(VVR)
8) Digital Circuits

i) List various transistor biasing methods.
Ans:- (any 4- 2 mks)

Types of biasing

i. Base bias (or fixed bias)
ii. Base bias with emitter feedback.
iii. Base bias with collector feedback
iv. Voltage divider bias (or self bias)
v. Emitter bias.

j) State the Bankhausen criteria of oscillations.
Ans:- (1 mark for each criteria)

An amplifier will work as an oscillator if and only if it satisfies a set of conditions called Barkhausen's criterion. It states that:

1) An oscillator will operate at that frequency for which the total phase shift around loop equals to 0° or 360°.

2) At the oscillator frequency, the magnitude of the product of open loop gain of the amplifier A and the feedback factor β is equal or greater than unity.

ie. $A\beta \geq 1$

k) Define gain and bandwidth of small signal amplifier.

Ans:- (1 mark for each)

Gain-Defined as the ratio of o/p voltage to the i/p voltage(or current), and given as- Av= Vo/Vi (OR A_I=Io/Ii)

Bandwidth-Defined as the range of frequencies over which the gain of the amplifier remains almost constant.

l) Define amplification factor (μ) of JFET.

Ans:- (Definition: 1 mark, Formula: 1 mark)

Amplification Factor

Amplification Factor is defined as the ratio of change in Drain to Source Voltage (ΔV_{DS}) to change in Gate to Source Voltage (ΔV_{GS}) at a constant I_D.

$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$, with I_D = constant

m) Convert the following numbers.

Ans:- (1 mark each)

i) $(5C7)_{16} = (\quad)_{10}$

$= 5 \times 16^2 + 12 \times 16^1 + 7 \times 16^0$

$= 1280 + 192 + 7$

$= (1479)_{10}$

ii) $(43)_8 = (\quad)_2$

$= (100\ 011)_2$

n) Draw a symbol and truth table of NOR gate.

Ans: (symbol = 1 mark, truth table = 1 mark)

NOR gate

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

2. Attempt any four of the following: 16

a) Draw a V-I characteristics of P-N junction diode in forward and reverse bias. Define static and dynamic resistance.

Ans:- (V-I characteristics = 2 marks, static resistance = 1 mark, dynamic resistance – 1 mark)

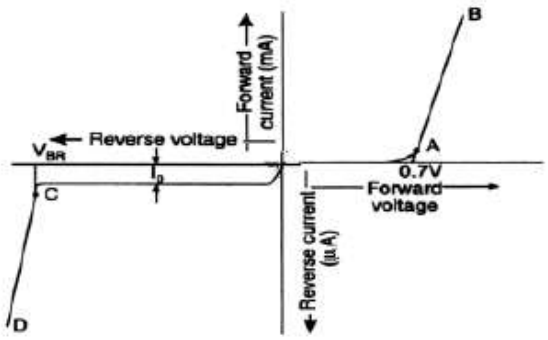


Fig: VI characteristics of PN Junction diode

(i) Static resistance:

The resistance of a diode at the operating point can be obtained by taking the ratio of V_F and I_F. The resistance offered by the diode to the forward DC operating conditions is called as **"DC or static resistance"**.

$$R_F = \frac{V_F}{I_F}$$

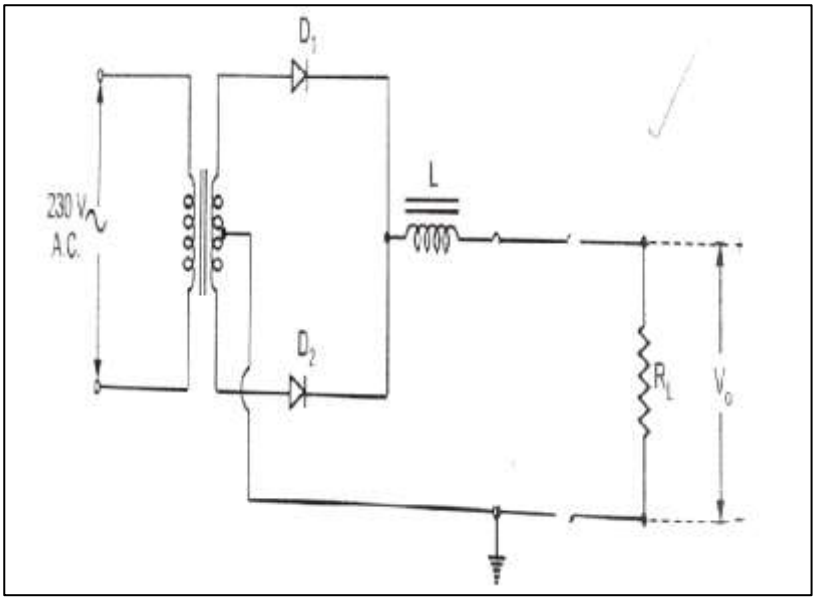
(ii) Dynamic resistance:

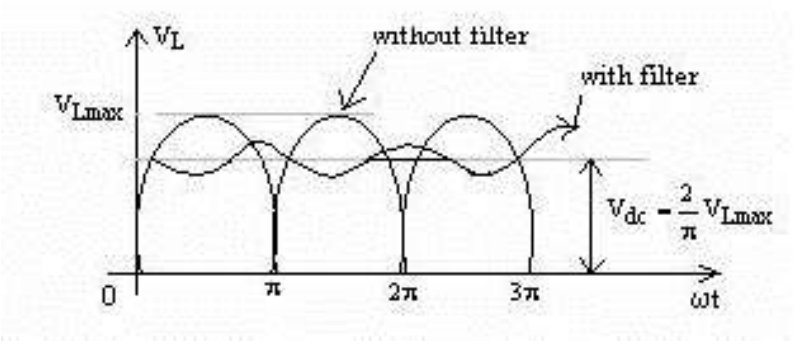
The resistance offered by a diode to the AC operating conditions is known as the **"Dynamic Resistance"**. It is the ratio of change in voltage to the resulting change in current.

$$r_{ac} = \frac{\Delta V_F}{\Delta I_F}$$

b) Draw a circuit diagram of centre tapped full wave rectifier with series inductor filter. Draw its input and output waveforms.

Ans;- (circuit diagram = 2 marks, waveforms – 2 marks)





c) Compare CB and CE configurations with respect to input resistance, output resistance, voltage gain and current gain.

Ans:- (each parameter 1 mark)

Parameter	CB	CE
Input Impedance	Low Or 50Ω	Medium Or 600Ω to 4kΩ
Current Gain	Less than or equal to 1 Or $\alpha = \frac{I_C}{I_E}$	High Or $\beta = \frac{I_C}{I_B}$
Voltage Gain	Medium	Medium
Output Impedance	High Or 50 kΩ	Medium Or 10 kΩ to 50 kΩ

d) Describe the voltage divider biasing technique of BJT with ckt. Diagram.
Ans: (Diagram = 2 marks, description = 2 marks)

Voltage Divider Bias:

R_1, R_2 and R_E are biasing resistors and V_{CC} is biasing voltage.

Voltage at base of transistor is

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

Applying KVL at input circuit,

$$V_B - V_{BE} - V_E = 0$$

Since V_{BE} is very small

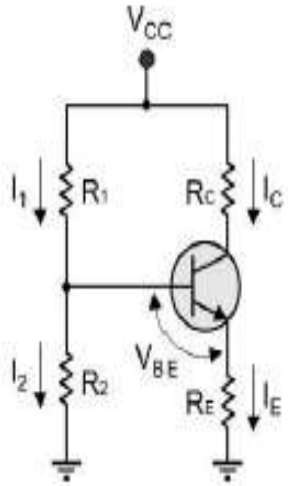
$$V_B = V_E$$

Now, $I_E = \frac{V_E}{R_E}$

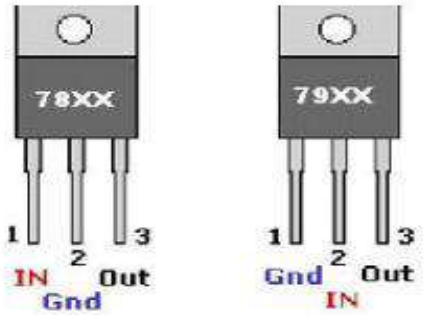
$$\therefore I_C = \frac{V_E}{R_E} \quad [since\ I_C \cong I_E]$$

Applying KVL to output circuit,

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$
$$V_{CE} = V_{CC} - I_E(R_C + R_E) \quad [since\ I_C \cong I_E]$$



e) Describe the functional pin diagram of regulator IC 78XX and 79XX.
Ans:- (Functional pin diagrams – 1 mks each, description – 1 mks each)



78XX – A three pin positive voltage regulator with

1. Input pin
2. Ground pin

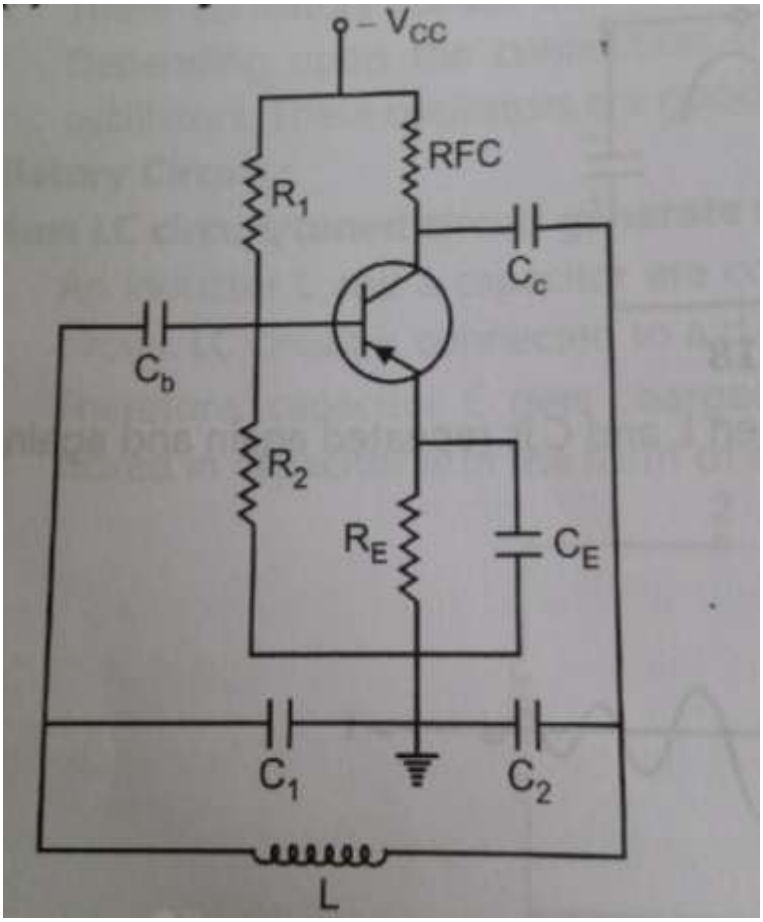
3. Output pin

79XX – A three pin negative voltage regulator with

1. Ground pin
2. Input pin
3. Output pin

f) Draw the circuit diagram of colpits oscillator. Explain its working principle. Write equation for output frequency.

Ans:- (diagram = 2 maqrks, working principle = 1 mark, equation = 1 mark)



There are two parts in circuit diagram: i) Single stage common emitter amplifier and ii) tank circuit.

The amplifier produces a phase shift of 180° and tank circuit also produces a phase shift of 180°. The total phase shift is 360° and hence the feedback is positive.

Ignoring the loading effects the feedback fraction is given by,

$\beta = \frac{C_1}{C_2}$

The voltage gain must be greater than 1/ β for oscillations to start i.e.

$\frac{1}{\beta} = \frac{C_2}{C_1}$

The frequency of oscillations is given by,

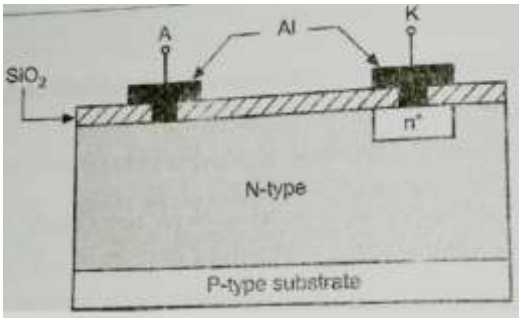
$$F = \frac{1}{2\pi\sqrt{L\,C_T}}$$

Where, $C_T = \frac{C_1\,C_2}{C_1 + C_2}$

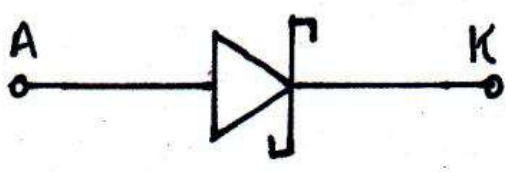
3. Attempt any four of the following: 16

a) Draw constructional details of Schottky diode draw its symbol and explain its working.

Ans:- (Contruction- 1 ½ mks, symbol- 1 mks, working 1 ½ mks)



Symbol-



Working - The metal region of a Schottky diode is heavily occupied with the conduction band electrons and the N-type region is lightly doped. There are no minority carriers as in other types of diodes, but there are only majority carriers as electrons. It operates only with majority carriers. When it is forward biased, higher energy electrons in the N regions are injected into the metal region where that gives up their excess energy very rapidly. Since there are no minority carriers as in

conventional diodes, there is no charge storage and hence there is no reverse recovery diode when it is switched from the forward-biased condition (i.e. ON state) to the reverse biased condition (i.e. OFF state). It has negligible storage time and hence there is a very rapid response to a change in bias. Because of this property, it acts as a very fast switching diode.

b) Describe thermal runaway of transistor and explain how it can be avoided.

Ans:- (thermal runaway- 2 mks, how it can be avoided (2 methods)- 2 mks)

Thermal Runaway-The reverse saturation current in semiconductor devices changes with temperature. The reverse saturation current approximately doubles for every 100 c rise in temperature. . As the leakage current of transistor increases, collector current (Ic) increases . The increase in power dissipation at collector base junction. . This in turn increases the collector base junction causing the collector current to further increase. . This process becomes cumulative. & it is possible that the ratings of the transistor are exceeded. If it happens, the device gets burnt out. This process is known as 'Thermal Runaway'.

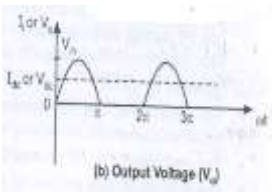
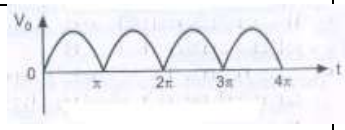
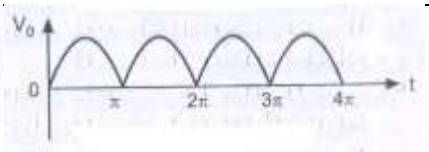
Thermal runaway can be avoided by

1) Using stabilization circuitry
2) Heat sink

c) Compare half wave, centre tap and bridge type full wave rectifier on the basis of

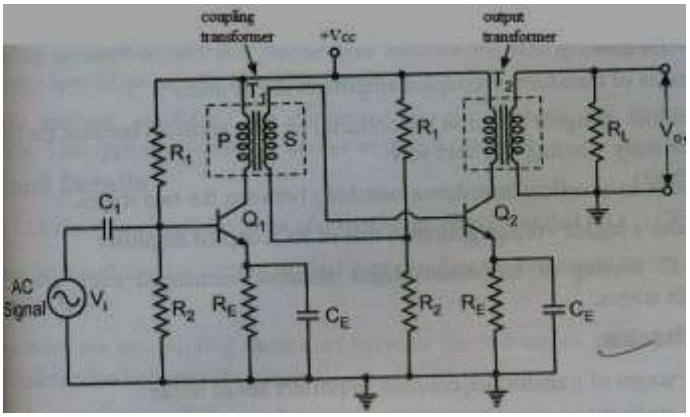
i) Ripple factor ii) Rectification efficiency
iii) TUF iv) Waveforms

Ans:- (each parameter 1 mark)

Parameters	HWR	FWCTR	FWBR
Ripple factor	1.21	0.482	0.482
Rectification efficiency	40.6%	81.2%	81.2%
TUF	0.282	0.693	0.812
Waveforms			

d) Draw the circuit diagram of two stage transformer coupled amplifier and describe the function of each component.

Ans:- (diagram = 2 marks, function = 2 marks)



Functions- The function of a coupling transformer T_1 is to couple the output AC signal from the output of the first stage to the input of the second stage, while transformer T_2 couples the output of AC signal to the load R_L.

The input capacitor C_1 is used to couple the input signal to the base of transistor Q_1.

The capacitor C_E connected at the emitters of transistor Q_1 and Q_2 are used to bypass the emitter to ground.

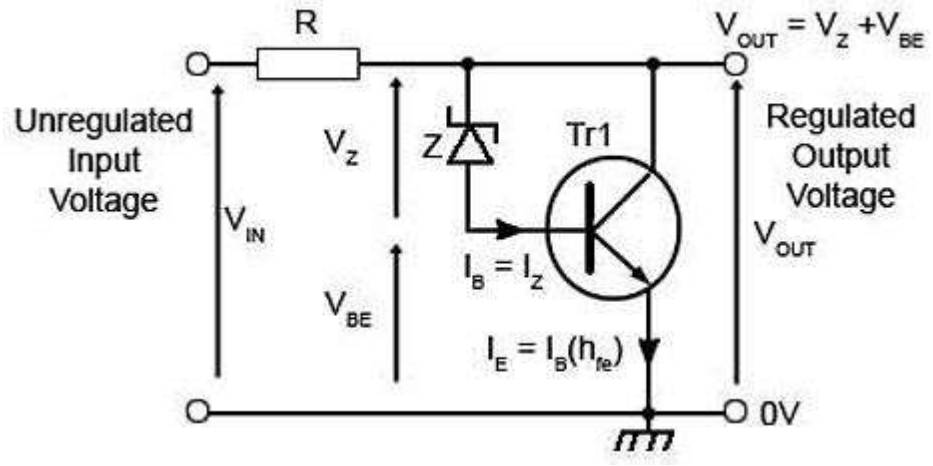
The resistors R_1, R_2, R_E and a capacitor C_E form the DC biasing and stabilization.

Note that, in this circuit, there is no coupling capacitor. The DC isolation between the two stages is provided by the transformer itself.

There exists no DC path between primary and secondary windings of a transformer.

e) Draw the circuit diagram of transistorized shunt regulator circuit and describe its operation.

Ans:-(Circuit diagram- 2 mks, working- 2 mks)



Working: - From the above circuit the load voltage is given by
VL= VZ + VBE Or VBE =VL – VZ

Since the load voltage for a given zener diode is fixed, therefore any decrease or increase in load voltage will have a corresponding effect on the base to emitter voltage VBE. The unregulated input voltage increases, load voltage also increases. As a result of this from equation (i) above, we find that VBE is also increases. And the base current IB increases. Due to this the collector current IC also increases. This causes the input current (IS) to increase, which in turn increases the voltage drop across series resistance (VRS) . Consequently, the load voltage decreases. If the output voltage decreases then VBE will decrease. This will reduce the collector current Ic. So more current will flow through the load and the load voltage will increase. This increase in load voltage will compensate the initial decrease in load voltage. Thus output voltage gets regulated.

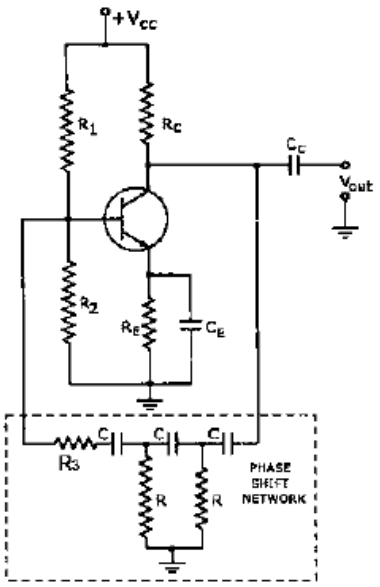
f) Draw and describe working principle of RC phase shift oscillator. Write the equation for output frequency.

Ans: (diagram = 2 marks, working= 1 mark, equation = 1 mark)

RC Phase shift Oscillator:

1) Circuit Diagram:
2) Working:
   - In RC phase shift oscillator, CE amplifier is used, which provides 180° phase shift between input and output.
   - In feedback network, three RC phase shift networks are used in which each network provides 60° phase shift, so that total phase shift is 180°.
   - The total phase shift around whole circuit is 360°.
   - So circuit gets positive feedback and works as an oscillator.
3) Frequency of Oscillations:

$$f_c = \frac{1}{2\pi RC\sqrt{6}}$$

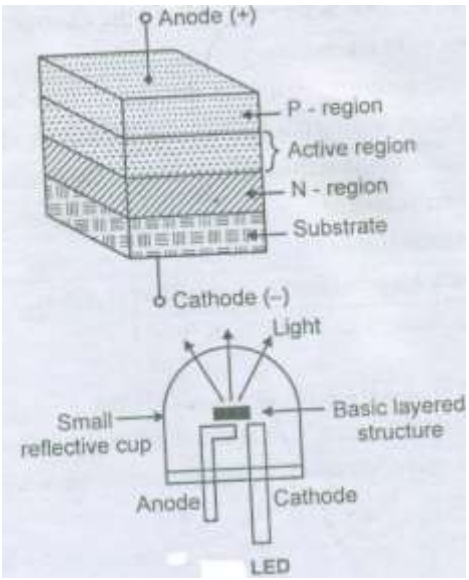


RC Phase Shift Oscillator

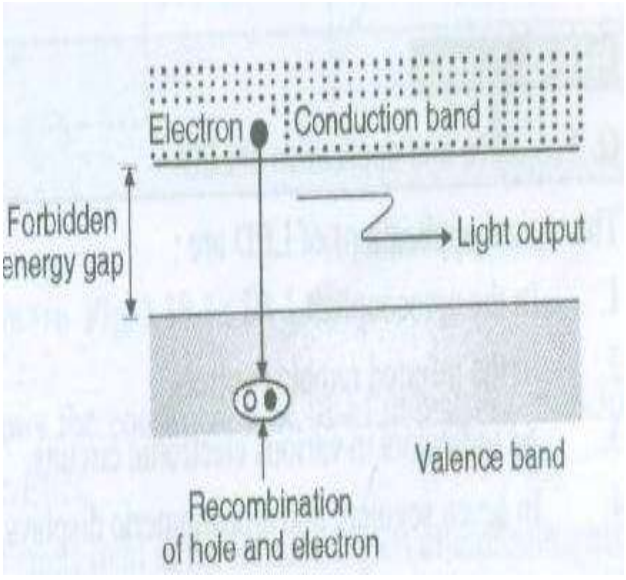
4. Attempt any four of the following: 16

a) Draw a construction of LED and explain its working.

Ans:-(Construction- 2 mks, working- 2 mks)



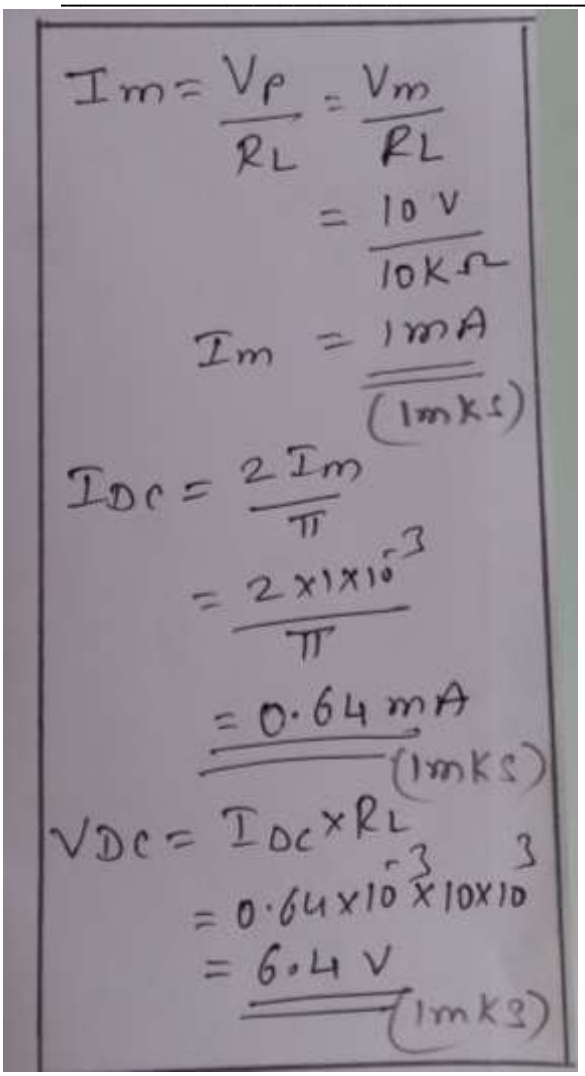
OR

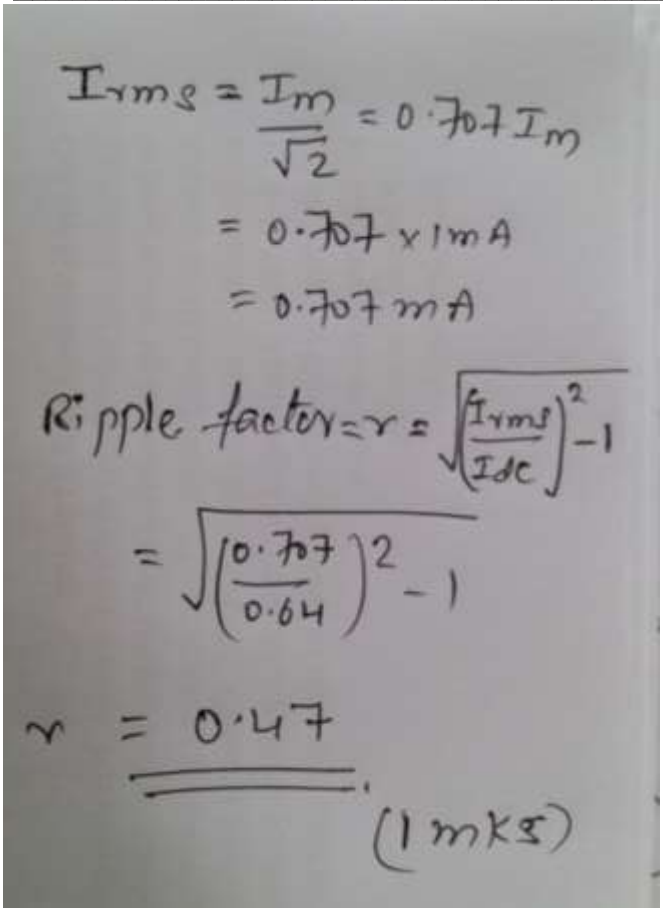


Working - When the junction is forward – biased the electron in the n-region combines with the holes.
These free electrons reside in the conduction band and at the higher energy level from the holes in the valence band. When the recombination takes place, these electrons return back to the valence band which is at a lower energy level than the conduction band. While returning back, the recombining electrons give away the excess energy in the form of light.

b) In full wave rectifier V_P = 10 V, R_L = 10 KΩ find VDC, IDC and ripple factor.

Ans:-


$I_m = \frac{V_p}{R_L} = \frac{V_m}{R_L}$
$= \frac{10\ V}{10K\Omega}$
$I_m = 1mA$ (1mks)
$I_{DC} = \frac{2I_m}{\pi}$
$= \frac{2 \times 1 \times 10^{-3}}{\pi}$
$= 0.64\ mA$ (1mks)
$V_{DC} = I_{DC} \times R_L$
$= 0.64 \times 10^{-3} \times 10 \times 10^{3}$
$= 6.4\ V$ (1mks)



$$I_{rms} = \frac{I_m}{\sqrt{2}} = 0.707 I_m$$

$$= 0.707 \times 1mA$$

$$= 0.707 mA$$

$$\text{Ripple factor} = r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{0.707}{0.64}\right)^2 - 1}$$

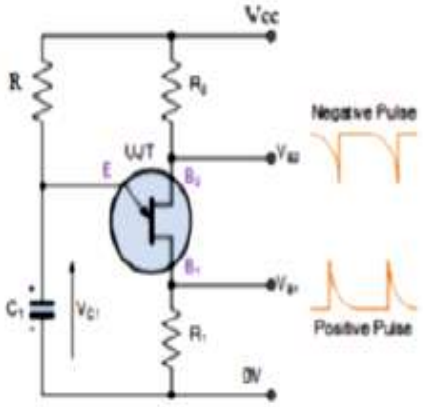
$$r = 0.47$$

(1 mks)

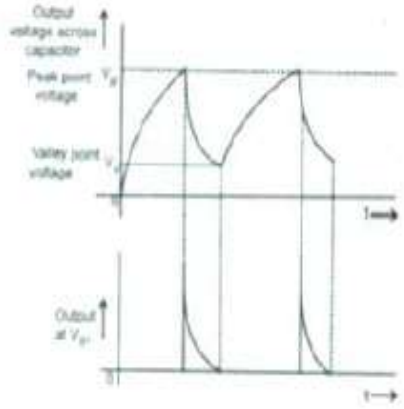
c) Draw the circuit diagram of UJT relaxation oscillator. Sketch the output waveform and explain the operation of oscillator.

Ans:-

Circuit diagram:- 01M



Waveform: 01M



Working principle: - 02M

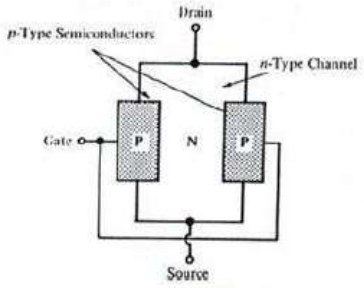
- When the supply voltage (V_{CC}) is switched ON, the capacitor charges through resistor (R), till the capacitor voltage reaches the voltage level (V_P) which is called as peak point voltage. At this voltage the UJT turns ON.
- As a result of this, the capacitor (C) discharges rapidly through resistor (R_1). When that capacitor voltage drops to level Vv (called valley- point voltage) the uni-junction transistor switches OFF allowing the capacitor (C) to charge again.
- In this way because of the charging and discharging of capacitor the exponential sweep voltage will be obtained at the emitter terminal of UJT. The voltage developed at base 1(V_{B1}) terminal is in the form of narrow pulses commonly known as trigger pulses.
- The sweep period depends upon time constant (R.C) and the sweep frequency can be varied by changing value of either resistance (R) or capacitor (C). Due to this fact, the resistor R is shown as a variable resistor.
- The sweep period is given by the relation

$$T = R.C.\ \log_e (1/1-n)$$

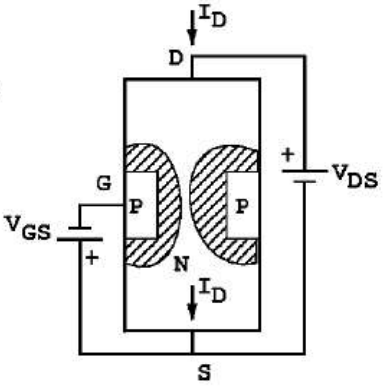
d) Draw and explain constructional details of n-channel JFET.

Ans:- (diagram = 2 marks, explanation = 2 marks)

N-channel JFET (FET):



n-channel JFET

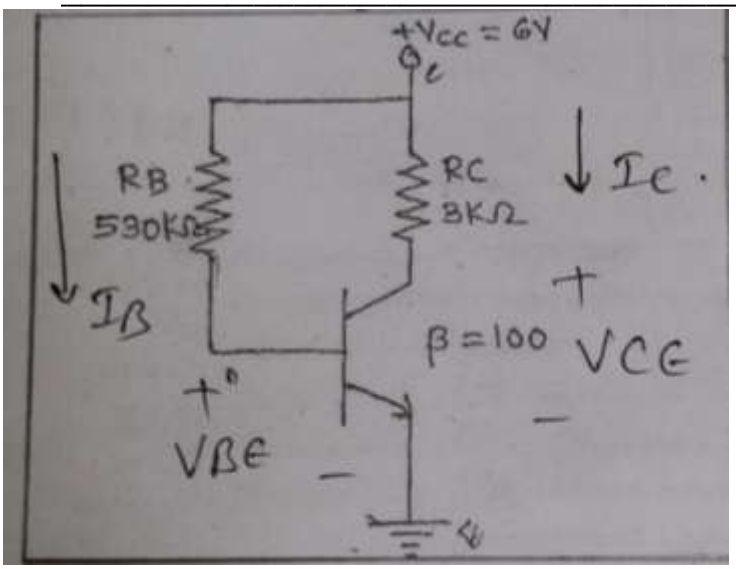


Construction:

The n-channel JFET has n-type semiconductor used as a channel which has two terminals, drain and source. Two p-type semiconductors are attached at both sides of n-channel and forms third terminal gate. Thus pn junction exists between gate and source.

1) When V_{GS} = 0 volt:
   When a voltage is applied between the drain and source with a DC supply voltage V_{DD} with V_{GS} = 0 V, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes drain current I_D. The value of drain current is maximum when V_{GS} = 0 V. This current is designated vy the symbol I_{DSS}.
2) When V_{GS} is negative:
   When V_{GS} is increased below zero i.e negative, the reverse voltage across the gate source junction is incrased. As a result depletion regions are widened. This reduces effective width of channe and therefore controls the flow of drain current through the channel.
   If V_{GS} is increased further, two depletion regions touch each other. The drain current reduces to zero. The gate to source voltage at which current reduces to zero is called as pinch-off voltage.

e) Draw a dc load line for the following circuit and determine operating point.
Ans:-


+Vcc = 6V
RB
530KΩ
RC
3KΩ
Ic
IB
β=100
VCE
VBE

Q4 e) from fig -

Apply KVL to input loop -

$V_{CC} = I_B R_B + V_{BE}$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$= \frac{6 - 0.7}{530 \times 10^3}$

$\boxed{I_B = 10\,\mu A}$ (1 mks)

$\therefore I_C = \beta I_B = 100 \times 10\,\mu A$

$\boxed{I_C = 1\,mA}$

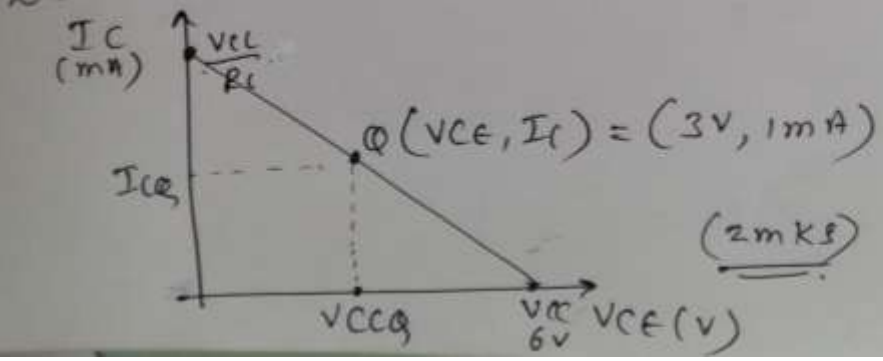
Apply KVL to o/p loop

$V_{CC} = I_C R_C + V_{CE}$

$6 = 1 \times 10^{-3} \times 3 \times 10^3 + V_{CE}$

$\boxed{V_{CE} = 6 - 3 = 3V}$ (1 mks)

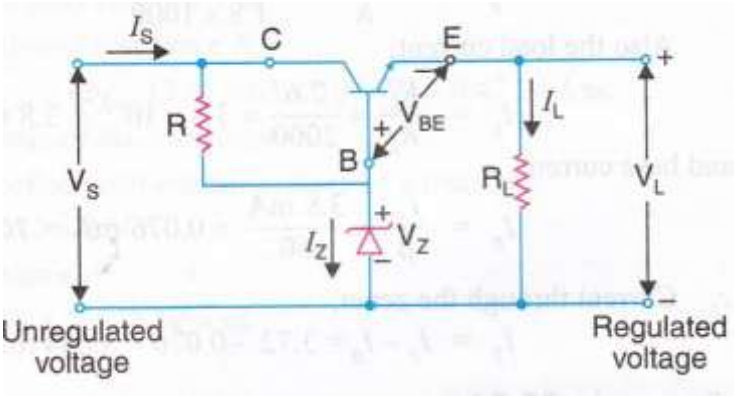
DC load line



(2 mks)

f) Describe how Zener diode is used as a voltage regulator.

Ans:- (Circuit – 2 mks, explanation- 2 mks)



Operation:-The unregulated DC supply is fed to the input terminal as shown in above fig. The output voltage is given by

VL=VZ-VBE

VZ being a zener voltage is assumed to be a constant therefore if the output voltage varies, and then there will be a change in VBE. If the output voltage increases due to some reason then VBE decreases and due to this base current decreases. Therefore collector current decreases. This will increase the collector to emitter voltage (VCE) across the transistor and VL will be regulated. If the output voltage decreases then exactly opposite action will takes place and the output voltage is regulated. The circuit's action may be summarized in the form of the following equation.

VL↓ → VBE↓ → IB↓ → IC↓ → VCE↑ → VL↓

5. Attempt any four of the following: 16

a) Define feedback. Give the advantages of negative feedback.

Ans:-(Definition- 2 mks, any 4 advantages- 2 mks)

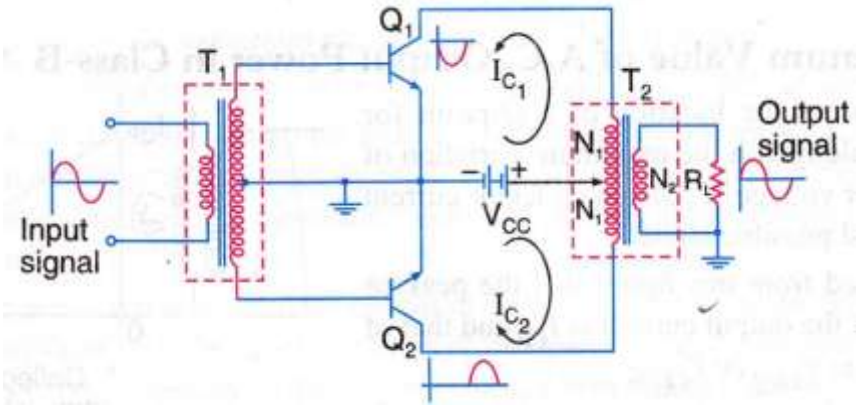
Definition- Feedback is a process in which a apart of o/p is fed to the input to get the desired o/p.

Advantages of Negative Feedback:

i) Stability becomes better as feedback increases.
ii) Noise decreases with feedback.
iii) Bandwidth increases.
iv) Input impedance increases.

b) Draw a circuit diagram of class B push pull power amplifier. Sketch input and output waveform. Describe its operation.

Ans:- (Diagram- 2 mks, waveforms – 1 mks, operation- 1mks)



Circuit diagram along with input output waveforms

Operation :- **01M**

- In class B amplifier transistor conduct only for half cycle of input signal.one conduct in positive half cycle and other conducts in negative half cycle.
- Transformer T_1 is called as input transformer called phase splitter and produces two signals which are 180 degree out of phase with each other.
- Transformer T_2 is called as output transformer and is required to couple the a.c signal from the collector to the load.
- When there is no input signal both the transistor Q_1 and Q_2 are cut off hence no current is drawn from V_{cc} supply. Thus there is no power wasted in stand by the power dissipation in both transistor is practically zero.
- During positive half cycle Q_1 ON Q_2 OFF and at the output half cycle is obtained during negative half cycle Q_1 OFF and Q_2 on hence another half cycle is obtained at the output.
- Then output transformer joins these two halves and produces a full sine wave in the load resistor.

c) For a Hartley oscillator if C = 100pF, L_1 = 30µH, L_2 = 1 x 10^{-8}H. Find the frequency of oscillation. Draw a circuit diagram of Hartley oscillator.

Ans:- (solving correct problem – 2 mks, diagram- 2 mks)

Given data- C= 100pF

L_1 = 30µH

L_2 = 1 x 10^{-8} H

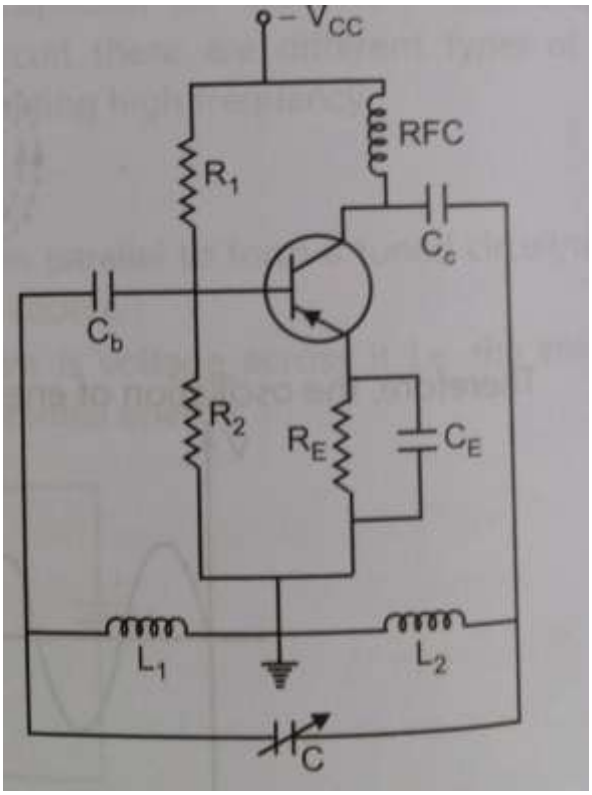
Frequency of oscillation is given as

$$Fo= \frac{1}{2\pi\sqrt{L_T . C}}$$

$L_T = L_1 + L_2$ =130 µH

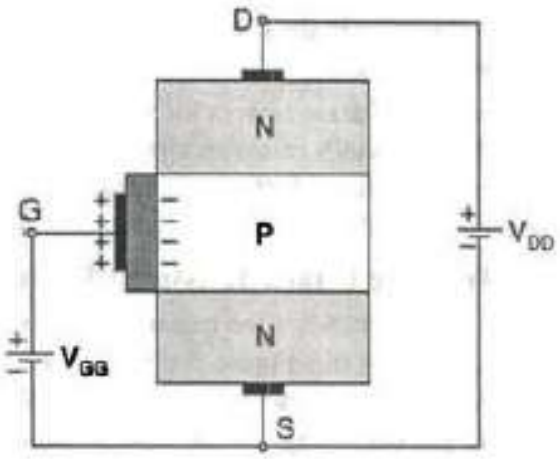
$$Fo = \frac{1}{2\pi\sqrt{100 * 10^{-12} * 130 * 10^{-6}}}$$

Fo= 1.4 MHz



d) Describe the working principle of enhancement type of n-channel MOSFET with diagrams.

Ans:- (Construction- 2 msk, Working 2 mks)



Working:

When V_{GS} is set at 0V and a voltage is applied between the drain and source, no current flows due to the absence of an N-channel. By keeping V_{DS} at some positive voltage and when V_{GS} is increased, the positive potential at the gate will push the holes (since like charges repel) in the P-substrate along the edge of the SiO_2 layer. The result is a depletion region near the SiO_2 insulating layer void of holes.

However, the electrons in the P-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. This is called Inversion layer.

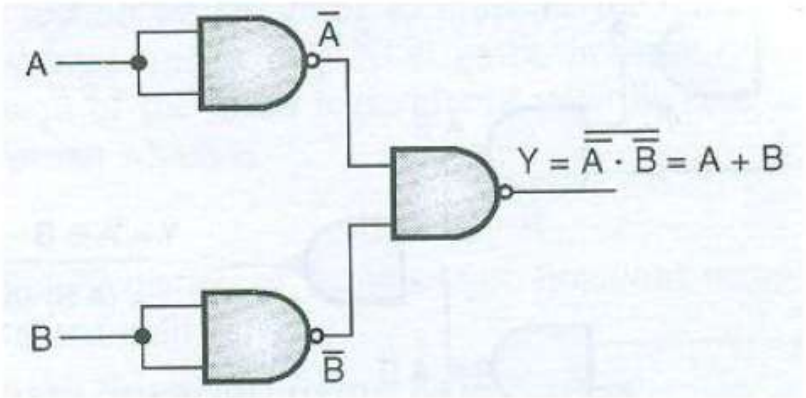
As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases, until eventually, the induced N-type region can support a measurable flow between drain and source.

e) Using NAND gate only draw following:

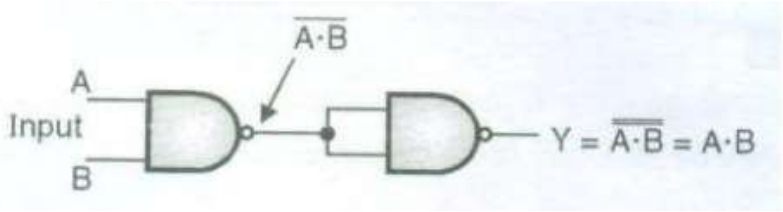
i) OR gate ii) AND gate

Ans:- (each 2 marks)

OR gate using NAND



AND gate using NAND



f) Describe the working of transistor as a switch with circuit diagram.

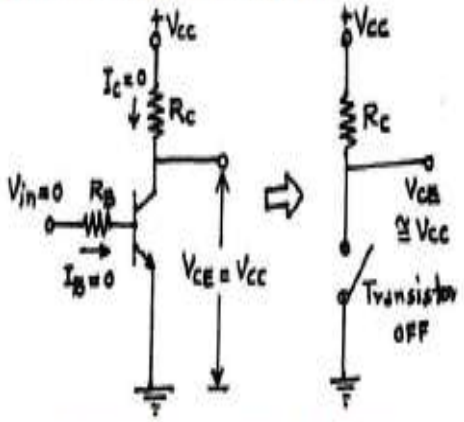
Ans:- (ON condition: diagram = 1 marks, explanation = 1 mark

OFF condition: diagram = 1 marks, explanation = 1 mark)

Transistor as Switch:

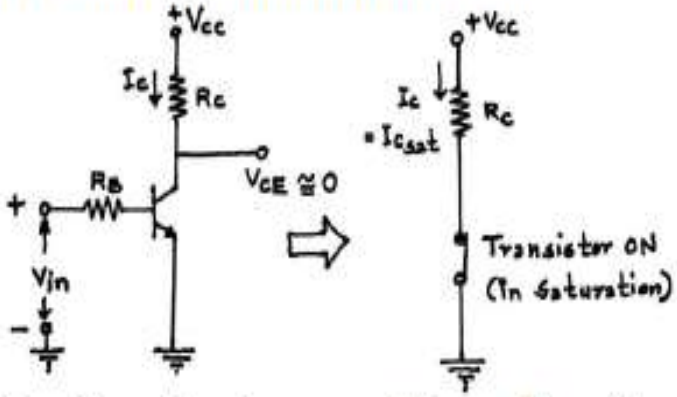
A transistor can be used for two types of applications viz. amplification and switching. For amplification, the transistor is biased in its active region.
For switching applications, transistor is biased to operate in the saturation (full on) or cut-off (full off) region.

(i) Transistor in cut-off region (Open switch):



In the cur-off region, both the junctions of transistor are reverse biased and very small reverse current flows through the transistor.
The voltage drop across the transistor (V_{CE}) is high, nearly equal to supply voltage V_{CC}. Thus, in cut-off region the transistor is equivalent to an open switch as shown in fig.(a).

(ii) Transistor in Saturation region (Closed switch):



When V_{in} is positive, a large base current flows and transistor saturates. In the saturation region, both the junctions of transistor are forward biased. The collector current is very large, the voltage drop across the transistor (V_{CE}) is very small, of the order of 0.2V to 1 V, depending on the type of transistor. Thus in saturation region, the transistor is equivalent to a closed switch.

6. Attempt any four of the following: 16

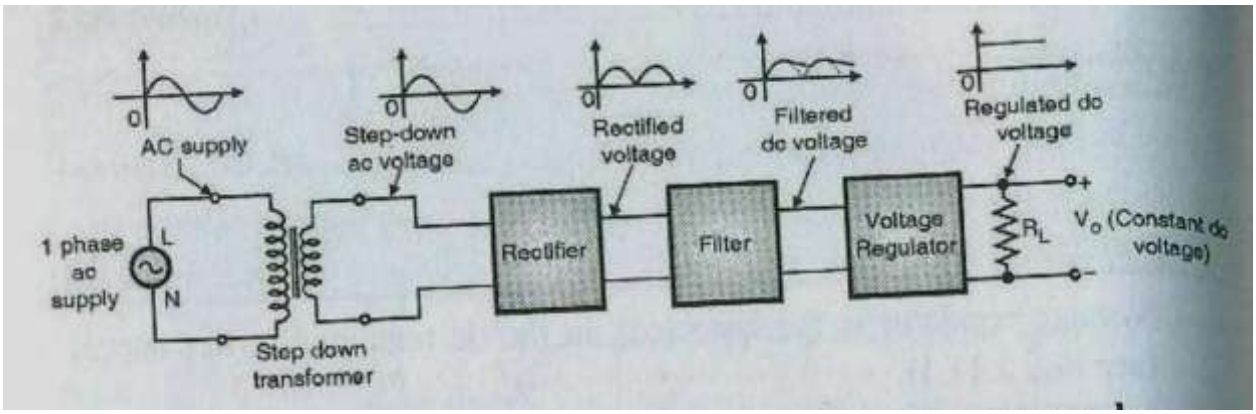
a) Draw a block diagram of regulated DC power supply and state the working of each block.

Ans:- (Block diagram- 2 mks, function of each block 2 mks)

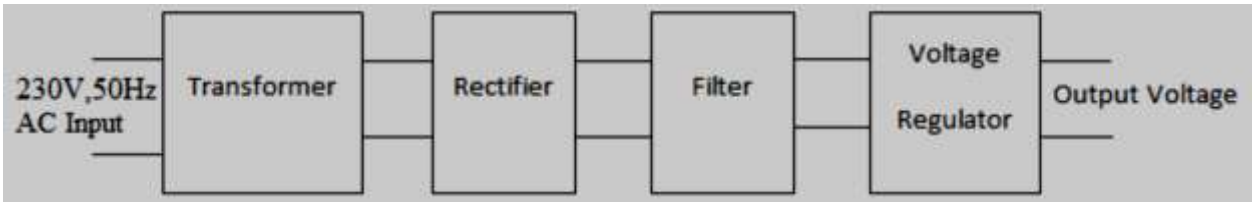
DC Power Supply:

There are four basic blocks of a DC regulated power supply. They are:

1) Step-down transformer
2) Rectifier
3) Filter
4) Voltage Regulator



OR



Functions of Each Block:

i) Step-down transformer: Reduces 230V, 50 hz ac voltage to required ac voltage level.

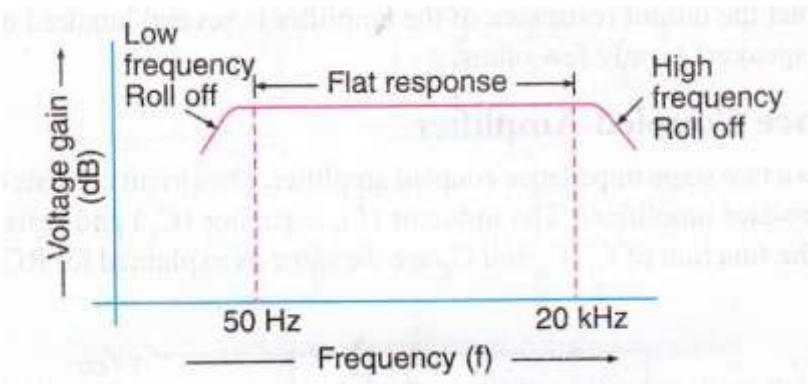
ii) Rectifier: Converts ac voltage into dc voltage. Typically bridge type full-wave rectifier is widely used.

iii) Filter: Used to remove fluctuations (ripples) present in dc output.

iv) Voltage regulator: Provides constant dc output voltage irrespective of changes in load current or changes in input voltage.
Voltage divider circuit is used to provide different dc voltages required for different electronic circuits.

b) Draw a frequency response of single stage amplifier and explain the effect of coupling capacitor and junction capacitor.

Ans:- (frequency response = 2 marks, Effect of Coupling capacitor = 1 mark, junction capacitor = 1 mark)

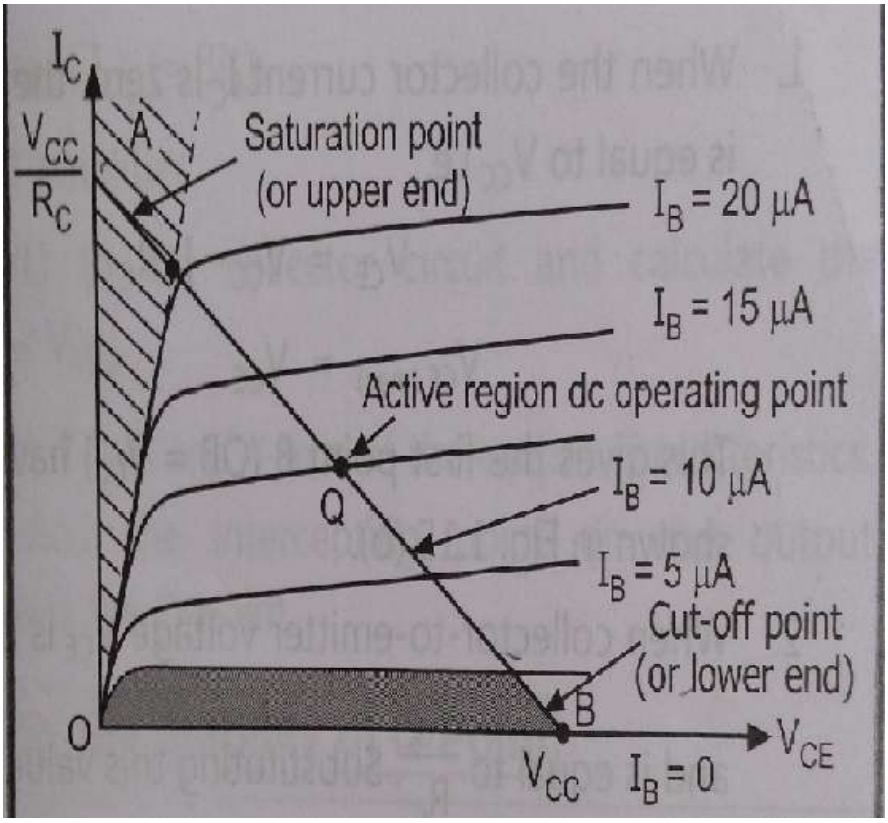


Effect of Coupling capacitor-The effect of coupling capacitor in this frequency range is such that it maintains a constant voltage gain. Thus as the frequency increases the reactance of capacitor decreases, which tends to increase the gain. However at the same time the lower capacitive reactance increases the loading effect of the next stage due to which the gain reduces. These two factors almost cancel each other. Thus a constant gain is maintained throughout this frequency range.

Effect of junction capacitor- In high frequency region, the voltage gain (or output voltage) decreases with the increase in frequency of an input AC signal due to the BJT internal junction and stray capacitance.

c) Draw output characteristics in CE mode. Indicate DC load line with Q-point, saturation region and cut-off region.

Ans:- (O/P characteristics with DC load line, Qpoint, saturation and cut off region- 4 mks)



d) Derive the relation between α and β wrt BJT.

Ans: - (Proper step wise relation derivation – 4 mks)

Relation between α and β:

Current gain of transistor in CB configuration is ,

$$\alpha = \frac{I_C}{I_E}$$

But $I_E = I_B + I_C$

$$\alpha = \frac{I_C}{I_B + I_C}$$

Dividing numerator and denominator by I_B,

$$\alpha = \frac{\frac{I_C}{I_B}}{1 + \frac{I_C}{I_B}}$$

But $\beta = \frac{I_C}{I_B}$ the current gain of transistor in CE configuration.

Therefore,

$$\boldsymbol{\alpha = \frac{\beta}{1 + \beta}}$$

OR

Current gain of transistor in CE configuration is ,

$$\beta = \frac{I_C}{I_B}$$

But $I_E = I_B + I_C$, so $I_B = I_E - I_C$

$$\beta = \frac{I_C}{I_E - I_C}$$

Dividing numerator and denominator by I_E,

$$\beta = \frac{\frac{I_C}{I_E}}{1 - \frac{I_C}{I_E}}$$

But $\alpha = \frac{I_C}{I_E}$ the current gain of transistor in CE configuration.

Therefore,

$$\boldsymbol{\beta = \frac{\alpha}{1 - \alpha}}$$

e) Compare BJT and FET for four points.

Ans:- (Any 4 points- 4 mks)

Sr. no.	BJT	JFET
1.	It is bipolar device i.e. current in the device is carried by electrons and holes.	It is unipolar device i.e. current in the device is carried by either electrons or holes.
2.	It is current controlled device i.e. base current controls the collector current.	It is voltage controlled device i.e. voltage at the gate terminal controls the amount of current flowing through the device.
3.	Input resistance is low, of the order of several KΩ	Input resistance is very high, of the order of several MΩ
4.	It has positive temperature coefficient of resistance at high current levels i.e. current increases as the temperature increases.	It has negative temperature coefficient of resistance at high current levels i.e. current decreases as the temperature increases.
5.	It suffers from minority carrier storage effects and therefore has lower switching speeds and cut-off frequency.	It does not suffer from minority carrier storage effects and therefore has higher switching speeds and cut-off frequency.
6.	It is more noisy as compared to FET.	It is less noisy.
7.	It is complicated to fabricate as an IC and occupies more space on the IC chip.	It is much simpler to fabricate as an IC and occupies less space on the IC chip.
8.	Thermal break down can occur.	Thermal break down cannot occur.

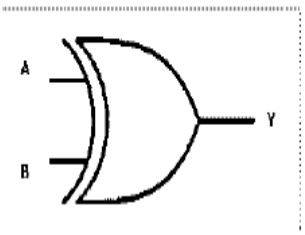
f) Describe EX-OR gate. Draw its symbol and truth table.
Ans☹ Definition- 2 mks, symbol – 1 mks, truth table- 1 mks)

An Ex-OR gate is a gate whose o/p is high(logic 1) for unequal inputs/dissimilar inputs

OR

An EX OR gate is a gate whose o/p is high(logic 1) for odd no. of high inputs
.

EX-OR GATE:-



$A \cdot \overline{B} + \overline{A} \cdot B$

Truth Table-

INPUT A	INPUT B	OUTPUT Y
0	0	0
0	1	1
1	0	1
1	1	0