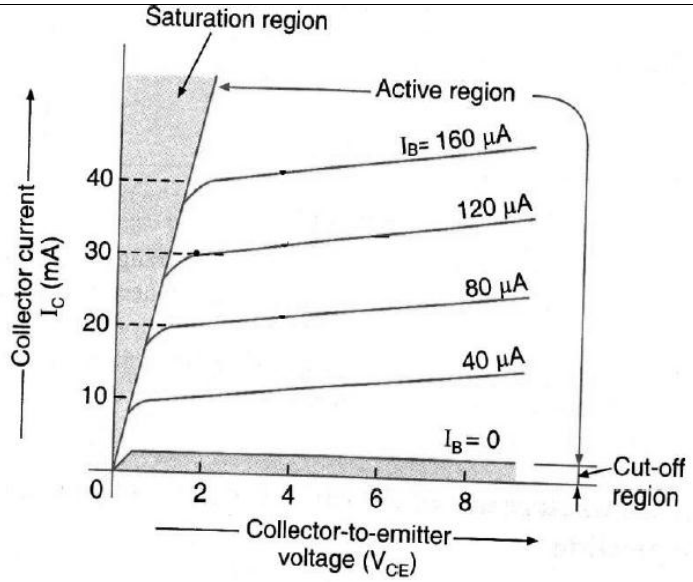
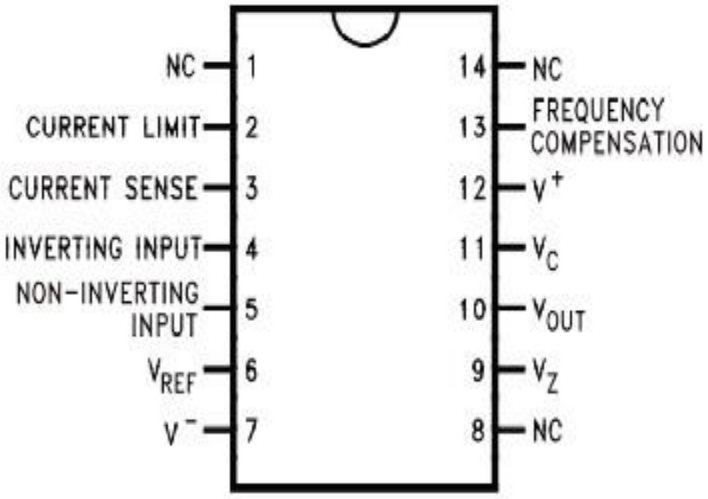
WINTER– 16 EXAMINATION (Subject Code: 17321)

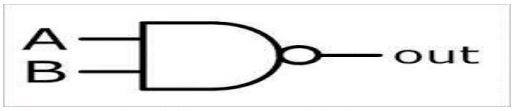
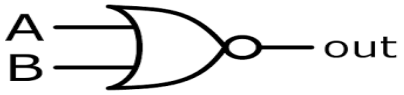
Model Answer

Important Instructions to examiners:

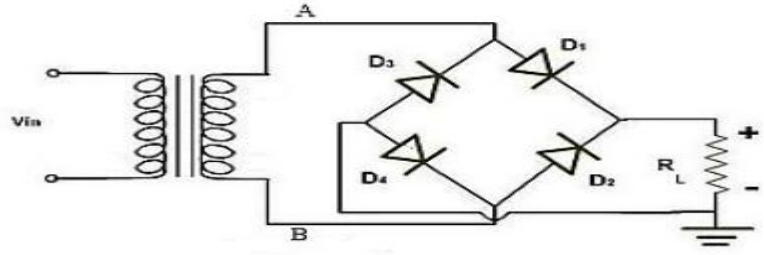
1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in thefigure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constantvalues may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
Q.1		**Attempt any SIX of following**	**12-Total Marks**
1	**A)**	**Draw symbol of P-N diode, Zener diode.**	**2 M**
	Ans:	**P-N diode**  **Zener diode**  	**1M** **1M**
	(b)	**Define the term rectification efficiency and rectifier.**	**2 M**
	Ans:	**Rectification efficiency** (η)-It is defined as the ratio of DC output power to the input power from the AC supply $\eta = \frac{DC\ Output\ Power}{AC\ input\ Power}$ **Rectifier-** It is an electronic circuit which is used to convert AC into pulsating DC. Rectifier is the initial state of regulated power supply.	**1M** **1M**
	(c)	**List the types of Biasing in BJT.**	**2 M**
	Ans:	Types of Biasing Circuits: i) Base bias (Fixed bias)	

	ii) Base bias with emitter feedback (Emitter feedback bias) iii) Base bias with collector feedback (Collector feedback bias) iv) Voltage divider bias (Self bias) v) Emitter bias	(any 4)
(d)	**Draw output characteristics showing different region in CE configuration.**	**2 M**
Ans:		**2 M**
(e)	**Define the term voltage regulation factor, state need of voltage regulation.**	**2 M**
Ans:	**Voltage Regulation factor**- It is the ability of power supply source to maintain a constant output voltage in spite of AC input fluctuations & change in load resistance. Voltage regulation=$\frac{VNL-VFL}{VFL}$*100 **Need of voltage regulation**-To protect electronic devices from variation in input voltage, load current & temperature.	**1M** **1M**
(f)	**Draw pin configuration of IC 723.**	**2 M**
Ans:		**2 M**
(g)	**Draw symbol of NAND Gate and NOR Gate.**	**2 M**

Ans:	**NAND Gate**  **NOR Gate**  	**1M** **1M**
(h)	**Convert : i) $(456)_D$ = ( )$_B$ ii) $(5A)_H$ = ( )$_D$**	**2 M**
Ans:	i)(456)D=(111001000)B ii)(5A)H = ( )D = 5 x 161 + 10 x160 = 80 + 10 = (90)D	**1M** **1M**
B)	**Attempt any TWO of following:**	**8 M**
(a)	**Compare intrinsic and extrinsic semiconductor (any 4 points).**	**4 M**
Ans:		**1 M for each point**

Intrinsic Semiconductor	Extrinsic Semiconductor
These are pure semi-conducting materials and no impurity atoms are added to it	When some impurity is added in the intrinsic semiconductor, extrinsic semiconductors can be produced.
The electrical conductivity is low.	The electrical conductivity is high.
The electrical conductivity of intrinsic semiconductors depends on their temperatures.	The electrical conductivity depends on the amount of impurity added in them.
e.g The crystals of pure elements like germanium and silicon	e.g. P & N type semiconductor

(b)	**Explain full wave bridged rectifier with the help of circuit diagram and input output waveform.**	**4 M**
Ans:	 **Operation:**	**2M**

1. In positive half cycle (0 to Π):

The end A of the secondary winding becomes positive and end B negative.

This makes diode D1 and D4 forward biased while diode D2 and D3 are reverse biased.

These two diodes will be in series through the load RL. The conventional current direction is as follows.

A – D1 – RL – D4 – B

This makes load voltage polarities as shown in the fig above. **1M**

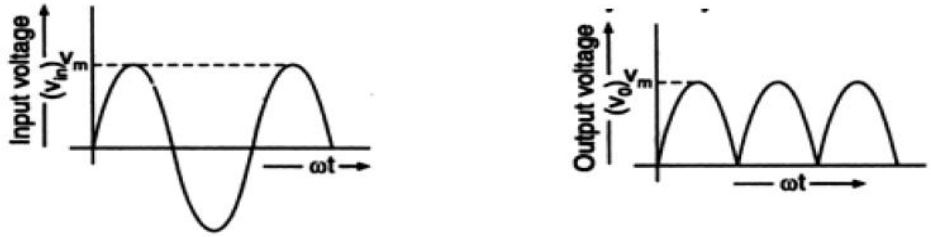
2. In negative half cycle (Π to 2Π).

The end B is positive and A is negative. This makes diode D2 and D3 forward biased and diode D1 and D4 is reverse biased.

The conventional current through diode D2 and D3 when it is conducting is as follows.

B – D2 – RL – D3 – A

Waveforms:



1M

(c)	**Explain working of n-p-n transistor in unbiased condition.**	**4 M**
Ans:	**Construction of NPN transistor:**	**2M**

For an unbiased transistor no external power supplies are connected to it.

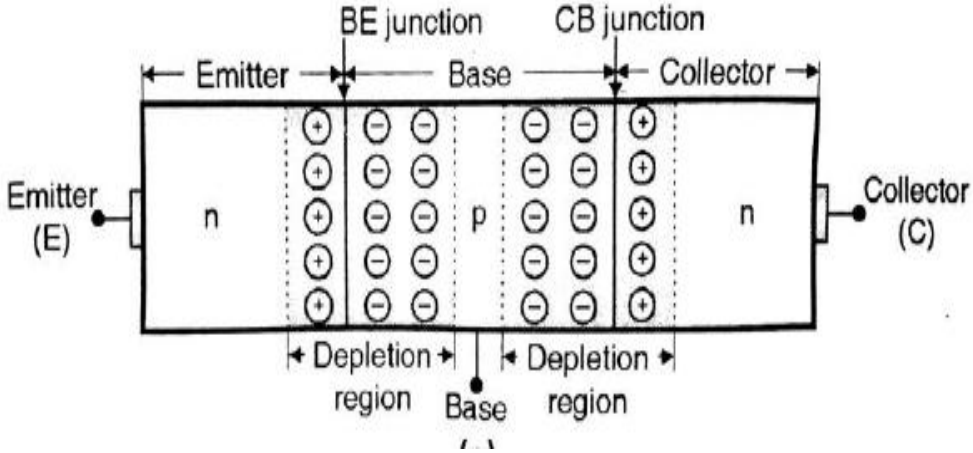
Base is sandwiched between collector & emitter terminal. It is thin & lightly doped layer.

Emitter & collector layers are wider than base & heavily doped than base.

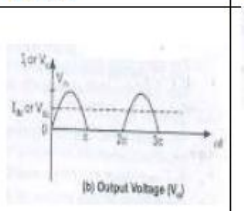
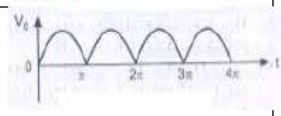
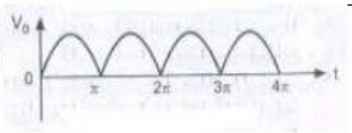
A transistor is formed of two P-N junctions. For unbiased P-N junctions, the depletion regions are formed. The fig(a) shows the depletion regions formed at the B-E and C-B junctions of n-p-n transistor.

Due to this depletion region any kind of current will not flow due to majority carrier but very small amount of current will flow because of thermally generated minority carrier.

To break this depletion layer there is a need of providing external power supply to transistor & this process is known as Biasing. **2M**



Q 2		Attempt any four of following :	16
	a)	**List specification of zener diode (any 4).**	4M
	Ans:	1. Zener Voltage 2. Maximum Zener current 3. Power dissipation 4. Operating temperature 5. Dynamic Resistance	1M each
	b)	**Compare half wave rectifier, full wave centre tapped rectifier and full wave bridge rectifier w.r.t. 1) Efficiency 2) Ripple factor 3) TUF 4) Output waveform**	4M
	Ans:		1M each for points
	c)	**Explain R-C coupled amplifier with circuit diagram.**	4M
	Ans:		Diagram:2 M & Explanation :2M

Parameters	HWR	FWCTR	FWBR
Ripple factor	1.21	0.482	0.482
Rectification efficiency	40.6%	81.2%	81.2%
TUF	0.282	0.693	0.812
Waveforms			

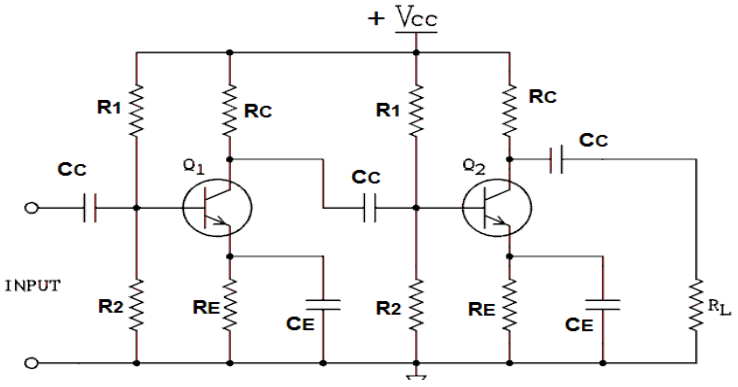


Fig.1

When a.c. signal is applied to the base of the first transistor, it is amplified and developed across the output of the 1st stage. This amplified voltage is applied to the base of next stage through the coupling capacitor Cc where it is further amplified and reappears across the out put of the second stage. Thus the successive stages amplify the signal and the overall gain is raised to the desired level. Much higher gains can be obtained by connecting a number of amplifier stages in succession (one after the other). Resistance-capacitance (RC) coupling is most widely used to connect the output of first stage to the input (base) of the second stage and so on.

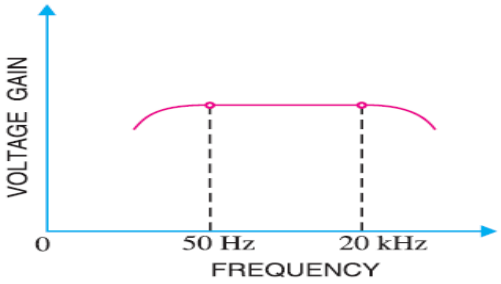
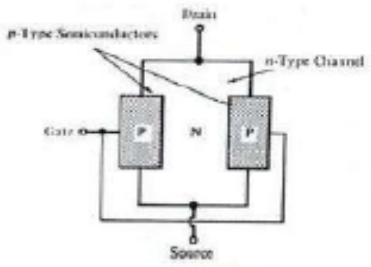


Fig.2

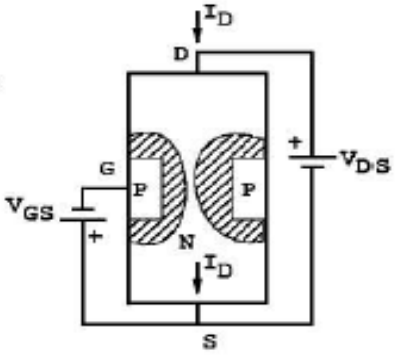
Frequency response curve: The curve representing the variation of gain of an amplifier with frequency is known as frequency response curve. It is shown in Fig. 2. The voltage gain of the amplifier increases with the frequency, f and attains a maximum value. The maximum value of the gain remains constant over a certain frequency range and afterwards the gain starts decreasing with the increase of the frequency. It may be seen to be divided into three regions.

1) Low frequency range (20 kHz).
2) Mid frequency range (50 Hz to 20 KHz) and
3) High frequency range (> 20 kHz)

d)	**Explain construction of n-channel JFET with neat sketch.**	**4M**
Ans:	**N-channel JFET (FET):**	**Diagram:2 M & Explanation :2M**



n-channel JFET



Construction:

The n-channel JFET has n-type semiconductor used as a channel which has two terminals, drain and source. Two p-type semiconductors are attached at both sides of n-channel and forms third terminal gate. Thus pn junction exists between gate and source.

1) When $V_{GS} = 0$ volt:
   When a voltage is applied between the drain and source with a DC supply voltage V_{DD} with $V_{GS} = 0$ V, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes drain current I_D. The value of drain current is maximum when $V_{GS} = 0$ V. This current is designated vy the symbol I_{DSS}.
2) When V_{GS} is negative:
   When V_{GS} is increased below zero i.e negative, the reverse voltage across the gate source junction is incrased. As a result depletion regions are widened. This reduces effective width of channe and therefore controls the flow of drain current through the channel.
   If V_{GS} is increased further, two depletion regions touch each other. The drain current reduces to zero. The gate to source voltage at which current reduces to zero is called as pinch-off voltage.

e) **Compare CE, CB, CC w.r.t. to 1) Current gain 2)Voltage gain 3) Input impedance 4) Output impedance.** **4M**

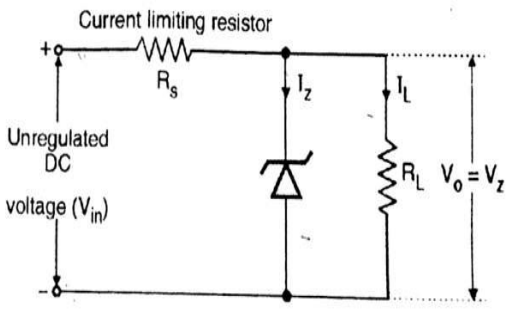
Ans: **1M each point**

Comparison between CB, CE and CC configurations:

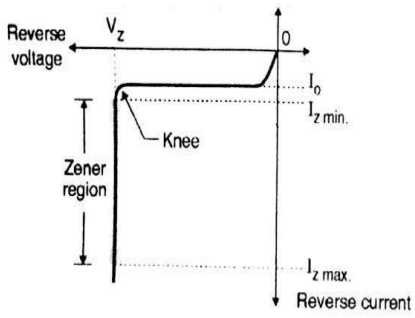
Parameter	CB	CE	CC
Input Impedance	Low Or 50Ω	Medium Or 600Ω to 4kΩ	High Or 1 MΩ
Current Gain	Less than or equal to 1 Or $\alpha = \frac{I_C}{I_E}$	High Or $\beta = \frac{I_C}{I_B}$	High Or $\gamma = \frac{I_E}{I_B}$
Voltage Gain	Medium	Medium	Less than or equal to 1
Output Impedance	High Or 50 kΩ	Medium Or 10 kΩ to 50 kΩ	Low Or 50Ω

f) **Explain with circuit diagram operation of zener diode as voltage regulator.** **4M**

Ans: **Diagram:2 M & Explanation :2M**



(a) Regulator circuit using Zener Diode



(b) Reverse characteristics of Zener Diode

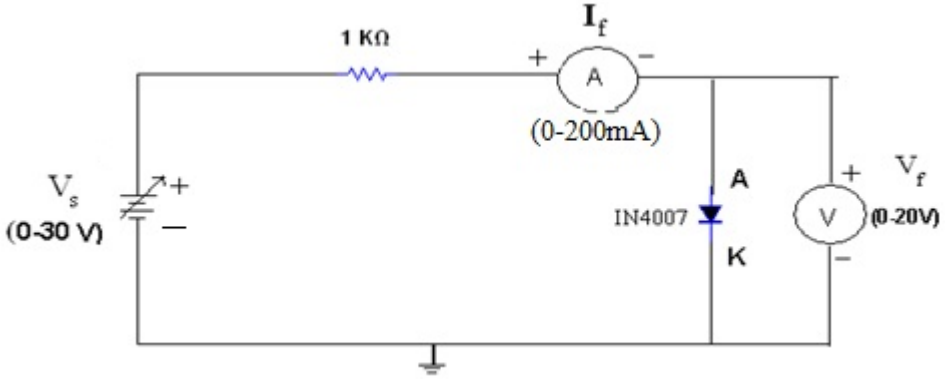
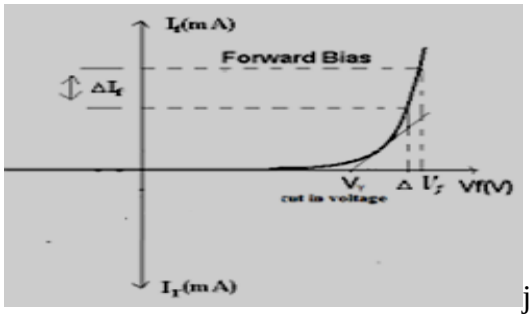
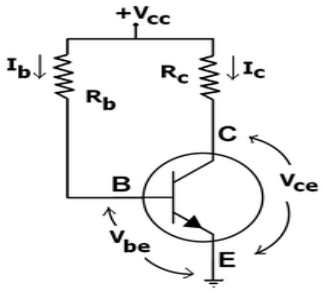
Zener Diode as Voltage Regulator:

A voltage regulator circuit should keep the load voltage constant in spite of changes in its input voltage or load current and temperature. The series resistance Rs is connected to limit the total current drawn from the unregulated dc supply. The zener diode regulator, as shown in fig.(a), is a shunt type voltage regulator because the control element i.e. zener diode is connected in parallel with the load resistance.

Working of Zener Voltage Regulator:

The input voltage Vin is an unregulated dc voltage which is obtained from a rectifier filter combination. Rs is the current limiting resistor and RL is the load resistor. The input voltage Vin should always be higher than the breakdown voltage V_Z. The zener diode is reverse biased and operates in the zener region of the reverse characteristics, as shown in fig.(b)

If Vin is higher than V_Z and if the Zener current I_Z is between I_{Zmin} and I_{Zmax} then the voltage across the Zener will remain constant equal to V_Z irrespective of any changes in Vin and I_L. As the output voltage is constant and equal to V_Z, we get regulated output voltage.

		The Zener current I_Z should not be higher than I_{Zmax}, otherwise excessive power dissipation will damage the Zener diode. The Zener current I_Z should not be less than I_{Zmin} because the Zener diode then cannot operate in the zener region and cannot maintain constant voltage across it. The regulator keeps the load voltage constant in spite of changes in input voltage and load current.	
Q. 3		**Attempt any FOUR of the following.**	**16**
	a)	**Draw experimental circuit diagram and characteristics for forward biased P-N junction diode.**	**4M**
	Ans:	  j	**Each Diagram:2 M**
	b)	**Explain with circuit diagram fixed bias method of BJT.**	**4M**
	Ans:	**Fixed bias (base bias)**  Fixed bias (Base bias) This form of biasing is also called base bias or fixed resistance biasing. The single	**Diagram:2 M & Explanation :2M**

power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$V_{cc} = I_B R_B + V_{be}$

Therefore,

$I_B = (V_{cc} - V_{be})/R_B$

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of R_B, the base current I_B is fixed. Therefore, this type is called *fixed bias* type of circuit.

Also for given circuit,

$V_{cc} = I_C R_C + V_{ce}$

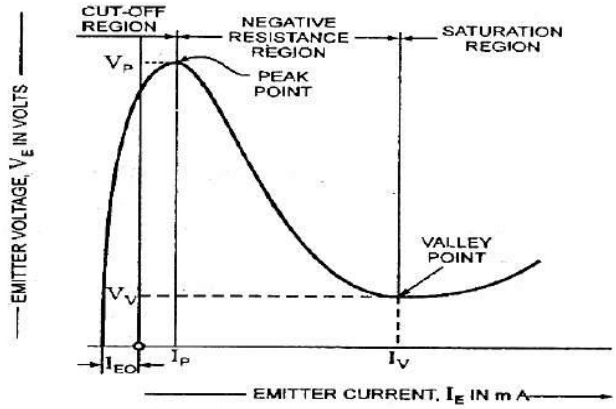
Therefore,

$V_{ce} = V_{cc} - I_C R_C$

$I_C = \beta I_B$

Thus I_C is obtained. In this manner, operating point given as (V_{ce},I_C) can be set for given transistor.

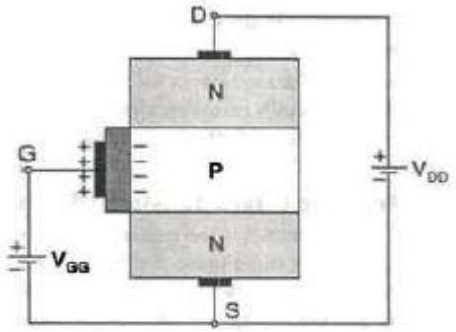
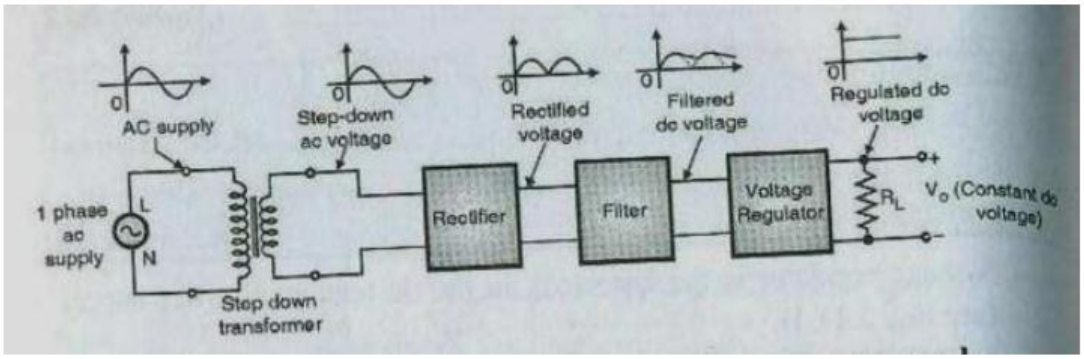
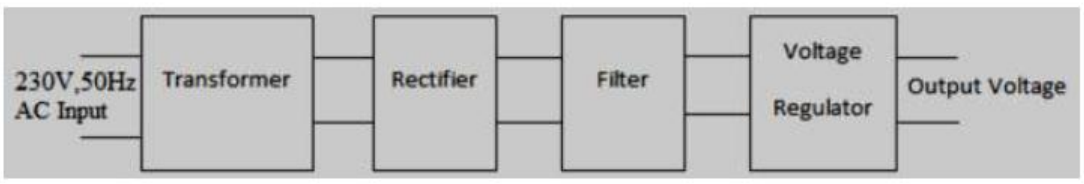
c)	**Draw and explain VI characteristics of UJT.**	**4M**
Ans:	**UJT Characteristics:**	**Diagram:2 M & Explanation :2M**



UJT Characteristic

The UJT characteristic is emitter voltage versus emitter current characteristic, as shown in the figure. For emitter voltages less than V_P (peak point voltage) the UJT is in the off state and magnitude of I_E is not greater than I_{EO}. The emitter current I_{EO} corresponds very closely with the reverse leakage current I_{CO} of a bipolar transistor. This region is known as the cut off region.

As the emitter voltage increases and reaches $V_P = (\eta V_{BB}+V_D)$, the UJT starts conducting. Then with increase in emitter IE the emitter voltage decreases as shown. The reduction in voltage across UJT is due to the drop in resistance R_{B1} with increase in the value of I_E. This region of operation is known as a "Negative Resistance" region, which is stable enough to be used in various applications. Eventually the "valley point" will be reached and further increase in I_E will place the device into saturation.

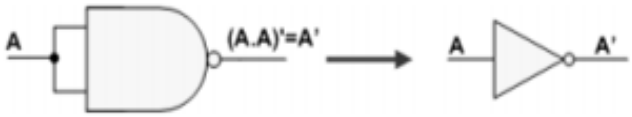
d)	**Draw and explain working principle of N-channel enhancement MOSFET.**	**4M**
Ans:	 **Working:** When V_{GS} is set at 0V and a voltage is applied between the drain and source, no current flows due to the absence of an N-channel. By keeping V_{DS} at some positive voltage and when V_{GS} is increased, the positive potential at the gate will push the holes (since like charges repel) in the P-substrate along the edge of the SiO_2 layer. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the P-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. This is called Inversion layer. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases, until eventually, the induced N-type region can support a measurable flow between drain and source.	**Diagram:2 M & Explanation :2M**
e)	**Draw block diagram of DC regulated power supply state function of each block.**	**4M**
Ans:	**DC Power Supply:** There are four basic blocks of a DC regulated power supply. They are: 1) Step-down transformer 2) Rectifier 3) Filter 4) Voltage Regulator  OR 	**Diagram:2 M & Explanation :2M**

		Functions of Each Block: i) Step-down transformer: Reduces 230V, 50 hz ac voltage to required ac voltage level. ii) Rectifier: Converts ac voltage into dc voltage. Typically bridge type full-wave rectifier is widely used. iii) Filter: Used to remove fluctuations (ripples) present in dc output. iv) Voltage regulator: Provides constant dc output voltage irrespective of changes in load current or changes in input voltage. Voltage divider circuit is used to provide different dc voltages required for different electronic circuits.	
	f)	**Explain NAND gate as universal gate implement AND, OR and NOT gate using NAND gate only.**	**4M**
	Ans:	A universal gate(NAND) is a gate which can implement any Boolean function without need to use any other gate type. NAND Gate is a Universal Gate: To prove that any Boolean function can be implemented using only NAND gates, we will show that the AND, OR, and NOT operations can be performed using only these gates.	**1M for each explanation**

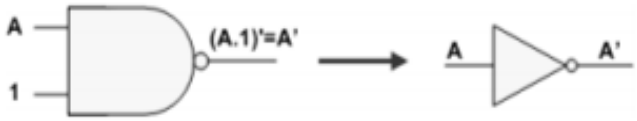
Implementing an Inverter Using only NAND Gate

The figure shows two ways in which a NAND gate can be used as **an inverter (NOT gate)**.

1. All NAND input pins connect to the input signal **A** gives an output **A'**.



2. One NAND input pin is connected to the input signal **A** while all other input pins are connected to logic **1**. The output will be **A'**.

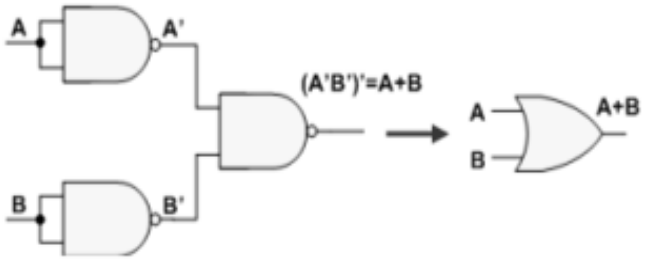


Implementing AND Using only NAND Gates

An AND gate can be replaced by NAND gates as shown in the figure (The AND is replaced by a NAND gate with its output complemented by a NAND gate inverter).

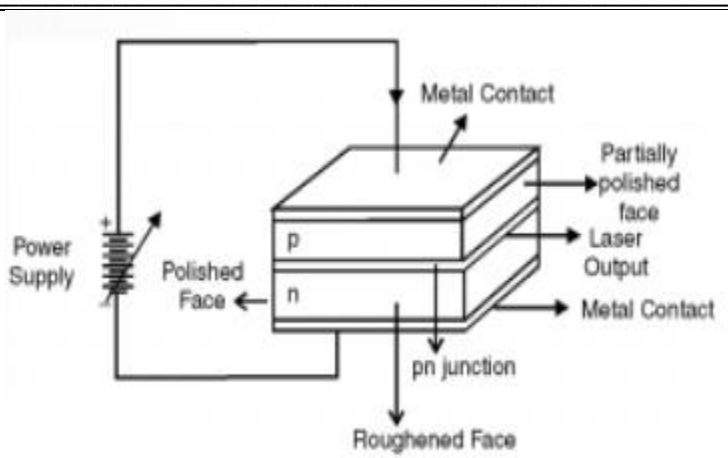
Implementing OR Using only NAND Gates

An OR gate can be replaced by NAND gates as shown in the figure (The OR gate is replaced by a NAND gate with all its inputs complemented by NAND gate inverters).



Thus, the NAND gate is a universal gate since it can implement the AND, OR and NOT functions.

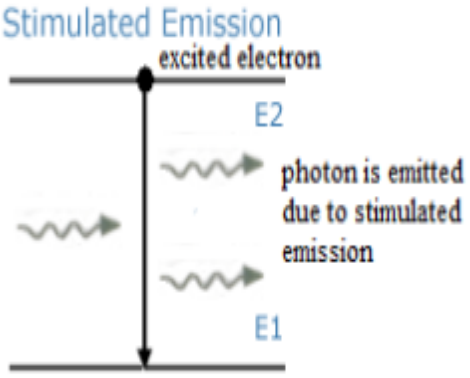
Q. 4		**Attempt any FOUR of following:**	**16 M**
	a)	**Explain operating principle of LASER.**	**4 M**
	Ans:	**LASER**	**(Diagram:1 M, Stimulated emission :2M,**



Working principle of LASER diode :

Stimulated Emission:

- In this process "amplification" of light takes place.
- If light energy strikes to the excited electron present in higher energy level, then electron will fall back to its original level.
- While returning back it will emit two photons. So one incident photon causes emission of two photons and hence light amplification takes place.
- This principle is used in LASER diode.



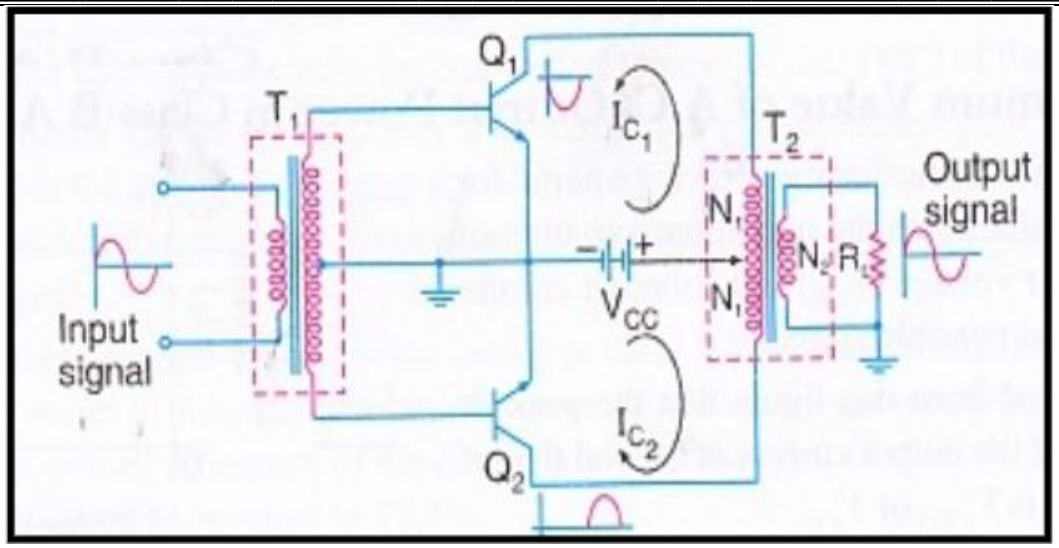
Operation:

- When the PN junction is forward biased by an external voltage source, electrons move across the junction and recombination occurs in the depletion region which results in the production of photons.
- As forward current is increased, more photons are produced which drift at random in depletion region.
- Some of these photons strike the reflective surface perpendicularly. These reflected photons move back and forth between two reflective surfaces as shown in fig above.
- The photon activity becomes so intense that at some point a strong beam of laser comes out of the partially reflective surface of the diode.

Operation 1M)

b)	**Explain class B push pull power amplifier with circuit diagram.**	**4 M**
Ans:	**class B push pull power amplifier**	**(Diagram:2 M, Explanatio**

n: 2M)



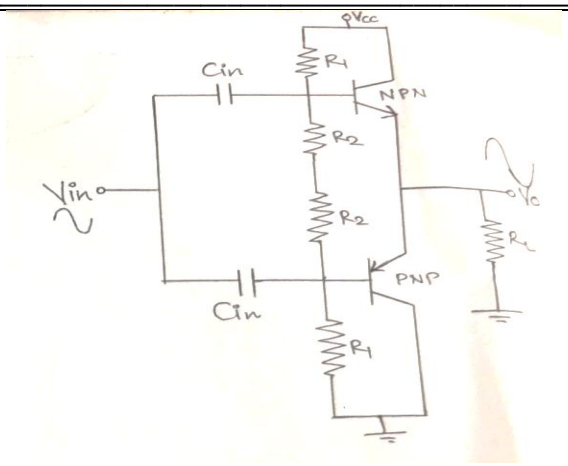
CIRCUIT DESCRIPTION:

- The circuit consists of two centre tapped transformers T_1 & T_2& two identical transistors Q_1& Q_2.
- The transformer T_1 is an input transformer and is called as phase splitter. It is required to produce two signal voltages, which are 180° out of phase with each other.
- These two signal voltages with opposite polarity, drive the input of transistors Q_1& Q_2..
- The transformer T_2 is an output transformer and is required to couple the a.c. output signal from the collector to the load.
- The transistors Q_1 and Q_2 are biased at cut off.
- The two emitters are connected to the centre tap of transformer T_1 secondary and the V_{CC} supply to the centre tap of transformer T_2 secondary.

WORKING:

- When there is no a.c. input signal applied, both the transistors Q_1& Q_2 are cut off. Hence no current is drawn from V_{CC}.
- DURING POSITIVE HALF CYCLE:
  - The base of the transistor Q_1 is positive and that of Q_2 is negative.
  - As a result of this Q_1 conducts, while the transistor Q_2 is OFF.
- DURING NEGATIVE HALF CYCLE:
  - The base of the transistor Q_2 is positive and that of Q_1 is negative.
  - As a result of this Q_2 conducts, while the transistor Q_1 is OFF.
- Thus at any instant any one transistor in the circuit is conducting.
- Then the output of the transformer joins these two halves & produces a full sine wave in the load resistor.

OR

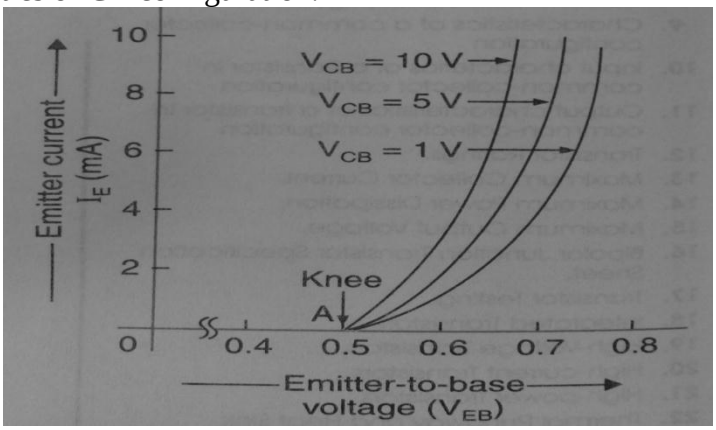


Circuit Description:

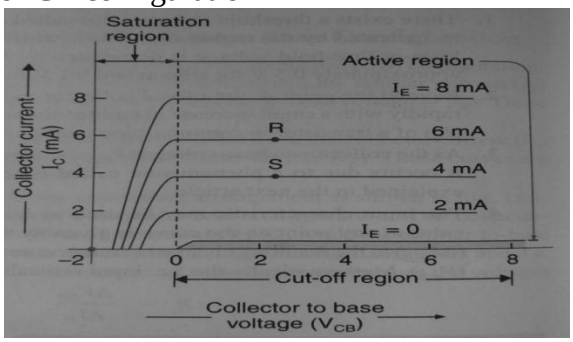
- Two transistors one NPN & other PNP is used in the circuit so they are complementary to each other.
- Biasing conditions used for both transistors are same so they are symmetrical.
- R_1, R_2, V_{CC} are used for voltage divider bias of transistors.
- Both transistors conduct for 180°as it is class B amplifier.
- Whenever one transistor is ON other push to be OFF so the name push pull.

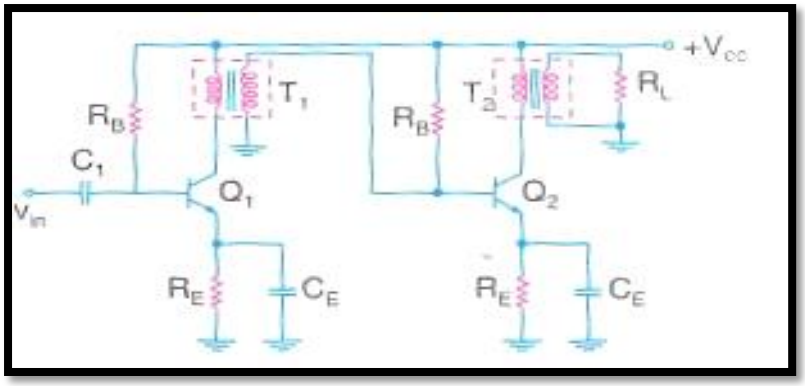
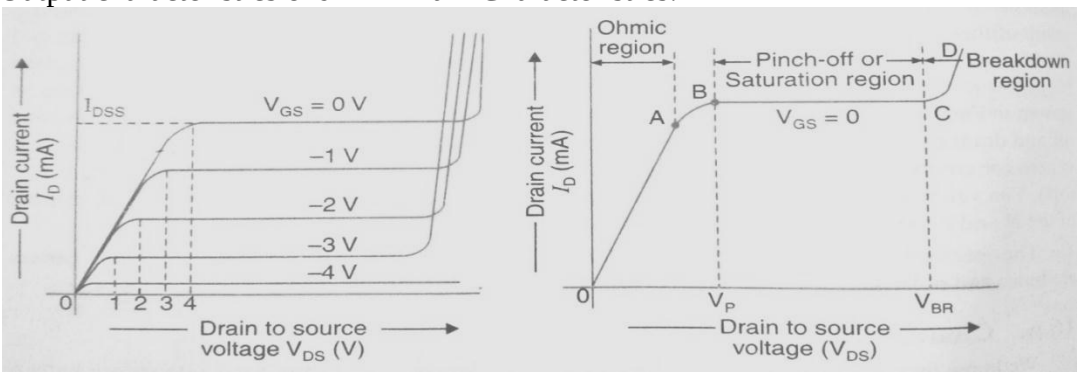
Working:

- Input signal V_{in} is applied to both the transistor through input capacitor.
- During positive half cycle of input:
  - The base of the transistors NPN & PNP is positive.
  - As a result of this NPN conducts & PNP remains OFF.
  - So we get half cycle in the output.
- During negative half cycle of input:
  - The base of the transistors NPN & PNP is negative.
  - As a result of this PNP conducts & NPN remains OFF.
  - So we get remaining half cycle in the output.

c)	**Draw input and output characteristics of CB configuration.**	**4 M**
Ans:	input characteristics of CB configuration. 	**(Input characteristics: 2M, Output characteristics: 2M)**

output characteristics of CB configuration



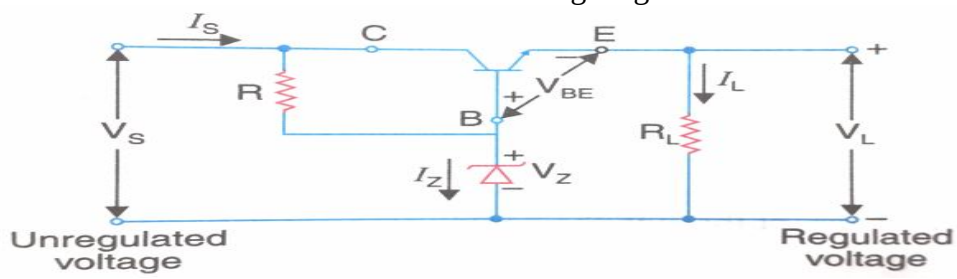
d)	**Explain with circuit diagram transformer coupled amplifier.**	**4 M**
Ans:	**1. TRANSFORMER COUPLED AMPLIFIER** **CIRCUIT DIAGRAM:**  **CIRCUIT DESCRIPTION:** The circuit consists of two single stage common emitter transistor amplifiers. The function of transformer (T_1) is to couple the a.c. output signal from the output of the first stage to the input of second stage, while transformer (T_2) couples the output signal to the load. The input coupling capacitor is C_1, while the emitter bypass capacitor is C_E. OPERATION: The operation of above circuit may be understood from the conditions that when an a.c. input signal is applied to the base transistor Q_1, it appears in the amplified form across primary winding of the transformer (T_1). The voltage developed across the primary winding is then transferred to the input of the next stage by the secondary winding of the transformer (T_1). The second stage the amplification in an exactly similar manner.	**(Diagram: 2M, Explanation: 2M)**
e)	**Draw and explain output characteristics of JFET.**	**4 M**
Ans:	Output characteristics of JFET Drain Characteristics:  	**(Draw characteristics: 2M, Explanation: 2M)**

- First we adjust gate to source voltage V_{GS} to zero volt. Then increase drain to source voltage V_{DS} in small suitable steps& record corresponding values of drain current I_D at each steps.
- A similar procedure may be used to obtain curves for different values of gate to source voltage V_{GS} i.e. V_{GS} = 1V, 2V, 3V & 4V.
- Now if we plot a graph with drain to source voltage V_{DS} along horizontal axis & drain current I_D along a vertical axis.
- The curve may be sub-divided into following regions:
  1. **OHMIC REGION**: The region is shown as a curve OA in the figure. In this region drain current increases linearly with the increase in drain to source voltage, obeying Ohm's law. The linear increase in drain current is due to the fact that N-type semiconductor bar act as resistor.
  2. **CURVE AB**: In this region drain current increases slowly as compared to that in ohmic region. It is because of the fact that with increase in drain to source voltage V_{DS} drain current also increases. This in turn increases reverse bias voltage across the gate-source junction. As a result of this depletion region grows in size, thereby reducing effective width of channel. At the drain to source voltage V_{DS} corresponding to point B, the channel width reduce to minimum value & is known as pinch off. Drain to source voltage V_{DS} at which the channel pinch off occurs is known as pinch off voltage V_P.
  3. **PINCH OFF REGION**: The region is shown as a curve BC in the figure. It is also called as constant current region & saturation region. In this region Drain current I_D remains constant at maximum value I_{DSS}. The drain current in pinch off region is dependent on V_{GS} & it is given by Shockley's equation, $I_D = I_{DSS}\{1-\frac{V_{GS}}{V_P}\}^2$
  4. **BREAKDOWN REGION**: The region is shown as a curve CD in the figure. In this region drain current increases rapidly with the increase in drain to source voltage. It happens because breakdown of gate to source junction due to avalanche effect. The drain to source voltage V_{DS} corresponding to point C is called as breakdown voltage.

f) Explain with circuit diagram transistorized series voltage regulator. — **4 M**

Ans:

Transistorized Series Voltage regulator:



In above fig. , transistor is connected in series with load therefore the circuit is known as a series regulator.

Diagram.:2 M, Explanation: 2M

- The transistor behaves as variable resistances whose value is determined by the amount of base current.
- $V_L = V_Z - V_{BE}$ OR $V_{BE} = V_Z - V_L$

WORKING:-

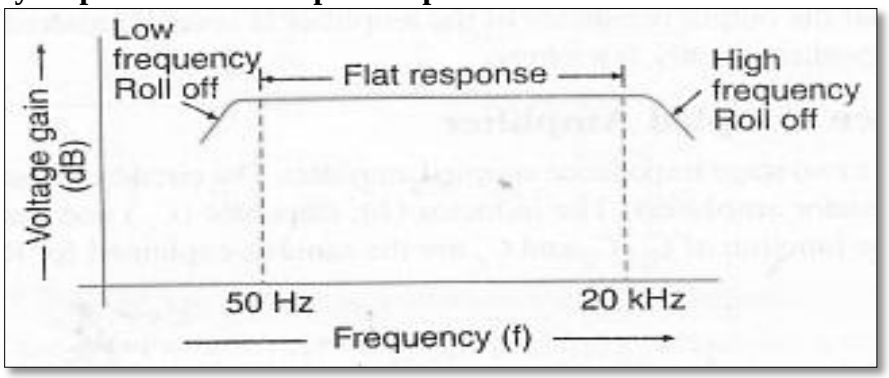
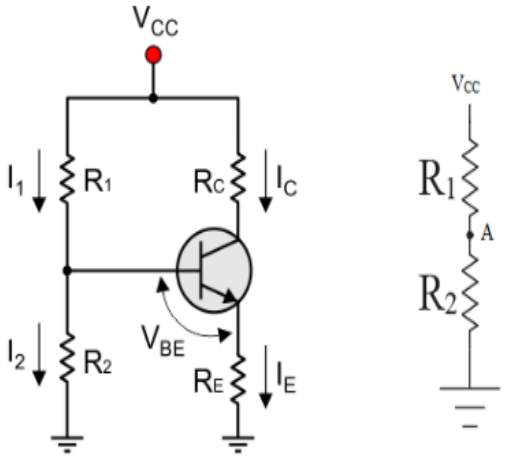
- Suppose that value of load resistance is increased. Because of this, the load current decreases and load voltage (V_L) tend to increase.
- From equation (1) that any increase in V_L will decrease V_{BE} because V_Z value is fixed.
- As a result of this the forward bias of the transistor is reduced which reduces its level of conduction.
- This increases V_{CE} of transistor which will slightly decrease the input current for the increase in the value of load resistance so that load voltage remains constant.
- The output of a transistor series regulator is approximately equal to zone voltage (V_Z)
- This regulator can also be used for larger load currents.

Q.5 **Attempt any FOUR of following:** **16 M**

a) **Compare BJT with FET (any 4 pts.).** **4 M**

Ans: **1m Each (Any 4 Points)**

SR. NO.	FET	BJT
1	It is unipolar device i.e. current in the device is carried either by electrons or holes	It is bipolar device i.e. current in the device is carried either by both electrons & holes
2	It is a voltage controlled device i.e. voltage at the gate (or drain) terminal controls amount of current flowing through the device.	It is a current controlled device i.e. the base current controls the amount of collector current.
3	Its input resistance is very high & is of order of several megaohms.	Its input resistance is very low compared to FET.
4	It has a negative temperature co-efficient at high current levels. It means that current decreases as temperature increases.	It has a positive temperature co-efficient at high current levels. It means that current increases as temperature increases.
5	It is less noisy.	It is comparatively noisier.
6	It has relatively lower gain bandwidth product as compared to BJT.	It has relatively higher gain bandwidth product as compared to FET.
7	It is simpler to fabricate as IC & occupies less space on chip compared to BJT.	It is comparatively difficult to fabricate on IC & occupies more space on chip compared to FET.
8	It is relatively immune to radiation.	It is susceptible to radiation
9	It does not suffer from minority- carrier storage effects & therefore has higher switching speeds & cut-off	It suffers from minority- carrier storage effects & therefore has lower switching speeds & cut-off frequencies.

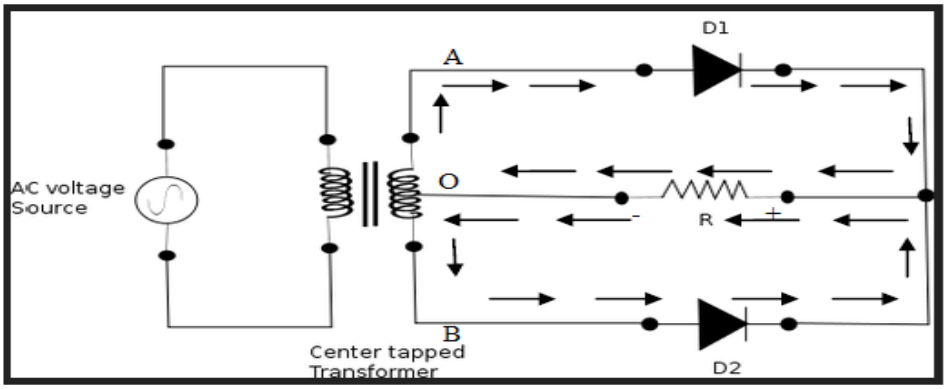
		frequencies.	
	b)	**State the need of multistage amplifier. Draw frequency response of R-C coupled amplifier.**	**4 M**
	Ans:	**The need of multistage amplifier** The voltage (or power) gain, obtained from a single stage small signal amplifier, is limited. Therefore, it is not sufficient for all practical applications. Therefore, in order to obtain greater voltage and power gain, we have to use a 'MULTISTAGE AMPLIFIER'. **Frequency response of R-C coupled amplifier.**  	**Need 2M, frequency response 2M**
	c)	**Draw circuit diagram of voltage divider biasing list two advantages of voltage divider biasing of BJT.**	**4 M**
	Ans:	**circuit diagram of voltage divider biasing of BJT**  **Two advantages of voltage divider biasing of BJT.** 1. It is very simple method of transistor biasing. 2. The biasing conditions can be very easily set. 3. there is no loading of source 4. It provides better bias stabilization. 5. The resistor R_E introduces a negative feedback. So all the advantages of negative feedback are obtained.	**Circuit diagram 2M, each advantage 1M**
	d)	**Explain with circuit diagram and input output waveform center trapped full wave rectifier.**	**4 M**

Ans:

Full wave Rectifier with Center tapped transformer(FWR):

- In full wave rectification, the rectifier conducts in both the cycles as two diodes are connected.

Circuit diagram:



- The circuit employs two diodes D1 and D2 as shown. A center tapped secondary winding AB is used with two diodes connected. So that each uses one half –cycles of input AC voltage.
- Diode D1 utilized the AC voltage appearing across the upper half (OA), while diode D2 uses the lower half winding (OB).
- The voltage V_s between the center-tap and either ends of secondary winding is half of the secondary voltage V_2 i.e $V_s = \frac{V_2}{2}$
- If the output voltage should be equal to the input voltage, a step up transformer with turns ratio $\frac{N_2}{N_1} = 2$ must be used. Thus the total secondary voltage V_2 is twice the primary voltage.

i.e, $V_s = V_1 = \frac{V_2}{2}$

Operation:

1. In positive half cycle (0-Π).

- The end A of the secondary winding becomes positive and end B negative.
- This makes diode D_1 forward biased and diode D_2 reverse biased. Therefore D_1 conducts while D_2 does not.
- The conventional current flow direction in the upper half winding as shown in the fig above.

  $A - D_1 - R_L - O$

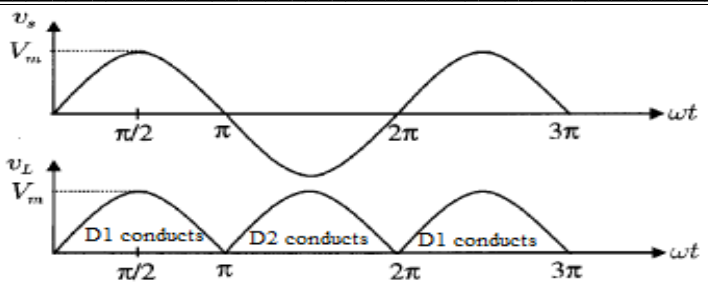
2. In negative half cycle (Π-2Π):

- End A of secondary winding becomes negative and end B positive. Therefore diode D_2 conducts while diode D_1 does not.
- The conventional current flow is as shown by the arrows in the above fig.

  $B - D_2 - R_L - O$

- From fig. current in the load R_L is in the same direction for both half-cycles of input AC voltage. Therefore DC is obtained across the load R_L.

Circuit Diagram 2M, Input Output Waveform 1M, Explanation 1M



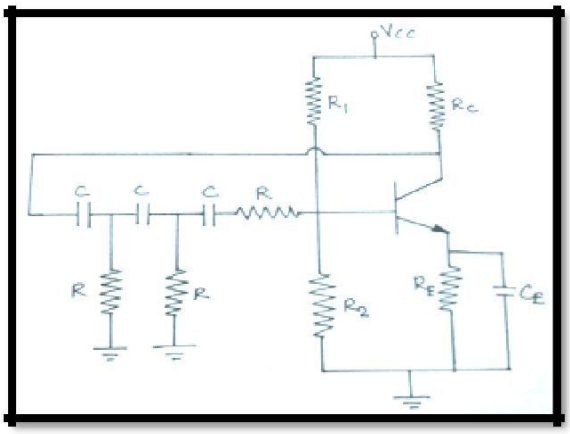
e) Differentiate between positive and negative feedback (any 4pts.). **4 M**

Ans: **Each point 1M**

SR. NO.	PARAMETER	POSITIVE FEEDBACK	NEGATIVE FEEDBACK
1.	Overall phase shift	0° or 360°	180°
2.	Feedback and input signal	Are in phase	Are out of phase
3.	Input signal	Increases due to feedback	Decreases due to feedback
4.	Output signal	Increases due to feedback	Decreases due to feedback
5.	Gain	Increases due to feedback	Decreases due to feedback
6.	Stability	Becomes poor as feedback increases	Becomes better as feedback increases
7.	Application	Oscillators, Schmitt trigger	Amplifier, regulated power supply, bootstrapping
8.	Noise	Increases with feedback	Decreases with feedback
9.	Bandwidth	Decreases	Increases
10.	Input impedance	Decreases	Increases
11.	Output impedance	Increases	Decreases

f) Explain RC phase shift oscillator with circuit diagram. **4 M**

Ans: **RC PHASE SHIFT OSCILLATOR.** **Diag. 2M, explanation 2M**

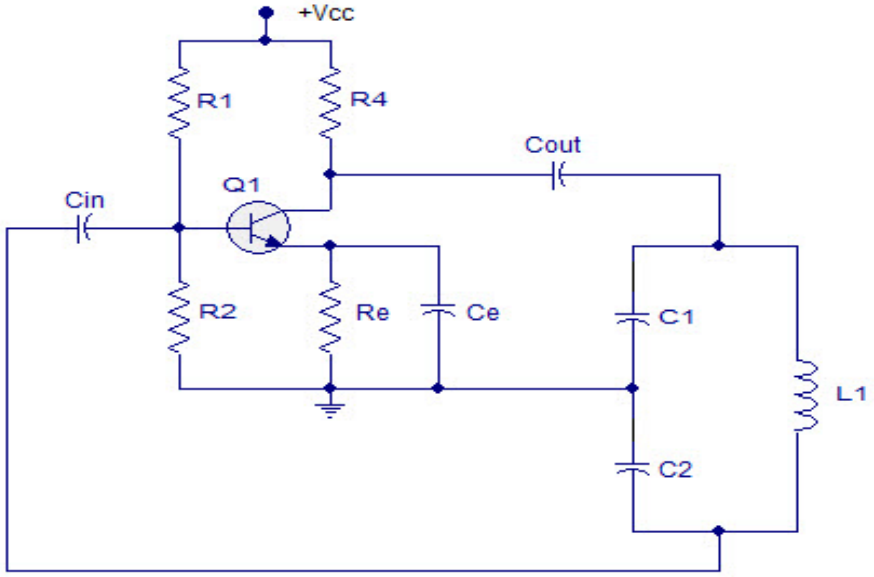


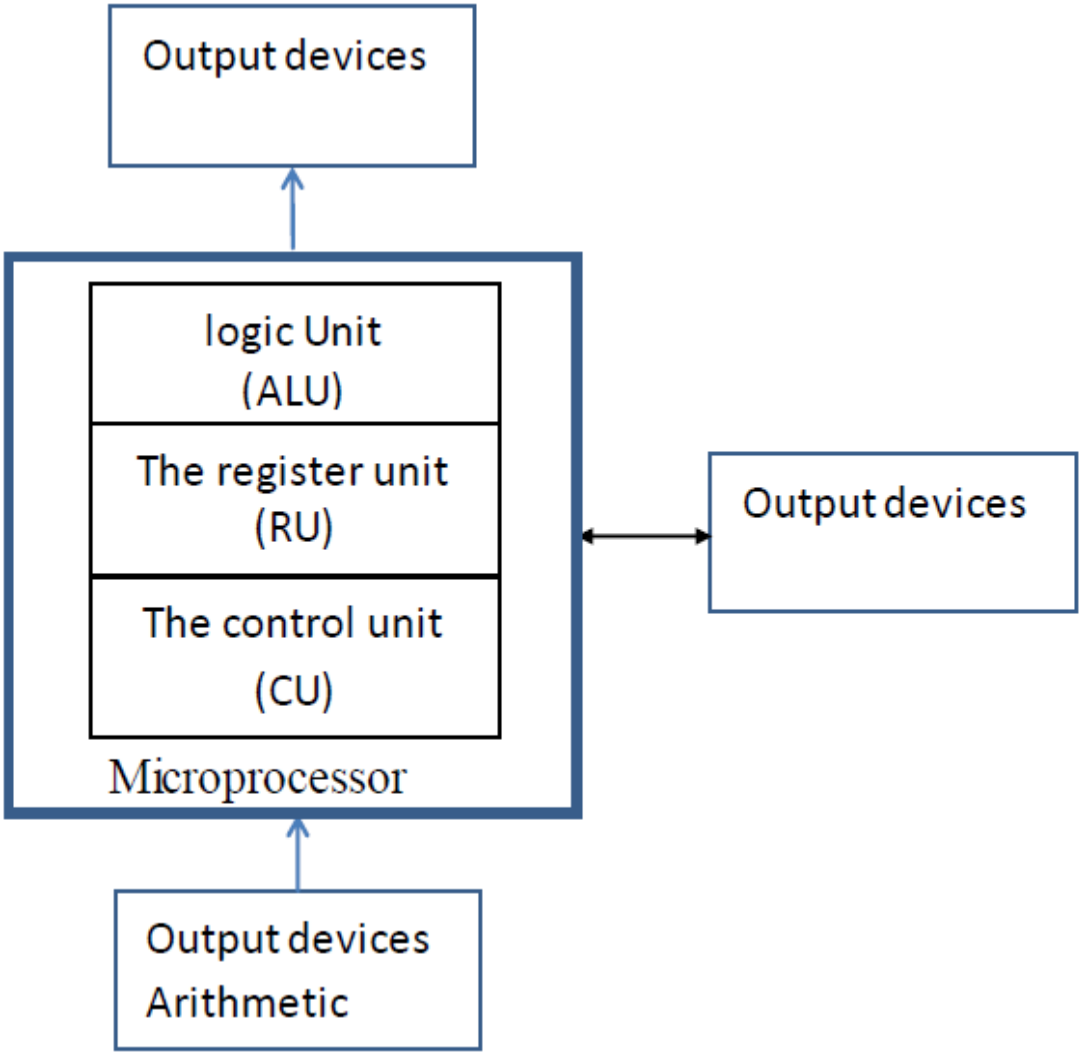
- Circuit consists of a single stage amplifier in common emitter configuration & RC phase shifting network.
- R_1, R_2, R_E provides biasing & C_E is bypass capacitor.

WORKING:

- Common emitter amplifier introduces 180^0 phase shift between input &output. & remaining 180^0 phase shift is produced by three identical basic RC phase shifting networks.
- Each RC network is designed to introduce a phase shift of 60^0.
- The phase shift around the loop is 360^0 only at one precise frequency.
  - This frequency of oscillations is equal to $\frac{1}{2\pi RC\sqrt{6}}$
  - The feedback factor $\beta = \frac{1}{29}$
    Therefore A_v =29.

Q.6		**Attempt any FOUR of following:**	**16 M**
	a)	**For Hartley oscillator C = 2 nF, L = 5.6 mH, Lz = 56 µH. Calculate frequency of oscillation.**	**4 M**
	Ans:	Given data- C= 2nF L1 = 5.6mH L2 = 56 µH Frequency of oscillation is given as $Fo = \frac{1}{2\pi\sqrt{L_T . C}}$ $L_T = L_1 + L_2$ =5.656 mH $F_o = \frac{1}{2\pi\sqrt{5.656}*10^{-3}*2*10^{-9}}$ =47.320 KH_z	
	b)	**Draw circuit diagram of Colpitts Oscillator. State its frequency of oscillation equation.**	**4 M**

	Ans:	 The frequency of oscillations is given by, $$F = \frac{1}{2\pi\sqrt{L\,C_T}}$$ Where, $$C_T = \frac{C_1\,C_2}{C_1 + C_2}$$	**Diag. 2M, Equation 2M**
	c)	**Draw and explain the basic block diagram of microprocessor.**	**4 M**
	Ans:	A CPU has three sub-units namely i) the Arithmetic logic Unit (ALU) ii) the register unit (RU) iii) the control unit (CU). They have been explained in the following sections.	**Diag. 2M, explanation 2M**



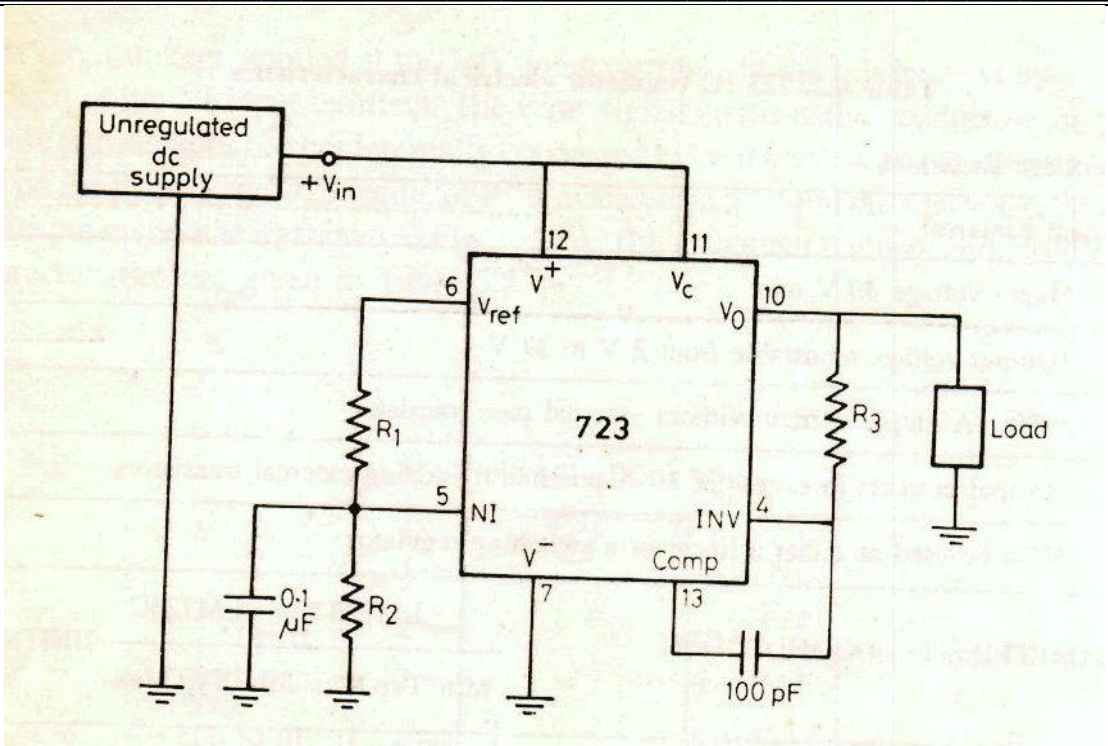
Arithmetic logic Unit:
This part of the microprocessor is responsible for performing all types of arithmetic (such as addition, subtraction, multiplication, division, etc.) and logical (such as AND, OR, EXOR, etc.) operation.

Register unit:
This unit contains several register meant for housing data during execution of any operation. Registers act like a data store. The data may either be stored in a register or may be recalled whether required, by executing different commands.

Control unit:
The necessary timing and control signals required for execution of any operation are generated by this part of the CPU. Sequencing of steps for execution of any operation is also decided by this unit.

d)	**Explain with circuit diagram IC 723 a dual voltage regulator.**	**4 M**

Ans:



IC 723 can be used as a dual voltage regulator.

$$Vo=V_{ref}\frac{R2}{R1+R2}$$

Diag. 2M, explanation 2M (any one diagram)

Or

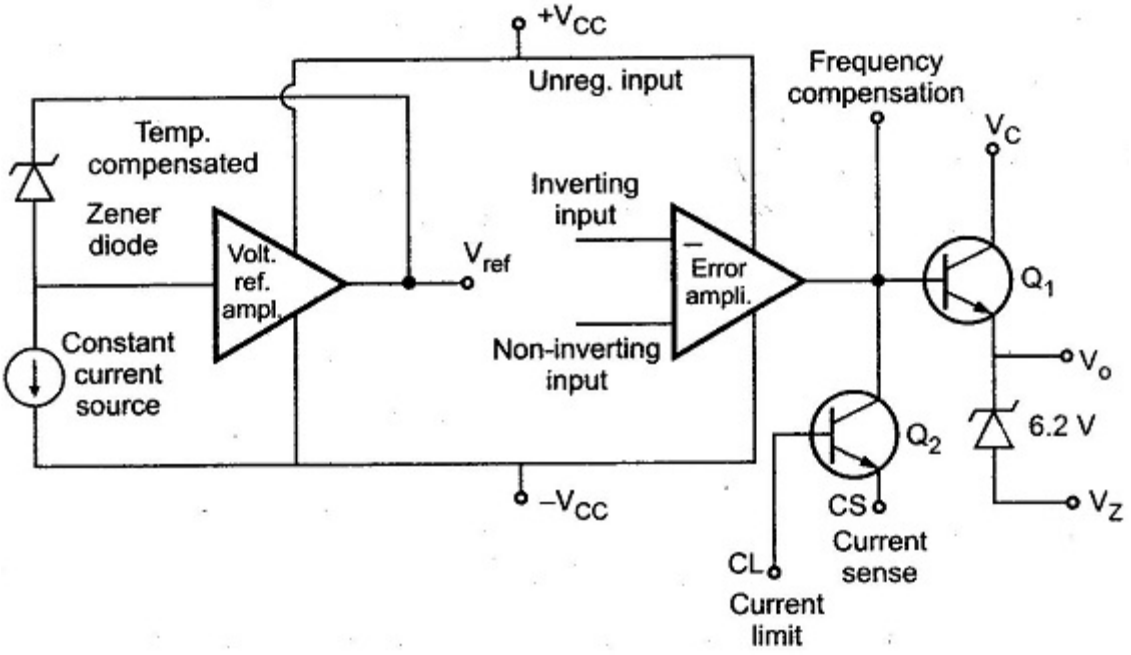
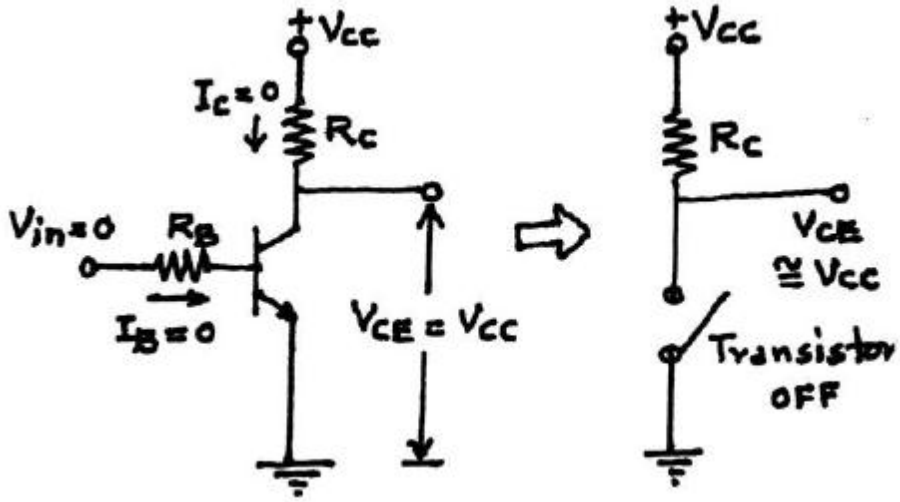


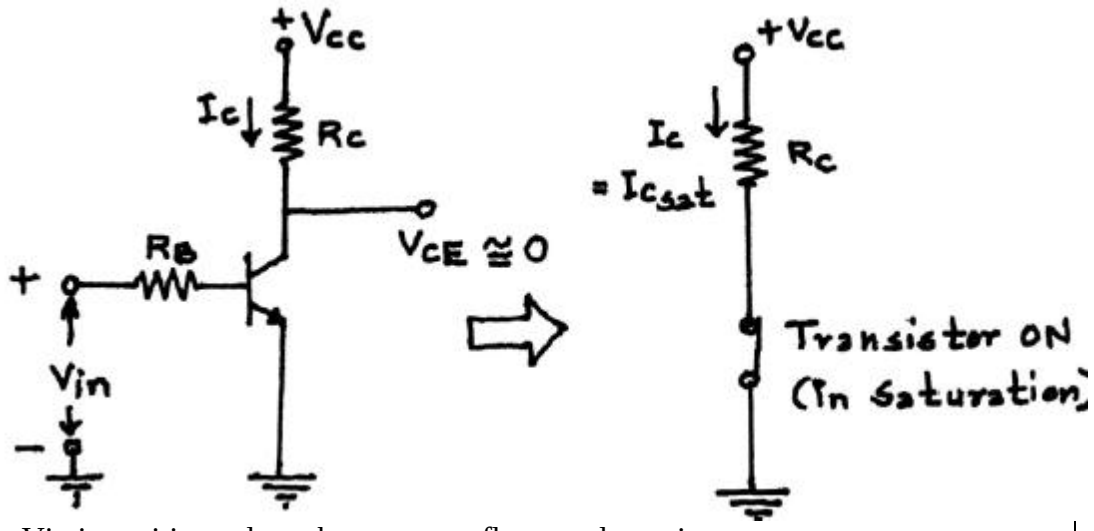
Fig. 2.110 Functional block diagram

Features of IC 723:-

1.Maximum load current of 150 mA
2.Positive & negative supply operation.
3.Internal Power dissipation of 800 mW
4.High ripple rejection
5.Built in short circuit protection.

	e)	**Explain with circuit diagram transistor as a switch.**	**4 M**

	Ans:	**Transistor as Switch:** A transistor can be used for two types of applications viz. amplification and switching. For amplification, the transistor is biased in its active region. For switching applications, transistor is biased to operate in the saturation (full on) or cut-off (full off) region. **(i) Transistor in cut-off region (Open switch):**	(OFF condition: diagram = 1 marks, explanation = 1 mark
			
		In the cur-off region, both the junctions of transistor are reverse biased and very small reverse current flows through the transistor. The voltage drop across the transistor (VCE) is high, nearly equal to supply voltage VCC. Thus, in cut-off region the transistor is equivalent to an open switch as shown in above fig. **ii)Transistor in Saturation region (Closed switch):**	ON condition: diagram = 1 marks, explanation = 1 mark



When Vin is positive, a large base current flows and transistor saturates.
In the saturation region, both the junctions of transistor are forward biased. The collector current is very large, the voltage drop across the transistor (VCE) is very small, of the order of 0.2V to 1 V, depending on the type of transistor. Thus in saturation region, the transistor is equivalent to a closed switch.

	f)	**Define α and β . Derive relation bet. α and β .**	**4 M**
		1) α It is defined as the ratio of collector current (IC) to emitter current (IE). $\alpha = \frac{I_C}{I_E}$ **2)β** It is defined as the ratio of collector current (IC) to base current (IB). $\beta = \frac{I_C}{I_B}$	**(Each definition 1 M Proper step wise relation derivation – 2mks**

Relation between α and β:

Current gain of transistor in CB configuration is ,

$$\alpha = \frac{I_C}{I_E}$$

But $I_E = I_B + I_C$

$$\alpha = \frac{I_C}{I_B + I_C}$$

Dividing numerator and denominator by I_B,

$$\alpha = \frac{\frac{I_C}{I_B}}{1 + \frac{I_C}{I_B}}$$

But $\beta = \frac{I_C}{I_B}$ the current gain of transistor in CE configuration.

Therefore,

$$\boldsymbol{\alpha = \frac{\beta}{1 + \beta}}$$

OR

Current gain of transistor in CE configuration is ,

$$\beta = \frac{I_C}{I_B}$$

But $I_E = I_B + I_C$, so $I_B = I_E - I_C$

$$\beta = \frac{I_C}{I_E - I_C}$$

Dividing numerator and denominator by I_E,

$$\beta = \frac{\frac{I_C}{I_E}}{1 - \frac{I_C}{I_E}}$$

But $\alpha = \frac{I_C}{I_E}$ the current gain of transistor in CE configuratior

Therefore,

$$\boldsymbol{\beta = \frac{\alpha}{1 - \alpha}}$$