Important Instructions to examiners:

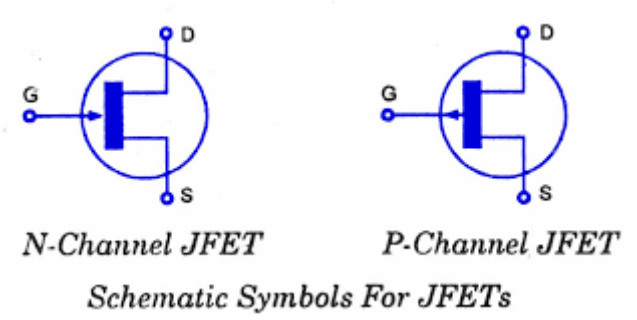
1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the Figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any Equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant Values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1 A) Attempt any six: **12M**

i) Draw the neat symbol of N-channel and P-channel FET

Ans: **1M each**

Symbol of N-channel and P-channel FET



N-Channel JFET *P-Channel JFET*

Schematic Symbols For JFETs

ii) Define intrinsic standoff ratio for UJT.

Ans: **Definition 1 M, Equation 1 M**

Intrinsic standoff ratio: It is defined as the ratio of the RB1 (base resistance 1) and the inter-base resistance (RBB).

$\eta = RB1/(RB1 + RB2)$

$\eta = RB1/(RBB)$

iii) List the Types of amplifier coupling.

Ans: **2M**

Types of amplifier coupling:

a) RC Coupling
b) Transformer Coupling

c) Direct Coupling

iv) Which type of MOSFET is called "Normally ON MOSFET"? Why?

Ans: **Type 1M, Reason 1M**

Depletion-mode MOSFET is normally ON MOSFET because it is ON at zero gate–source voltage (V_{GS}).

Whereas Enhancement-mode MOSFETs are off at zero gate–source voltage (V_{GS}), and it can be turned on by pulling the gate voltage either higher than the source voltage for NMOS or lower than the source voltage for PMOS.

v) Define operating principle of tuned circuit.

Ans: **2M**

Operating principle of tuned circuit:

A parallel tuned circuit consists of a capacitor C and inductor L in parallel. If an alternating voltage is applied across this parallel circuit, the frequency of oscillations will be that of the applied voltage. However, if the frequency of applied voltage is equal to the natural or resonant frequency of LC circuit, then electrical resonance will occur. Under such conditions, the impedance of the tuned circuit becomes maximum and the line current is minimum.

vi) State maximum efficiency of class-A power amplifier.

Ans: **2M**

The maximum efficiency of class-A power amplifier is 25%

OR

The maximum possible value of collector efficiency of a class A amplifiers 50%.

vii) Compare amplifier and oscillator on:

i) Type of feedback used

ii) Input signal

Ans: **1M each**

Comparison between amplifier and oscillator:

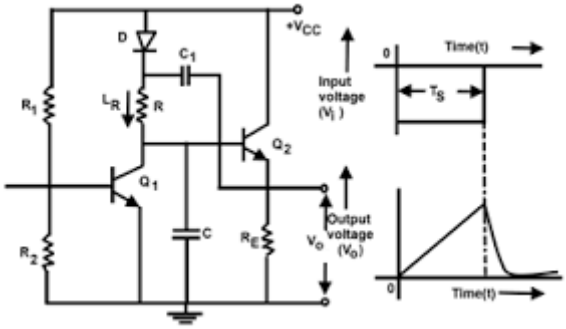
Parameter	Amplifier	Oscillator
Type of feedback used	Negative feedback	Positive feedback
Input signal	Sinusoidal wave	No input signal required

viii) Draw neat circuit of bootstrap time base generator.

Ans: **Diagram 2M, waveform optional**

Circuit diagram of bootstrap time base generator:

Input



B) Attempt any two: 8M

i) Compare CB,CE and CC on the basis of

i) Input resistance(Ri)
ii) Output resistance(Ro)
iii) Current gain(Ai)
iv) Voltage gain(Av)

Ans: 1M each point

NOTE: the value can be different for the defined parameters according to reference book

Comparison between CB,CE,CC

Parameters	CB	CE	CC
Input resistance(Ri)	Low (50 Ohm)	Moderate (1 KOhm)	High (300 KOhm)
Output resistance(Ro)	High (1 M Ohm)	Moderate (50 K)	Low (300 Ohm)
Current gain(Ai)	Less than Unity	High	High
Voltage gain(Av)	High, Same as CE	High	Less than Unity

ii) Describe the concept of thermal runaway. How it can be avoided?

Ans: Thermal runaway – 2 M, how it is avoided – 2 M

Concept of thermal runaway:

1. The reverse saturation current in semiconductor devices changes with temperature. The reverse saturation current approximately doubles for every 100 c rise in temperature.

2. As the leakage current of transistor increases, collector current (Ic) increases

3. The increase in power dissipation at collector base junction.

4. This in turn increases the collector base junction causing the collector current to further increase.

5. This process becomes cumulative. & it is possible that the ratings of the transistor are exceeded. If it happens, the device gets burnt out. This process is known as 'Thermal Runaway'.

Thermal runaway can be avoided by :

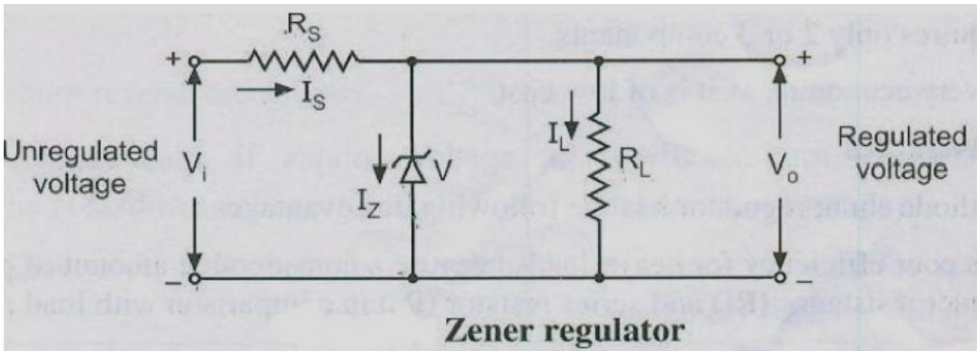
1) Using stabilization circuitry

2) Heat sink

iii) Draw circuit of Zener diode as a voltage regulator and explain its working with neat V-I characteristics.

Ans: **Diagram: 2M, Working:2M**

Circuit of Zener diode as voltage regulator: **2M**



Working: **2M**

- For proper operation, the input voltage Vi must be greater than the Zener voltage Vz. This ensures that the Zener diode operates in the reverse breakdown condition. The unregulated input voltage Vi is applied to the Zener diode.
- Suppose this input voltage exceeds the Zener voltage. This voltage operates the Zener diode in reverse breakdown region and maintains a constant voltage, i.e. Vz = Vo across the load inspite of input AC voltage fluctuations or load current variations. The input current is given by,
- I_S = Vi – Vz / Rs = Vi – Vo / Rs
- We know that the input current IS the sum of Zener current Iz and load current IL.

- ***Therefore, IS = Iz + IL***
- ***or Iz = Is - IL***
- As the load current increase, the Zener current decreases so that the input current remains constant. According to Kirchhoff's voltage law, the output voltage is given by,

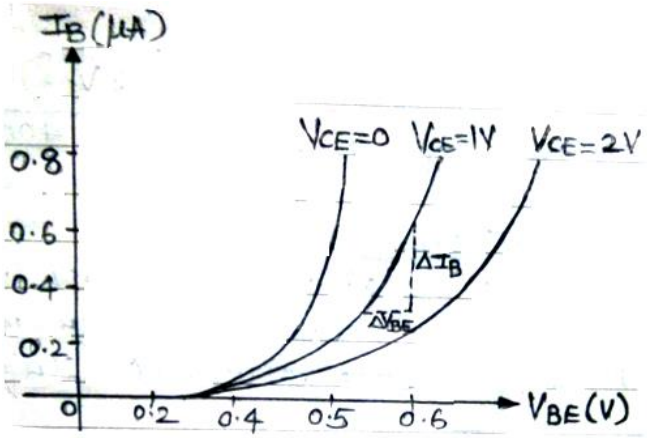
- ***Vo = Vi – Is. Rs***
- As the input current is constant, the output voltage remains constant (i.e. unaltered or unchanged). The reverse would be true, if the load current decreases. This circuit is also correct for the changes in input voltage.
- As the input voltage increases, more Zener current will flow through the Zener diode. This increases the input voltage Is, and also the voltage drop across the resistor Rs, but the load voltage Vo would remain constant. The reverse would be true, if the decrease in input voltage is not below Zener voltage.
- Thus, a Zener diode acts as a voltage regulator and the fixed voltage is maintained across the load resistor RL.

Q2 Attempt any four:- **16M**

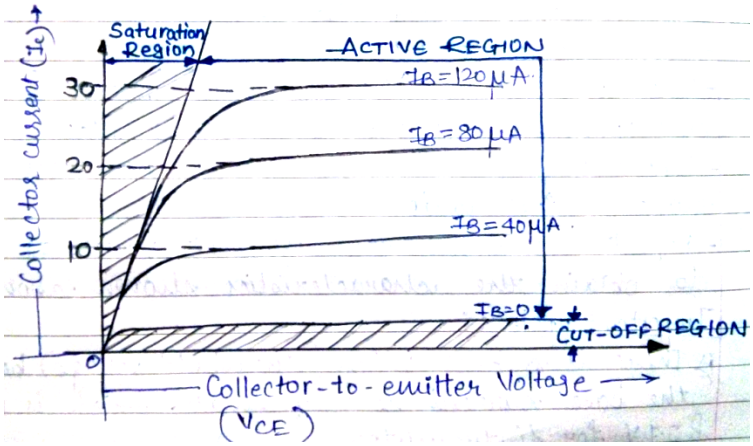
A) Draw labelled input and output characteristic of BJT in CE configuration

Ans:- **Input characteristics : 2M, output characteristics: 2M**

Input characteristics:



Output characteristics:



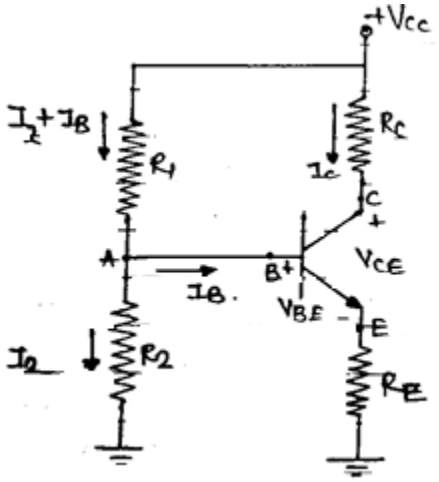
B) List the type of biasing of transistor. Draw neat circuit diagram of voltage divider bias.

Ans:- **Types of biasing : 2M, voltage divider bias diagram 2M**

Types of biasing of transistors:

1. Base bias or fixed bias
2. Base bias with emitter feedback.
3. Voltage divider bias
4. Emitter bias

Voltage divider bias:

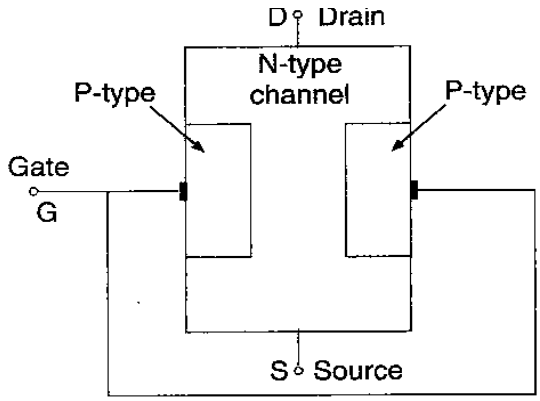


C) With the help of neat construction of JFET, explain its working principle

Ans:- Construction 2 Marks, Working principle 2 Marks

NOTE: N-channel as well as P-channel is acceptable

CONSTRUCTION OF N-CHANNEL JFET:

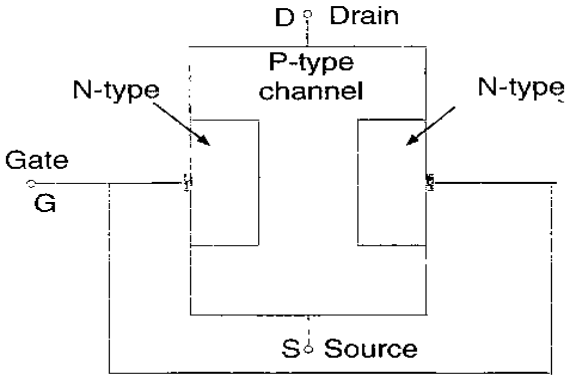


(*a*) N-channel.

It consists of an N-type semiconductor bar with two P type heavily doped regions diffused on opposite sides of its middle part. P-type regions from two PN junctions. The space between the junctions (i.e. N-type regions) is called a channel. Both the P-type regions are connected internally & a single wire is taken out in the form of a terminal called the gate (G). The electrical connections called ohmic contacts are made to both ends of the N type semiconductor & are taken out in the form of two terminals called drain (D) & source (S).

OR

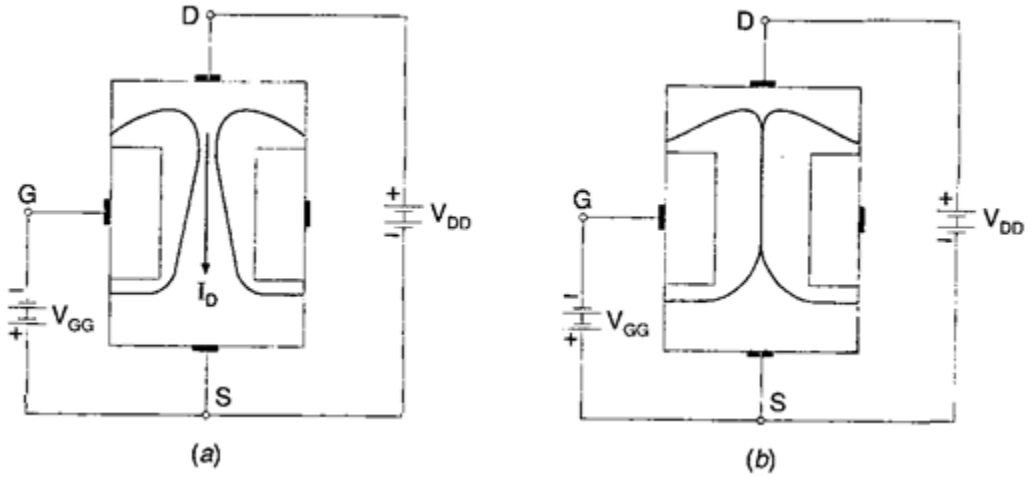
CONSTRUCTION OF P-CHANNEL JFET:



(*b*) P-channel.

A P-channel JFET is shown in above figure. Its construction is similar to that of N-channel JFET, except that it consists of P-channel & N-type regions. The current carriers in P-channel JFET are holes which flow through P type channel.

Working principle:



- The application of negative gate voltage or positive drain voltage with respect to source, reverse biases the gate- source junction of an N-channel JFET. The effect of reverse bias voltage is to form depletion regions within the channel.
- When a voltage is applied between the drain & source with dc supply voltage (V_{DD}), the electrons flows from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current (I_D) & its conventional direction is from drain to source. The value of drain current is maximum, when no external voltage is applied between the gate & source & is designated by the symbol I_{DSS}.
- When V_{GG} is increased, the reverse bias voltage across gate-source junction is increased. As a result of this depletion regions are widened. This reduces the effective width of the channel & therefore controls the flow of drain current through the channel.
- When gate to source voltage (V_{GG}) is increased further, a stage is reached at which two depletion regions touch each other as shown in fig (b).

At this value of V_{GG} channel is completely blocked or pinched off & drain current is reduced to zero. The value of V_{GS} at which drain current becomes zero is called pinch off voltage designated by the symbol V_P or $V_{GS(OFF)}$. The value of V_P is negative for N-channel JFET.

D) Define: α and β related to transistor . Describe relation between them

Ans:- **Define α: 1M, Define β: 1M, relation : 2M**

α :

It is current gain in common base configuration. It is defined as the ratio of collector current to emitter current.

$$\alpha = \frac{I_C}{I_E}$$

β:

IT is current gain in common emitter configuration. It is defined as the ratio of collector current to base current.

$$\beta = \frac{I_C}{I_B}$$

Relation between α& β:

Current gain (**α**) of CB configuration = $\frac{I_C}{I_E}$

Current gain of (**β)** of CE configuration = $\frac{I_C}{I_B}$

We know that

$I_E = I_B + I_C$……..(1)

Dividing equation (1) by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

Therefore $\frac{1}{\alpha} = \frac{1}{\beta} + 1$ [since $\alpha = \frac{I_C}{I_E}$, $\beta = \frac{I_C}{I_B}$]

Therefore $\frac{1}{\alpha} = \frac{1+\beta}{1+\beta}$

$\alpha (1 + \beta) = \beta$

$\alpha + \alpha \beta = \beta$

$\alpha = \beta - \alpha \beta$

$\alpha = \beta(1 - \alpha)$

Therefore $\beta = \frac{\alpha}{1-\alpha}$

E) List the types of feedback connection. Draw block diagram representation of them (anyone)

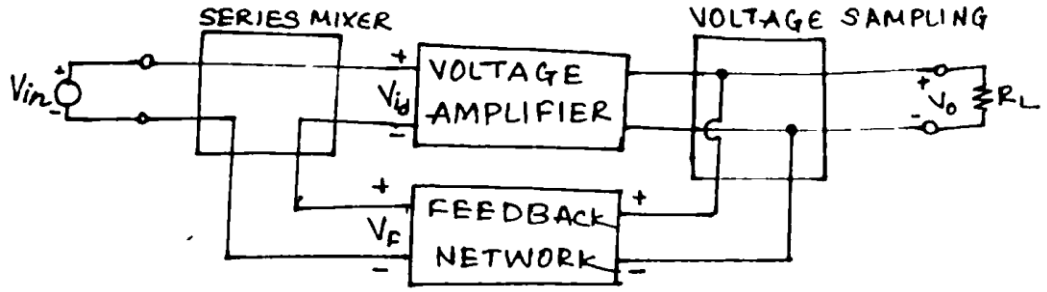
Ans:- **Types: 2Marks, diagram any one: 2Marks**

Types of feedback connection:

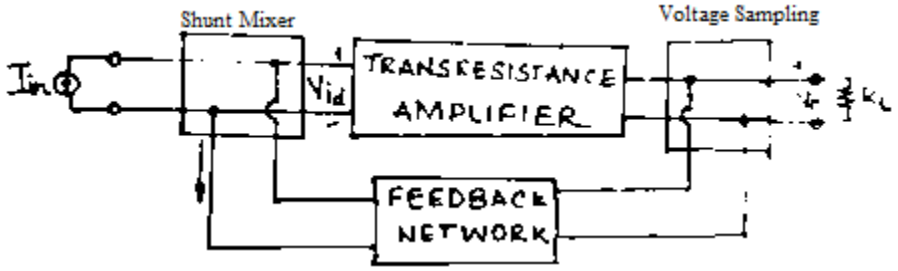
1. Voltage series
2. Voltage shunt
3. Current series
4. Current shunt

Block diagram :- (any one)

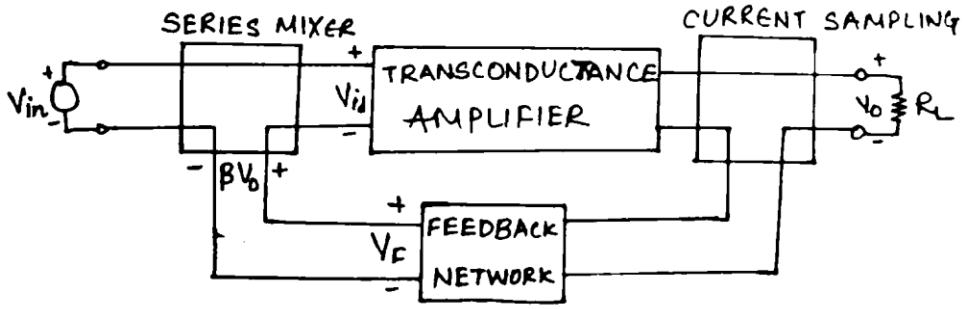
VOLTAGE SERIES NEGATIVE FEEDBACK:-



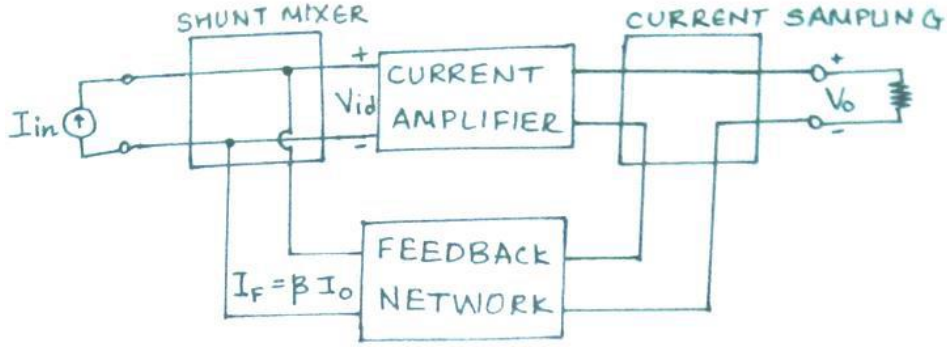
VOLTAGE SHUNT NEGATIVE FEEDBACK:-



CURRENT SERIES NEGATIVE FEEDBACK:-



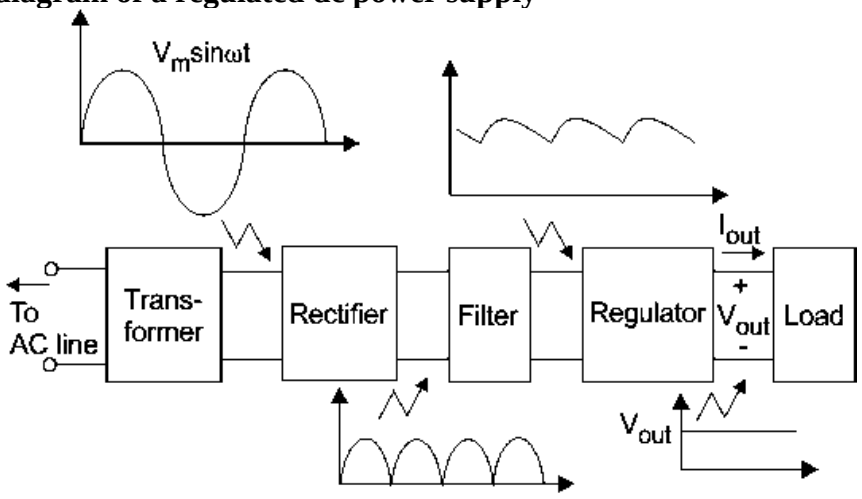
CURRENT SHUNT NEGATIVE FEEDBACK:-



F) Draw block diagram of DC regulated power supply and explain function of each block with waveform.

Ans:- **Block diagram 1M, waveforms for each block 1M, Explanation 2M**

Functional block diagram of a regulated dc power supply



Components of typical linear power supply

1. A step down transformer
2. A rectifier
3. A DC filter
4. A regulator

Operation of Regulated Power Supply:-

Step Down Transformer:-

A step down transformer will step down the voltage from the ac mains to the required voltage level. The turn's ratio of the transformer is so adjusted such as to obtain the required voltage value. The output of the transformer is given as an input to the rectifier circuit.

Rectification:-

Rectifier is an electronic circuit consisting of diodes which carries out the rectification process. Rectification is the process of converting an alternating voltage or current into corresponding direct (dc) quantity. The input to a rectifier is ac whereas its output is unidirectional pulsating dc. Usually a full wave rectifier or a bridge rectifier is used to rectify both the half cycles of the ac supply (full wave rectification)

DC Filter :-

The rectified voltage from the rectifier is a pulsating dc voltage having very high ripple content. But this is not we want, we want a pure ripple free dc waveform. Hence a filter is used. Different types of filters are used such as capacitor filter, LC filter, Choke input filter, π type filter.

Regulator:

This is the last block in a regulated DC power supply. The output voltage or current will change or fluctuate when there is change in the input from ac mains or due to change in load current at the output of the regulated power supply or due to other factors like temperature changes. This problem can be eliminated by using a regulator. A regulator will maintain the output constant even when changes at

the input or any other changes occur. Transistor series regulator, Fixed and variable IC regulators or a zener diode operated in the zener region can be used depending on their applications. IC's like 78XX and 79XX are used to obtained fixed values of voltages at the output. With IC's like LM 317 and 723 etc we can adjust the output voltage to a required constant value.

Q 3Attempt any four :- **16M**

A) Explain working of transistor as a switch with waveform.

Ans:- **Explain 3 M, waveforms 1M**

- The switch operates between two states namely saturation and cut-off state.
- The saturation state occurs when both the junctions(i.e. emitter-base junction and collector-base junction) of transistor are forward biased.
- The cut off state occurs when both the junctions of transistors are reverse biased.

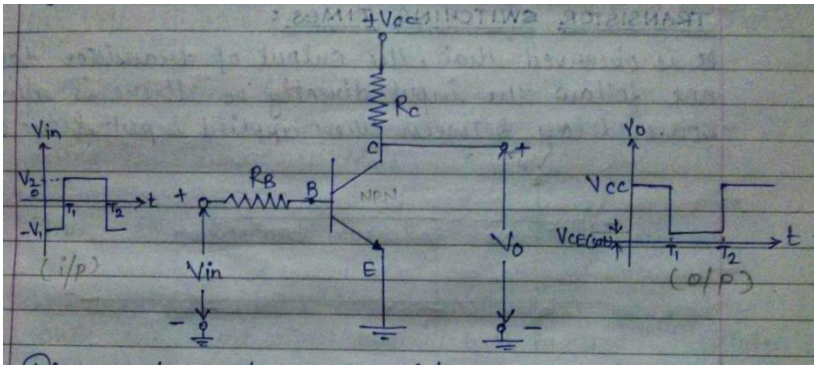


Figure above shows transistor as a switch with input and output waveforms.

- A input (V_{in}) is applied at the base of the transistor. At time T_1, the input voltage (V_{in})is equal to'-V_1' and emitter-base junction is reverse biased.∴ the transistor is in cut-off and hence practically no current exists in the circuit.
- $\therefore I_B = 0, I_C = \beta . I_B = 0$
  Apply KVL to output loop

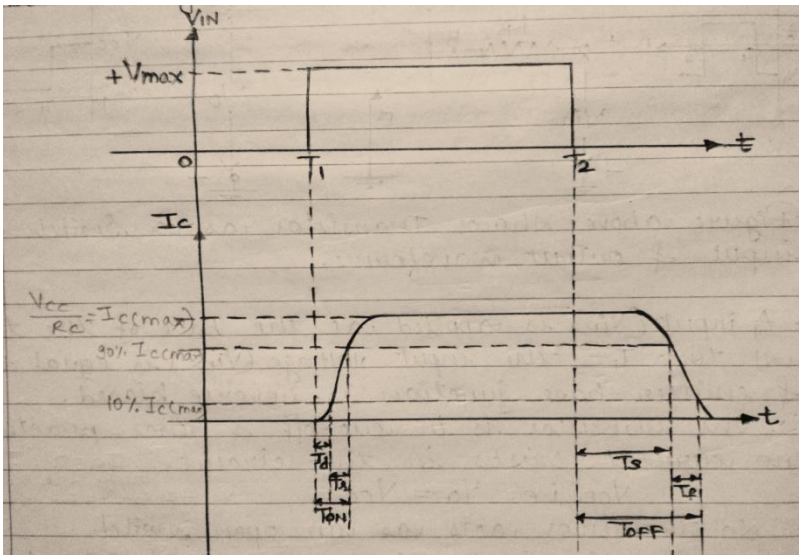
$$\therefore V_{CC} - I_C R_C - V_O = 0$$
$$\therefore V_{CC} = V_O \ldots\ldots (AS I_C R_C = 0)$$
$$\therefore V_{CC} = V_{CE} = V_O$$

- So transistor acts as an open switch.
- For the time interval $T_1 < t < T_2$, the input voltage is equal to V_2, both the emitter base and collector base junctions are forward biased and the transistor is in saturation.
- The output voltage $V_0 = V_{CE\,(sat)} = 0.2V$ for silicon and collector current is maximum $I_C = \frac{V_{CC}}{R_{CC}}$.
- So transistor acts as a closed switch.
- By applying KVL to output loop:

$$V_{CC} - I_C R_C - V_O = 0$$
$$V_O = V_{CC} - I_C R_C$$

As I_C is maximum, $I_C R_C$ is also maximum.
∴V_O is negligible i.e.$V_{CE(sat)}$.

Waveform:-



NOTE:-Waveform with DC load line showing cutoff and saturation region is also accepted.

B) Compare BJT and FET (any 4 point)

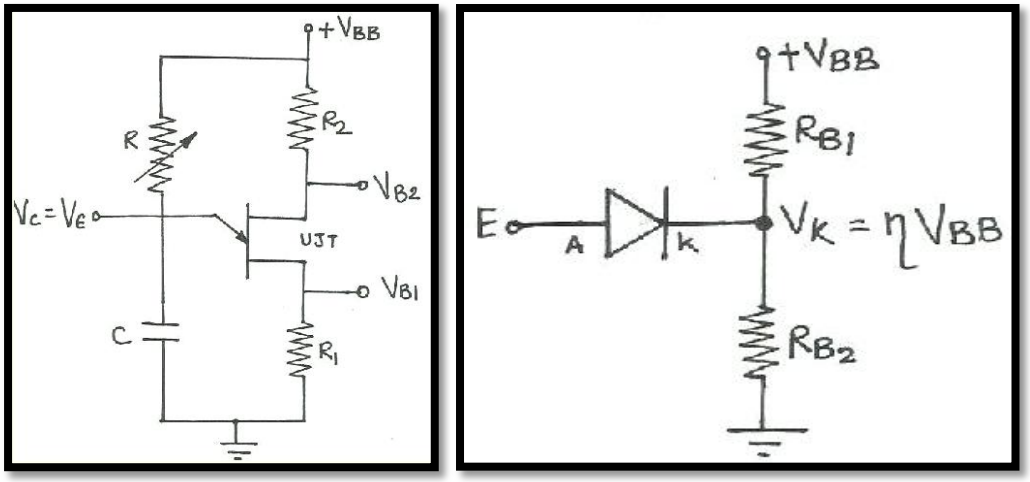
Ans:- **1Mark each point. Consider any four points**

SR. NO.	FET	BJT
1	It is unipolar device i.e. current in the device is carried either by electrons or holes	It is bipolar device i.e. current in the device is carried either by both electrons & holes
2	It is a voltage controlled device i.e. voltage at the gate (or drain) terminal controls amount of current flowing through the device.	It is a current controlled device i.e. the base current controls the amount of collector current.
3	Its input resistance is very high & is of order of several megaohms.	Its input resistance is very low compared to FET.
4	It has a negative temperature co-efficient at high current levels. It means that current decreases as temperature increases.	It has a positive temperature co-efficient at high current levels. It means that current increases as temperature increases.
5	It is less noisy.	It is comparatively more noisy.
6	It has relatively lower gain bandwidth product as compared to BJT.	It has relatively higher gain bandwidth product as compared to FET.
7	It is simpler to fabricate as IC & occupies less space on chip compared to BJT.	It is comparatively difficult to fabricate on IC & occupies more space on chip compared to FET.
8	It is relatively immune to radiation.	It is susceptible to radiation
9	It does not suffer from minority- carrier storage effects & therefore has higher switching speeds & cut-off frequencies.	It suffers from minority- carrier storage effects & therefore has lower switching speeds & cut-off frequencies.

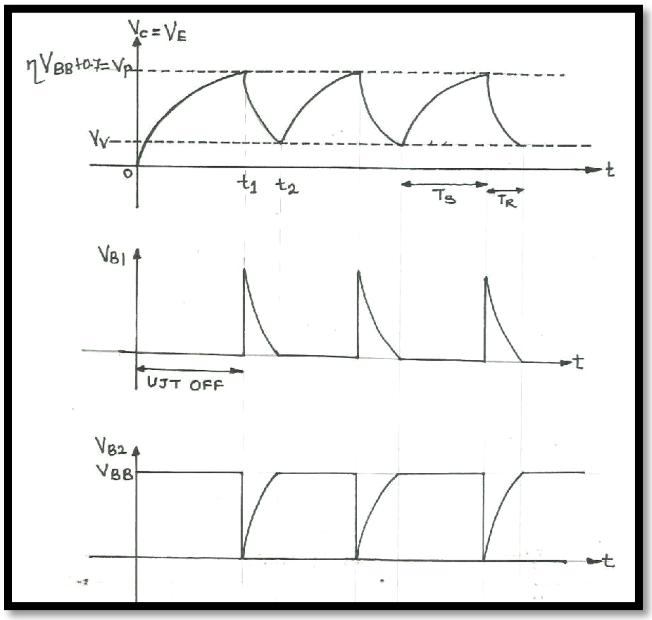
C) Describe working of UJT relaxation oscillator with circuit and waveform.
Ans:- **Circuit diagram 1M, Explanation 2Marks, Waveforms 1M**

UJT RELAXATION OSCILLATOR:

Circuit diagram:



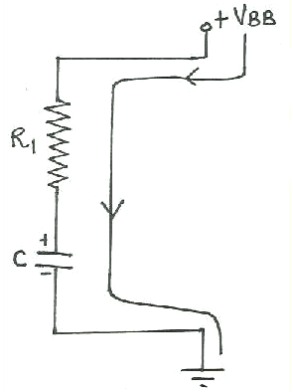
WAVEFORMS:-:



At t = 0:

- Supply voltage + V_{BB} is given the circuit then $V_C = V_E = V_A = 0$ Volts
- By internal potential divider voltage at cathode is
- $V_K = + \eta V_{BB.}$
- If V_A (V_E) < V_K, then internal PN junction (diode) is reverse biased.
- Therefore, it acts as open switch and UJT is OFF.

At, t >0 :



- Current flows from + V_{BB} to ground through resistor R1 and capacitor C. Thus capacitor starts charging exponentially as constant voltage source + V_{BB} is applied.
- Hence in waveform from t = 0, and t > 0, $V_C = V_E$ increasing exponentially.
- Therefore no current flows through UJT.
- $\therefore V_{R1} = I.R1 = 0$

$\therefore V_{B1} = 0.$

At t > 0,

- $V_{B2} = V_{BB} - V_{R2}$
- $\therefore V_{B2} = V_{BB}$ ----- (Since $V_{R2} = I.R2 = 0$ as I = 0)

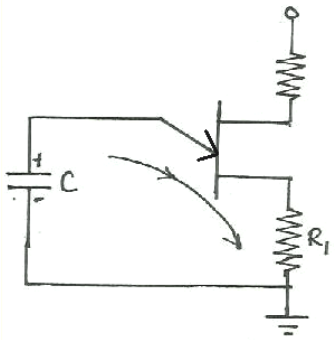
At $t = t_1$:

- Increasing voltage across capacitor is now become $V_C = (\eta V_{BB} + 0.7)$ Volts. Which is equal to anode voltage from equivalent circuit.

$\therefore V_C = V_E = V_A = (\eta V_{BB} + 0.7)$ Volts.

- As $V_A > V_K$ internal PN junction (diode) is forward biased hence it acts as a closed switch, and UJT is ON i.e. UJT starts conducting.
- $V_{B1} = V_{R1}$ = maximum and $V_{B2} = V_{BB} - V_{R2} = 0$

At $t > t_1$:



- Charged capacitor finds path for discharging. Charged capacitor discharges exponentially through ON UJT & resistor R1. i.e. V_c decreases.
- As $V_{B1} = V_c$, therefore V_{B1} also starts decreasing exponentially.

At $t = t_2$:

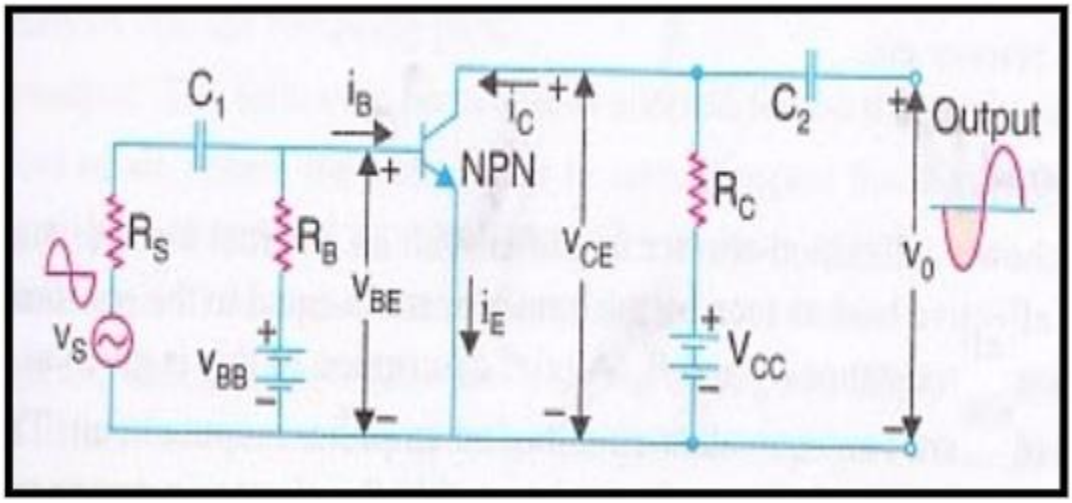
- Decreasing capacitor voltage reached to a point where $V_A = V_k$ (as $V_C = V_E = V_A$)
- $\therefore$ Again internal PN junction (diode) reverse biases.

- Therefore UJT is OFF & no current flows through it.
- Therefore all the waveforms continuously repeat themselves.

D) Draw circuit diagram of single stage CE amplifier with Input and Output waveform.

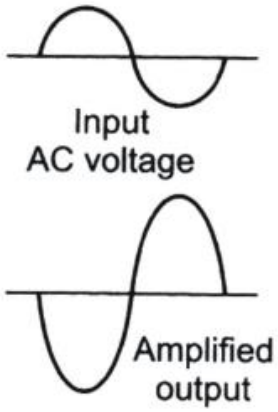
Ans:- circuit diagram 2Marks, input waveform 1M, output waveform 1M

CIRCUIT DIAGRAM:



NOTE: -Circuit diagram with voltage divider bias is also accepted

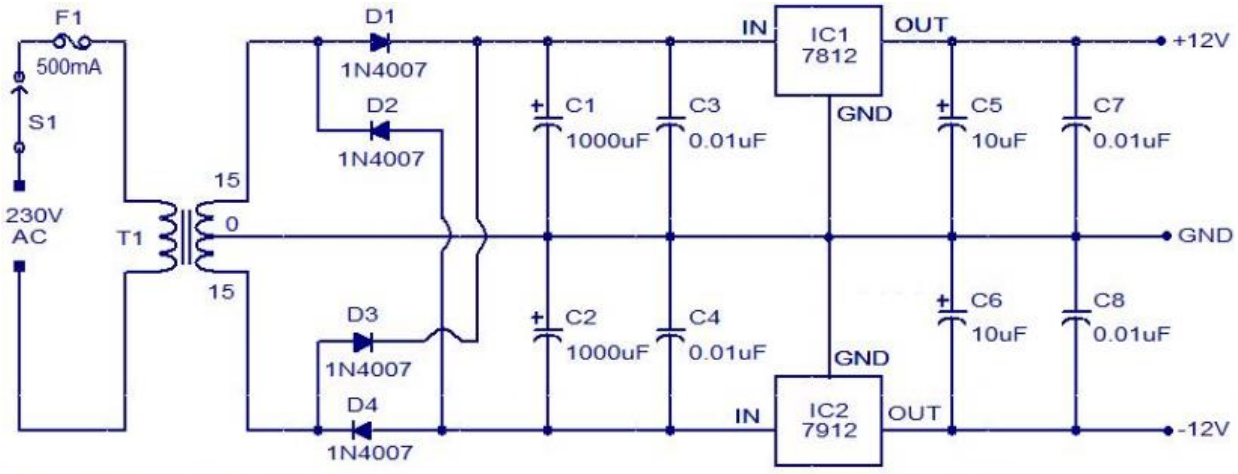
Waveform:-



E) Draw circuit diagram of DC regulated power supply for ± 12Vusing IC 78XX and 79XX.

Ans:- Diagram 4M

Note: Values of capacitor & diode are not compulsory.



F) Define:-

i) Load regulation

ii) Line regulation

Ans:- **Each definition 2Marks**

i) LOAD REGULATION:

The ratio of change in per unit DC output voltage when load current changes from No load to Rated full load to the DC output voltage at full load. It is mathematically expressed as,

$$LOADREGULATION = \frac{V_{NL} - V_{FL}}{\Delta I_L}$$

Where,
VNL=Voltage at no load
VFL=voltage at full load
IL=Load current

ii) LINE REGULATION:

The change in output voltage with respect to per unit change in input voltage is defined as LINE REGULATION. It is mathematically expressed as,

$$LINEREGULATION = \frac{\Delta V_L}{\Delta V_S}$$

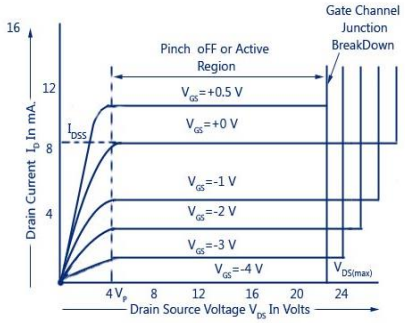
Where,
ΔV_L The change in output voltage

ΔVs =The change in input voltage

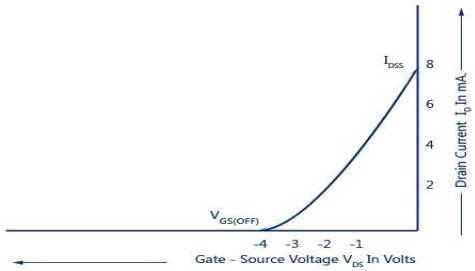
Q4 Attempt any four: **16M**

A. Draw labeled drain and transfer characteristics of JFET .

Ans: **2M each**



Drain characteristics of JFET

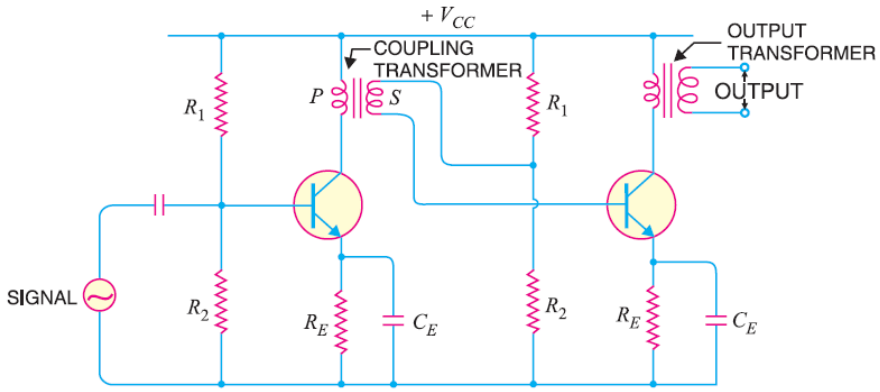


Transfer characteristics of JFET

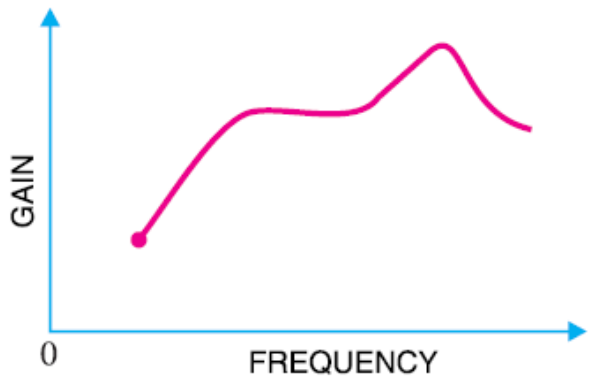
B. Draw circuit of transformer coupled transistor amplifier and also draw it's frequency response.

Ans: **Diagram:3M,Frequency response:1M**

Diagram:

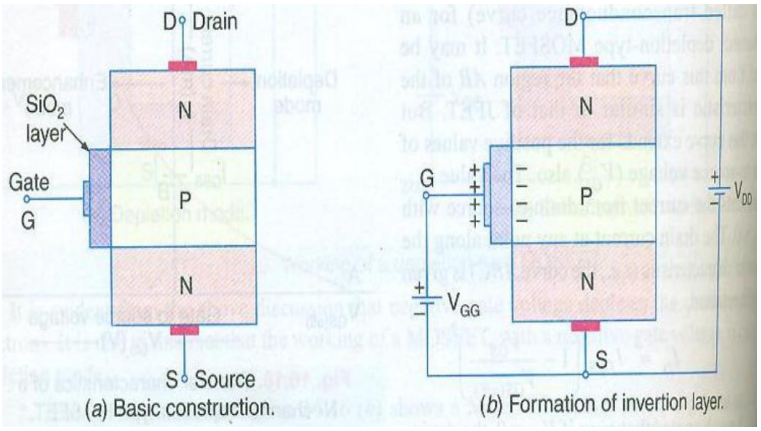


Frequency response:



C. Explain the working of enhancement type MOSFET with neat construction.

Ans: **Diagram: 2M, Working:2M**

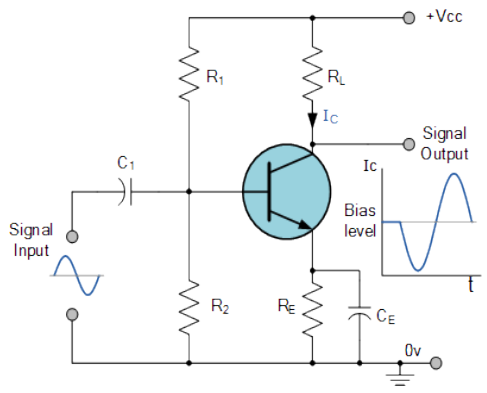


Working:

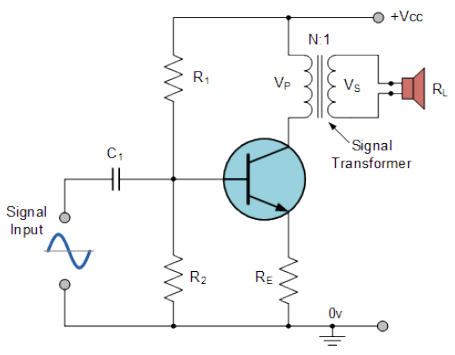
- The enhancement type MOSFET has no depletion mode and it operates only in enhancement mode.
- It has no physical channel as it is present in DMOSFET.
- MOSFET is always operated with the positive gate to source voltage. When the gate to source voltage is zero, the VDD supply tries to force free electrons from source to drain. But the presence of P- region does not permit the electrons to pass through it. Thus there is no drain current for VGS= 0. Due to this fact, the enhancement type MOSFET is also called normally OFF MOSFET.
- When some positive voltage is applied at the gate, it induces a negative charge in the P- type substrate just adjacent to the silicon dioxide layer. The induced negative charge is produced by attracting the free electrons from the source. When the gate is positive enough, it can attract a number of free electrons. This form a thin layer of electrons, which stretches from source to drain, this effect, is equivalent to producing a thin layer of N- type channel in the P- type substrate. This layer of free electrons is called N- type inversion layer.
- The minimum gate to source voltage which produces inversion layer is called threshold voltage.

D. Draw the diagram of class-A power amplifier and explain its working.

Ans : **Circuit of class-A power amplifier:2M, Working:2M**



OR



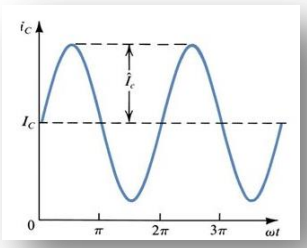
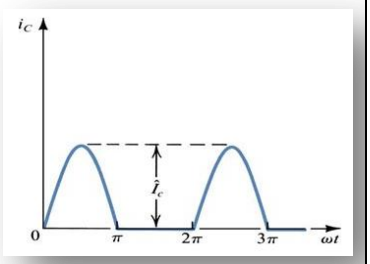
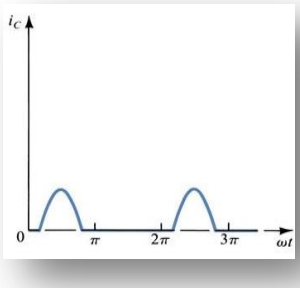
Working:

- The most commonly used type of power amplifier configuration is the **Class-A Amplifier**. The Class A amplifier is the most common and simplest form of power amplifier that uses the switching transistor in the standard common emitter circuit configuration.
- The transistor is always biased "ON" so that it conducts during one complete cycle of the input signal waveform producing minimum distortion and maximum amplitude to the output.
- The main function of the power amplifier, which are also known as a "large signal amplifier" is to deliver power, which is the product of voltage and current to the load.
- Basically a power amplifier is also a voltage amplifier but the difference being that the load resistance connected to the output is relatively low, for example a loudspeaker of 4 or 8Ωs resulting in high currents flowing through the collector of the transistor.
- Hence an amplifier is required to drive such large resistive loads such as a loudspeaker or to drive a motor in a robot and for these types of applications where high switching currents are needed Power Amplifiers are required.
- The Class A amplifier has overall conversion efficiency is very low due to large collector currents means a considerable amount of power is lost in the form of heat.

E. Compare class A, class B and class C power amplifier on the basis of

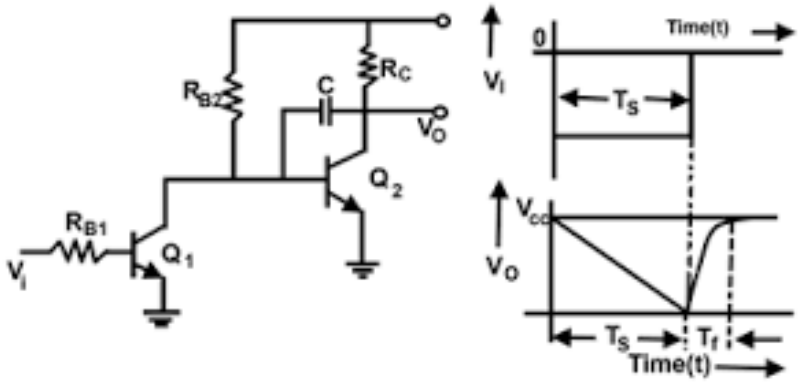
i) Operating point
ii) Efficiency
iii) Conduction angle
iv) O/p waveforms

Ans: **1M each point**

Parameters	**Class-A**	**Class-B**	**Class-C**
Operating point	Centre of DC load line	On the X-axis(in cut –off region)	Below X-axis(below cut-off region)
Efficiency	Lowest 25% to 50%	Higher (78.5%)	Very high 95%
Conduction angle	360^0 or full cycle	180^0 or half cycle	Less than 180^0
Output waveform			

F. Draw circuit and waveforms of Miller sweep generator. List two application of it.

Ans: Diagram :2M, Waveform: 1M, Application : 1M



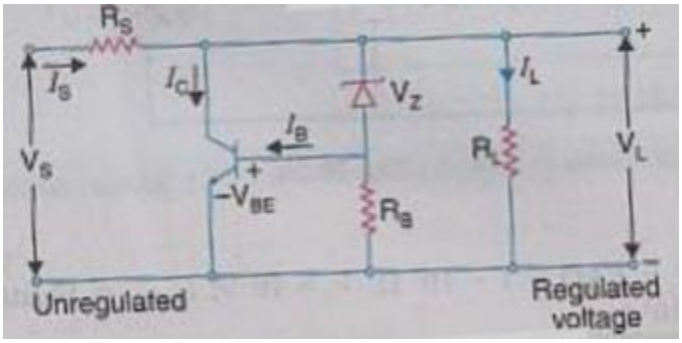
Applications of Miller Sweep Generator: (any two)

1. Applications where linear output is expected.
2. Television (TV)
3. CRO
4. To convert step waveform into ramp waveform.

Q5.Attempt any four: 16M

A) Draw circuit of transistorized shunt voltage regulator and explain its working.

Ans: Circuit Diagram : 2M , Working : 2 M



Explanation:-

From the above circuit the load voltage is given by

$V_L = V_Z + V_{BE}$ Or $V_{BE} = V_L - V_Z$ …… (i)

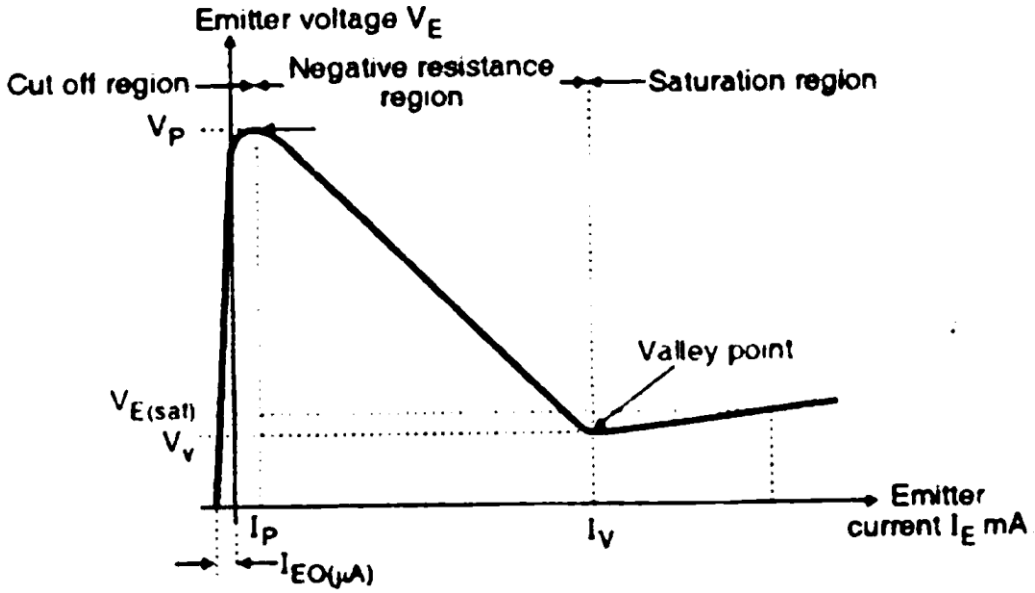
Since the load voltage for a given zener diode is fixed, therefore any decrease or increase in load voltage will have a corresponding effect on the base to emitter voltage V_{BE}.

The unregulated input voltage increases, load voltage also increases. As a result of this from equation (i) above, we find that V_{BE} is also increases. And the base current $I_B$increases. Due to this the collector current I_C also increases. This causes the input current (I_S) to increase, which in turn increases the voltage drop across series resistance (V_{RS}) . Consequently, the load voltage decreases.

If the output voltage decreases then V_{BE} will decrease. This will reduce the collector current Ic. So more current will flow through the load and the load voltage will increase. This increase in load voltage will compensate the initial decrease in load voltage. Thus output voltage gets regulated.

B) Draw VI characteristics of UJT and label it.

Ans: **VI characteristics: 2M , labeling : 2M**



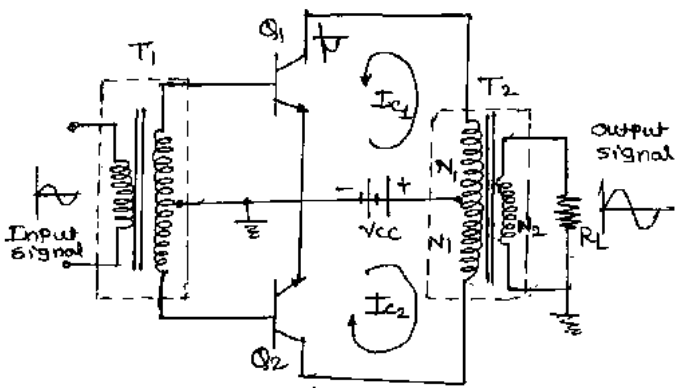
C) Explain operation of Class B push pull amplifier with circuit diagram.

Ans: **Circuit diagram : 2M , Working : 2M**

In class B amplifier transistor conducts only for half cycle of input signal. This type of output signal gives large distortion.

- In order to avoid this we use two transistors connected in push-pull arrangement. One conducts in positive half cycle and other conducts in negative half cycle.
- Transistor T1 is called as input transformer and is called phase splitter and produces two signals which are 1800 out of phase with each other.
- Transistor T2 is called output transformer and is required to couple the a.c. output signal from the collector to the load.

Class-B Push-Pull Amplifier

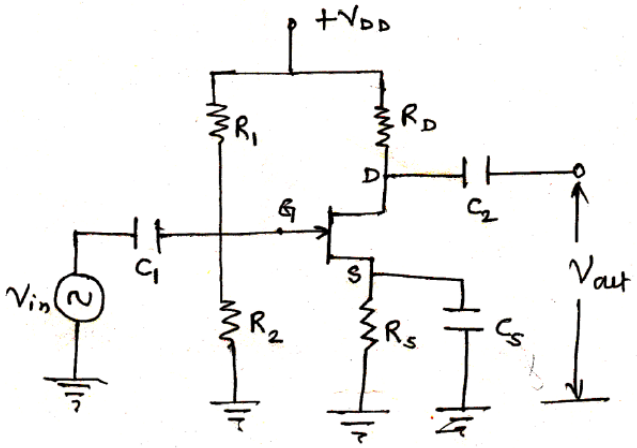


Working:

- When there is no input signal both the transistor Q1 and Q2 are cut-off. Hence no current is drawn from VCC supply. Thus there is no power wasted in standby the power dissipation in both transistor is practically zero.
- During positive half cycle the base of Q1 is positive and Q2 is negative. As a result of this Q1 conduct, while the transistor Q2 is OFF. And at the output half cycle is obtained.
- During negative half cycle, Q1 turns OFF and Q2 conducts, and another half cycle is obtained at the output. At any instant only one transistor in the circuit is conducting. Each transistor handles one half of the input signal.
- Thus at a time only one transistor will conduct. The conductance angle for each transistor is 180 degrees, hence complete sine wave is produced across the load.

D) Draw circuit of common source FET amplifier and explain its working.

Ans: Circuit diagram : 2M , Working Principle : 2M



Common Source FET amplifier

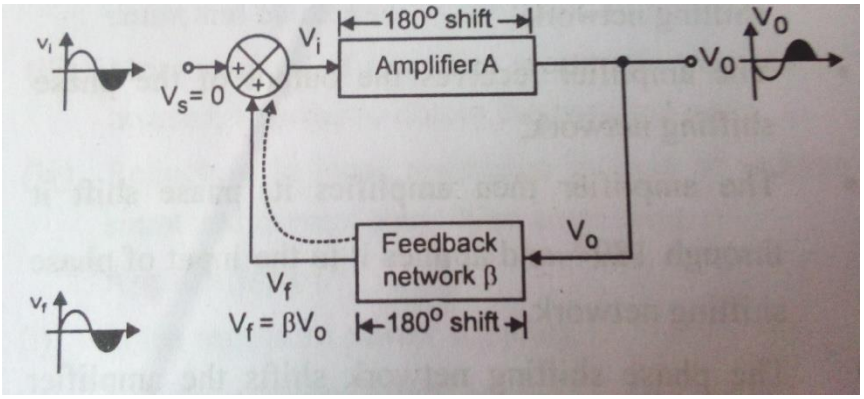
Operation: - When small a.c. signal is applied to the gate, its produces variation in the gate to source voltage. This produces variation in the drain current. As the gate to source voltage increases the current also increases. As the result of this voltage drop across RD also increases. This causes the drain voltage to decreases.
In positive half cycle of the input ac signal the gate to source voltage becomes less negative. This will increase the channel width and increase the level of drain current ID. ThusIDvarysinusoidally above its Q point value.
The drain to source voltage V_{DS} is given by $V_{DS} = V_{DD} - I_D R_D$.
Therefore as I_D increases the voltagedrop $I_D R_D$ will also increase and voltage V_{DS} will decrease.
If ΔI_D is large for a small value of ΔV_{GS} , the ΔV_{DS} will also be large and we get amplification. Thus the AC output voltage V_{DS} is 180º out of phase with AC input voltage.

E) State Barkhausen's criteria required for oscillations. List two applications of oscillator.

Ans: Barkhausen's criteria : 2M , Applications (any four points) : 2M

Oscillator are basically ac signal generators which you use in your laboratories. Oscillators generate alternating voltage of desired shape at desired frequency. Oscillators work on the principle of positive feedback.

Barkhausen's Criteria:



An amplifier will work as an oscillator if and only if it satisfies a set of conditions called Barkhausen's criterion.

It states that:

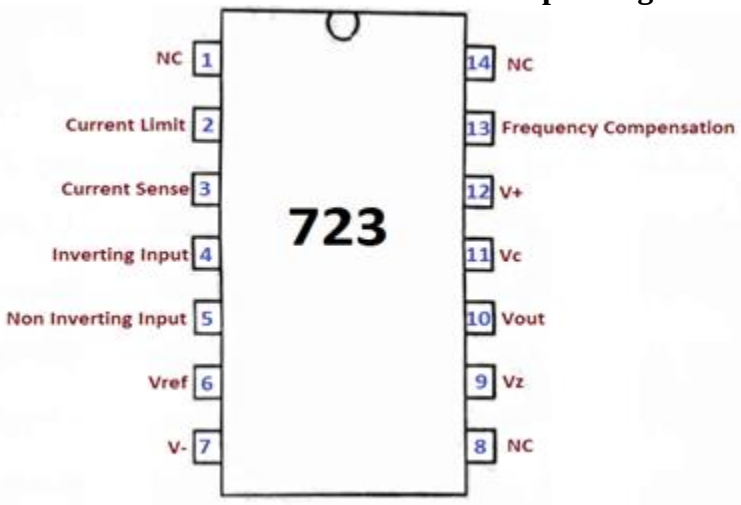
1. An oscillator will operate at that frequency for which the total phase shift around loop equals to 0◦ or 360◦.
2. At the oscillator frequency, the magnitude of the product of open loop gaun of the amplifier A and the feedback factor β is equal or greater than unity.
   ie. $A\beta \geq 1$

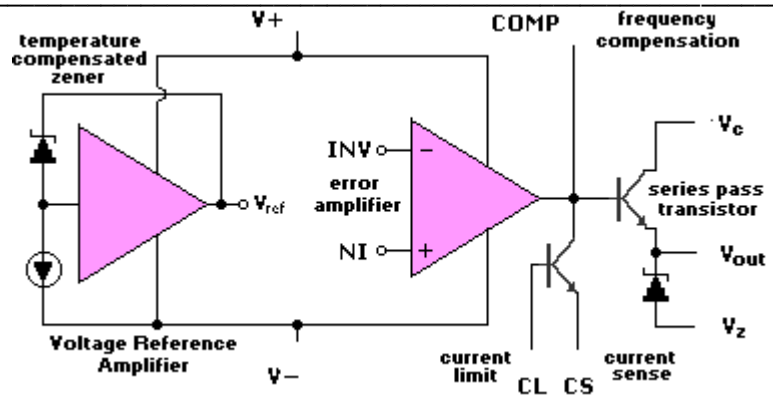
Applications of Oscillator:

1. Low and medium sine wave generators.
2. In the radio and TV transmitters.
3. In frequency synthesizers.
4. In special type of receivers.

F) Draw pin diagram and functional block diagram of IC 723.

Ans: **pin diagram : 2M, block diagram: 2M**



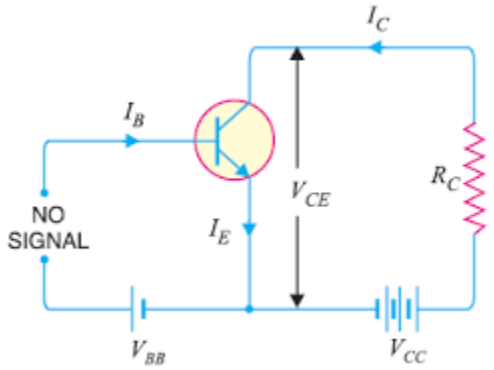


Q6. Attempt any four: **16M**

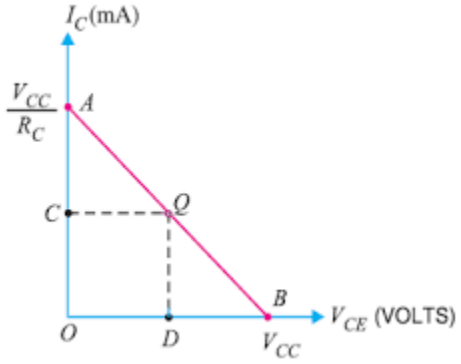
A) Explain concept of DC load line used in BJT.

Ans:

- Q-point is the operating point of the transistor (I_{CQ},V_{CEQ}) at which it is biased. The concept of Q-point is used when transistor act as an amplifying device and hence is operated in active region of input output characteristics. To operate the BJT at a point it is necessary to provide voltages and currents through external sources.
- To draw DC load line of a transistor we need to find the saturation current and cutoff voltage. The saturation current is the maximum possible current through the transistor and occurs at the point where the voltage across the collector is minimum. The cutoff voltage is the maximum possible voltage across the collector and occurs at zero collector current. A common emitter amplifier is shown the figure below:

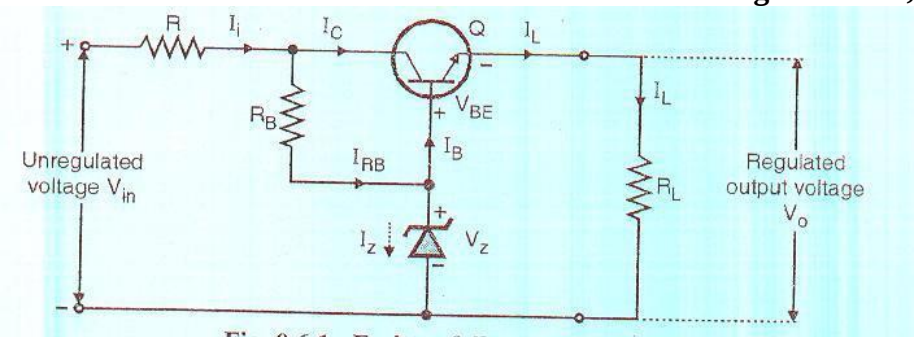


Applying KVL to the collector circuit,
V_{CC}-V_{CE} - I_C.R_C=0
Rearranging this equation we get,
I_C = (-1/R_C).V_{CE}+ (V_{CC}/R_C)
Compare the above equation with equation of a straight line ie.y=mx+c
Substituting V_{CE}=0, we get I_C=V_{CC}/R_C
Substituting I_C=0, we get V_{CE}=V_{CC}
This straight line is called as DC load line.



B) Draw circuit of transistorized series voltage regulator and explain its working.

Ans: Circuit diagram : 2M , Working : 2M



In this circuit transistor Q acts as a control element. This transistor Q is connected in series with the load hence the circuit is called as Series Voltage Regulator. Other components in the circuit are Zener diode (V_Z), and two resistors R & R_B.

Zener diode V_Z is operated in breakdown region and provides constant voltage V_Z.

Resistance R_B provides the limiting current to Zener diode.

The total current in the circuit is decided by resistance R.

As V_Z & V_{BE} of the transistor are constant, output voltage across RL will also be constant. To find output voltage V_O,

Applying KVL to o/p loop of the circuit

$V_{BE} + I_L R_L - V_Z = 0$

Therefore, $V_O = I_L R_L = V_Z - V_{BE}$

$V_O = V_Z - V_{BE}$

If output voltage increases then V_{BE} decreases. Due to reduction in $V_{BE,}$ I_B decreases ,and I_C decreases.

This will increase the collector to emitter voltage across the transistor and V_O will be regulated this is because

V_O=Vin - V_{CE} .

If the output voltage decreases, then exactly opposite action will take place and the output voltage is regulated

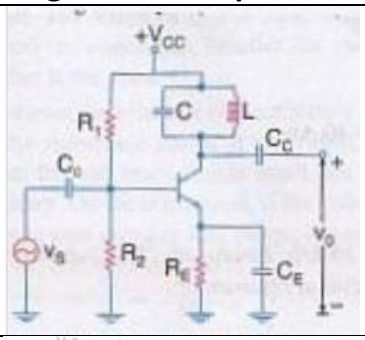
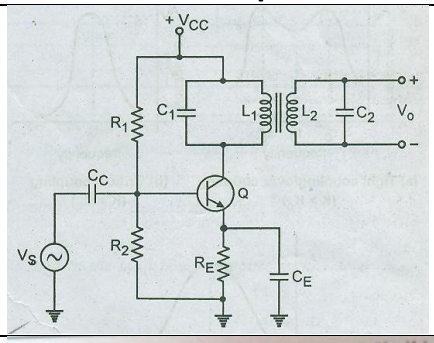
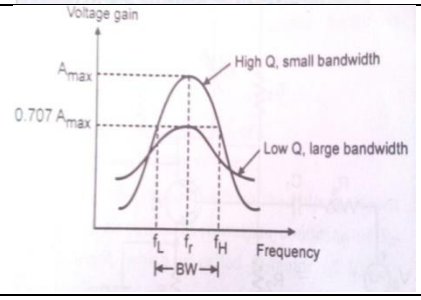
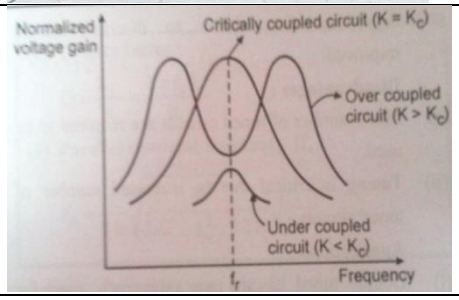
C) List any four advantages of –ve feedback.

Ans: 4 Advantages 4M

1) Less amplitude distortion
2) High stabilized gain
3) Higher fidelity
4) Less phase distortion
5) Noise reduces
6) Increased bandwidth
7) Less frequency distortion

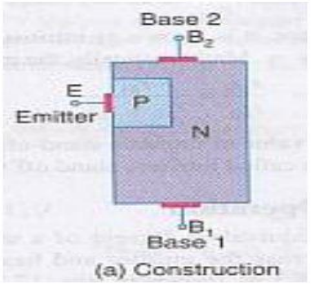
D) Compare single tuned and double tuned amplifier on i) circuit diagram ii) frequency response.

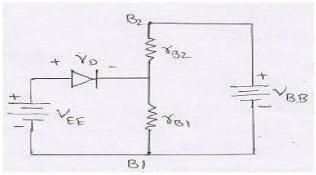
Ans : Each circuit diagram : 2M , Each frequency response : 2M

Parameter	Single tuned amplifier	Double tuned amplifier
Circuit diagram		
Frequency Response		

E) Describe the operation of UJT with its equivalent circuit.

Ans: Circuit diagram: 2M,Working : 2M





- Fig. shows the equivalent circuit of a unijunction transistor with voltage source V_{EE} connected across emitter and base1 and V_{BB} connected across base1 and base2. Hence the diode is reversed biased by a

voltage drop across the r_{B1} and its own barrier potential (V_D). Thus total reverse bias voltage across a diode is equal to sum of $\eta.V_{BB}$ and VD.

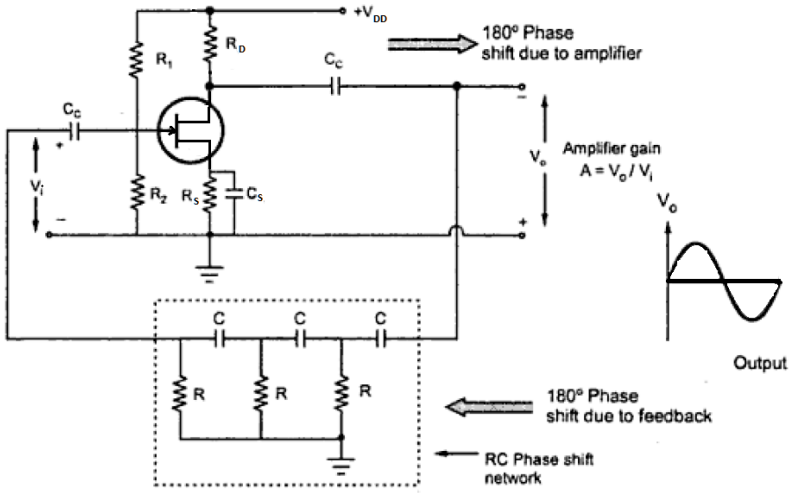
- As long as the V_{EE} is below the total reverse bias voltage (i.e. $\eta.V_{BB} + V_D$) across the diode, it remains reverse biased and there is no emitter current.
- However if the V_{EE} voltage reaches or exceeds the value equal to ($\eta.V_{BB} + V_D$), the diode conducts V_{EE}, which causes the diode to conduct, is called peak point voltage.

$$V_P = \eta . V_{BB} + V_D$$

- When the emitter current begins to flow, the UJT is said to be fired, triggered or turned on.

F) Draw labeled circuit of RC phase shift oscillator. State the formula for frequency of oscillation.

Ans: Circuit diagram : 3M, frequency response formula:1M



NOTE:- Diagram with BJT is also accepted.

Formula for frequency of oscillation is given by,

$$f = \frac{1}{2\pi CR\sqrt{6}}$$