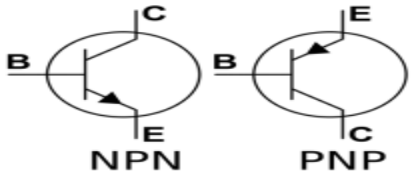
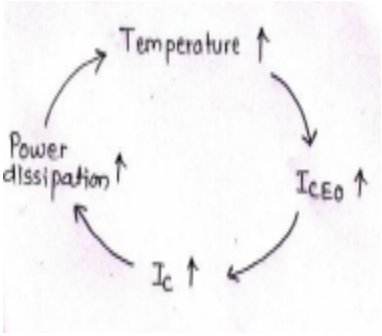
WINTER– 16 EXAMINATION (Subject Code: 17319)

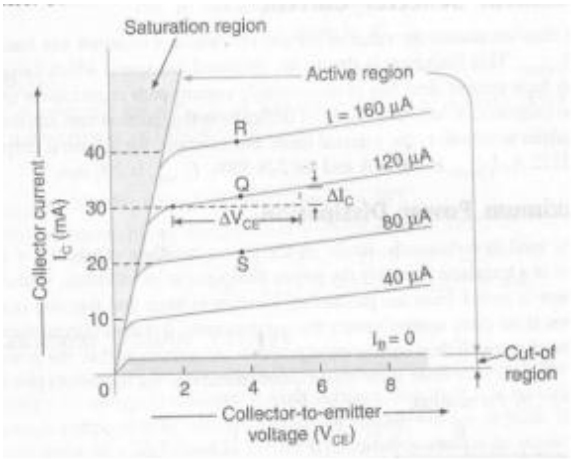
Model Answer

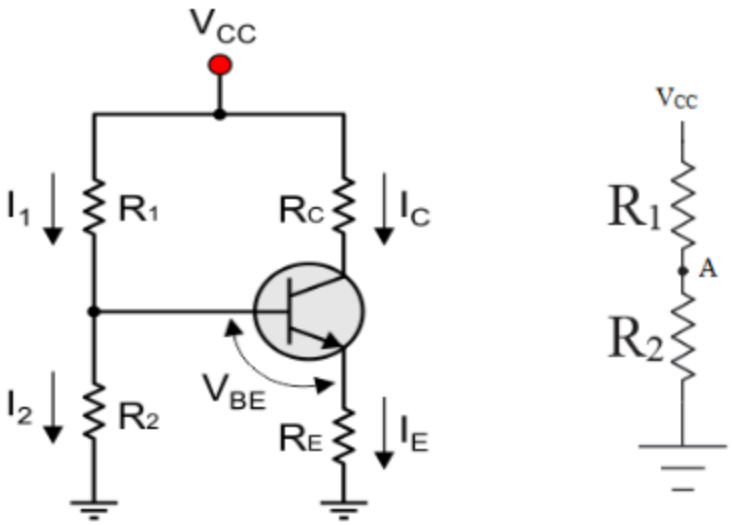
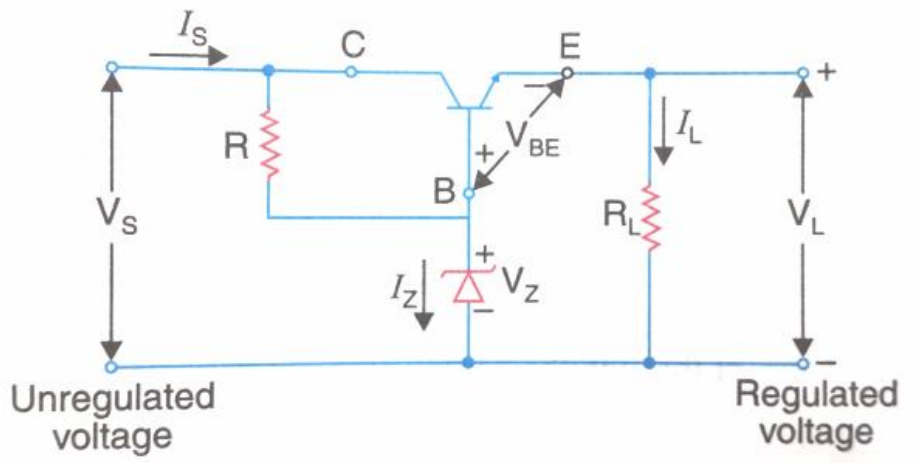
Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
Q.1		**Attempt any SIX of following:**	**12-Total Marks**
	a)	**Draw symbol NPN and PNP transistor.**	**2 M**
	Ans:	Symbol Of NPN and PNP BJT 	**(1M each)**
	b)	**What are different types of amplifier coupling?**	**2 M**
	Ans:	Types of amplifier coupling: ***(ANY TWO)*** 1. Resistance – capacitance (RC) coupling. 2. Transformer coupling 3. Direct coupling	**(1M each)**
	c)	**Define intrinsic stand of ratio for UJT.**	**2 M**
	Ans:	Intrinsic standoff ratio: It is defined as the ratio of the R_{B1} (base resistance 1) to the inter-base resistance (R_{BB}). $$\eta = \frac{R_{B1}}{R_{BB}} = \frac{R_{B1}}{R_{B1}+R_{B2}}$$	**(Definition :1M, Equation :1M)**

d)	**List various transistor biasing methods .**	**2 M**
Ans:	Transistor biasing methods: 1. Base bias / Fixed Bias 2. Base bias with emitter feedback 3. Voltage divider bias/ Self bias 4. Emitter bias	**(1/2 M each)**
e)	**State the effect of V_{GS} on channel conductivity on N-channel JFET .**	**2 M**
Ans:	As the V_{GS} is increased above zero the following effects are noted : 1. The value of pinch off voltage is reached at smaller value for drain current as compared to that when $V_{GS} = 0$ 2. The value of V_{DS} is decreased as compared to that when VGS = 0. i. e. Conductivity decrease when V_{GS} is increased. Conductivity increases when V_{GS} is decreased.	**(1M Each point)**
f)	**What is thermal runaway? How it can be avoided?**	**2 M**
Ans:	Thermal Runaway: • We know that $I_C = \beta I_B + (1+ \beta). I_{CO}$ Where I_{CO} is the leakage current. • I_{CO} is strongly dependent on temperature. • The flow of collector current produces heat within the transistor. • This raises the transistor temperature. • If no stabilization is done, I_{CO} further increases. • If I_{CO} increases, I_C increases by $(1+ \beta). I_{CO}$ • The increased I_C will raise the temperature of the transistor which in-turn will increase the I_{CO}. • This effect is cumulative and in a fraction of a second I_c becomes so large causing transistor to burn up. • This self-destruction of an unstabilized transistor is known as Thermal Runaway.  Thermal Runaway can be avoided using: • IC should be kept constant • This is done by causing I_B to decrease automatically with temperature increase. • This principle is used to provide stabilization of I_C by designing it as biasing circuit of different types and later providing compensation technique. • And also by Heat sink.	**(Thermal Runaway: 1M, Ways to avoid :1M)**

g)	**State the need of regulator.**	**2 M**
Ans:	NEED OF VOLTAGE REGULATORS DC voltage obtained by using rectifier and filter is not constant; this DC voltage may result in an error or may damage other electronic devices or circuits e.g. 1. In oscillators it may lead to phase shift. 2. In amplifiers it may lead to change in voltage gain or power gain. 3. It may lead to calibration error in measuring instruments. 4. It may produce distortions in output of audio and video amplifiers. Hence to avoid this errors DC voltage regulators are necessary to keep the output DC voltage constant.	**(State Need :2M)**
h)	**State the conditions for sustained oscillations.**	**2 M**
Ans :	Conditions for sustained oscillations: • The total shift introduced, as the signal proceeds from input terminals through the amplifier & amp; feedback network & amp; back again to the input is precisely 0° or 360°. • The magnitude of the loop gain A V β must be equal to 1 at the frequency of oscillations. $\lvert A_v\beta \rvert = 1$ & $\theta = 0°$ or $360°$.	**(1M for each condition)**
b)	**Attempt any TWO of following:**	
a)	**Draw the output characteristics of common emitter configuration. What is the effect of base current I_B on collector current I_C with reference to characteristics?**	
Ans:	Output characteristics of Common Emitter configuration:  Effect of Base current I_B on Collector current I_C : As I_B increases above 0 µA; value of I_C also increases.	**(Output Char. 2M; Label: 1M, Effect 1M)**

b)	**Draw the circuit diagram of voltage divider biasing method of BJT.How stability in operating point is obtained?**	**4 M**
Ans:	 Stability in operating point is obtained by As $I_C = V_{TH}/R_E$, the increase in collector current due to temperature will cause the voltage drop across R_E This in turn decreases V_{BE} which cause I_B to decrease hence I_C decreases to restore its original value. Thus good stabilization of operating point is ensured for D.C. bias.	**(Diagram:2 M, Stability of operating point :2M)**
c)	**Draw circuit diagram of transistorized series voltage regulator and explain it's working.**	**4 M**
Ans:	**Transistorized Series Voltage regulator:**  • In above fig. since transistor is connected in series with load therefore the circuit is known as a series regulator. • The transistor behaves as variable resistances whose value is determined by the amount of base current. $V_L = V_Z - V_{BE}$ OR $V_{BE} = V_Z - V_L$ $V_L = V_I - V_{CE}$	**(Diagram: 2M, Explanation :2M)**

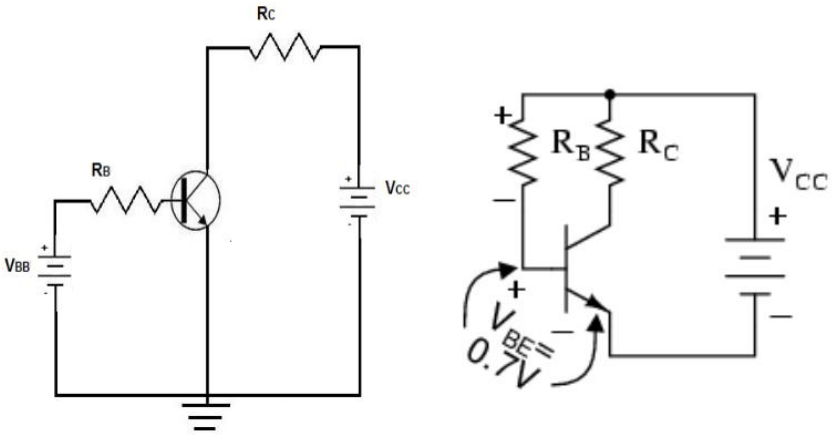
WORKING:-

- Suppose that value of load resistance is increased. Because of this, the load current decreases and load voltage (V_L) tend to increase.
- From equation (1) that any increase in V_L will decrease V_{BE} because V_Z value is fixed.
- As a result of this forward bias of the transistor is reduced this reduces its level of conduction.
- This increases V_{CE} of transistor which will slightly decrease the input current for the increase in the value of load resistance so that load voltage remains constant.
- The output of a transistor series regulator is approximately equal to zone voltage (V_Z)
- This regulator can also be used for larger load currents.

OR

$V_L \uparrow V_{BE} \downarrow I_B \downarrow I_C \downarrow V_{CE} \uparrow V_L \downarrow$

Q 2		**Attempt any FOUR:**	**16M**
	a)	**With the help of neat circuit diagram, Explain the working of fixed bias method for BJT.**	**4M**
	Ans:	Fixed bias method for BJT:	**(Diagram: 2M, Explanation :2M)**



Consider the base-emitter loop in the above circuit,
Apply KVL,

$$V_{CC} - I_B R_B - V_{BE} = 0$$
$$\therefore I_B R_B = V_{CC} - V_{BE}$$
$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since VCC and VBE are fixed values, the selection of RB fixes the value of IB.

Above equation can be simplified as, $IB \approx \frac{V_{CC}}{R_B}$ ------$[V_{BE} \ll V_{CC}]$

Apply KVL to collector-emitter loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$
$$V_{CE} = V_{CC} - I_C R_C$$

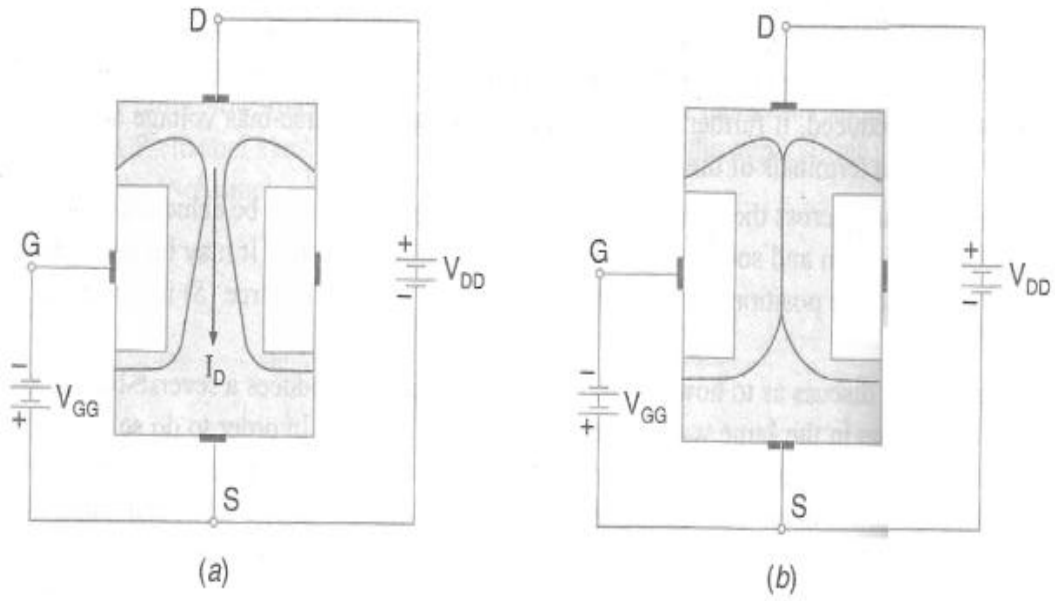
For common emitter configuration,

$$I_C = \beta I_B$$
$$I_C = \beta \frac{V_{CC}}{R_B}$$

From above, collector current I_C is β times greater than base current and is not dependant on resistance of collector circuit (R_C).
I_{CE} and V_{CE} are dependent on β. But β is dependent on temperature.
∴ It is impossible to obtain a stable 'Q' point in a fixed bias circuit.
Because of this fact, base bias is never used in amplifier circuit.

b) Describe the working principal of N- channel JFET with diagram. **4M**

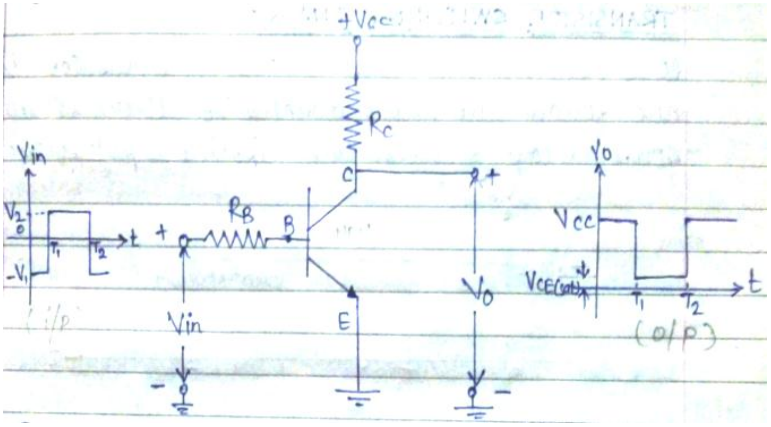
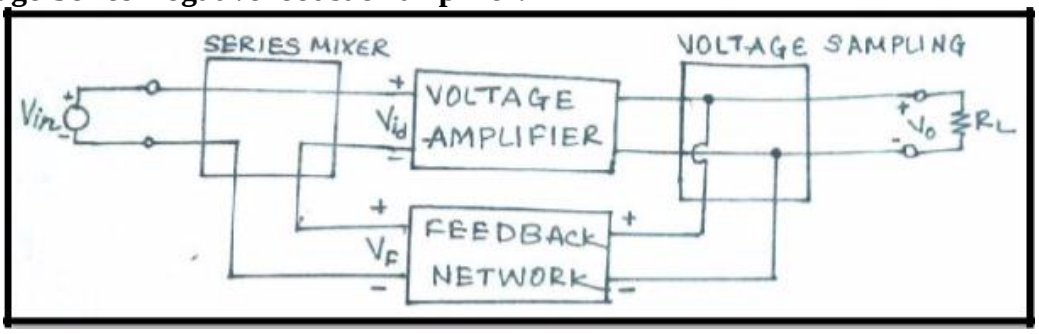
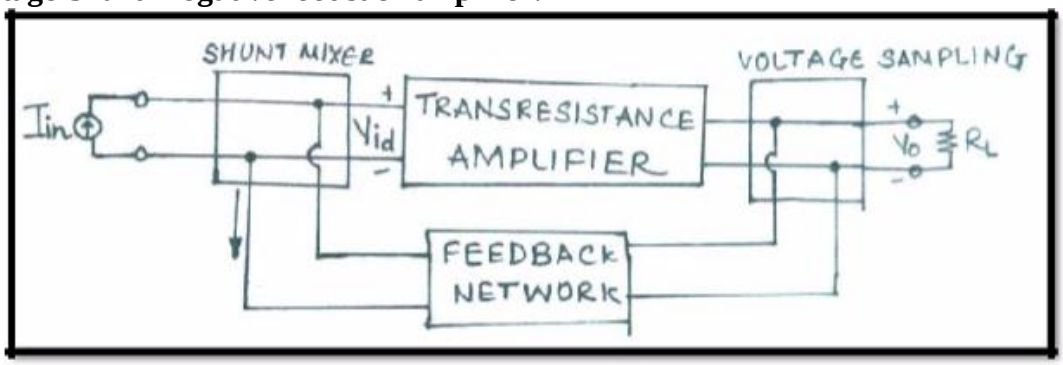
Ans: **N-Channel JFET**: **2M**

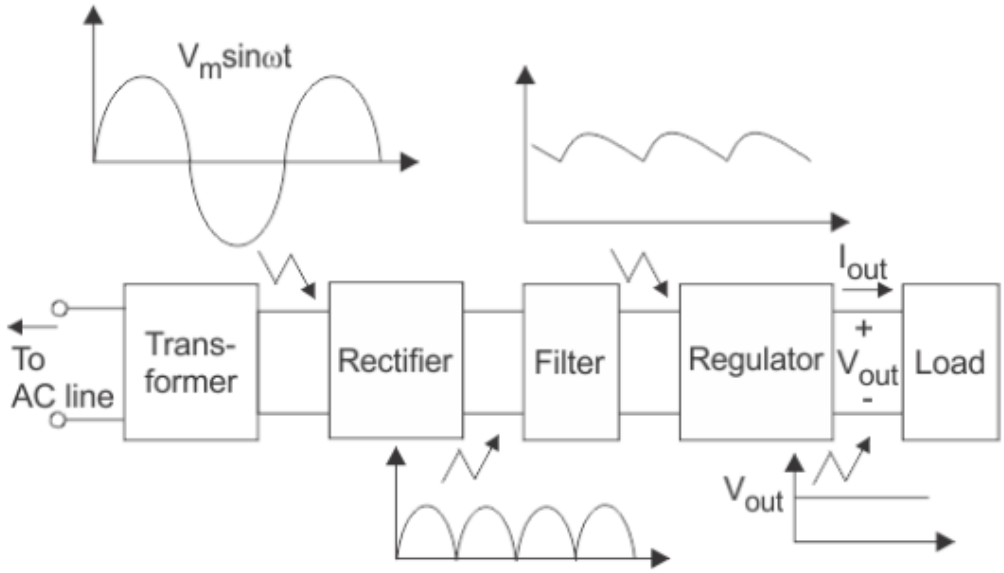


2M

Working:

- The application of negative gate voltage or positive drain voltage with respect to source, reverse biases the gate- source junction of an N-channel JFET. The effect of reverse bias voltage is to form depletion regions within the channel.
- When a voltage is applied between the drain & source with dc supply voltage (V_{DD}), the electrons flows from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current (I_D) & its conventional direction is from drain to source. The value of drain current is maximum, when no external voltage is applied between the gate & source & is designated by the symbol I_{DSS}.
- When V_{GG} is increased, the reverse bias voltage across gate-source junction is increased. As a result of this depletion regions are widened. This reduces the effective width of the channel & therefore controls the flow of drain current through the channel.
- When gate to source voltage (V_{GG}) is increased further, a stage is reached at which two depletion regions touch each other as shown in fig (b).
- At this value of V_{GG} channel is completely blocked or pinched off & drain current is reduced to zero. The value of V_{GS} at which drain current becomes zero is called pinch off voltage designated by the symbol V_P or $V_{GS(OFF)}$. The value of V_P is negative for N-channel JFET.

c)	**Draw trasistor as switch. What is voltage across transistor (V_{CE}) and current through transistor (I_C). When transistor is ON and OFF?**	**4M**
Ans:	**Transistor as a switch:** 	**2M**
	When transistor is OFF: $V_{CE} \cong V_{CC}$ Volts $I_C \cong 0$	
	When transistor is ON: $V_{CE} = V_{CE(SAT)} \cong 0.2$ V $I_C = \frac{V_{CC}}{R_C}$	**1M** **1M**
d)	**Draw block diagram of voltage shunt and voltage series feedback.**	**4M**
Ans:	**Voltage Series Negative feedback amplifier:** 	**2 M**
	Voltage Shunt Negative feedback amplifier: 	**2M**

e)	**Draw the block diagram of regulated power supply.Write the function of each block diagram.**	**4M**
Ans:	**Functional block diagram of a regulated dc power supply** 	**Diagram: 2M**

Function of each block:

1. Step Down Transformer:

A step down transformer will step down the voltage from the ac mains to the required voltage level. The turn's ratio of the transformer is so adjusted such as to obtain the required voltage value. The output of the transformer is given as an input to the rectifier circuit.

2. Rectifier

Rectifier is an electronic circuit consisting of diodes which carries out the rectification process. Rectification is the process of converting an alternating voltage or current into corresponding direct (dc) quantity.

Examples of rectifiers: full wave rectifier or a bridge rectifier

3. DC Filter:

The rectified voltage from the rectifier is a pulsating dc voltage having very high ripple content. To remove the ripple content and to get a pure ripple free dc waveform. Hence a filter is used.

Different types of filters are: capacitor filter, LC filter, Choke input filter, π type filter.

4. Regulator:

This is the last block in a regulated DC power supply. The output voltage or current will change or fluctuate when there is change in the input from ac mains or due to change in load current at the output of the regulated power supply or due to other factors like temperature changes. This problem can be eliminated by using a regulator. A regulator will maintain the output constant even when changes at the input or any other changes occur.

Explanation: 2M

Q. 3 **Attempt any FOUR:** **16 M**

a) **Compare CB, CE, CC configuration of BJT with reference to following points. i) Input impedance ii) Output impedance iii) Current gain iv) Voltage gain.** **4M**

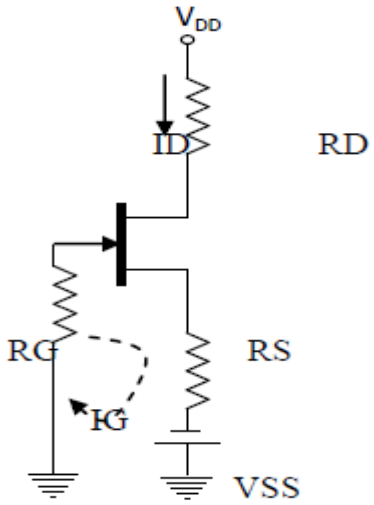
Ans:

Parameters	CB	CE	CC
Input Impedance	Low (100Ω)	Low(750Ω)	Very High(750KΩ)
Output Impedance	Very High(450KΩ)	High(45KΩ)	Low(50Ω)
Current Gain	Less than unity	High(100)	High(100)
Voltage Gain	High(About150)	Very High (about 500)	Less than 1

(Note: The value for the parameters are optional) 1M each

b) **With the help of neat circuit diagram, explain the working of self bias method for FET.** **4M**

Ans: **Circuit Diagram** **2M**



Explanation: **2M**

Fig shows the circuit of source biasing for JFET. FET gate is grounded via a resistor R_G. This type of biasing uses ± supply voltages as shown in fig. in this case the circuit behaves as a potential divider bias circuit with V_G equal to V_{SS}

D.C. analysis:-

From the circuit:-

For VGS apply KVL as shown –

$V_{GS} - I_D R_S + V_{SS} = 0$

$V_{SS} = V_{GS} + I_{D}.R_S$

$V_{GS} = V_{SS} - I_D.R_S$

Expression for V_{DS},

Apply KVL to the drain circuit

$V_{DD} - I_D R_D - V_{DS} - I_D R_S + V_{SS} = 0$

$V_{DD} + V_{SS} = I_D (R_D + R_S) + V_{DS}$

$V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S)$

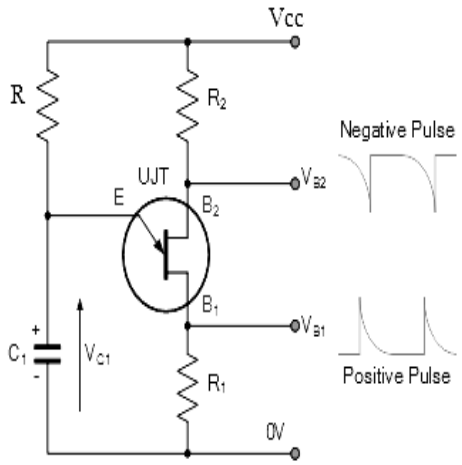
The value of the drain current can be obtained by Shockley's equation. Thus the Q point of JFET amplifier using source biasing is given by.

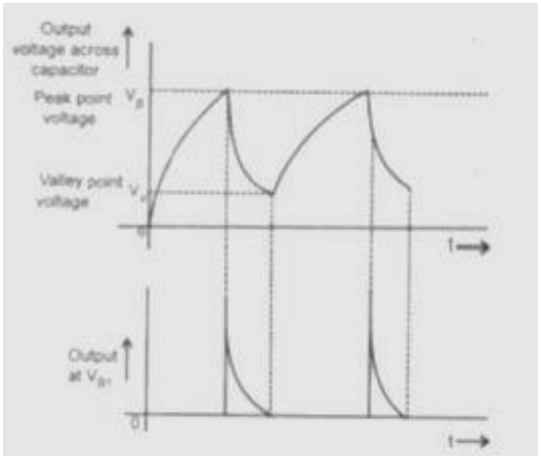
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{DS(off)}}\right)^2$$

$$V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S)$$

c) Draw circuit diagram of UJT Relaxation Oscillator and describe its working principle. **4M**

Ans: **Circuit Diagram:-** **Each diagram:1 M & Description :2M**



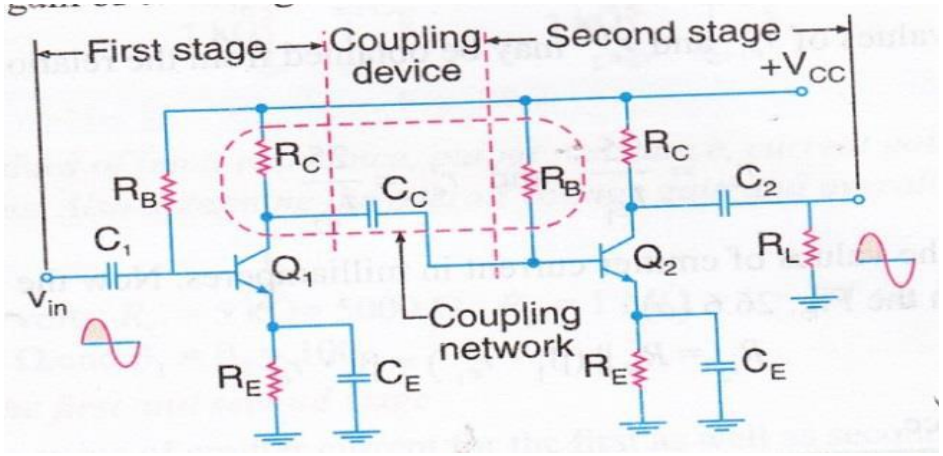


Working principle: -

- When the supply voltage (V_{CC}) is switched ON, the capacitor charges through resistor (R), till the capacitor voltage reaches the voltage level (V_P) which is called as peak point voltage. At this voltage the UJT turns ON.
- As a result of this, the capacitor (C) discharges rapidly through resistor (R_1). When that capacitor voltage drops to level Vv (called valley- point voltage) the uni-junction transistor switches OFF allowing the capacitor (C) to charge again.
- In this way because of the charging and discharging of capacitor the exponential sweep voltage will be obtained at the emitter terminal of UJT. The voltage developed at base 1(V_{B1}) terminal is in the form of narrow pulses commonly known as trigger pulses.
- The sweep period depends upon time constant (R.C) and the sweep frequency can be varied by changing value of either resistance (R) or capacitor (C). Due to this fact, the resistor R is shown as a variable resistor.
- The sweep period is given by the relation

$$T = R.C.\ \log_e (1/1-\eta)$$
$$T = 2.3\ R.C.\ \log_{10} (1/1-\eta)$$

d)	**Draw circuit diagram of two stage RC coupled amplifier. State the need of multistage amplifier.**	**4M**
Ans:	**Circuit Diagram:-**	**2M**



Need of Multistage Amplifier: **2 M**

The output from a single stage amplifier is usually insufficient to drive an output device. So that additional amplification over two or three stages is necessary.

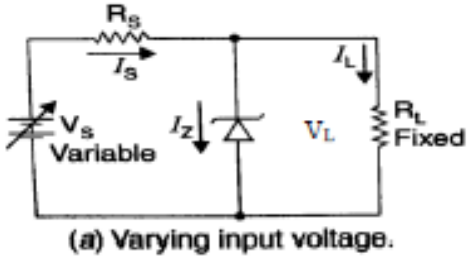
- To achieve this, output of each amplifier stage is coupled in some way to the input of the next stage. The resulting system is referred to as multi-stage amplifier or cascade amplifier, where the output of first amplifier is fed as input to second amplifier.
- To increase the overall gain of the amplifier multistage amplifier is needed.

e)	**Draw and describe working of Zener diode as voltage regulator.**	**4M**
Ans:	**Working:**	**1M**

Part I:REGULATION BY VARYING INPUT VOLTAGE :-

A resistance (Rs) is connected in series with the zener diode to limit current in the circuit. For proper operation, the input voltage (Vs) must be greater than the zener voltage (Vz). Where, R_z= zener resistance

$$Is=Iz + I_L$$



(a) Varying input voltage.

1M

Here the load Resistance is kept fixed and input voltage is varied within the limits

Case1:- WHEN INPUT VOLTAGE IS INCREASED **1M**

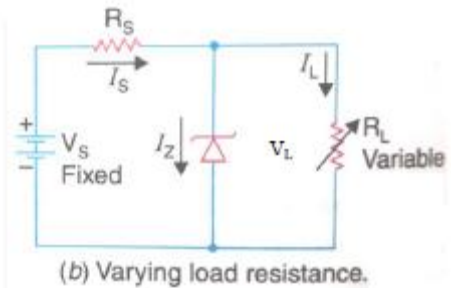
When input voltage is increased the input current (Is) also increases. Thus current through zener diode gets increased without affecting the load current(I_L).The increase in input voltage also increases the voltage drop across the resistance Rs thereby keeping the V_L constant.

Case 2:- WHEN INPUT VOLTAGE IS DECREASED

When input voltage is decreased, the input current gets reduced, as a result of this Iz also decreases. The voltage drop across Rs will be reduced and thus the load voltage (V_L) and load current (I_L) remains constant.

Part II: REGULATION BY VARYING LOAD RESISTANCE:- **1M**

In this method the input voltage is kept constant whereas load resistance RL is varied.



(b) Varying load resistance.

Case 1:- WHEN LOAD RESISTANCE IS INCREASED

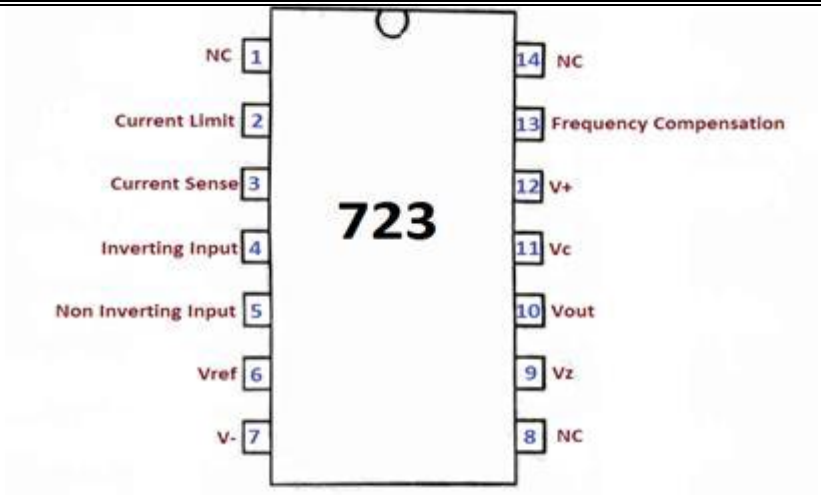
When load resistance is increased, the load current reduces, due to which the zener current I_Z increases. Thus the value of input current and voltage drop across series resistance is kept constant. Hence the load voltage remains constant.

Case 2:- WHEN LOAD RESISTANCE IS REDUCED

When load resistance is decreased, the load current increases. This leads to decrease in I_Z. Because of this the input current and the voltage drop across series resistance remains constant. Hence the load voltage is also kept constant.

f) **Sketch pin diagram of IC 723. Give any four advantages of IC voltage regulator over discrete voltage regulator.** **4M**

Ans: **2M**

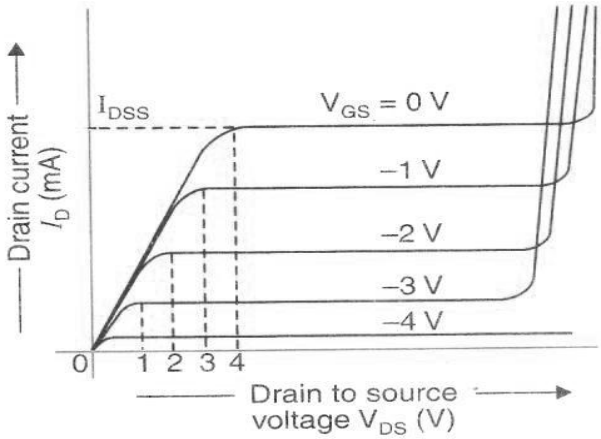


2M

Advantages of IC voltage regulator over discrete voltage regulator are: **(1/2 M each)**

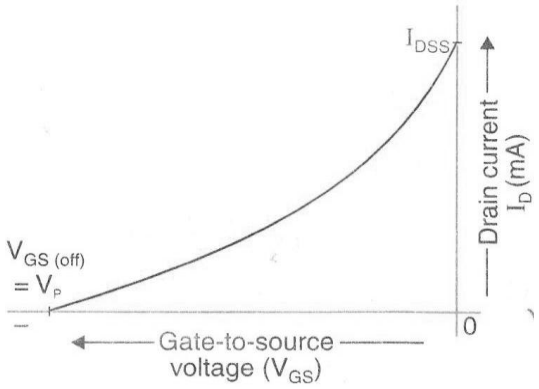
i) Improved performance
ii) High quality precise regulation.
iii) Current limiting, self protection against temperature.
iv) Remote control operation over a wide range of input voltages

Q. 4	(A)	Attempt any THREE:	12 M
	a)	**Draw transfer and drain characteristics of JFET. Give relation between μ, r, d.**	4 M
	Ans:	**Drain characteristics of JFET**	2M



1M

Transfer characteristics of JFET

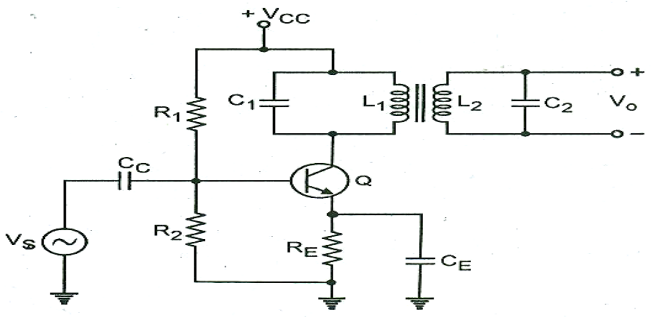


Relation between μ, r_d ,and g:-

1M

$$\mu = r_d * g$$

	b)	**Draw the circuit diagram of double tuned amplifier and describe it's working.**	4 M
	Ans:	**Circuit Diagram:-**	2 M

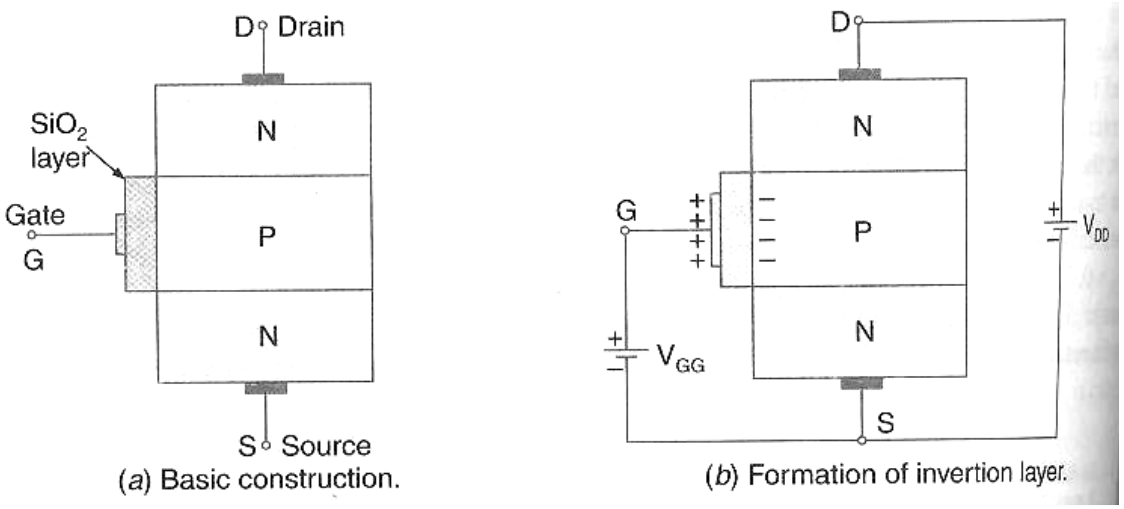


2M

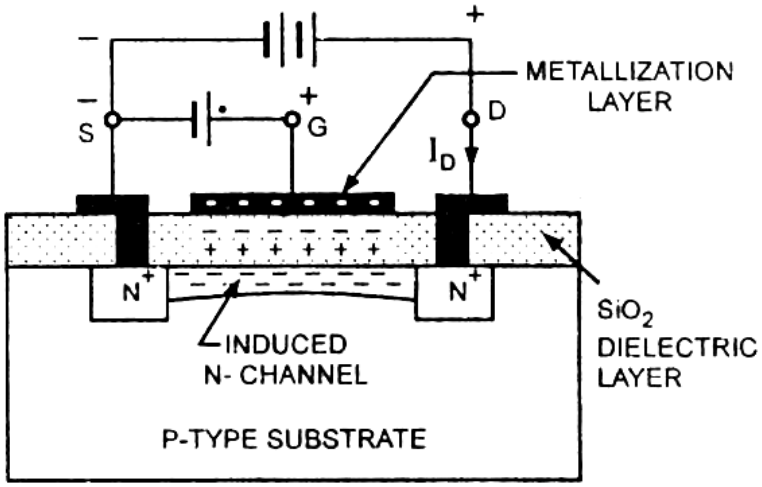
Working:

- The signal to be amplified is applied at the input terminal through the coupling capacitor C_C
- The resonant frequency of the tuned circuit L_1 C_1 is made equal to that of the signal Frequency.
- Under these conditions the tuned circuit offers very high impedance to the input signal. As a result of this, a large output appears across the tuned circuit. The output from this tuned circuit is inductively coupled to the L_2C_2 tuned circuit.
- The double tuned voltage amplifiers are extensively used in intermediate frequency (IF) amplifiers in radio and TV receivers.

c)	**Explain the working of N-channel E-MOSFET.**	**4 M**
Ans:		**2M**



OR



Operation of N-Channel E-MOSFET

Working Principle:- **2M**

Case1:- When V_{GS}=0 volt

If V_{GS}=0 volt and a +ve voltage applied between its drain and source, then due to the absence of the n-type channel a zero drain current will result.

Case2:- When V_{GS}=positive and V_{DS}=positive

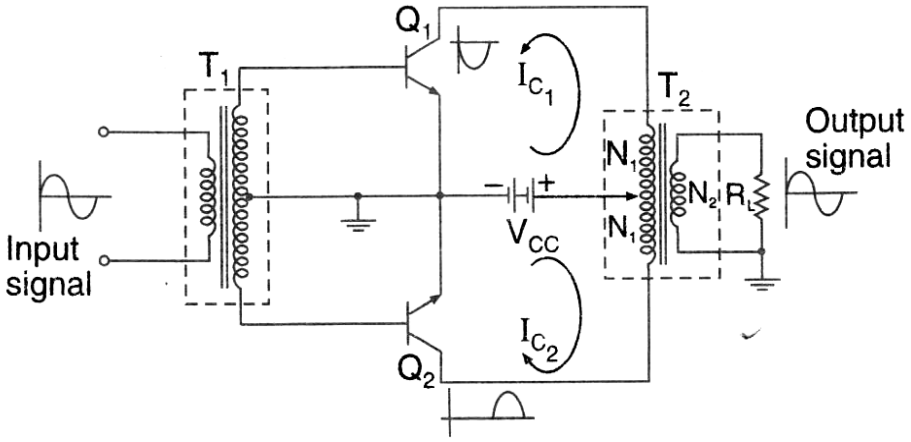
- The +ve potential at the gate terminal will repel the holes present in the p-type substrate.
- This results in creation of a depletion region Sio_2 insulting layer. But the minority carriers i.e the electrons in the p-type substrate will be attracted towards the gate terminal and gather near the surface of Sio_2 layer.
- As we increase the positive V_{GS}, the number of electrons gathers near Sio_2 layer we increase.
- The electron concentration near Sio2 layer increase to such an extent that it creates an induced n-channel. This connects the n-type doped region. This induced n-channel is called 'inversion layer'. The drain current then start flowing through this induced channel. And the value of V_{GS} at which this conduction begins is called as 'threshold voltage' $V_{GS\,(TH)}$.

Case 3:- Effect of increasing in V_{DS}

- The $+V_{GS}$ is kept constant and the V_{GS} is increased gradually .due to this, the gate terminal becomes less and less +ve with respect to drain. So less number of electrons is attracted towards gate terminal and the induced channel becomes narrow that means the channel width will be reduced to a point of pinch off and the saturation condition will occur, hence I_D will remains constant.

d) **Explain class B push-pull amplifier with neat diagram.** **4 M**

Ans: **Circuit Diagram:-** **2M**



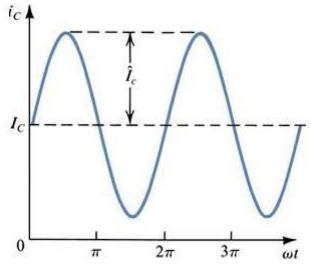
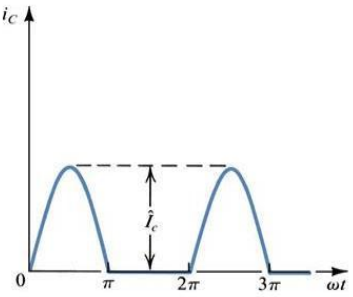
Operation :-

- In class B amplifier transistor conduct only for half cycle of input signal.one conduct in positive half cycle and other conducts in negative half cycle.
- Transformer T_1 is called as input transformer called phase splitter and produces two signals which are 180 degree out of phase with each other. **2M**
- Transformer T_2 is called as output transformer and is required to couple the a.c signal from the collector to the load.

- When there is no input signals both the transistor Q_1 and Q_2 are cut off hence no current is drawn from Vcc supply. Thus there is no power wasted in stand by the power dissipation in both transistor is practically zero.
- During positive half cycle Q_1 ON Q_2 OFF and at the output half cycle is obtained during negative half cycle Q_1 OFF and Q_2 on hence another half cycle is obtained at the output.
- Then output transformer joins these two halves and produces a full sine wave in the load resistor.

e) Differentiate between class A and class B amplifier on the following basis. i) Position of Q points on load line ii) Distortion in output voltage iii) Collector current waveform iv) Efficiency.

Ans: **1M each for point**

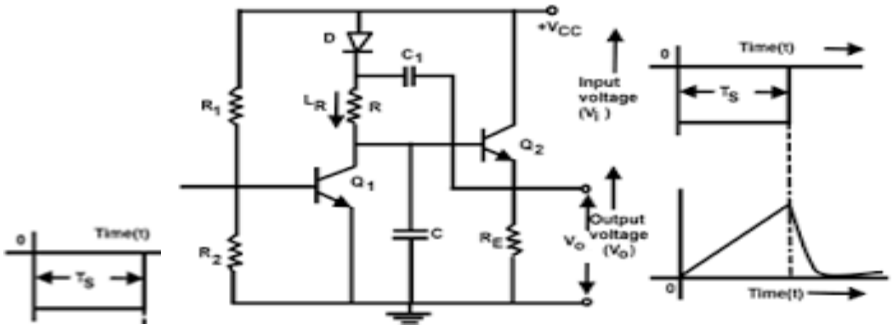
PARAMETERS	CLASS-A	CLASS-B
Position of Q point on load line	Centre of DC load line	On the X-axis(in cut –off region)
Distortion in output	No distortion	Distorted output
Collector current waveform		
Efficiency	Lowest 25% to 50%	Higher (78.5%)

f) Describe working of bootstrap time base generator with circuit diagram.

Ans:

Fig. Below shows a practical form of bootstrap circuit. Here transistor Q_1 acts as a switch and transistor Q_2 acts as an emitter follower (i.e. a unit gain amplifier). **2M**

Circuit Diagram:

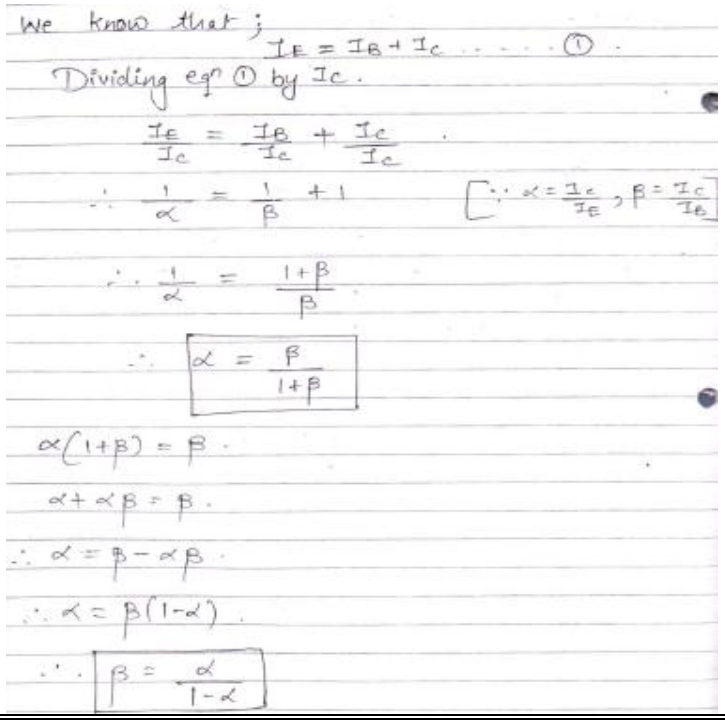


Circuit Operation:

- Initially transistor Q_1 is ON and Q_2 is OFF. Therefore capacitor C_1 is charged to V_{CC} through the diode forward resistance (R_F). At this instance output voltage is zero.
- When negative pulse is applied to the base of transistor Q_1, it turns OFF. Since Q_2 is an emitter follower, therefore the output voltage V0 is same as base voltage of Q_2.
- Thus when Q_1 turns OFF, the capacitor C_1 starts charging this capacitor C through resistor (R). As a result of these both the base voltage of Q_2 and output voltage begins to increase from zero.
- As the output voltage increases diode D becomes reverse biased, because of the fact that the output voltage is coupled through the capacitor (C_1) to the diode.
- Since the value of capacitor (C_1) is much larger than that of capacitor (C), therefore the voltage across capacitor (C_1) practically remains constant.
- Thus voltage drop across resistor (R) and hence current (I_R) remains constant, means capacitor C is charged with constant current.
- This causes voltage across capacitor C (and hence the output voltage) to increase linearly with time.
- The circuit pulls itself by its own bootstrap and hence it is known as bootstrap sweep circuit.

2M

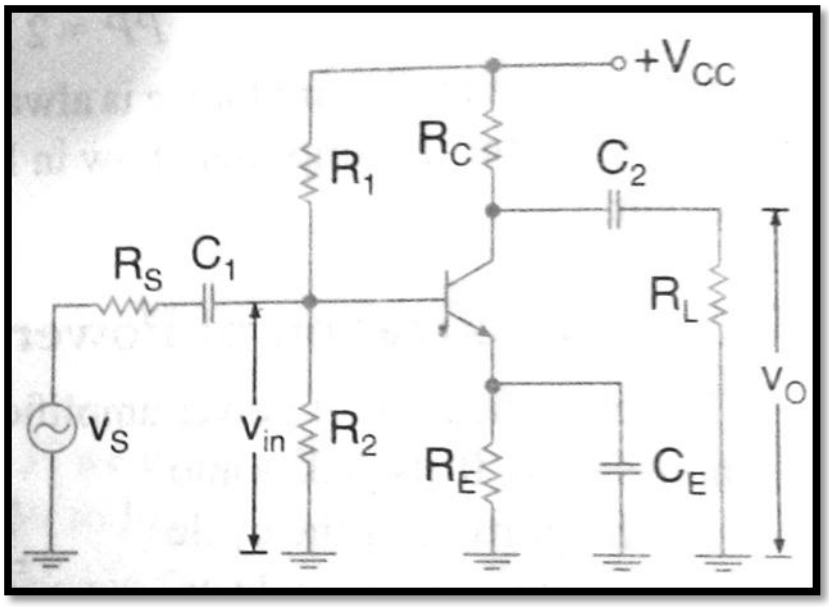
Q.5		Attempt any FOUR :	16 M
	a)	**Define α, β with respect to transistor configuration. State the relation between α and β.**	4M
	Ans:	α is defined as current gain in common base configuration. It is given by $\alpha = \frac{I_C}{I_E}$ β is defined as current gain in common emitter configuration. It is given by $\beta = \frac{I_C}{I_B}$ relation between α & β	Define:0.5 M



1.5M

1.5M

b)	**For RC phase shift oscillator the components values are as follows: R = 8.2 k2, C = 0.01 µf, R1 =1.2 KΩ , RF = 39 KΩ . What will be the frequency of oscillation?**	**4M**
Ans:	formula :- $f = \frac{1}{2\pi RC\sqrt{6}}$ Solution :- $f = \frac{1}{2\pi R.C.\sqrt{6}}$ $= \frac{1}{2\pi \times 8.2k\Omega \times 0.01\mu f \times \sqrt{6}}$ $= 792.77\ Hz$ frequency of oscillations = 792.77 Hz	**1M** **2M** **1M answer with unit**
c)	**Draw the circuit diagram of single stage class A power amplifier and describe its working.**	**4M**
Ans:	**Circuit Diagram:**	**2M**



Circuit Description: **2M**

- The input a.c. signal is applied across the base emitter terminals of the transistor & output is taken across collector emitter terminals of the transistor. V_{BB} supply forward biases the emitter base junction & V_{CC} supply reverse biases the output junction.
- The Q point is determined by the V_{CC} supply along with the resistance R_C. The resistances R_1 , R_2, R_E form the biasing & stabilisation circuit & thus establishes

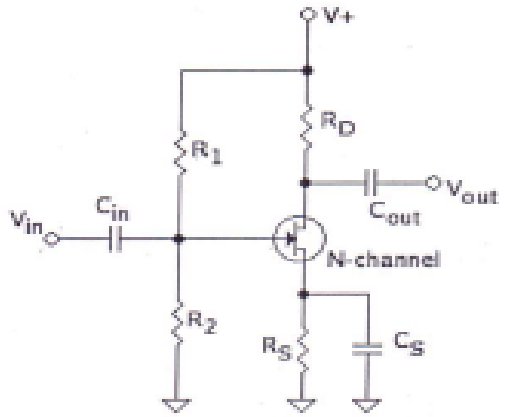
proper operating point.

- Input capacitor ($C_{in} \approx 10\mu F$) : It blocks DC voltage to the base, if it is not provided the source resistance comes across R_2,so that transistor gets unbiased. It allows ac to pass & isolates source resistance from R_2.

Class A amplifier is basically, a common emitter amplifier. This circuit is called direct coupled class A power amplifier. The only difference between this circuit and small signal version, considered earlier, is that the signals handled by the power amplifier circuit are in the range of volts. And the transistor used is a power transistor, capable of operating in the range of few watts.

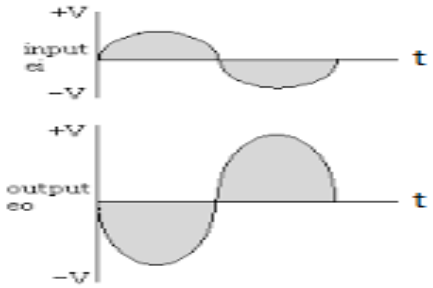
d) **How FET can be used as an amplifier? Explain with neat sketch.** **4M**

Ans: **COMMON SOURCE FET AMPLIFIER:** **Diagram:2 M & Explanation:2M**



• Above circuit shows CS –N channel FET amplifier.
• Voltage divider biasing circuit is used.
• CI & C2 arc coupling capacitors used to couple input AC signal & output respectively.
• Cs is a bypass capacitor which keeps the source of FET effectively.

Explanation:



DURING POSITIVE HALF CYCLE:
• As the gate to source voltage increases, the drain current I_D also increases.
• As a result of this, the voltage drop across resistor R_D also increases
• This causes the drain voltage to decrease. As $V_{DS}=V_{DD}-I_DR_D$.
• It means that the positive half cycle of the input produces negative half cycle of the output voltage.

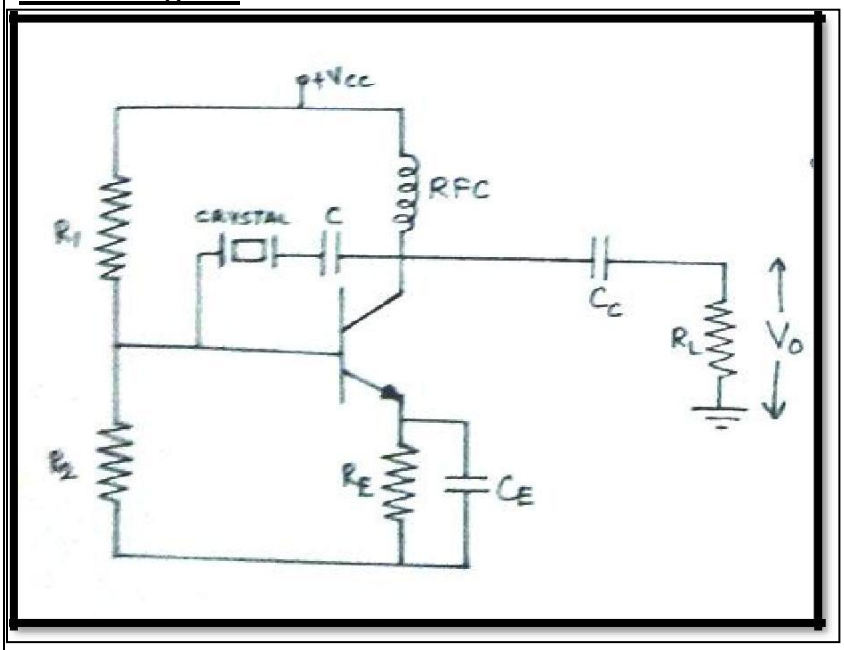
• In other words output voltage is 180^0 out of phase with the input voltage

DURING NEGATIVE HALF CYCLE:

• As the gate to source voltage decreases. The drain current also decreases.
• As a result of this, the voltage drop across resistor R_D also decreases.
• This causes drain voltage to increase. As $V_{DS}=V_{DD}-I_DR_D$.
• It means that negative half cycle of the input produces positive half cycle of the output voltage.
• In other words output voltage is 180 out of phase with the input voltage.

e) Draw the circuit diagram of crystal oscillator, and give the basic principle of Piezoelectric crystal. **4M**

Ans: **Circuit diagram:** **2M**



2M

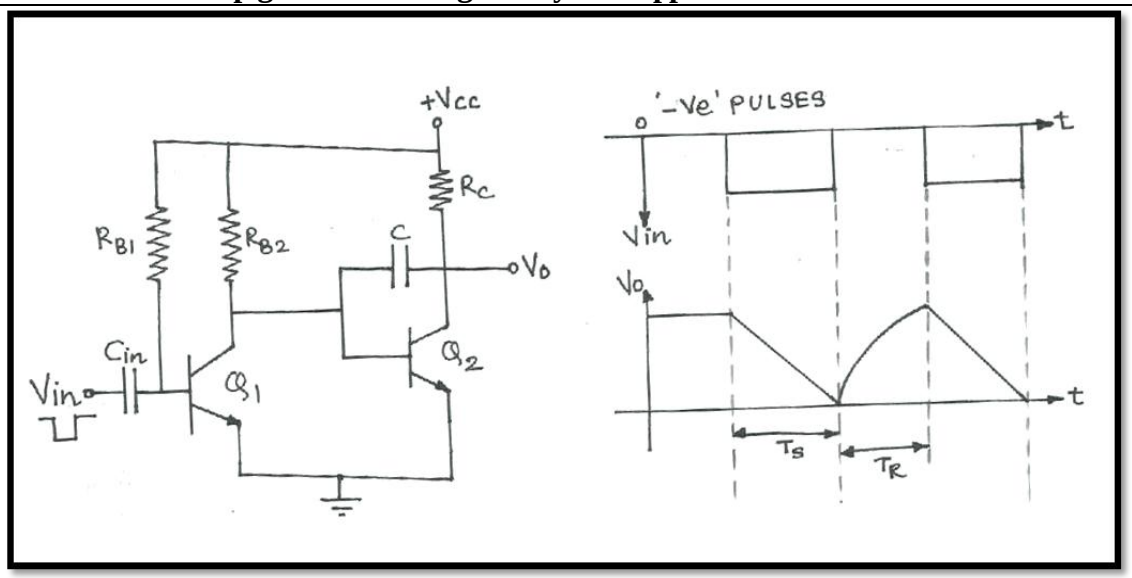
Crystal Oscillator Principle:

Crystal exhibits a property called as piezo-electric property, which states that:

When the crystal is placed across an ac source, it starts vibrating. The amount of vibration depends upon the frequency of the applied voltage (By changing the frequency , we can find a frequency at which the crystal vibrations reach its maximum value & this frequency called as resonant frequency

$$fr= \frac{1}{2\pi\sqrt{LC}}$$

Also if mechanical force is applied to crystal then it generates electric potential.

	f)	**Draw Miller sweep generator and give any two applications.**	**4M**
	Ans:		**2M**
		Applications : (Any Two) i) Used in CRO ii) In television iii) Application where linear output is expected iv) To convert step waveform into RAMP waveform.	**1M each**
Q.6		**Attempt any FOUR :**	**16 M**
	a)	**In CE configuration if β = 98, leakage current I_{CEO}) = 50 µA. If base current is 0.5 mA. Determine I_C and I_E.**	**4 M**
	Ans:	$I_C = \beta . I_B + (1+\beta) I_{CEO}$ $= (98)(0.5mA) + (1+98)\ 50\,\mu A$ $= 0.049 + 4.95 \times 10^{-3}$ $= 53.95\ mA$ $I_E = I_B + I_C$ $= 0.5mA + 53.95\ mA$ $= 54.45\ mA.$	**½ M each Formula** **2M** **1M**

b) Distinguish between series and shunt voltage regulator (any four points) — **4 M**

Ans: — **1M each**

Sr. No.	SHUNT VOLTAGE REGULATOR	SERIES VOLTAGE REGULATOR
1	Control element is connected in shunt with load.	Control element is connected in series with load.
2	High Output impedance.	Low Output impedance.
3	It has protection against short circuit of transistor.	It does not have protection against short circuit of transistor.
4	Good voltage regulation even at high load current.	Not so good voltage regulation at high load current.
5	Poor voltage regulation.	Better voltage regulation.
6	Good efficiency for low load current.	Good efficiency for high load current.
7	The output DC voltage is constant.	The output DC voltage is not absolutely constant.
8	Suitable for light loads.	Suitable for heavy loads.
9	Control element has to bear the load voltage across it. So it is a high voltage low current device.	Control element has to bear the load current. So it is a low voltage high current device.
10	Supply current is higher than load current as $I = I_L + I_{SH}$	Supply current is same as load current. But input voltage is higher than output voltage as $V_i = V_O + V_S$

c) State the effect of negative feedback on following parameter i) Bandwidth, ii) Noise, iii) Gain ,iv) Distortion — **4 M**

Ans: — **1M each**

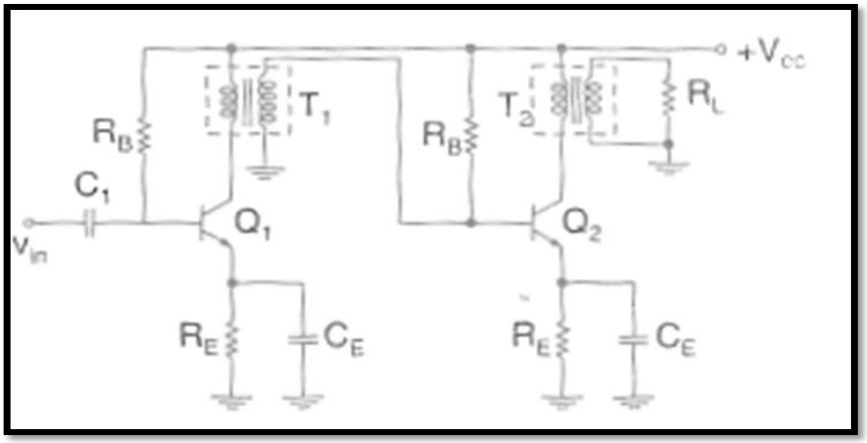
i) Bandwidth increases.
ii) Distortion reduces.
iii)Noise decreases
iv) Gain decreases.

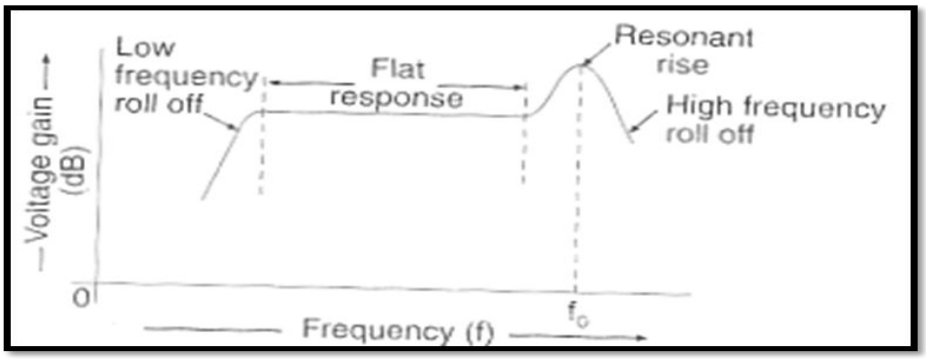
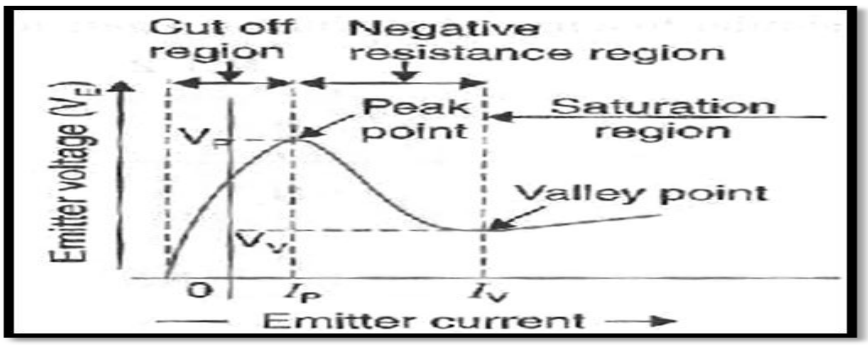
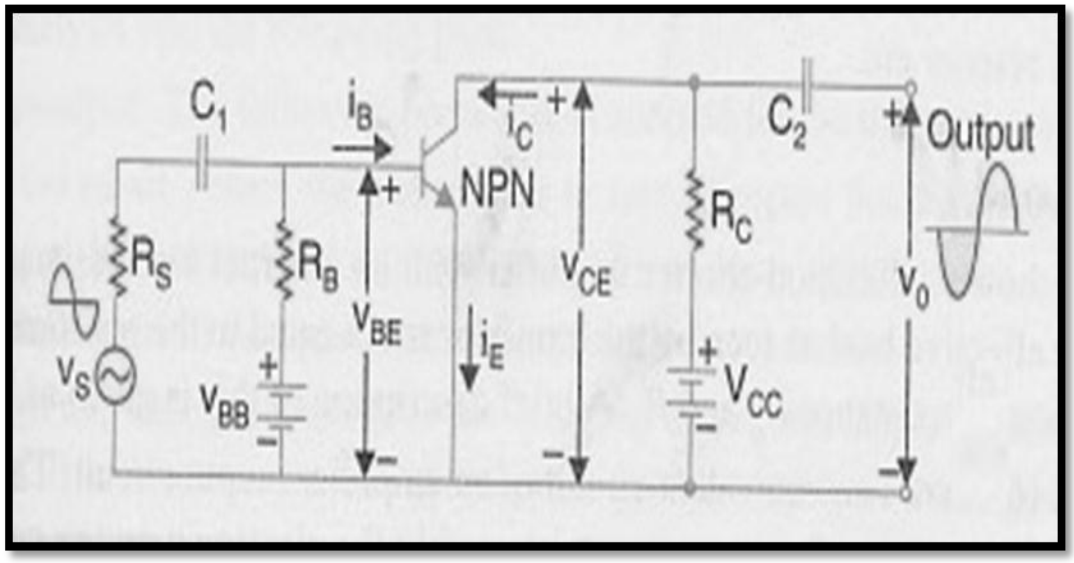
d) Draw circuit diagram of two stage transformer coupled amplifier. Draw its frequency response. — **4 M**

Ans: — **2M**

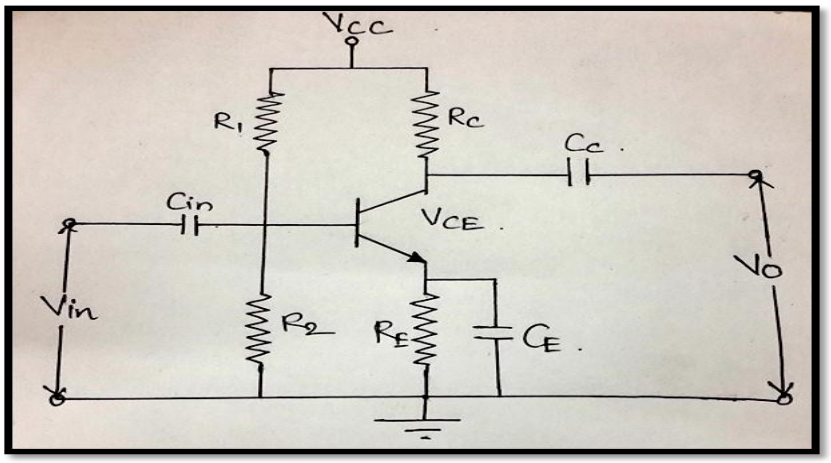
CIRCUIT DIAGRAM:

Two stage transformer coupled amplifier



	FREQUENCY RESPONSE OF TRANSFORMER COUPLED AMPLIFIER 	**2M**
e)	**Sketch neat labeled VI characteristics of unijunction transistor.**	**4 M**
Ans:	**V-I CHARACTERISTICS OF UJT:** 	**2M for chara.** **1M for regions in chara.** **1M for labelling**
f)	**Draw circuit diagram of single stage CE amplifier and state function of each component.**	**4 M**
Ans:	**CIRCUIT DIAGRAM:**  **OR**	**2M**

PRACTICAL COMMON EMITTER AMPLIFIER:



2M

Function of components:

- The input a.c. signal is applied across the base emitter terminals of the transistor & output is taken across collector emitter terminals of the transistor. V_{BB} supply forward biases the emitter base junction & V_{CC} supply reverse biases the output junction.
- The Q point is determined by the V_{CC} supply along with the resistance R_C. The resistances **R_1 , R_2, R_E form the biasing & stabilization circuit & thus establishes proper operating point.**
- **Input capacitor** ($C_{in} \approx 10\mu F$) : It blocks DC voltage to the base, if it is not provided the source resistance comes across R_2,so that transistor gets unbiased. It allows a.c. to pass & isolates source resistance from R_2.
- **Emitter bypass capacitor (C_E):** C_E acts as open for D.C so R_E offers very high value resistance hence stabilization of Q-point is achieved due its negative feedback. Where C_E acts as short for A.C input signal hence it bypasses R_E so it provides very high gain due to its low value. And amplification of signal is more due to high gain.