MODEL ANSWER

SUMMER– 17 EXAMINATION

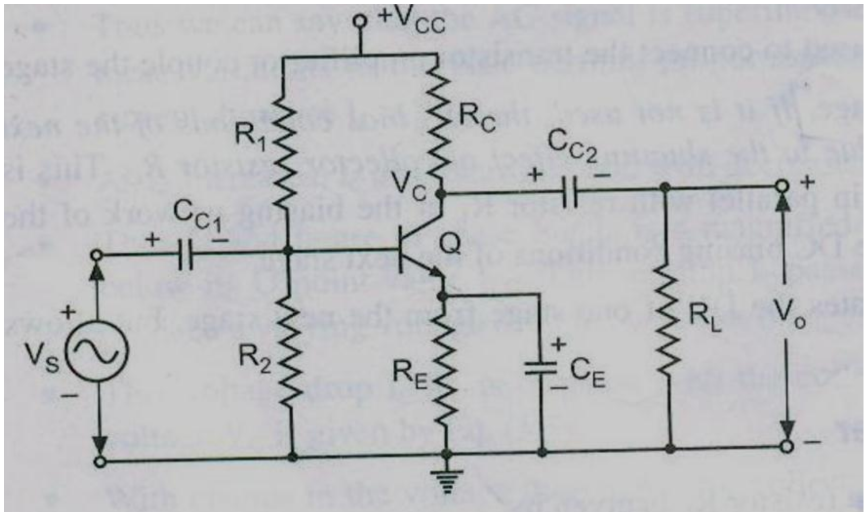
Subject Title: Electronics Devices and Circuits. Subject Code: 17319

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

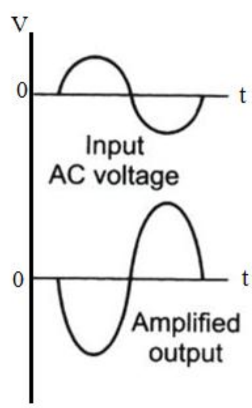
Q. No.	Sub Q.N.	Answer	Marking Scheme
Q.1	**(A)**	**Attempt any SIX:**	**12-Total Marks**
	(a)	**What is transistor? State any two applications of transistor.**	**2M**
	Ans:	The two PN - junction formed by sandwiching either p- type or n- type semiconductor between a pair of opposite types is known as transistor. **<u>(OR)</u>** A transistor is a semiconductor device used to amplify and switch electronic signals and electrical power. **<u>(OR)</u>** An electronic device that can work as an amplifier, transforming weak electrical signals into strong ones. It is normally made from silicon or other semiconductors. **<u>Two applications of transistor are:</u>** 1. As a switch 2. As an amplifier 3. As a multivibrator 4. As an oscillator etc.	**Any relevant correct definition : 1M** **Application (any two) :1M**
	(b)	**Define operating point (Q) of the transistor as an amplifier.**	**2M**
	Ans:	**<u>Q point:</u>** For proper operation of transistor in any application, we set fixed levels of voltage (V_{CEQ}) & current (I_{CQ}) in a transistor. These values of current & voltage define the point at which transistor operates. This point is called operating point. It is also known as quiescent point or Q point.	**Definition : 2M**

		(OR) Q-point is the operating point of the transistor (I_{CQ}, V_{CEQ}) at which it is biased.	
	(c)	**Draw the circuit diagram and waveforms of single stage CE amplifier.**	**2M**
	Ans:	**Circuit diagram :**	**1M**

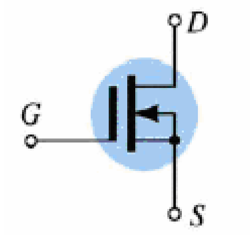
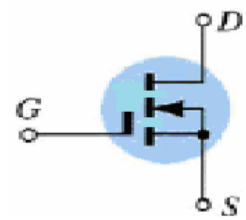
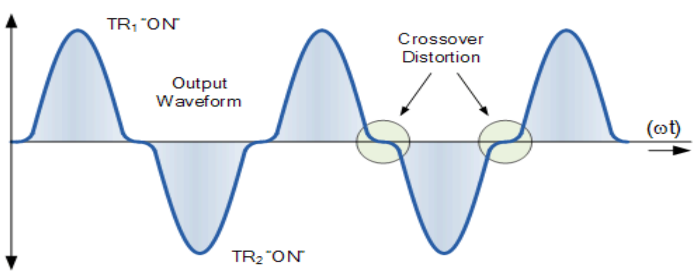


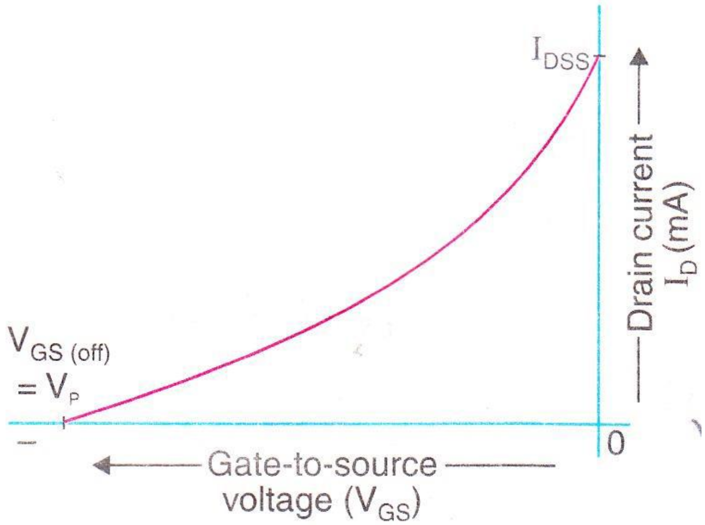
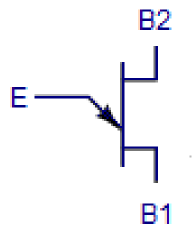
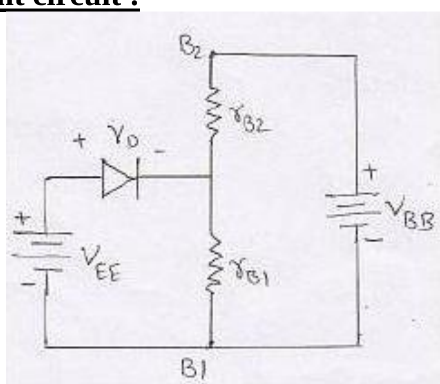
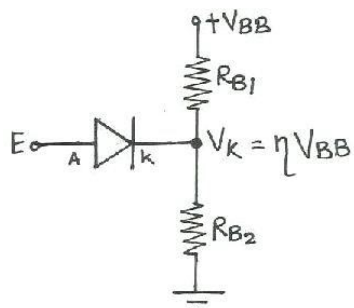
Single-stage led CE amplifier

Waveform:- **1M**

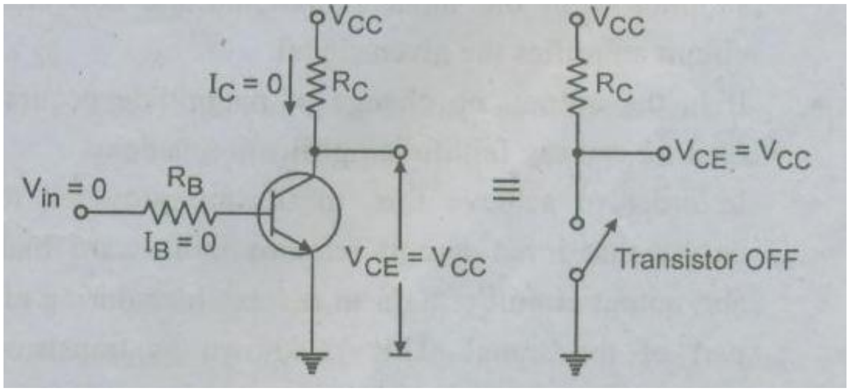


	(d)	**Draw the symbol of N-channel MOSFET. State any two application of MOSFET.**	**2M**
	Ans:	**Symbol:**	**Any one Symbol : 1M**

		 OR  N-channel D-MOSFET N-channel E-MOSFET **<u>Applications of MOSFET:</u>** 1. Used as a switch. 2. Used in radio systems. 3. Used in audio frequency power amplifiers.	**Application (any two): 1M**
	(e)	**Define tuned amplifier. State types of resonant circuit.**	**2M**
	Ans:	**<u>Definition</u>**: An amplifier which amplifies a specified frequency (or a narrow band of frequencies) is called a tuned amplifier. **<u>Types of resonant circuit:</u>** **1.** Series resonant circuit. **2.** Parallel resonant circuit.	**Definition : 1M** **Types :1M**
	(f)	**What is cross-over distortion?**	**2M**
	Ans:	**<u>Definition :</u>**  When the signal changes or "crosses-over" from one transistor to the other at the zero voltage point it produces an amount of "distortion" to the output wave shape. These results in a condition that is commonly called Crossover Distortion.	**2M**
	(g)	**Draw the transfer characteristics of N-channel JFET.**	**2M**

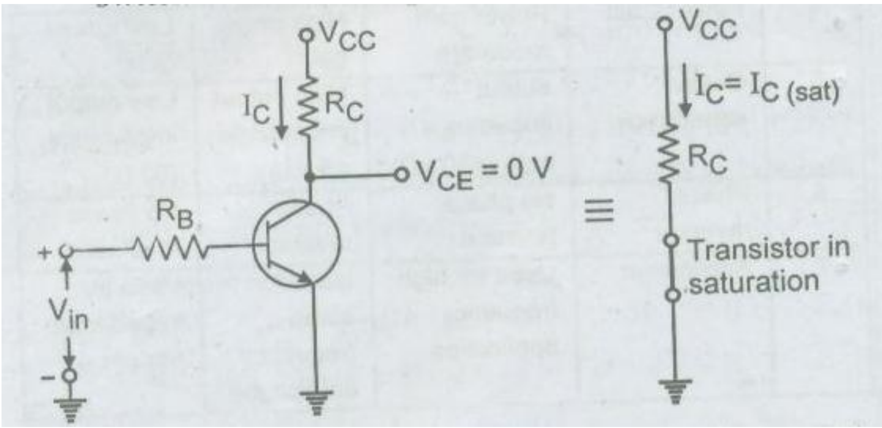
Ans:		**Characteristics : 1M** **Labeling 1M**
(h)	**Draw the symbol and equivalent circuit of UJT.**	**2M**
Ans:	**Symbol :**  **<u>Equivalent circuit :</u>**  **<u>OR</u>** 	**Symbol : 1M** **Equivalent circuit : 1M**
B)	**Attempt any TWO:**	**8M**
(a)	**Explain how transistor works as a switch. Also draw its input and output waveforms.**	**4M**
Ans:	**<u>Explanation:</u>** The transistor can be used for two types of application viz. amplification and switching. For the amplification, transistor is biased in its active region. Whereas for switching applications it is biased to operate in the saturation (full ON) or cut off (full OFF) region.	**3M**

a. Transistor in cut- off region:



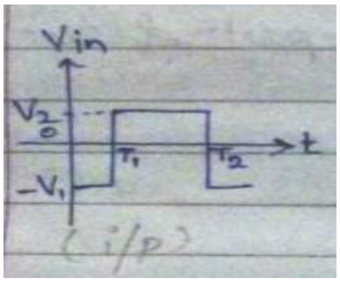
- In the cut –off region both the junction of a transistor are reverse biased and very small reverse current flows through the transistors.
- The voltage drop across the transistor (V_{CE}) is high. Thus, in the cut off region the transistor is equivalent to an open switch as shown in figure.

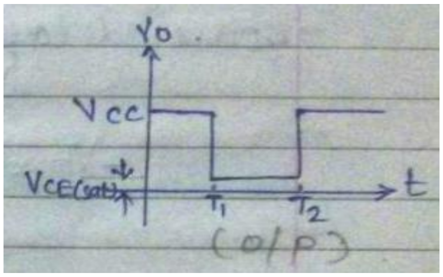
b. Transistor in the saturation region:



- When Vin is positive a large base current flows and transistor saturates.
- In the saturation region both the junctions of a transistor are forward biased. The voltage drop across the transistor (VCE) is very small, of the order of 0.2 V to 1V depending on the type of transistor and collector current is very large.
- In saturation the transistor is equivalent to a closed switch.

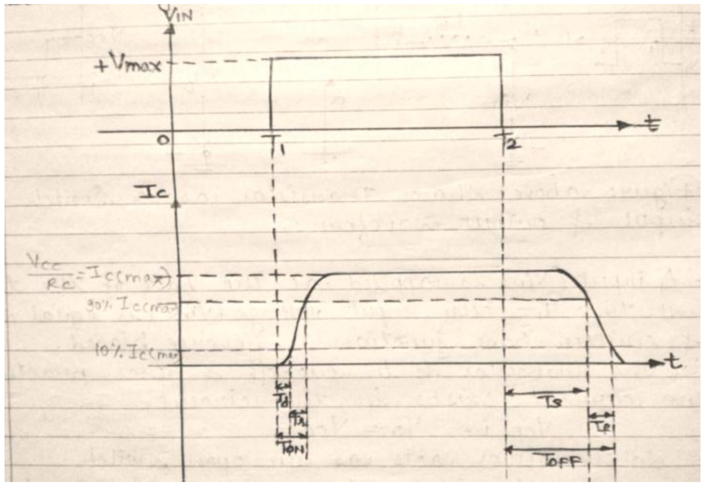
Waveforms:





1M

OR



(b) Explain the concept of DC load line and operating point for biasing circuit. **4M**

Ans:

DC load line: *(D.C load line : 1M)*

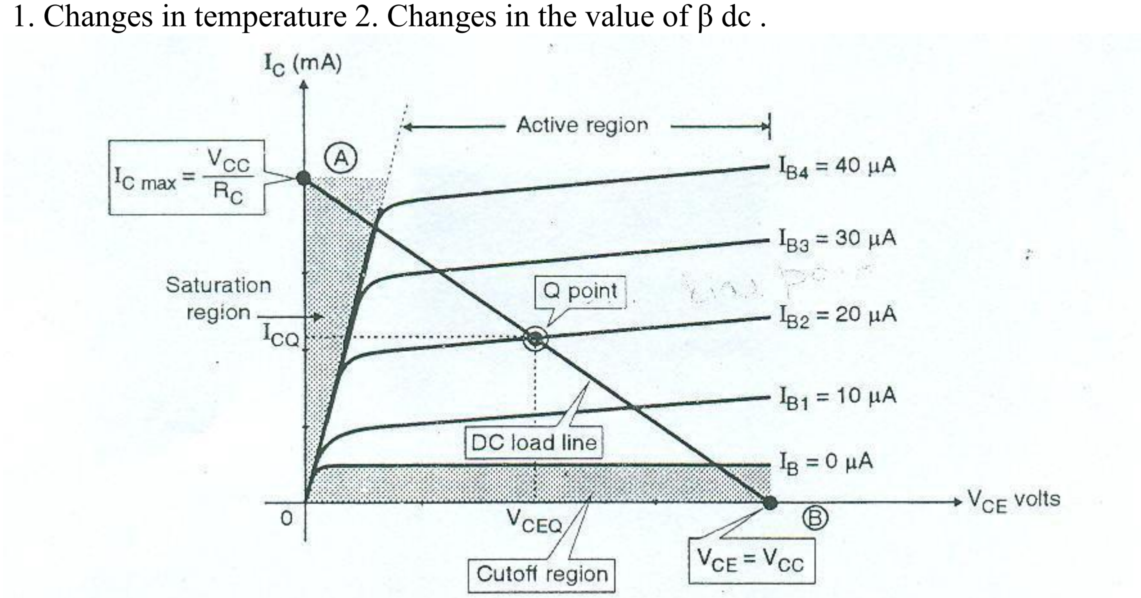
The DC word indicates that this line is drawn under the dc operating conditions without any ac signal at the input.

And the word load line is used because the slope of this line is – $1/R_C$ where R_C is the load resistance.

Operating Point : *(Explanation : 2M)*

- It is the point on the load line which represents the dc current through a transistor (I_{CQ}) and the voltage across it (V_{CEQ}) when no ac signal is applied.
- The dc load line is a set of infinite number of such operating points and the user or designer can choose any point on the dc load as the operating point.
- The position of operating point on the load line is dependent on the application of the transistor.
- The factors affecting the stability of Q-point are:

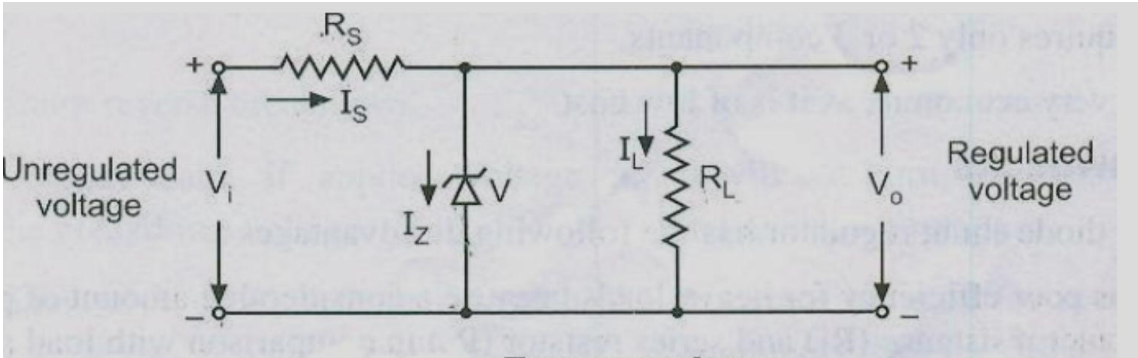
1. Changes in temperature 2. Changes in the value of β dc .



(1M)

(c) Describe the action of zener voltage regulator with neat diagram. Write any two limitations of unregulated power supply. **4M**

Ans: **Circuit Diagram:** **1M**



Zener regulator

Working : **2M**

- For proper operation, the input voltage V_i must be greater than the Zener voltage Vz. This ensures that the Zener diode operates in the reverse breakdown condition. The unregulated input voltage V_i is applied to the Zener diode.
- Suppose this input voltage exceeds the Zener voltage. This voltage operates the Zener diode in reverse breakdown region and maintains a constant voltage, i.e. Vz = Vo across the load inspite of input AC voltage fluctuations or load current variations. The input current is given by,

$$\mathbf{I_S = V_i - V_z / Rs = V_i - V_o / Rs}$$

- The input current I_S the sum of Zener current Iz and load current I_L.

$$I_S = I z + I_L$$

OR

$$I z = Is - I_L$$

- As the load current increase, the Zener current decreases so that the input current remains constant.
- According to Kirchhoff's voltage law, the output voltage is given by,

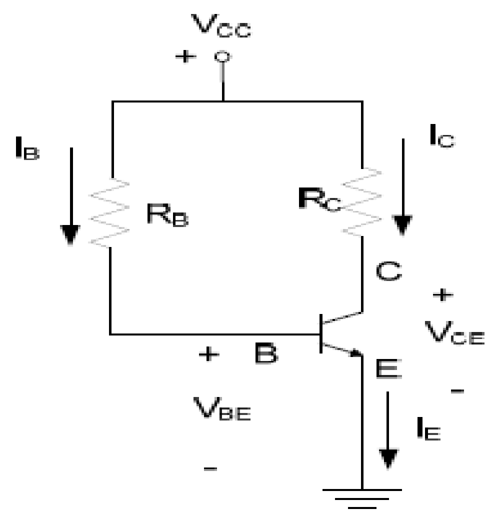
$$Vo = Vi - Is.\ Rs$$

- As the input current is constant, the output voltage remains constant, the reverse would be true, if the load current decreases. This circuit is also correct for the changes in input voltage.
- As the input voltage increases, more Zener current will flow through the Zener diode. This increases the input voltage Is, and also the voltage drop across the resistor Rs, but the load voltage Vo would remain constant. The reverse would be true, if the decrease in input voltage is not below Zener voltage.
- Thus, a Zener diode acts as a voltage regulator and the fixed voltage is maintained across the load resistor RL.

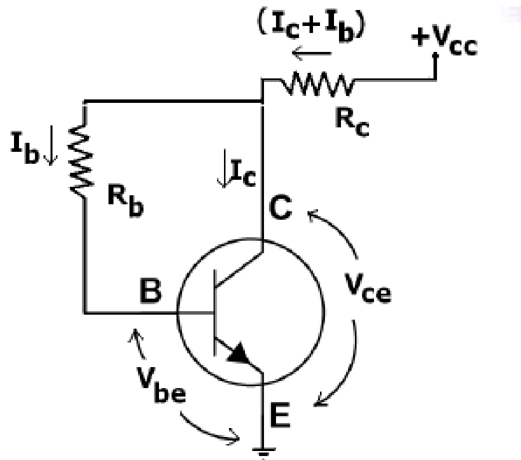
Limitations of unregulated power supply: **1M**

1. Output voltage is affected significantly by changes in mains voltage and changes in load current.

2. As the load current increases or decreases, the output voltage will decrease or increase

		due to the finite output impedance of the supply caused by transformer winding resistance, inductance etc.	
Q 2		**Attempt any FOUR:**	**16M**
	(a)	**List the types of biasing method of transistor. Explain any one method.**	**4M**
	Ans:	**Types of biasing of transistors:** 1. Base bias or fixed bias 2. Base bias with emitter feedback. 3. Voltage divider bias ***Note: Any one method can be considered*** 1. **Base bias:**  **Explanation:-** The value of collector current is given by the relation. $$I_C = \beta \frac{V_{CC}}{R_B} = \frac{V_{CC}}{R_B / \beta}$$ The above relation shows that the collector current is β times greater than the base current and is not at all dependent on the resistance of the collector circuit. It may be noted from the equations that the values of collector current (I_C) and collector-to emitter voltage (V_{CE}) are dependent on β. But β is strongly dependent upon temperature. It means that collector current and collector – to emitter voltage of a bias circuit (which sets the Q-points of a transistor) will vary with the change in value β of due to variation in temperature. It means that it is impossible to obtain a stable Q-point in a base –bias circuit. Because of this fact, the base bias is never used in amplifier circuits. **OR**	**1M** **1M** **2M**

2. Base bias with emitter feedback: **1M**



Explanation: **2M**

This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point.

In this biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source Vcc.

So any thermal runaway will induce a voltage drop across the R_C resistor that will reduce the transistor's base current.

Applying KVL

$$V_{CC} = (I_C+I_B)R_C + V_{CE} \text{------ (1)}$$

$$V_{CE} = I_BR_B + V_{BE} \text{------(2)}$$

Since, $I_C = \beta.I_B$ so from equation (1) & (2)

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}$$

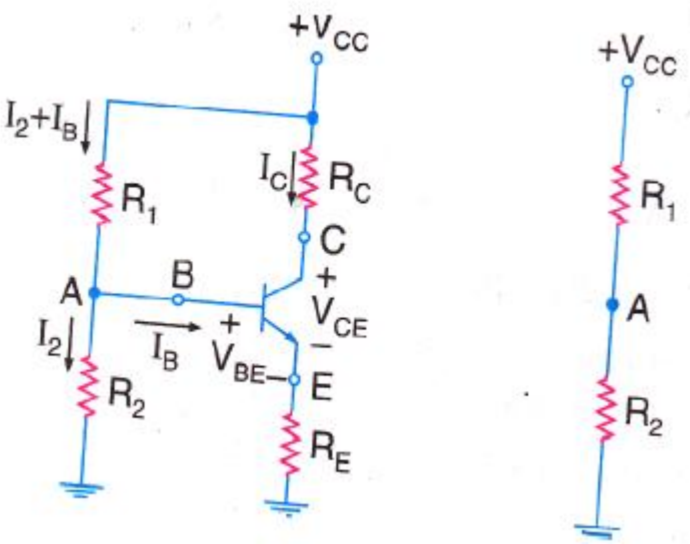
$$I_C = \beta[\frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}]$$

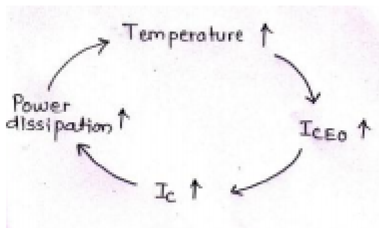
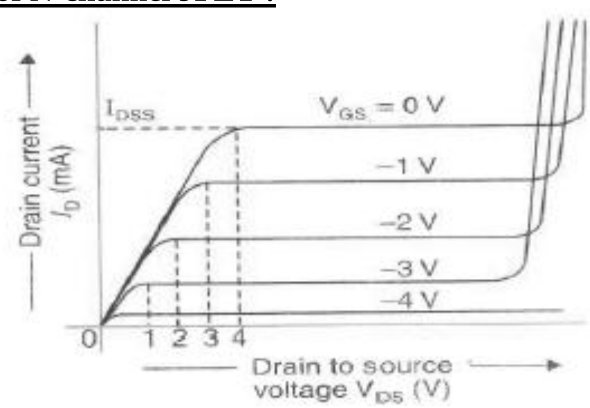
If $R_B << R_C$

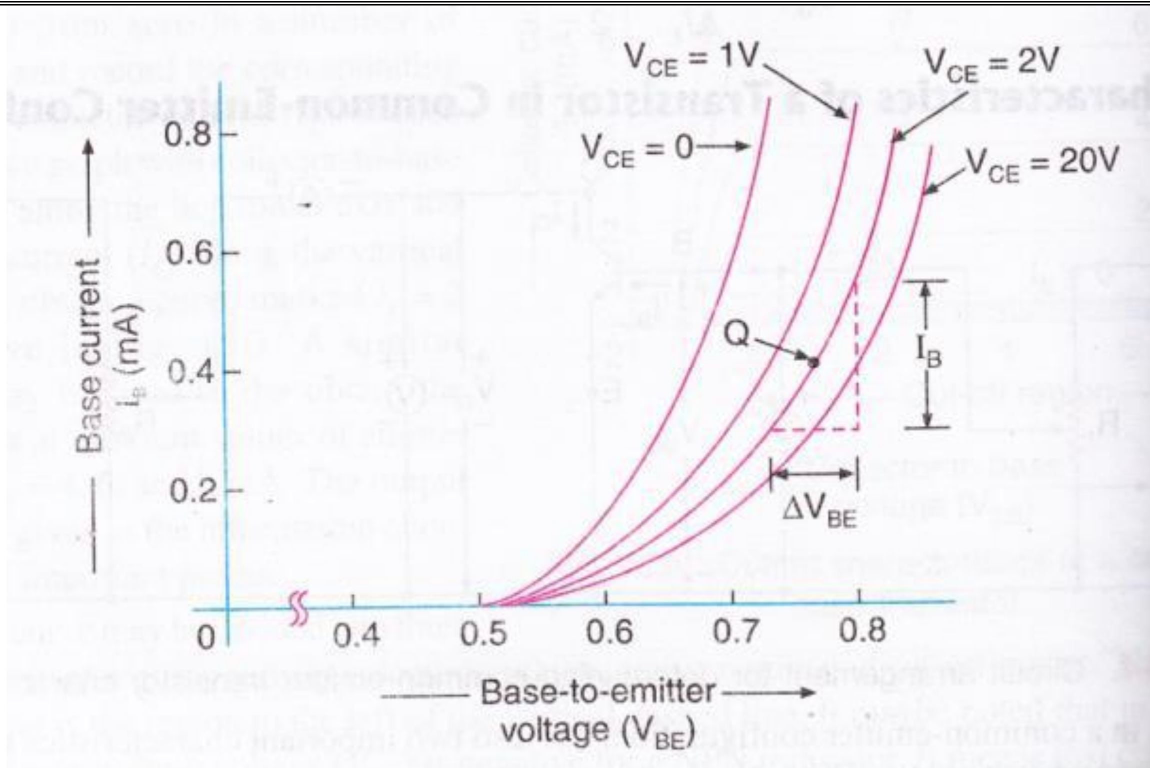
$$I_C = \frac{V_{CC} - V_{BE}}{R_C}$$

OR

3.Voltage divider bias: **1M**

		 **Explanation:-** The name voltage divider is derived from the fact that resistor R_1 and R_2 form a potential divider across the V_{CC} supply. The voltage drop across resistor R_2 forward biases the base – emitter junction of a transistor. The emitter resistor (R_E) provides the D.C. stability. It is evident from that the voltage at the transistor base (due to the voltage divider network of resistors R_1 and R_2). $$V_B=Vcc*R_2/(R_2+R_1)$$ Neglecting V_{BE} Therefore value of emitter current, $$I_E = V_E/R_E$$ And the value of collector current, $$I_C = I_E$$ The voltage drop across the collector resistor, $$V_{RC} = I_C * R_C$$ And the voltage at the collector (measured with respect to the ground) $$V_C = V_{CC} - V_{RC} = V_{CC} – I_C * R_C$$ The voltage from collector – to – emitter. $$V_{CE} = V_C – V_E = V_{CC} – I_C * R_E$$ $$V_{CE} = V_{CC} – I_E(R_C + R_E) \ldots\ldots\ldots\ldots\ldots\ldots(I_C = I_E)$$	**2M**
	(b)	**What is thermal runaway? How it can be avoided?**	**4M**
	Ans:	**Concept of thermal runaway:** 1.We know that $$I_C = \beta\ I_B + (1+ \beta).\ I_{CO}$$ Where I_{CO} is the leakage current and I_{CO} is strongly dependent on temperature. 2. Leakage current approximately doubles for every 10^0 c rise in temperature. 3 As the leakage current of transistor increases, collector current (Ic) increases (1+ β) times. 4. The increase in power dissipation at collector base junction. 5. This in turn increases the collector base junction causing the collector current to further increase.	**2M**

		6. This effect is cumulative and in a fraction of a second Ic becomes so large causing transistor to burn up. This self-destruction of an unstabilized transistor is known as Thermal Runaway.  **<u>Thermal runaway can be avoided by :</u>** 1) Using stabilization circuitry 2) Heat sink	**Diagram : 1M** **1M**
	(c)	**Sketch the drain characteristics of N-channel JFET for various values of V_{GS}. State the condition at which the drain current essentially becomes constant.**	**4M**
	Ans:	**<u>Drain characteristics of N-channel JFET :</u>**  The drain current remains constant at its maximum value i.e. I_{DSS} in the pinch off or saturation region. The drain current in the pinch off region depends upon the gate to source voltage given by $$I_D = (1 - \frac{VGS}{VP})^2$$	**2M** **2M**
	(d)	**Draw and explain the input and output characteristics of CE configuration.**	**4M**
	Ans:	**<u>Input Characteristics-</u>**	**1M**



1M

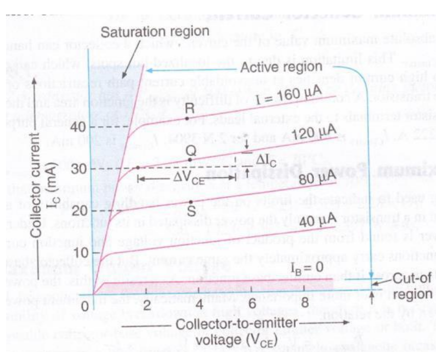
Explanation:

Input Characteristics gives the relationship between the base current I_B and V_{BE} for a constant collector to emitter voltage V_{CE}.

1. There exists a threshold or knee voltage(Vk) below which the base current is very small.The value of knee voltage is 0.5V for silicon and 0.1V for germanium transistors.
2. Beyond the knee, the base currnt(I_B) increases with the increase (V_{BE}) for a constant V_{CE}.
3. As the collector-to-emitter (V_{CE}) is increased above 1 V, the curve shift downwords.

1M

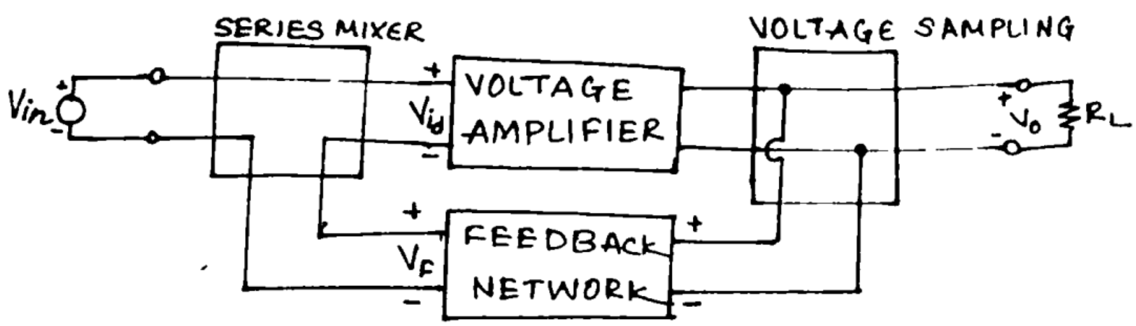
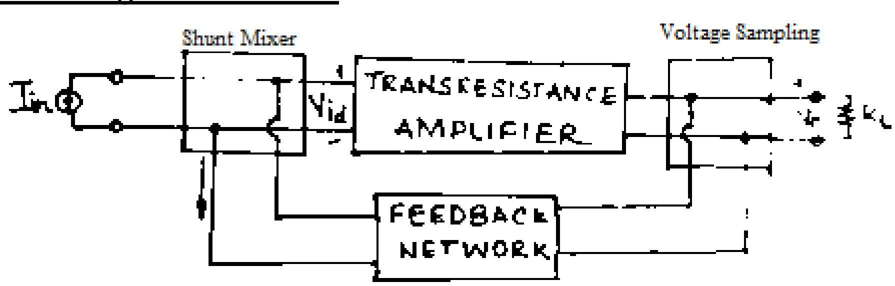
Output Characteristics:

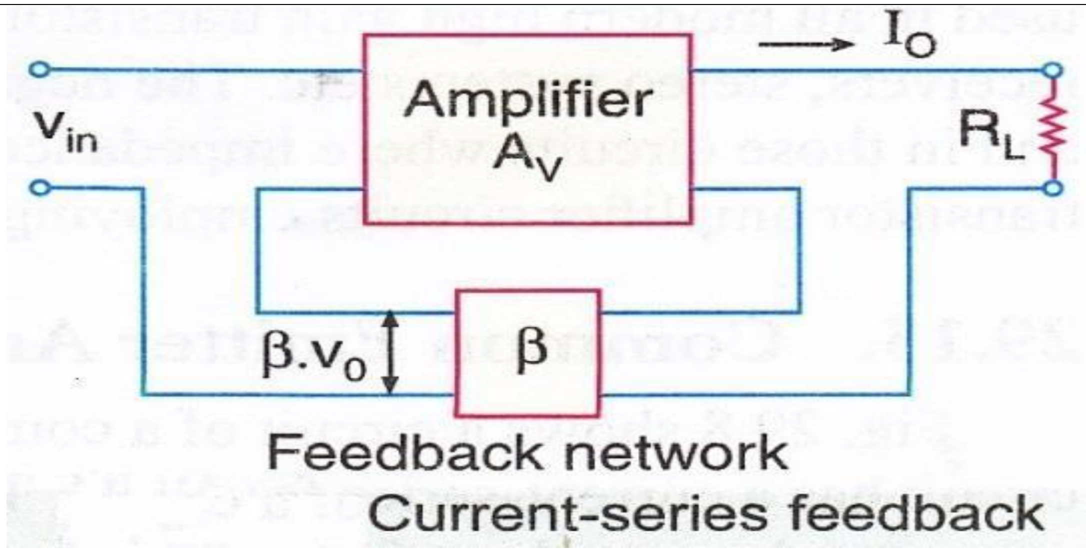
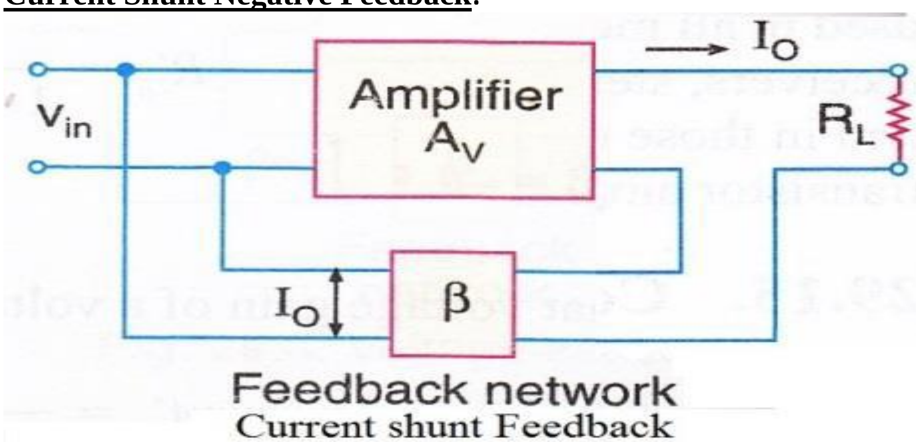
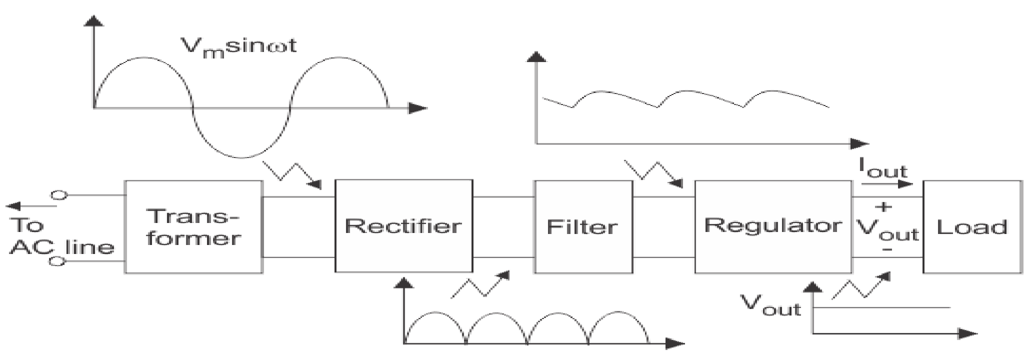


Explanation:-

1M

Output characteristics give the relation between the collector current I_C and V_{CE} for constant

		base current I_B. 1.The output characteristics are be divided into three important regions namely saturation region, active region and cut-off region. 2.As the collector-to-emitter voltage ($V_{CE)}$is incresse above zero,the collector current (I_C) increases rapidly to a saturation value, depending upon the value of base current. 3.When collector-to emitter voltage (V_{CE}) is increase further , the collector current slightly increases. 4.When base current is zero, a small collector current exists. This is called leakage current.	
	(e)	**List different types of negative feedback. Draw their diagrams.**	**4M**
	Ans:	**<u>Types of negative feedback connection:</u>** 1. Voltage series 2. Voltage shunt 3. Current series 4. Current shunt ***<u>Note: Any one diagram should be considered</u>*** **<u>Voltage Series Negative Feedback:-</u>**  **<u>Voltage Shunt Negative Feedback</u>:-**  **<u>Current Series Negative Feedback:-</u>**	**2M** **2M**

		 Current-series feedback **Current Shunt Negative Feedback:-**  Current shunt Feedback	
	(f)	**Explain the block diagram of regulated power supply and also state its need.**	**4M**
	Ans:	**Diagram:**  Block diagram of a regulated Dc power supply consist of the following blocks namely:	**2M** **1M**

1) Transformer + Rectifier
2) Filter
3) Voltage regulator.

1. **Transformer**:- The AC main voltage is applied to a step down transformer. It reduces the amplitude of ac voltage and applies it to a rectifier.
2. **Rectifier**: The rectifier is usually Centre tapped or bridge type full wave rectifier. It converts the ac Voltage into a pulsating dc voltage.
3. **Filter**: The pulsating dc (or rectified ac) voltage contains large ripple. This voltage is applied to the Filter circuit and it removes the ripple. The function of a filter is to remove the ripples to provide pure DC voltage at its output. This DC output voltage is not a steady DC voltage but it changes with the change in load current. It has poor load and line regulation. The voltage obtained so is the unregulated DC voltage.
4. **Voltage Regulator**: The unregulated DC voltage is applied to a voltage regulator makes this DC

1M

Necessity of regulated power supply:

The major disadvantage of a power supply is that the output voltage changes with the variations in the input voltage or The D.C output voltage of the rectifier also increase similarly, In many electronic applications, it is desired that the output voltage should remain constant regardless of the variations in the input voltage or load. In order to get ensure this; a voltage stabilizing device called voltage regulator is used.

Q. 3 **Attempt any FOUR :** **16M**

(a) **Compare CB, CC& CE configurations. (any 4 points)** **4M**

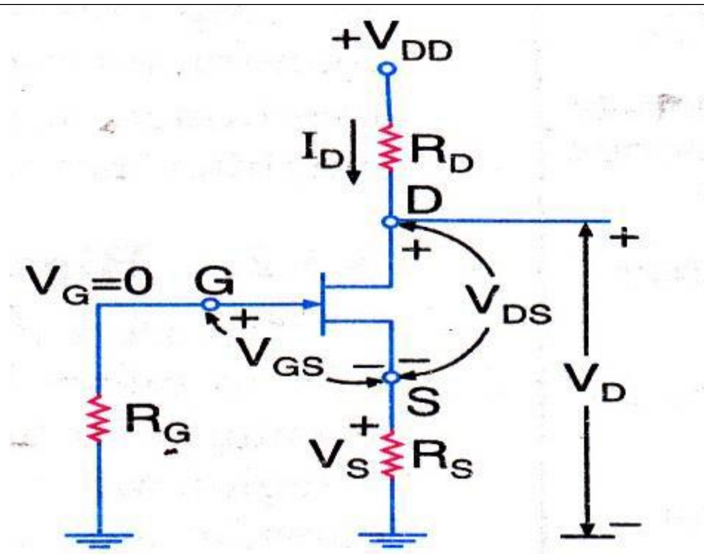
Ans: **4M- each point 1M**

Parameters	CB	CE	CC
Input Impedance	Low(100Ω)	Low(750Ω)	Very High(750KΩ)
Output Impedance	Very High(450KΩ)	High(45kΩ)	Low(50Ω)
Current Gain	Less than unity	High (100)	High(100)
Voltage Gain	High(About150)	Very high(about 500)	Less than 1

(b) **With the help of neat circuit diagram explain the working of self bias method for FET.** **4M**

Ans:

Diagram:



2M

Explanation:

2M

Fig shows the circuit of source biasing for JFET. FET gate is grounded via a resistor RG. This type of biasing uses ± supply voltages as shown in fig. in this case the circuit behaves as a potential divider bias circuit with VG equal to VSS

D.C. analysis:-

From the circuit:-

For V_{GS} apply KVL as shown –

$$V_{GS} – I_D R_S + V_{SS} = 0$$
$$V_{SS} = V_{GS} + I_D . R_S$$
$$V_{GS} = V_{SS} – I_D . R_S$$

Expression for V_{DS},

Apply KVL to the drain circuit

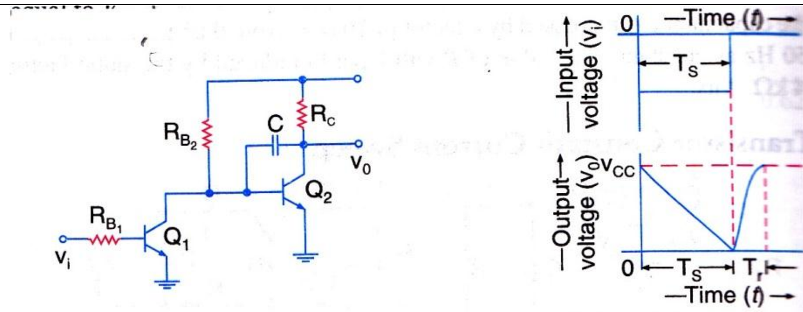
$$V_{DD} – I_D R_D - V_{DS} – I_D R_S + V_{SS} = 0$$
$$V_{DD} + V_{SS} = I_D (R_D + R_S) + V_{DS}$$
$$V_{DS} = V_{DD} + V_{SS} – I_D (R_D + R_S)$$

The value of the drain current can be obtained by Shockley's equation. Thus the Q point of JFET amplifier using source biasing is given by.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{DS(off)}}\right)^2$$

$$V_{DS} = V_{DD} + V_{SS} – I_D (R_D + R_S)$$

(c)	**Draw and explain the working of miller sweep generator.**	4M
Ans:	**Diagram:**	2M



(a) Miller sweep circuit.

(b) Associated input and output waveforms.

Working:

- Consider initially the transistor Q_1 is ON and Q_2 is OFF. The output voltage is equal to V_{CC}. **2M**
- When a pulse of negative polarity is applied at the base of the transistor Q_1.The emitter-base junction of the transistor Q_1 is reverse biased and it turns OFF. This causes the transistor Q_2 to turn ON.
- As the transistor Q_2 conducts, the output voltage begins to decrease towards zero. The time constant of the discharge is given by the relation,

$$\tau = R_B * C$$

- When the input pulse is removed, the transistor Q_1 turns ON and Q_2 turns OFF.As the transistor Q_1 turns OFF, the capacitor (C) charges quickly, through resistor R_C to V_{CC} with a time constant (τ) equal to R_{CC}. The waveform of the generated sweep or the output voltage (v_0).

(d) Describe how excellent impedance matching is achieved with transformer coupling. **4M**

Ans: **4M**

- Transformer coupled amplifiers provide excellent impedance matching between the individual stages. This ability makes it very useful in a multistage amplifier as a final stage.
- It is used to transfer power to the low impedance load (such as speaker). The impedance of a speaker varies from 4 Ω to 16 Ω, whereas the output resistance of a transistor amplifier is several hundred ohms.
- In order to match the load impedance, with that of the amplifier output, a step-down transformer of proper turns ratio is used. The resistance of the secondary winding of the transformer is made equal to the speaker impedance, while that of the primary winding is made equal to the output resistance of the amplifier.

(e) State load and line regulation. **4M**

Ans: **Load Regulation:** **1M**

It is defined as the change in output voltage when the load current is changed from zero (no load) to maximum (full load) value. Mathematically it is expressed as,

Load Regulation== $\frac{VNL-VFL}{VFL}$ **, Vin Constant** **1M**

Where
V_{NL} = Voltage at no load (IL = 0)
V_{FL} voltage at full load (IL = IL Max)

Line Regulation: — 1M

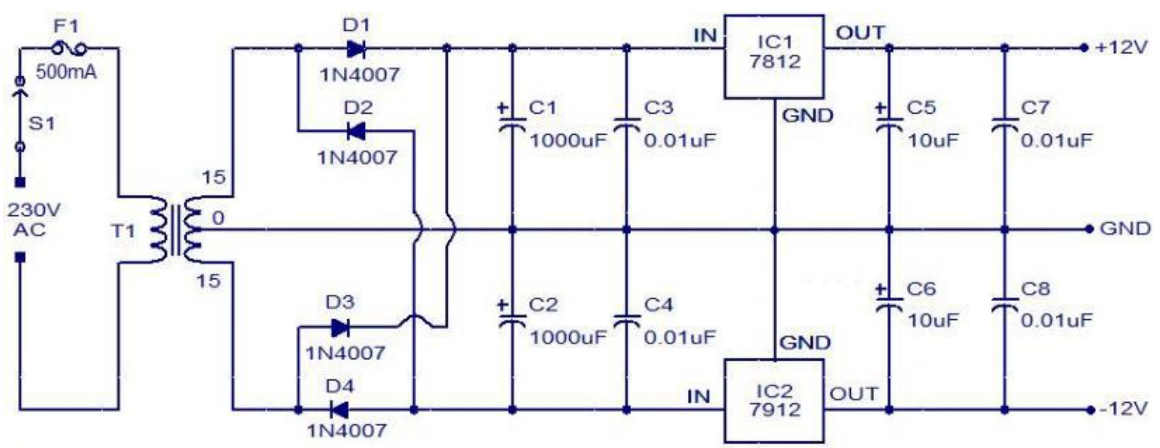
The change in output voltage with respect to per unit change in input voltage is defined as line regulation. It is mathematically expressed as,

$$\textbf{Line regulation} = \Delta V_L / \Delta V_S$$ — 1M

Where,
ΔV_L = The change in output voltage
ΔV_S= The change in input voltage

(f) Draw the dual power supply capable of giving ± 12 V using three terminal regulator IC's and describe its working. — **4M**

Ans: **Diagram:** — **3M**



Working: — **1M**

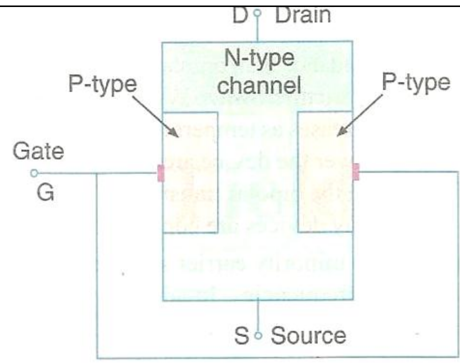
1. A full wave rectifier & filter produces the unregulated D.C input to the regulatorIC7812 and IC7912.
2. IC 7812 produces a fixed positive voltage of +12 V.
3. IC 7912 produces a fixed positive voltage of -12 V
4. The output capacitor C_7 and C_8 is used for improving the transient response of IC. This capacitor also helps in reducing the noise present at the output due to load variations.

Q. 4 Attempt any FOUR : — **16M**

(a) Explain the construction and working of N-channel JFET. — **4M**

Ans:

Construction of N-Channel JFET: — **1½M**



(*a*) N-channel.

Construction Explanation: **1½M**

- It consists of an N-type semiconductor bar with two P type heavily doped regions diffused on opposite sides of its middle part.
- P-type regions from two PN junctions. The space between the junctions (i.e. N-type regions) is called a channel.
- Both the P-type regions are connected internally & a single wire is taken out in the form of a terminal called the gate (G).
- The electrical connections called ohmic contacts are made to both ends of the N type semiconductor & are taken out in the form of two terminals called drain (D) & source (S).

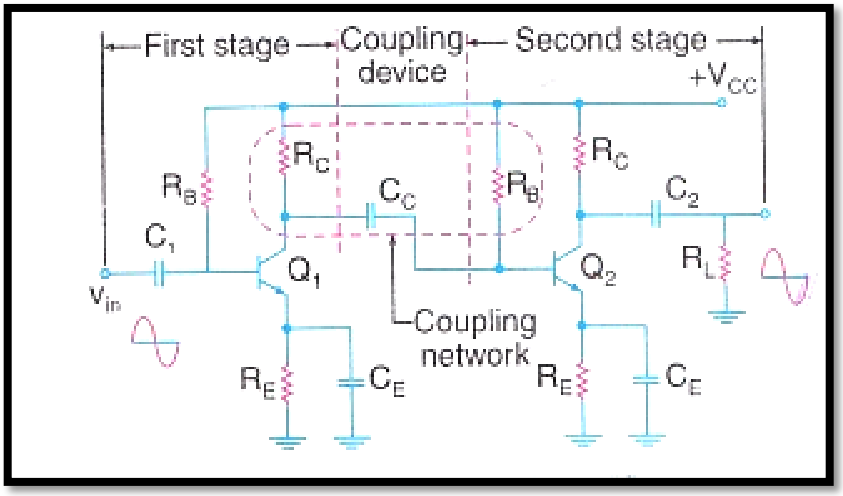
Working of N-channel JFET: **1M**

- The application of negative gate voltage or positive drain voltage with respect to source, reverse biases the gate- source junction of an N-channel JFET and forms depletion regions within the channel.
- When a voltage is applied between the drain & source with dc supply voltage (V_{DD}), the electrons flows from source to drain through the narrow channel existing between the depletion regions causes the drain current (I_D) & its conventional direction is from drain to source.
- The value of drain current is maximum, when no external voltage is applied between the gate & source & is designated by the symbol I_{DSS}.
- When V_{GG} is increased, the reverse bias voltage across gate-source junction is increased. As a result of this depletion regions are widened. This reduces the effective width of the channel & therefore controls the flow of drain current through the channel.
- When gate to source voltage (V_{GG}) is increased further, a stage is reached at which two depletion regions touch each other as shown in fig (b).
- At this value of V_{GG} channel is completely blocked or pinched off & drain current is reduced to zero. The value of V_{GS} at which drain current becomes zero is called pinch off voltage designated by the symbol V_P or $V_{GS(OFF)}$. The value of V_P is negative for N-channel JFET.

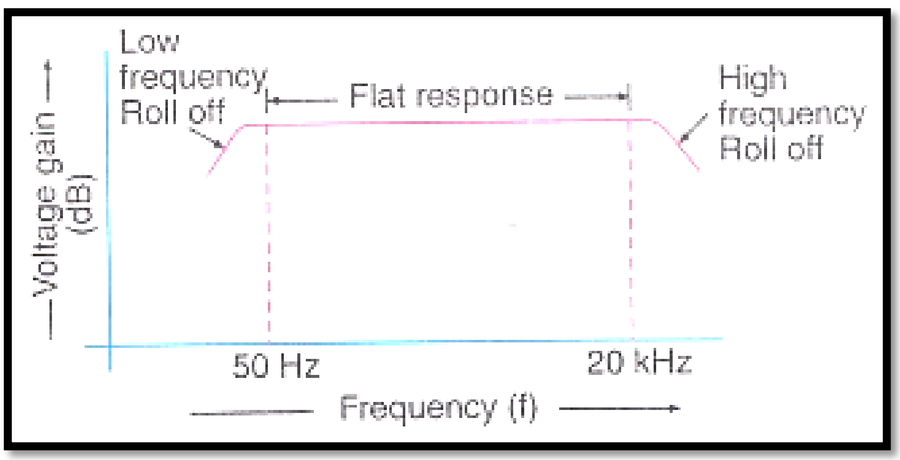
(b) **Draw the circuit diagram and frequency response of two stage RC coupled amplifier.** **4M**

Ans:

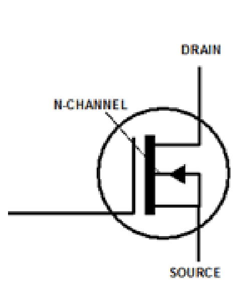
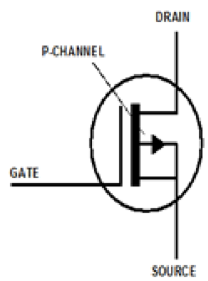
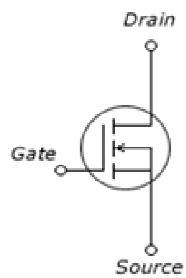
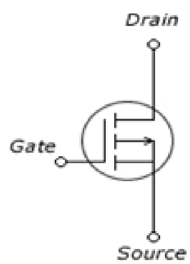
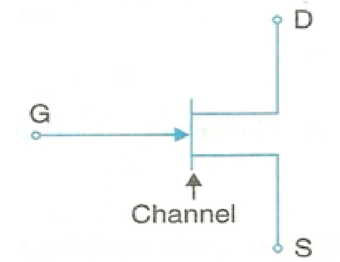
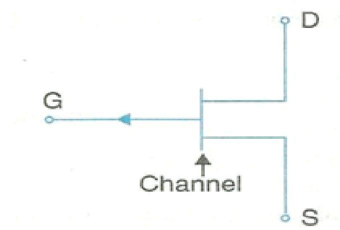
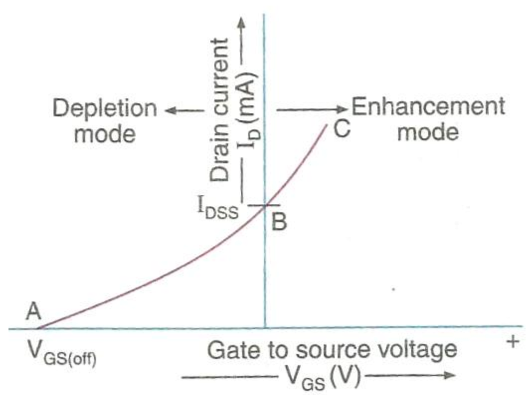
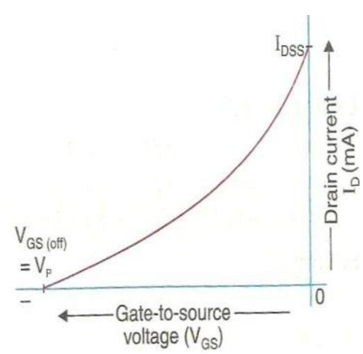
Circuit Diagram:

<table>
<tr><td></td><td></td><td>


FREQUENCY RESPONSE OF RC COUPLED AMPLIFIER:



</td><td>(Circuit Diagram 2M & Frequency response 2M)</td></tr>
<tr><td></td><td>(c)</td><td>Differentiate the MOSFET and FET for the following points :
(i)Schematic symbol
(ii)Trans conductance curve
(iii)Modes of operation
(iv)input impedance</td><td>4M</td></tr>
<tr><td></td><td>Ans:</td><td></td><td></td></tr>
</table>

Parameter	MOSFET	FET
Schematic Symbol	 N-channel Depletion MOSFET  P-channel Depletion MOSFET  N-channel Enhancement MOSFET  N-channel Enhancement MOSFET **(NOTE : any one symbol can be considered)**	 (a) N-Channel.  (a) P-Channel. **(NOTE : any one symbol can be considered)**
Trans conductance curve		
Modes of operation	Depletion mode and Enhancement mode	Depletion Mode only
Input impedance	Very High	High

1M for each point

(d) **Compare the small signal; amplifier and power amplifier w.r.to following points :**
(i)Input voltage
(ii)output power
(iii)output impedance
(iv)Applications

4M

Ans:

Parameter	Small signal amplifier	Power Amplifier
Input voltage	LOW(few mV)	HIGH(2-4 V)
output power	LOW	HIGH
output impedance	HIGH(4-10 kΩ)	LOW(5-20Ω)
Applications	Used as pre-amplifier	Used in output stage

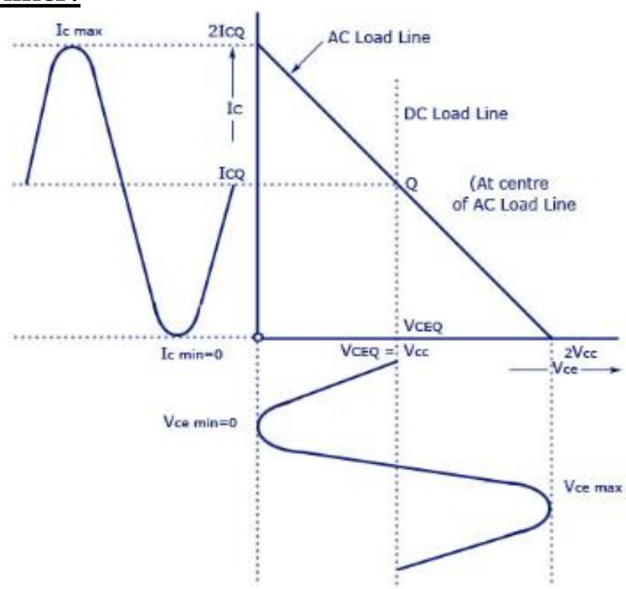
(1M for each point)

(e) **Sketch the output waveforms of class A, class AB and class C with respect to operating point on load line.** **4M**

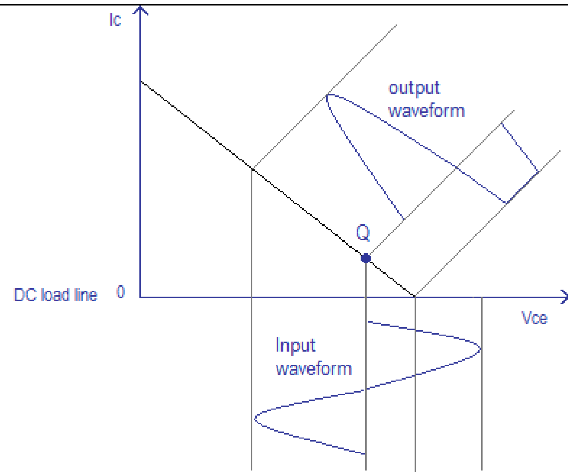
Ans:

(1M for each waveform and 1M for correct labeling)

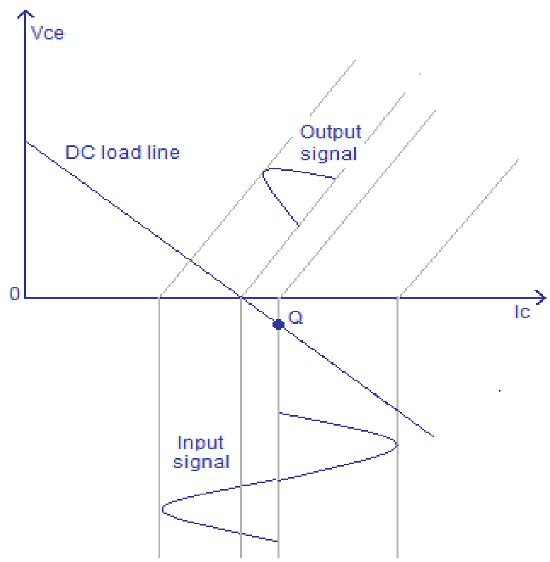
Class-A Power amplifier:



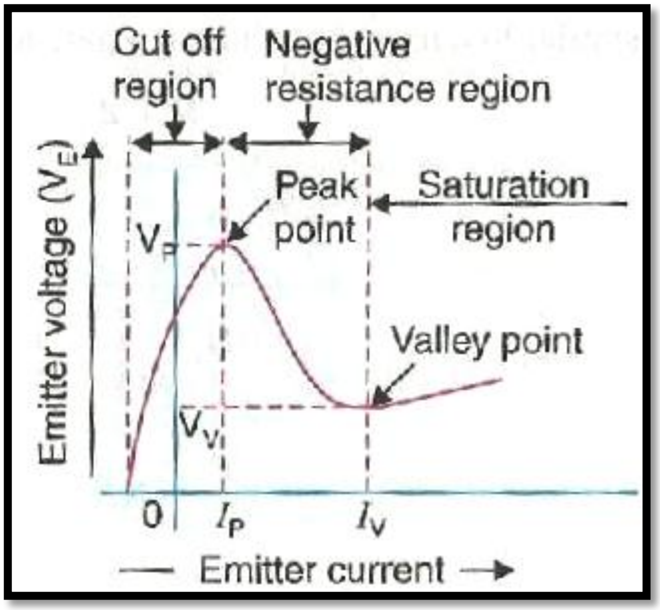
Class-AB Power amplifier:



Class C Power amplifier:



(f)	**Draw V-1 characteristic of UJT. State any two applications of UJT.**	**4M**
Ans:	**V-1 characteristic of UJT:**	**2M**

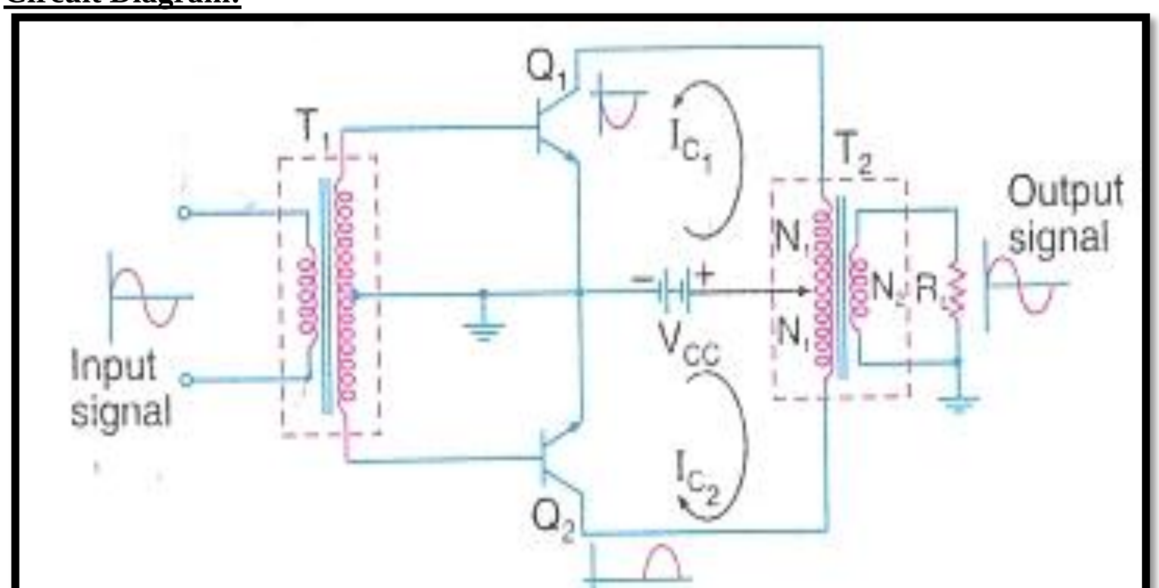


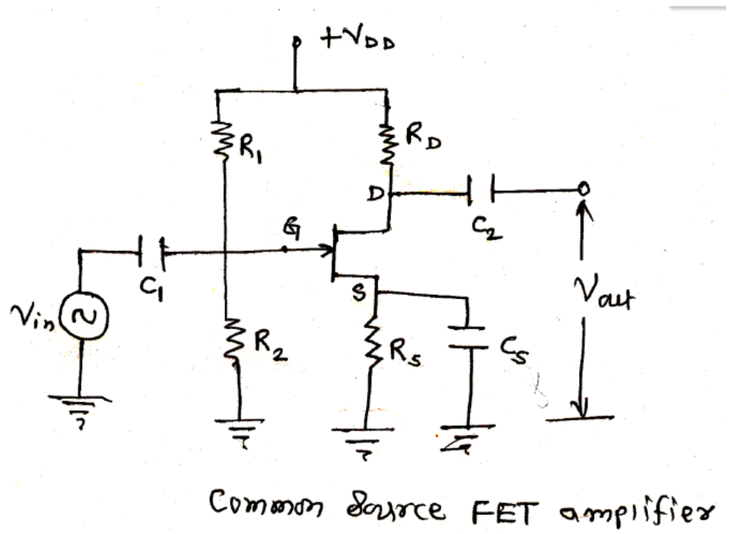
Applications of UJT: (Any two can be considered)

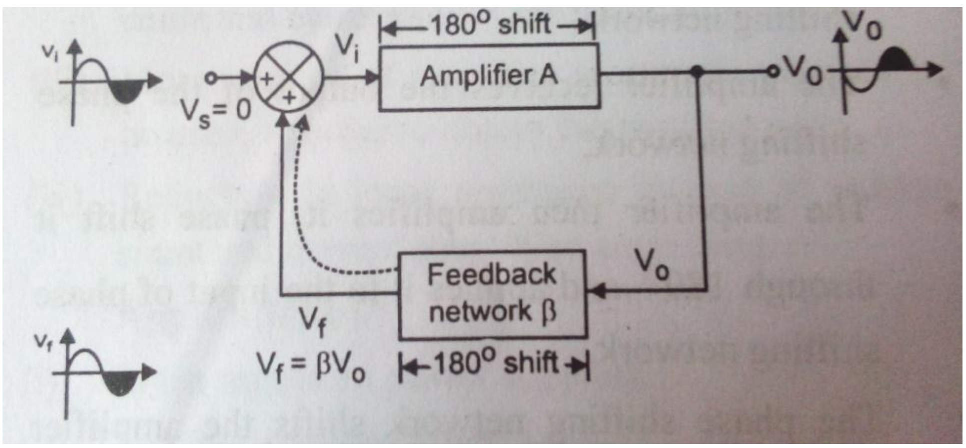
- It is used as trigger device for SCR's and TRIAC's.
- It is used as non-sinusoidal oscillator.
- It is used as saw-tooth generator.
- It is used as timing circuits.

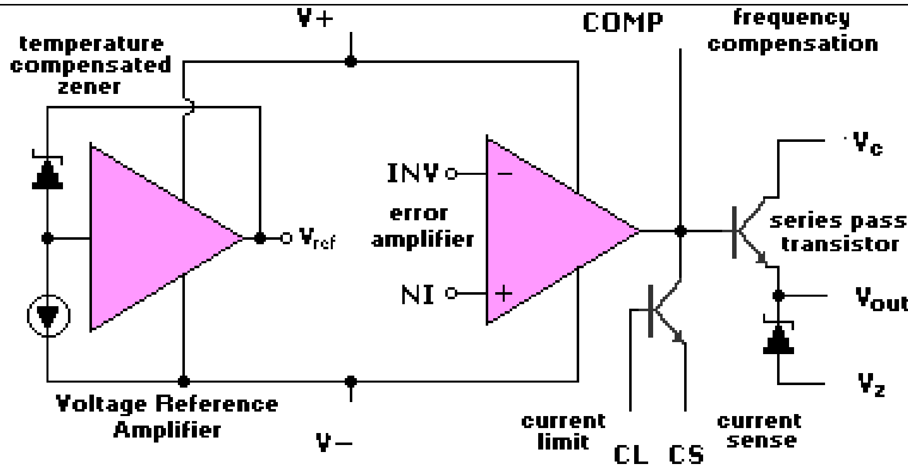
(1M for each Application)

Q.5		**Attempt any FOUR :**	**16**
	(a)	**Derive relation between α & β with respect to BJT.**	**4M**
	Ans:	**Relation between α& β:** Current gain (**α**) of CB configuration = $\frac{I_C}{I_E}$ Current gain of (**β**) of CE configuration = $\frac{I_C}{I_B}$ We know that ; $I_E = I_B + I_C$……………………..(1) Dividing equation (1) by I_C $\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$ Therefore $\frac{1}{\alpha} = \frac{1}{\beta} + 1$ [since $\alpha = \frac{I_C}{I_E}$, $\beta = \frac{I_C}{I_B}$] Therefore $\frac{1}{\alpha} = \frac{1+\beta}{\beta}$ $\alpha(1 + \beta) = \beta$ $\alpha + \alpha\beta = \beta$ $\alpha = \beta - \alpha\beta$ $\alpha = \beta(1 - \alpha)$	**½M** **½M** **2M**

		Therefore $\beta = \frac{\alpha}{1-\alpha}$ OR $\alpha = \frac{\beta}{1+\beta}$	**1M**
	(b)	**The phase shift oscillator uses equal resistance of 1 MΩ & equal capacitances of 68PF. At what frequency does the circuit oscillate? And also find value of resistance to produce a frequency of 800 kHz if phase shift oscillator uses 5PF capacitor.**	**4M**
	Ans:	Q. 5 (b). 2M for part (i) & 2M for part (ii) (i) Given : Phase shift oscillator, $R = 1M\Omega$ $C = 68pF$. Calculate : frequency of operation = ?. Formula : $f = \frac{1}{2\pi RC\sqrt{6}}$ Solution : $f = \frac{1}{2\pi RC\sqrt{6}}$ $= \frac{1}{2\pi \times 1M \times 68p \times \sqrt{6}}$. $= 955.51\ Hz$. ∴ frequency of oscillations = 955.51 Hz. (ii) Given : Phase shift oscillator, $f = 800\ KHz$. $C = 5pF$. Calculate : R = ? Formula : $R = \frac{1}{2\pi fC\sqrt{6}}$ Solution : $R = \frac{1}{2\pi fC\sqrt{6}}$ $= \frac{1}{2\pi \times 800kHz \times 5pF \times \sqrt{6}}$ $= 16.24\ M\Omega$. ∴ Required resistance is 16.24 MΩ for 800kHz freq..	**2M** **2M**
	(c)	**Explain the working of class-B push-pull amplifier.**	**4M**
	Ans:	**<u>Circuit Diagram:</u>**  **<u>Circuit Description:</u>** • The circuit consists of two centre tapped transformers T_1 & T_2& two identical transistors Q_1& Q_2.	**(2M circuit diag. ,2M working)**

		• The transformer T_1 is an input transformer and is called as phase splitter. It is required to produce two signal voltages, which are 180° out of phase with each other. • These two signal voltages with opposite polarity, drive the input of transistors Q_1& Q_2.. • The transformer T_2 is an output transformer and is required to couple the a.c. output signal from the collector to the load. • The transistors Q_1 and Q_2 are biased at cut off. • The two emitters are connected to the centre tap of transformer T_1 secondary and the V_{CC} supply to the centre tap of transformer T_2 secondary. **Working:** • When there is no a.c. input signal is applied both the transistors Q_1& Q_2 are cut off. Hence no current is drawn from V_{CC}. • DURING POSITIVE HALF CYCLE: The base of the transistor Q_1 is positive and that of Q_2 is negative. As a result of this Q_1 conducts, while the transistor Q_2 is OFF. • DURING NEGATIVE HALF CYCLE: The base of the transistor Q_2 is positive and that of Q_1 is negative. As a result of this Q_2 conducts, while the transistor Q_1 is OFF. • Thus at any instant any one transistor in the circuit is conducting. • Then the output of the transformer joins these two halves & produces a full sine wave in the load resistor.	
	(d)	**Explain with neat sketch how FET can be used as an amplifier.**	**4M**
	Ans:	**Circuit Diagram:**  **Operation: -** When small a.c. signal is applied to the gate, its produces variation in the gate to source	**2M**

		voltage. This produces variation in the drain current. As the gate to source voltage increases the current also increases. As the result of this voltage drop across RD also increases. This causes the drain voltage to decreases. In positive half cycle of the input ac signal the gate to source voltage becomes less negative. This will increase the channel width and increase the level of drain current ID. Thus IDvariessinusoidally above its Q point value. The drain to source voltage V_{DS} is given by $V_{DS} = V_{DD} - I_D R_D$. Therefore as I_D increases the voltage drop $I_D R_D$ will also increase and voltage V_{DS} will decrease. If $\Delta I_D$is large for a small value of ΔV_{GS}, the ΔV_{DS} will also be large and we get amplification. Thus the AC output voltage V_{DS} is 180º out of phase with AC input voltage.	2M
	(e)	**State Barkhausen criterion of oscillation.**	4M
	Ans:	 An amplifier will work as an oscillator if and only if it satisfies a set of conditions called Barkhausen's criterion. It states that: • An oscillator will operate at that frequency for which the total phase shift around loop equals to 0◦ or 360◦. • At the oscillator frequency, the magnitude of the product of open loop gaun of the amplifier A and the feedback factor β is equal or greater than unity. ie. $A\beta \geq 1$	**2M for each condition**
	(f)	**Draw the functional block diagram of IC 723. State any two features of 723.**	4M
	Ans:	**<u>Functional block diagram of IC 723:</u>**	**(2M Functional B.D. and 1M each feature)**

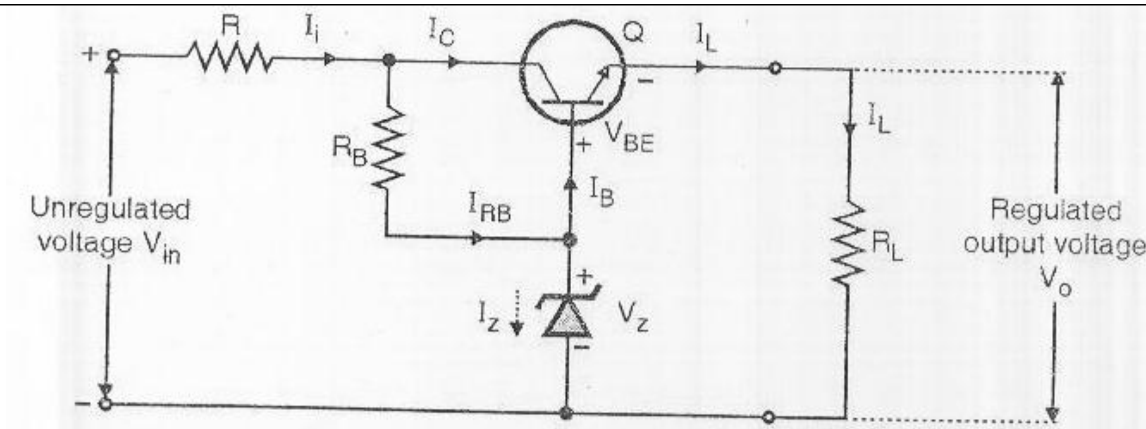


Features of 723:

(Any 2 features can be considered)

1.Unregulated dc supply voltage at the input between 9.5V and 40V.
2. Adjustable regulated output voltage between 2 to 37V.
3. Maximum load current of 150mA.
4. Positive or negative supply operation.
5. Internal power dissipation of 800Mw.
6. Built in fold back current limiting.
7. Built in short circuit protection.
8. High ripple rejection.

Q.6		**Attempt any FOUR :**	**16M**
	(a)	**Discuss steps to be taken to design transistor biasing and stabilizing circuit.**	**4M**
	Ans:	• Transistor biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor. • Establishing correct operating point requires proper selection of bias resistors and load resistors to provide the appropriate input current and collector voltage conditions. • The biasing network should ensure proper zero signal collector current. • The biasing network should ensure that V_{CE} does not fall below 0.5V for Ge transistors and 1V for Si transistors at any instant and it should also ensure the stabilization of operating point. • Once stabilization is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor i.e operating point is fixed.	**Explanation : 4M**
	(b)	**Draw circuit diagram of transistorised series voltage regulator and explain its working.**	**4M**
	Ans:	**Circuit Diagram :**	**2M**



2M

Explanation :

- In this circuit transistor Q acts as a control element. This transistor Q is connected in series with the load hence the circuit is called as Series Voltage Regulator. Other components in the circuit are Zener diode (V_Z), and two resistors R & R_B.
- Zener diode V_Z is operated in breakdown region and provides constant voltage V_Z.
- Resistance R_B provides the limiting current to Zener diode.
- The total current in the circuit is decided by resistance R.
- As V_Z& V_{BE} of the transistor are constant, output voltage across R_L will also be constant. To find output voltage V_O,

Applying KVL to o/p loop of the circuit

$$V_{BE} + I_L R_L – V_Z = 0$$

$$\text{Therefore, } V_O = I_L R_L = V_Z – V_{BE}$$

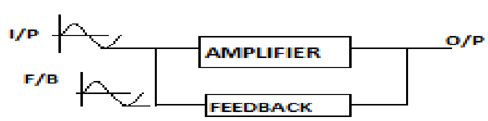
$$\mathbf{V_O = V_Z – V_{BE}}$$

As V_{BE} is constant (approx. 0.6V to 0.7V).

Therefore output voltage of this circuit is decided by Zener diode V_Z.

(c) **State the meaning of positive and negative feedback with neat sketch.** **4M**

Ans: **Positive feedback:** If the feedback signal (Voltage or current) is applied in such a way that it is in phase with input signal and thus increases it, then it is called as positive feedback. It is also called as regenerative feedback or direct feedback. **2M**

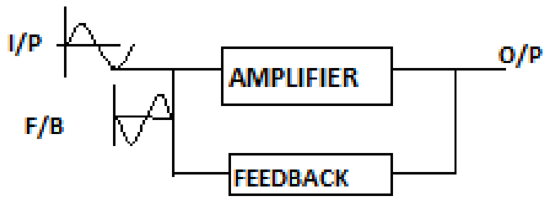
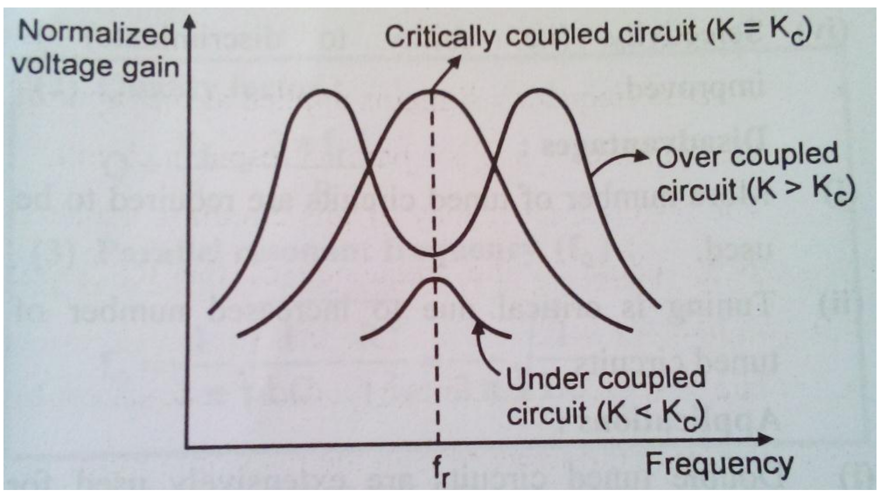


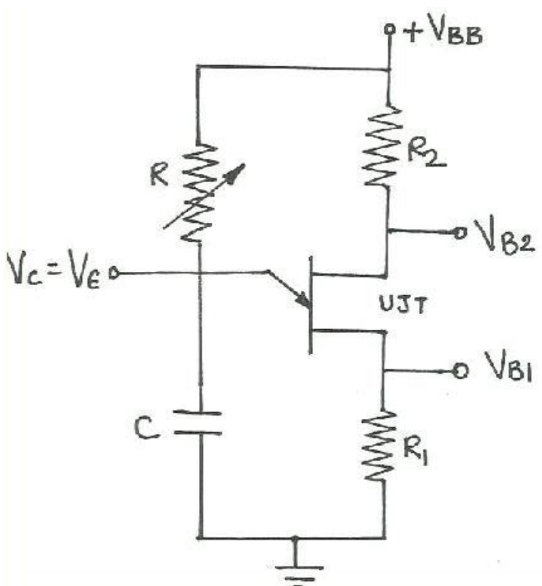
POSITIVE FEEDBACK

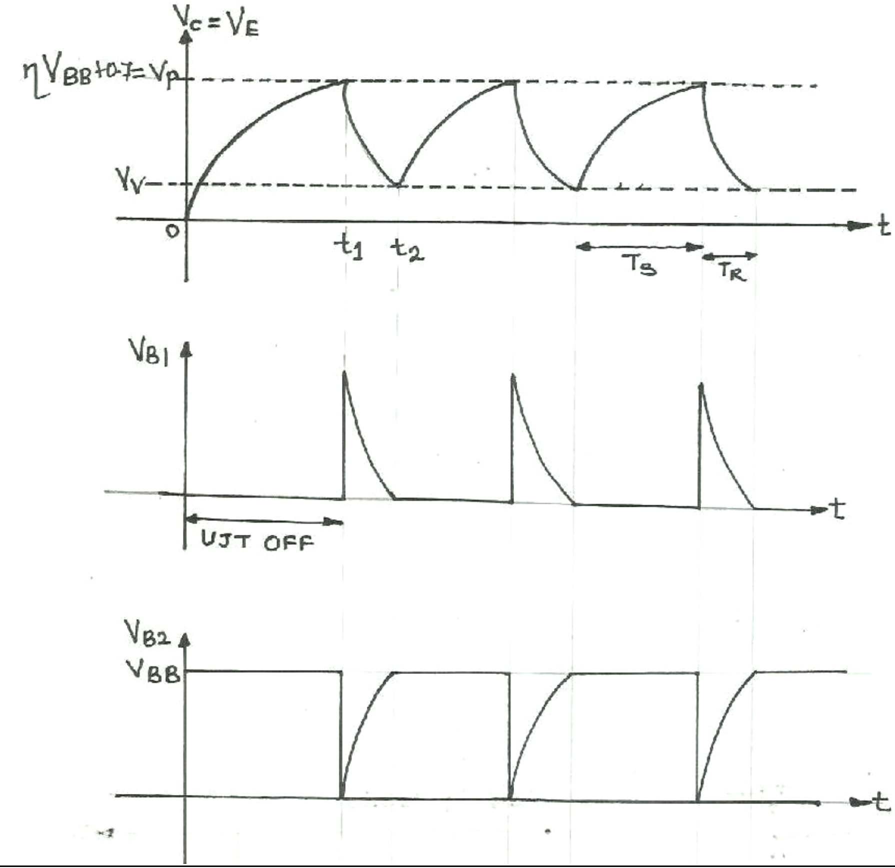
Overall phase shift is 0^0 or 360^0. The voltage gain of positive feedback is given by,

$$Av = \frac{Av}{1- \beta Av}$$

Negative feedback : If the feedback signal (voltage or current) is applied in such a way that it is out of phase with the input signal and thus decreases it, then it is called as negative feedback. It is also called as degenerative feedback or inverse feedback. **2M**

		 NEGATIVE FEEDBACK Overall phase shift is 180^0. The voltage gain of negative feedback is given by, $$Av = \frac{Av}{1+\beta Av}$$	
	(d)	**Plot frequency response of doubled tuned amplifier and explain it.**	**4M**
	Ans:	**Frequency Response :**  **Explanation :** A plot of normalized voltage gain at resonance as a function of frequency for different values of K is shown: 1. The gain of double tuned amplifier at resonance is a function of K and is maximum at critical coupling ie K = Kc. 2. If actual K, coefficient of coupling is less than coefficient of critical coupling ie. K<Kc ,circuit is under coupled and the response resembles usual resonance curve except that the top of the curve is somewhat flat near resonance. 3. And when K>Kc circuit is over coupled. The over coupled circuit has two peaks in response characteristics one on each side of resonant frequency.	**2M** **2M**
	(e)	**The ac equivalent circuit of crystal has these value L = 1H, C = 0.01 PF, R = 1000 Ω & C_m =20 PF. determine the series resonant and parallel resonant frequencies.**	**4M**
	Ans:	**Given**: L = 1H C = 0.01 PF R = 1000 Ω C_m =20 PF	

		Required: fs (series) = ? **fs (parallel) = ?** **<u>For series resonant :</u>** $$fs = \frac{1}{2\pi\sqrt{LC}}$$ $$fs = \frac{1}{2\pi\sqrt{1 * 0.01 * 10^\wedge - 12}}$$ = 1.591 MHz	**2M**
		<u>For parallel resonant :</u> $$fs = \frac{1}{2\pi\sqrt{L\left(\frac{C*Cm}{C+Cm}\right)}}$$ $$fs = \frac{1}{2\pi\sqrt{1\left(\frac{0.01*10^{-12}*20*10^\wedge-12}{0.01*10^{-12}+20*10^\wedge-12}\right)}}$$ = 1.591 MHz	**2M**
	(f)	**Draw circuit diagram & waveform of voltage sweep generator using UJT.**	**4M**
	Ans:	**<u>Circuit Diagram :</u>**  **<u>Waveforms :</u>**	**2M**

		Vc = VE ηVBB+0.7=Vp Vv 0 t t1 t2 Ts TR VB1 UJT OFF VB2 VBB	**2M**