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Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more.Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the Figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any Equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant Values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

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Q.1 a) Attempt any SIX of the following.   **12M**

i.   Define:

1) input bias current

2) input offset current

Ans: (*Input bias current: 1Marks & Input offset current: 1Marks*)

1) Input bias current:
An input bias current I_B is defined as the average of the two input bias current, I_{B1} & I_{B2},
$I_{B=} I_{B1} + I_{B2}/2$
Where $I_{B1=}$ dc bias current flowing into the non - inverting input
       $I_{B2=}$ dc bias current flowing into the   inverting input.

2) Input offset current:
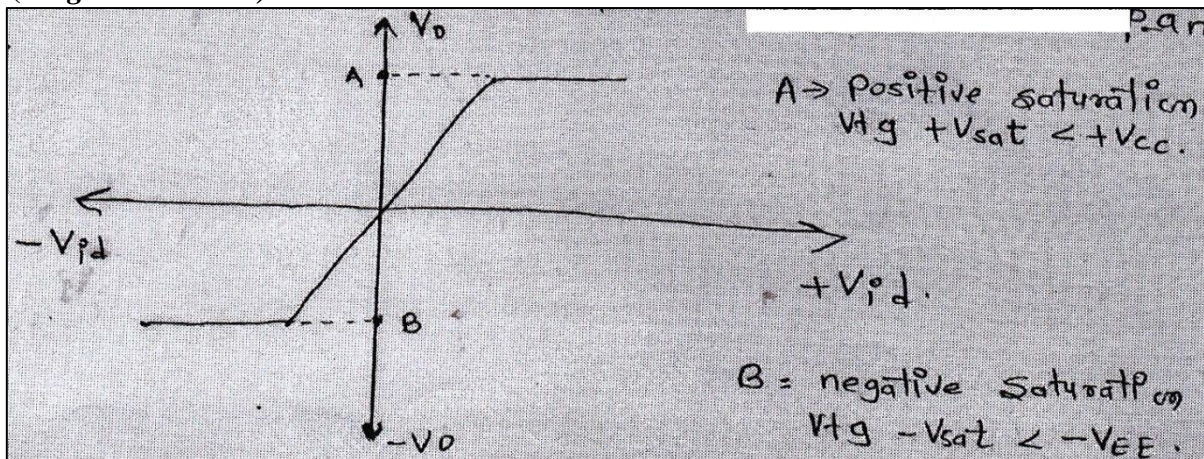The input offset current I_{io} is defined as the algebraic difference between two input bias currents I_{B1} & $I_{B2.}$
$I_{io =}| I_{B1} - I_{B2}|$
Maximum I_{io}= 200nA dc for 741 type op. amp.

**ii.   Draw ideal voltage transfer curve of an op.amp**

Ans: (*Diagram: 2Marks*)

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iii.   **List any four specification of ICLM 324.**

Ans*: (Each Specification ½ Mark)*

- Supply vtg =32 V.
- Differential i/p vtg= -0.3 V to +32 V.
- Operating temp= 0^0c to $+70^0$ c
- Input current =50mA.
- Power dissipation = molded DIP=1130mw
- Cavity DIP= 1260mw.
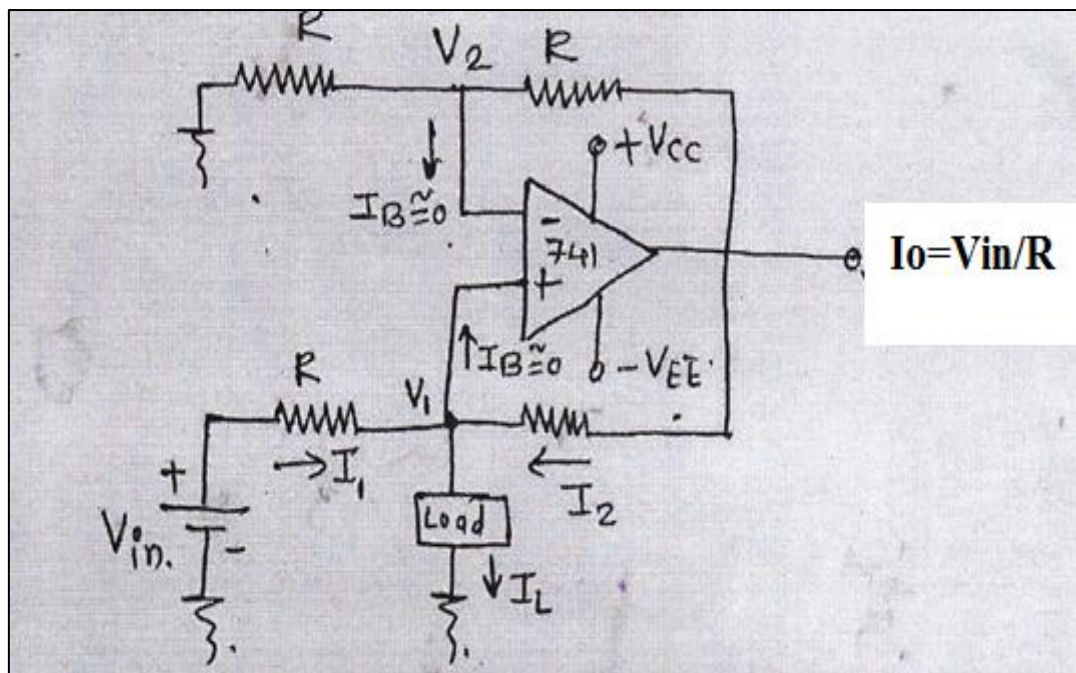
iv.   **Draw the circuit diagram of positive peak detector.**

Ans: (*Diagram: 2Marks*)
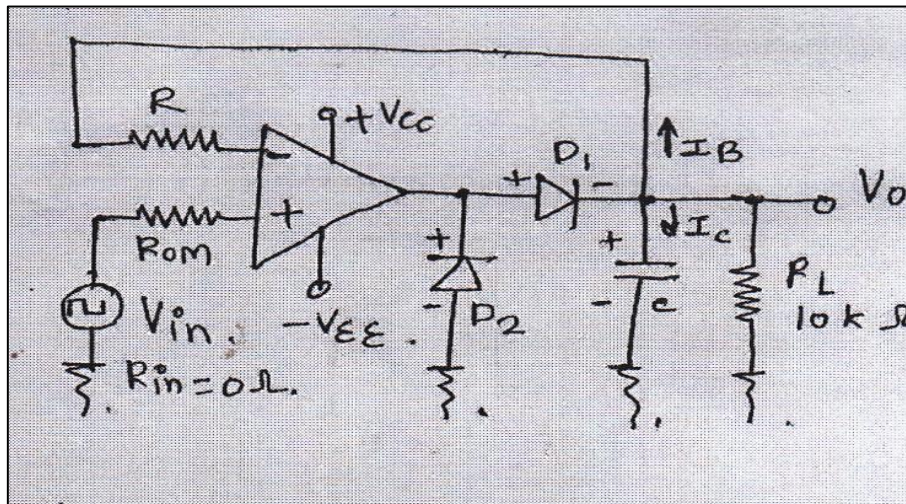
v.   **Draw Voltage to current converter with grounded load.**

Ans: (*Diagram: 2Marks*)

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vi.   **Define :**
   1) Roll-Off Rate
   2) Order Of Filter
Ans: *(Each definition: 1Marks)*

   1) **Roll-off rate:** The gain falls off rapidly in the stop band. The rate at which it falls off is called as the roll-off rate.
      The roll-off rate is decided by order of filter.

   2) **Order of filter:** The high pass & low pass filters the term pole and order will have the same meaning. That means the no. Of poles will equal to the filter order.

vii.   **Draw circuit of notch filter.**
Ans: *(Diagram: 2Marks)*
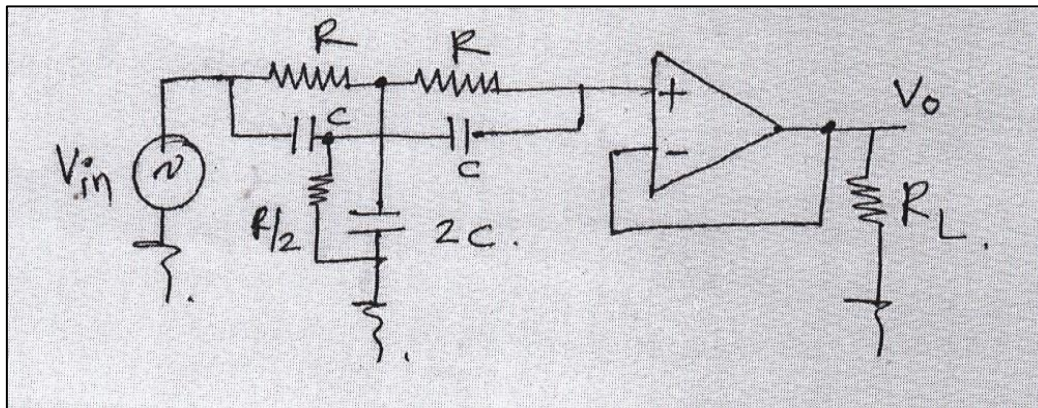
viii.   **State functions of following pins of Ic555.**
   1) Threshold
   2) Discharge
Ans: *(Each function: 1Marks)*

   1) **Threshold:** This is the non-inverting input terminal of comparator 1, which monitors the voltage across the external capacitor. When the voltage across capacitor is greater than threshold voltage $2/3Vcc$, the comparator1 output goes high, which in turn switches the output of the timer low.

   2) **Discharge:** This pin is connected internally to the collector of transistor Q_1, When the output is high Q_1 is off and acts as an open circuit to the external capacitor c connected across it. on other hand, when the output is low, Q_1 is saturated and acts as short circuit, shorting out the external capacitor c to ground.

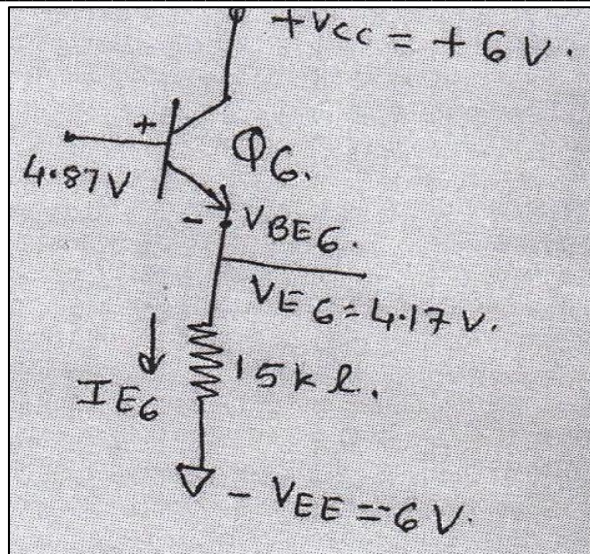**b) Attempt any TWO of the followings: 8M**
   i.   What is the use of level shifter stage? Draw its circuit diagram.
Ans: *(Diagram: 2Marks & Use: 2Marks)*

      Generally, the level shifter circuit is used after the intermediate stage to shift the dc level at the output of the intermediate stage downward to zero volts with respect to ground.

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ii. **State ideal values of following parameters of op-amp as well as state typical values of following parameters of op-amp IC741.**

Ans: *(Any four parameter) & (01 mark for each parameter)*

Parameter	Ideal Value	Typical Value
I/P resistance	$\infty\Omega$	$2M\Omega$
O/P resistance	$0\ \Omega$	$75\ \Omega$
Vtg gain	∞	2×10^{5}
Bandwidth	∞	1 MHz
CMRR	∞	90 dB
Slew rate	∞	0.5 V/µSec
offset Vtg	0	2 mV

iii) Draw and explain ideal voltage transfer curve of op-amp.
Ans: *(Diagram: 2Marks & Explanation: 2Marks)*
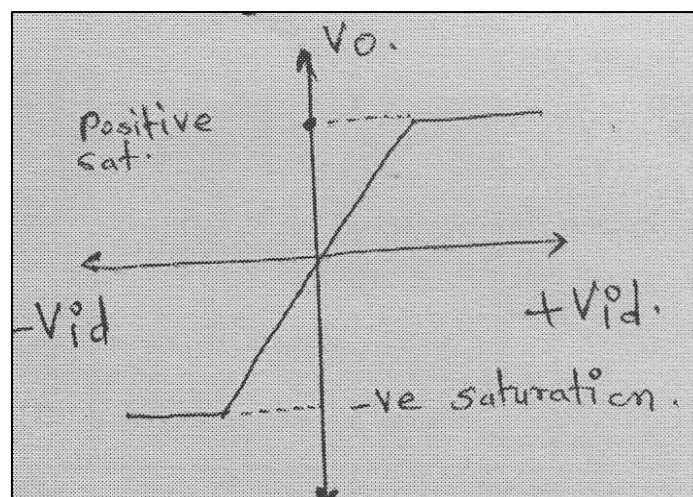
Output voltage V_0 is plotted against input difference voltage V_{id}, Keeping gain A constant.

1) The output vtg cannot exceed the positive and negative saturation voltages. These saturation voltages are specified by an output vtg, swing rating of the op-amp for given values of supply voltage.

2) This means that the output voltage is directly proportional to the input difference voltage only until it reaches the saturation voltage and that thereafter output voltage remains constant. The curve is called ideal because output offset voltage is assume to be zero.
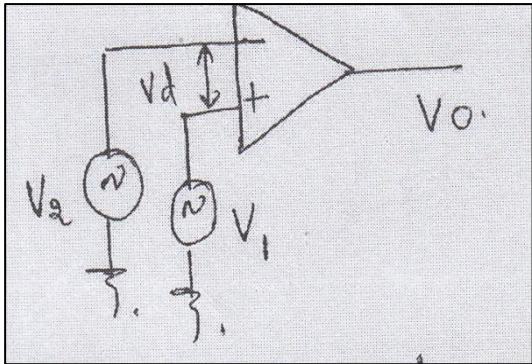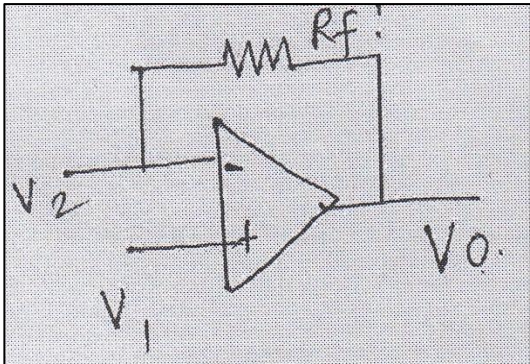
Q.2 Attempt any <u>FOUR</u> of the following.   16M
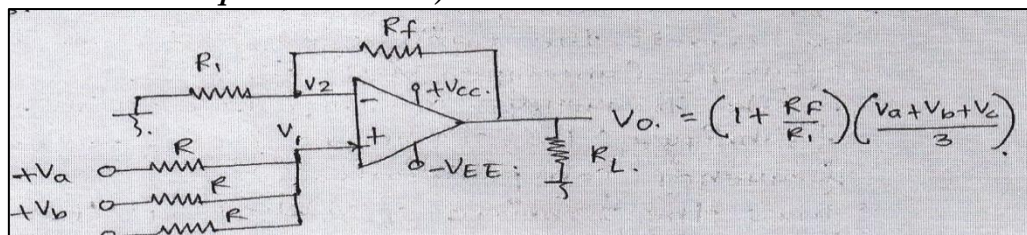 **a) Compare open loop and closed loop configuration of op-amp on following basis:**
  i)   Circuit diagram
  ii) Gain
  iii) Bandwidth
  iv) Application
Ans: *(Each point: 1 mark)*

SR NO.	OPEN LOOP	CLOSED LOOP
1	Circuit Diagram:	Circuit Diagram:
2	Gain high (2×10^5)	Gain low (10, 100 etc)
3	Low	High
4	Comparator	Amplifier

  b) With neat sketch derive the expression for output voltage of non-inverting averaging amplifier.
 Ans: *(Diagram: 2Marks & Equation: 2Marks)*

$$V_o = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{V_a + V_b + V_c}{3}\right)$$

$$V_1 = \frac{R/2}{R + R/2} V_a + \frac{R/2}{R + R/2} V_b + \frac{R/2}{R + R/2} V_c$$

$$V_1 = \frac{V_a}{3} + \frac{V_b}{3} + \frac{V_c}{3} = \frac{V_a + V_b + V_c}{3}$$

output voltage Vo is,

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1$$

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) \frac{V_a + V_b + V_c}{3}}$$

Equation **.:**Shows that the output voltage is equal to the average of all input voltages times the gain of the circuit($1+Rf/ R_1$).Hence it is called as averaging amplifier.

c) **With neat diagram explain the concept of frequency compensation and offset nulling.**
Ans: *(Diagram: 1Marks & Explanation: 1Marks & Offset nulling: 2 Marks)*

In practice all possible efforts are made to convert the multiple break frequency op-amp (uncompensated) into the single break frequency of op-amp using some technique, This technique, is called as frequency compensation.

Thus the technique of modifying the loop gain frequency response of the system op-amp from multiple break frequency to the single break frequency to ensure stability is called as frequency compensation.
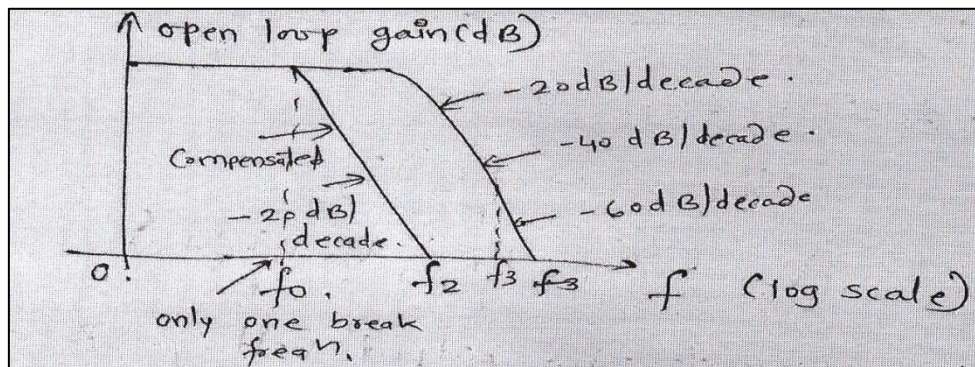
- **Offset nulling:** When both the inputs are connected to the same voltage, the output should be zero, This concept is called as offset nulling.

d) **Draw neat diagram of active integrator and obtain expression for output voltage.**
Ans: *(Diagram: 2Marks & Expression: 2Marks)*
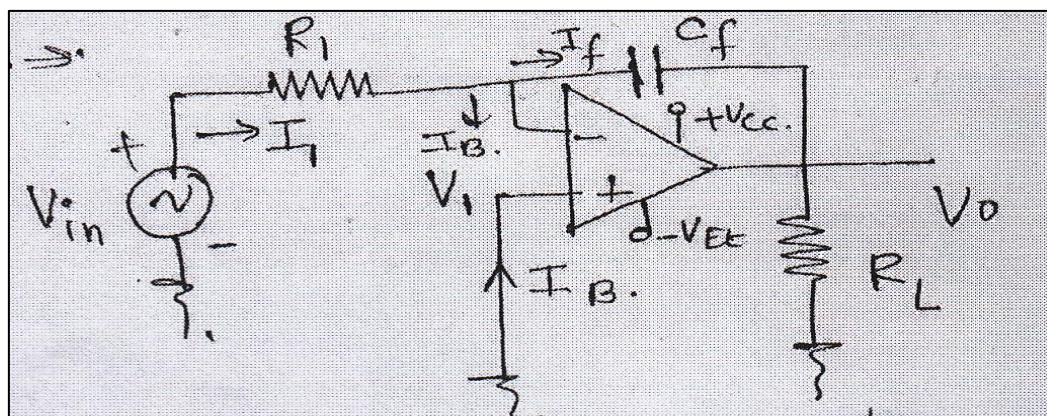
According to Kirchhoff's current equation,
$I_1= I_B + I_f$
I_B negligible (small) $I_1 \approx I_f$

The relationship between current through and voltage across the capacitor is,

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$$i_c = C \cdot \frac{dv_c}{dt}$$

$$\therefore \quad \frac{V_{in} - V_2}{R_1} = C_f \left(\frac{d}{dt} (V_2 - V_0) \right)$$

$V_1 = V_2 \approx 0$, becoze A is very large.

$$\frac{V_{in}}{R_1} = C_f \cdot \frac{d}{dt}(-V_0)$$

∴ The o/p Vtg: can be obtained by integrating both side respect to time,

$$\int_0^t \frac{V_{in}}{R_1} dt = \int_0^t C_f \cdot \frac{d}{dt}(-V_0) dt$$

$$= -C_f(-V_0) + V_0 \Big|_{t=0}$$

$$\therefore \quad \boxed{V_0 = -\frac{1}{R_1 C_f} \int_0^t V_{in}\, dt + c} \qquad \begin{array}{l} c \text{ is} \\ \text{proportiond} \\ \text{constd.} \end{array}$$

e) **Determine the ouput voltage for an open loop differential amplifier with $V_1=1.2$ Vdc and $V_2=1$ Vdc. Assume op-amp as μA741.**

Ans:

$V_1 = 1.2$ Vdc

$V_2 = 1$ vdc   **01 Mark**

op-amp μA 741   So gain $= 2 \times 10^5$ (max)   **01 Mark**

$V_0 = $ Gain $(V_1 - V_2)$ ——   or M

$\quad = 2 \times 10^5 \,(1.2 - 1)$ **02 Mark**

$\quad = 2 \times 10^5 \,(0.2)$ 0² mark.

$$\boxed{V_0 = 4 \times 10^4 \text{ volt}}$$

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f) **Construct and draw the circuit to get the output voltage $V_0 = 3V_1 + 2V_2$ where V_1 and V_2 are input voltages.**

Ans: *(Construct: 2 Marks & Circuit Diagram: 2Marks)*
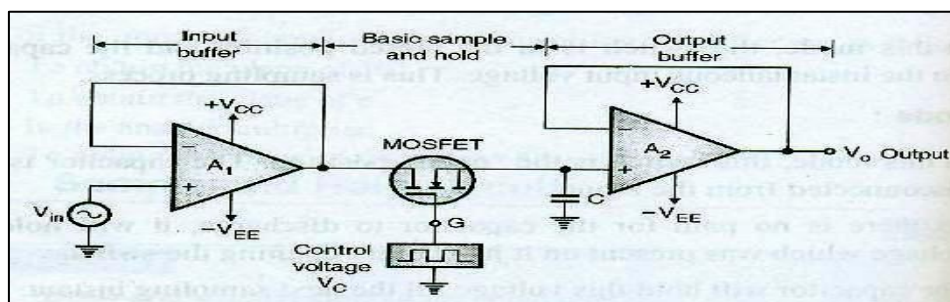
The value of R_1, R_2 may be different.
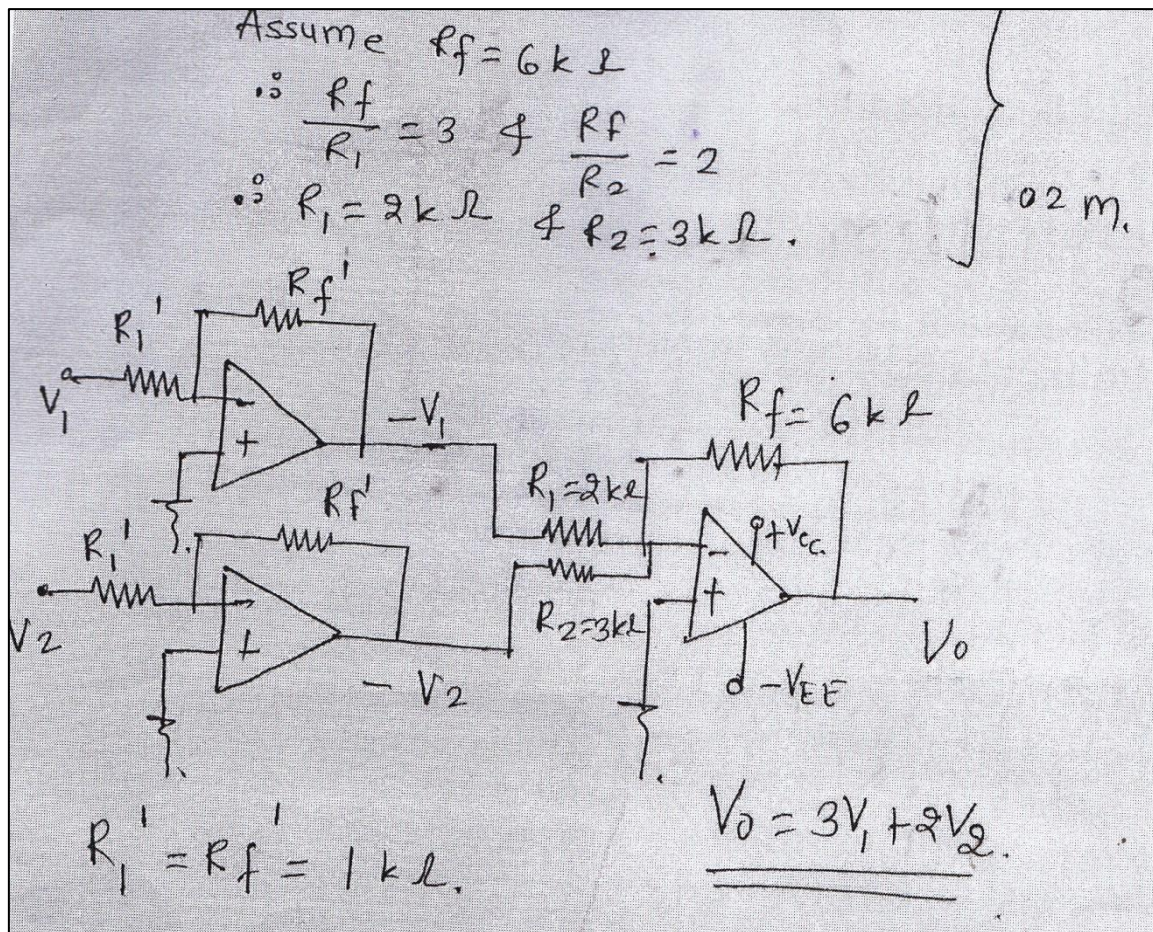
Q.3 Attempt any FOUR of the following: **16M**

a) **Draw and explain sample and hold circuit using Op-Amp.**

Ans: *(Diagram: 2Marks & Explanation: 2Marks)*

- The n-channel MOSFET is driven by a control voltage VC acts as a switch.The control voltage VC is applied to the gate of the MOSFET.
- The circuit diagram can be split into three stages. First stage is the voltage follower second one is the switch and capacitor and the third one is a gain the voltage follower.

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- When VC is high the MOSFET turns on and acts like a closed switch .This is sampling mode .The capacitor charges through the MOSFET to the instantaneous input voltage.
- As soon as VC=0 the MOSFET turns off and the capacitor is disconnected from OPMP1output. Capacitor cannot discharge through amplifier A2 due to its high impedance. Thus this is the hold mode in which the capacitor holds the latest sample value.
- The time period during which the voltage across capacitor is equal to input voltage is called <u>sample period</u>.
- The time period during which the voltage across capacitor is constant is called <u>Hold</u> <u>period.</u>

b) Compare between comparator and Schmitt trigger
**Ans: (Any valid 4 points: 4 marks)**

Sr. No	Parameter	Comparator	Schmitt trigger
1	**Definition**	It compares the two input voltages.	It converts any wave shape into square waves.
2	**Feedback**	In Comparator, open loop System.	It uses positive feedback.
3	**Hysteresis**	It does not exhibit Hysteresis.	It exhibit hysteresis.
4	**External reference voltage.**	It has only one reference Voltage.	It has two reference voltage V_{UTP}.

c) State the need of peak to peak detector and draw its circuit diagram.
Ans: *(2 marks need of peak detector and   2marks for circuit diagram)*

Need of peak detector:
- It is used to determine or detect the highest or maximum peak value of the input signal applied. **<u>or</u>**
- It is used to determine the positive or negative peak **<u>or</u>**
- The difference between the two peaks Of the input signal.

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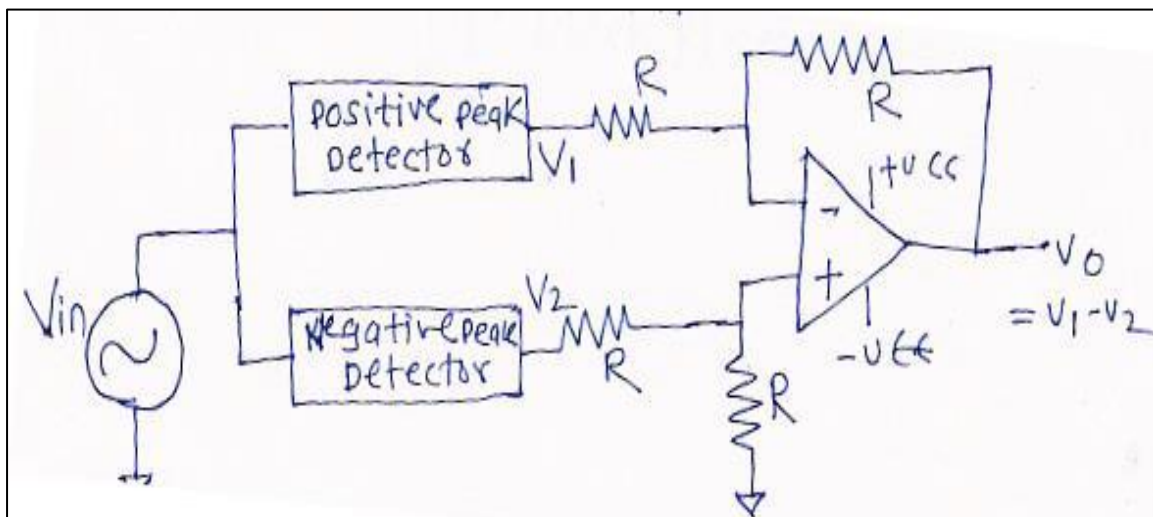
d) State the need of signal conditioning and signal processing .List applications of instrumentation amplifier.

Ans: *(2 marks need of signal processing and conditioning & 2marks for application)*

- In an instrumentation system, a transducer is used for sensing various   parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc.
- However the transducer output cannot be used directly as an input to the rest of the instrumentation system
- In many applications, the signal needs to be conditioned and processed. The signal conditioning can be of different types such as rectification, clipping, clamping etc. Sometimes the input signal needs to undergo certain processing such as integration, differentiation, amplification etc.
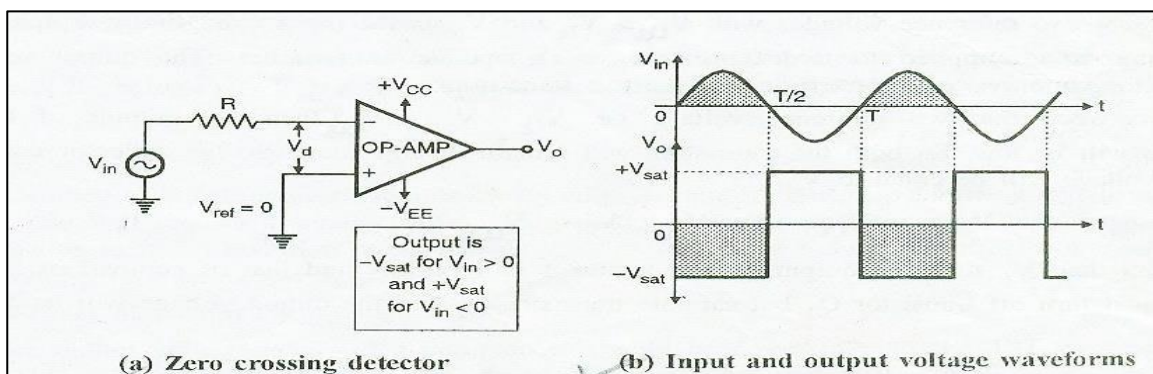
- **Application (Any 2)**

    1) Electronic weighing scale
    2) Temperature indicator
    3) Temperature controller
    4) Pressure monitoring and control
    5) Light intensity meter
    6) Measurement of flow and thermal conductivity
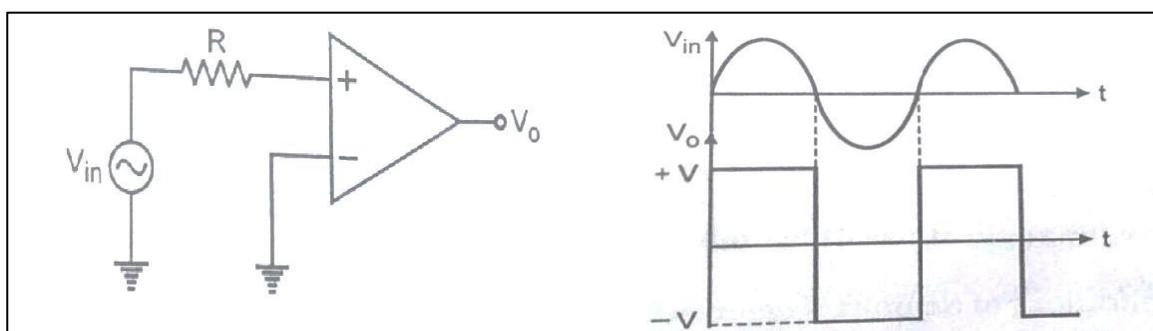
e) Draw the circuit diagram and input output waveform of inverting and non-inverting ZCD (zero crossing detector)

Ans: *(1 mark for circuit diagram and 1 mark for waveform of inverting ZCD) & (1 mark for circuit and 1 mark for waveform of Non inverting ZCD)*

- Inverting Zero crossing detector:

(a) Zero crossing detector   (b) Input and output voltage waveforms

- Non - Inverting Zero crossing detector:

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f) Draw and explain voltage to current converter with floating load .List its 4 applications.
Ans: *(1 Marks for circuit diagram & 1 mark for explanation and 2 marks for application)*

Fig. Voltage to current converter with floating load
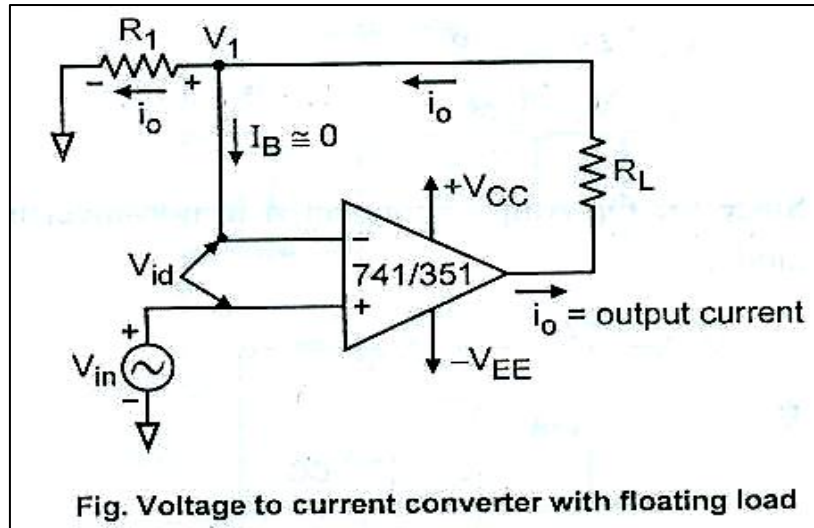
- The input voltage is applied to the non-inverting (+) input terminal of the OP- AMP. Load resistance R_L is connected in place of the feedback resistor

- This circuit is also called as current series negative feedback amplifier

- This is because the feedback voltage across R_1 is proportional to the output current I_o and appears in series with the input voltage.

Apply KVL to the

input loop $V_{in} = V_{d} + V_f$

But as the open loop gain A_v of this OP- AMP is very large $V_d \approx 0$

$V_{in} = V_f$

But $V_{in} = R_1 \times I_o$ …………(as $I_B \approx 0$)

Therefore $I_o = V_{in} / R_1$

Thus the input voltage is converted into output current and the circuit act as a
V to I converter.
- Applications:(any relevant applications can be considered)
  1. Zener Diode Tester
  2. Diode Match Finder

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Q.4 Attempt any __FOUR__ of the following: 16M

   a) Design and draw low pass filter with a cut-off frequency of 2KHz and a pass band gain of 2
Ans: *(1 mark for R1 and Rf & 1mark for R & 2 marks for Designed circuit)*

Solution: Pass band Gain (A_f) is given by
$A_{f = 1 +} \frac{Rf}{R1}$
Here $A_f = 2$

Therefore $2 = 1 + \frac{Rf}{R1}$
$\frac{Rf}{R1} = 1$
i.e $R_{1 =} Rf$
(any value of $R1$ $_{in}$ kΩ can be assumed)
Assume R1 = 10kΩ,   Therefore $R_f = 10$kΩ
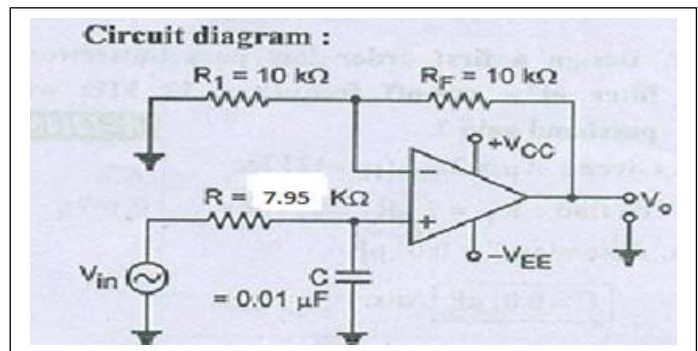Assume C= 0.01 µF (any value of C< 1 µF is valid)
$f_c = 1/ 2\pi RC$.
Given $f_c = 2$kHz

Therefore, $2 \times 10^3 = 1/ 2\pi RC$

R= $1/ 2\pi \times 2 \times 10^3 \times 0.01 \times 10^{-6}$

R= 7.95 **kΩ**
.:Therefore, R= 7.95 kΩ

b) Design first order low pass Butterworth filter with a cut-off frequency of 2KHz and a pass band gain of 2. Draw the designed circuit
Ans: *(1 mark for R1 and Rf & 1mark for R & 2 marks for Designed circuit)*

Solution: Pass band Gain (A_f) is given by
$A_{f = 1 +} \frac{Rf}{R1}$
Here $A_f = 2$
Therefore $2 = 1 + \frac{Rf}{R1}$
$\frac{Rf}{R1} = 1$
i.e $R_{1 =} Rf$
(any value of $R1$ $_{in}$ kΩ can be assumed)
 Assume R1 = 10kΩ,   Therefore $R_f = 10$kΩ
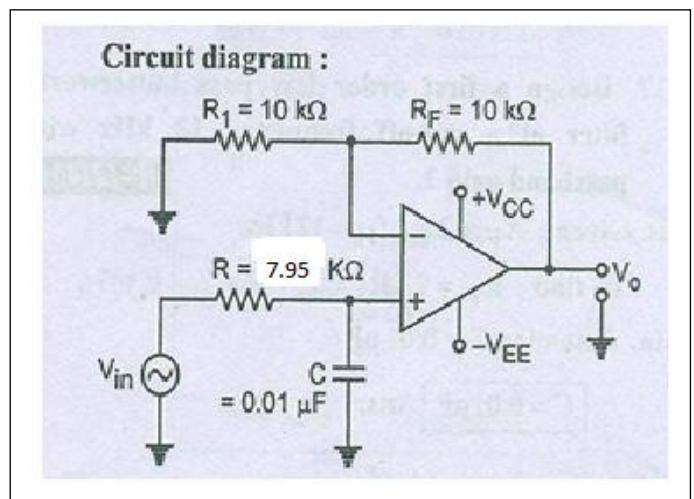Assume C= 0.01 µF (any value of C< 1 µF is valid)
 $f_c = 1/ 2\pi RC$.
 Given $f_c = 2$kHz

Therefore, $2 \times 10^3 = 1/ 2\pi RC$

R= $1/ 2\pi \times 2 \times 10^3 \times 0.01 \times 10^{-6}$

R= 7.95 **kΩ**
.: Therefore, R= 7.95 kΩ

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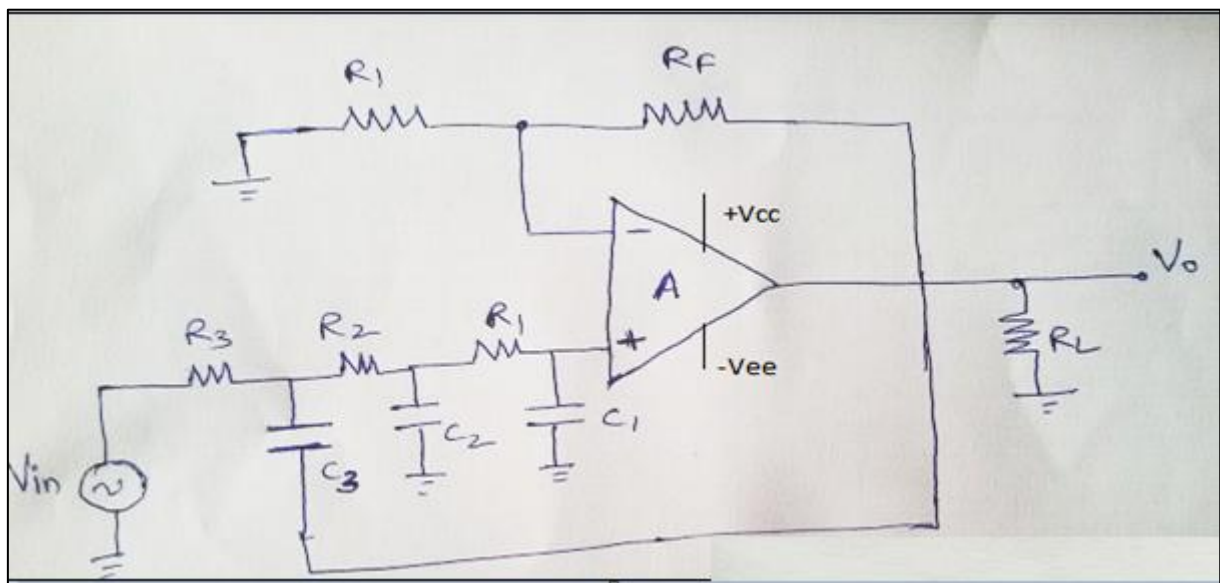_____

c) **Suggest and draw Op-Amp based circuit using Butterworth filter to fulfill the following response.**

Ans: *(1 mark for identifying the circuit and 3 marks for correct circuit diagram)*
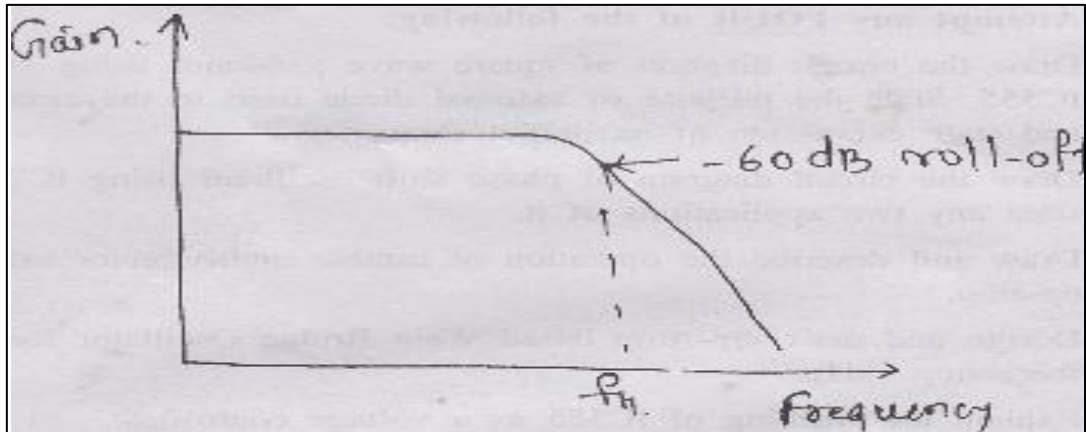
Suggested Op-amp based circuit is third order low pass filter. The circuit diagram is as given below

d) **Describe the operation of wide band-pass filter with the help of circuit diagram.**
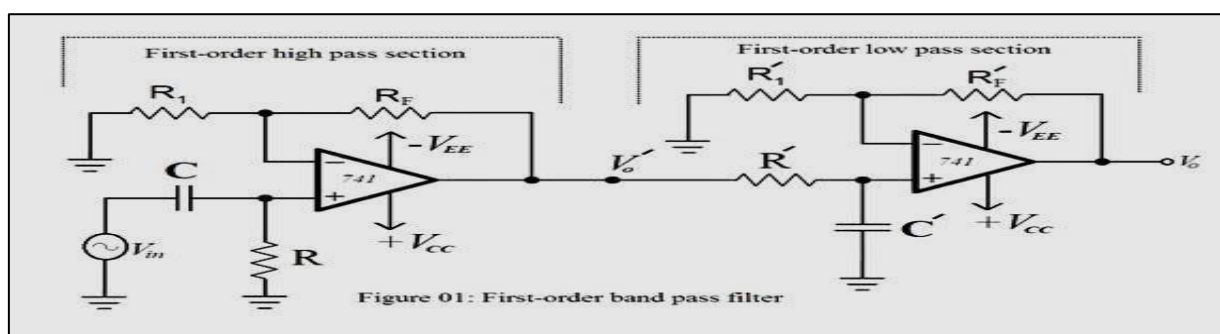
**Ans:** *(circuit diagram 2 marks operation 2 marks)*

Figure 01: First-order band pass filter

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OPERATION:

- A **band-pass filter** passes all signals within a lower-frequency limit and an upper-frequency limit and rejects all other frequencies that are outside this specified band.

- This type of filter has a maximum gain at a *resonant frequency*.
- A band pass filter is the combination of high pass and low pass filter combination
- It has a pass band between two cut off frequency f_H and f_L such that $f_H > f_L$. Any input frequency outside this pass band is *attenuated*.

- There are two types of band pass filters wide band pass and narrow band pass.
- If the quality factor Q < 10 and Q > 10 then it would be wide band pass and narrow band pass filter.
- The relationship between Q, the 3-dB *bandwidth* and the center frequency f_c is given by,

e) Draw only circuit of notch filter .Write formula of notch frequency f_N.

Ans: *(Circuit diagram 3 marks and frequency formula 1marks)*

Fig: Notch filter
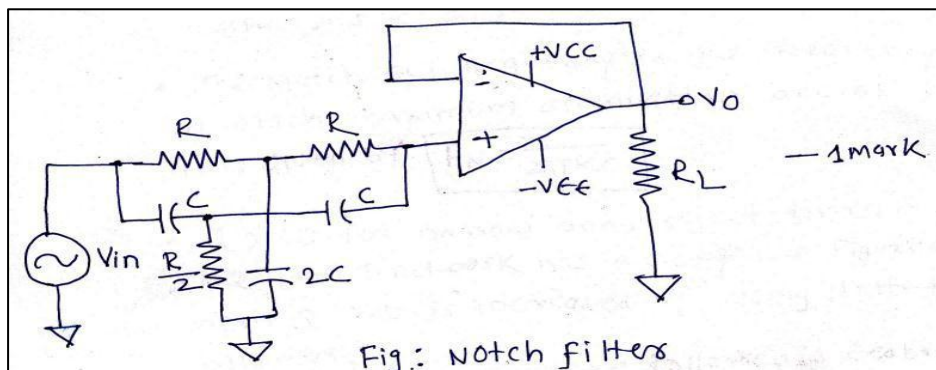
- Formula for notch frequency is $f_N = 1/2\pi RC$

f) Classify the filters on the following basis:
   i) component used
   ii) frequency range
   iii) frequency response
   iv) nature of passband and stop band

Ans: *(each correct classification – 1 mark)*

i.   On the basis of component used, filters can be divided as active and passive filters.
ii. On the basis of frequency range, can be divided as AF (audio frequency) or RF (radio frequency) filters.
iii. On the basis of frequency response filters can be divided as high pass, low pass, band pass and band reject filters.
iv. On the basis of nature of pass band and stop band, they can be divided as narrow band pass, wide band pass, narrow band reject and wide band reject filters.
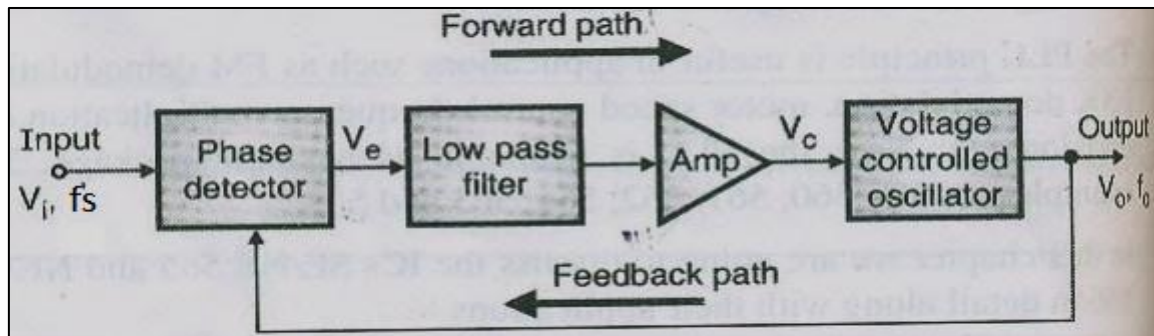
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Q.5 Attempt any FOUR of the following:　　　　　　　　　　　　　　　　　　　**16M**

a) **Describe the operation of phase detector and role of VCO in PLL.**

Ans:　*(Phase detector: 2Marks& role of VCO: 2Marks)*



- **Phase Detector:** The two input to phase detector are the input voltage at frequency (fs) & the feedback voltage at frequency (fo) from VCO.
  The phase detector compares these two input signals & produce error voltage (Ve) which is directly proportional to the difference of two frequencies.
      It acts as multiplier i.e. Ve α (fs ± fo)
- **VCO**: The output frequency of VCO is directly proportional to the V_C, then these frequency fo is compared with i/p frequency fs by phase detector & it is adjusted to fo continuous by until it is equal to i/p frequency (fs).

b) **Draw & describe the operation of water level controller using IC 555.**

Ans:　(*Diagram: 2Marks & Explanation: 2Marks)*
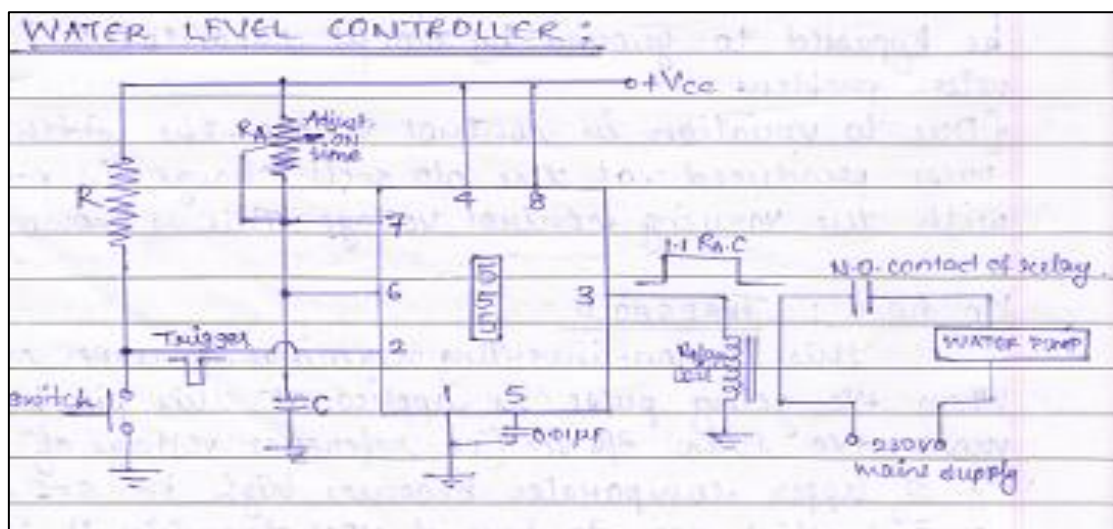
- In water level controller, IC 555 is used in the monostable multivibrator mode.
- As soon as switch is ON, a trigger pulse is produced & applied to pin no 2 of IC 555 & the output of IC 555 goes high.
- It will remain high for time period $T_{ON} = 1.1R_A.C$
- The high output of IC 555 will energize the relay coil & close the normally open (N.O) contact of the relay to connect the 230 volt ac supply to the water pump motor.
- The motor will remain on for the on for the ON time of monostable circuit. $T_{ON}=1.1.R_A.C$

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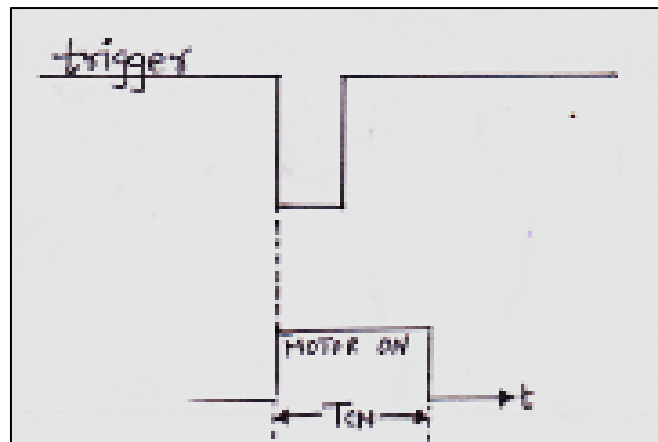
c) Explain the use of PLL in FM detection.
Ans: *(Diagram: 2Marks & Explanation: 2Marks)*
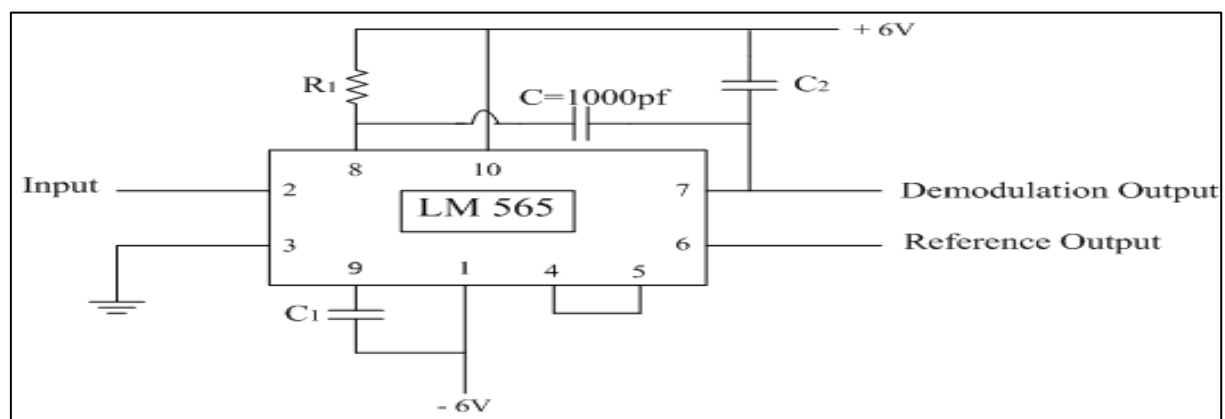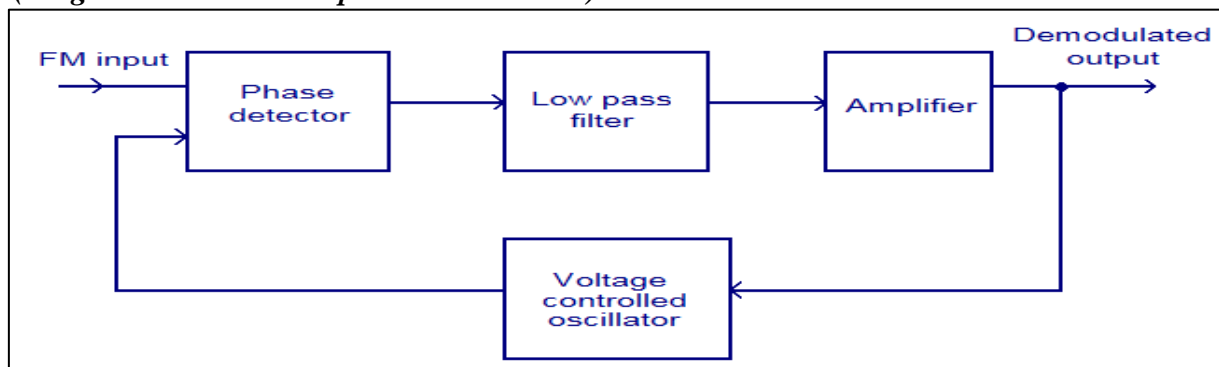
- FM demodulator detects the demodulations signal & it is constructed using PLL.
- The above diagram shows the FM demodulator using PLL.
- The FM signal which is to be demodulated is applied at the input of the PLL.
- As the PLL is locked to the FM, the VCO starts tracking the instantaneous frequency in the FM input signal.
- The error voltage produce at the output of the amplifier is proportional to deviation of input frequency from the center frequency of FM. Thus the ac component of the error voltage represents the modulating signal. Thus at the error amplifier output we get demodulated FM output.
- The FM modulator using PLL ensures a high linearity between the instantaneous input frequency & VCO control voltage.

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d) Draw the pin diagram of IC 555 & explain the function of various pins.
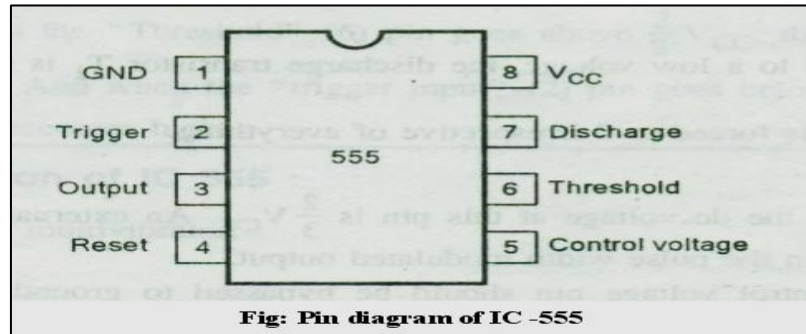**Ans:*(Diagram: 1Marks & Explanation: 3Marks)***

Fig: Pin diagram of IC –555

- **Pin 1**: **Ground Terminal:** This is the reference or ground point of the IC & it is to be connected to the ground terminal of the DC voltage source used to supply power to timer IC.

- **Pin 2: Trigger Terminal:** in the stable state, $\overline{Q}$ output is high & this makes IC output low. Triggering pulse or train of pulse are applied to this pin. When –ve going pulse is applies at this pin but the amplitude is more negative than 1/3 V_{CC} (i.e. reference voltage of lower comparator); then o/p of lower comparator goes high $\overline{Q}$ (i.e. now, S=1 & R=0. .: flip flop becomes set. Due to this $\overline{Q}$=0; which goes to the base of NPN transistor, hence transistor is off. Due to this external capacitor start charging & output of timer goes high.

- **Pin 3: Output Terminal:** This is the output of the timer & the load is connected to this pin. the status of output pin (high/low)is decided by the two comparators in the functional diagram of IC555

- **Pin 4: Reset Terminal:** Whenever the timer IC is to be reset or disabled, a negative pulse is applied to pin 4, and thus is named as reset terminal. The output is reset irrespective of the input condition. When this pin is not to be used for reset purpose, it should be connected to + V_{CC} to avoid any possibility of false triggering.

- **Pin 5: Control Voltage Terminal:** The dc voltage at this pin is 2/3 V_{CC}& external voltage applied to this pin change this these hold level as well as the triggering level by connecting a pot between pin no 5 & 1.when this pin is not in used, it should be bypassed to ground by 0.01 microfarad capacitor to avoid any noise problem.

- **Pin 6**: **Threshold Terminal:** This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of 2/3 V_{CC}. The amplitude of voltage applied to this terminal is responsible for the set state of flip-flop. When the voltage applied in this terminal is greater than 2/3Vcc, the upper comparator switches to +Vsat and the final output gets low.

- **Pin 7**: **Discharge Terminal:** this pin is connected to the collector of NPN transistor. When $\overline{Q}$=1this transistor turns on & when $\overline{Q}$ =0 it turns off.

- **Pin 8: Supply Terminal:** Supply voltage of + 5V to +18V canbe applied to this pin with respect to ground.

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**e) Explain how monostable multivibrator can we used as frequency divider.**
Ans: *(Diagram: 2Marks & Explanation: 2Marks)*
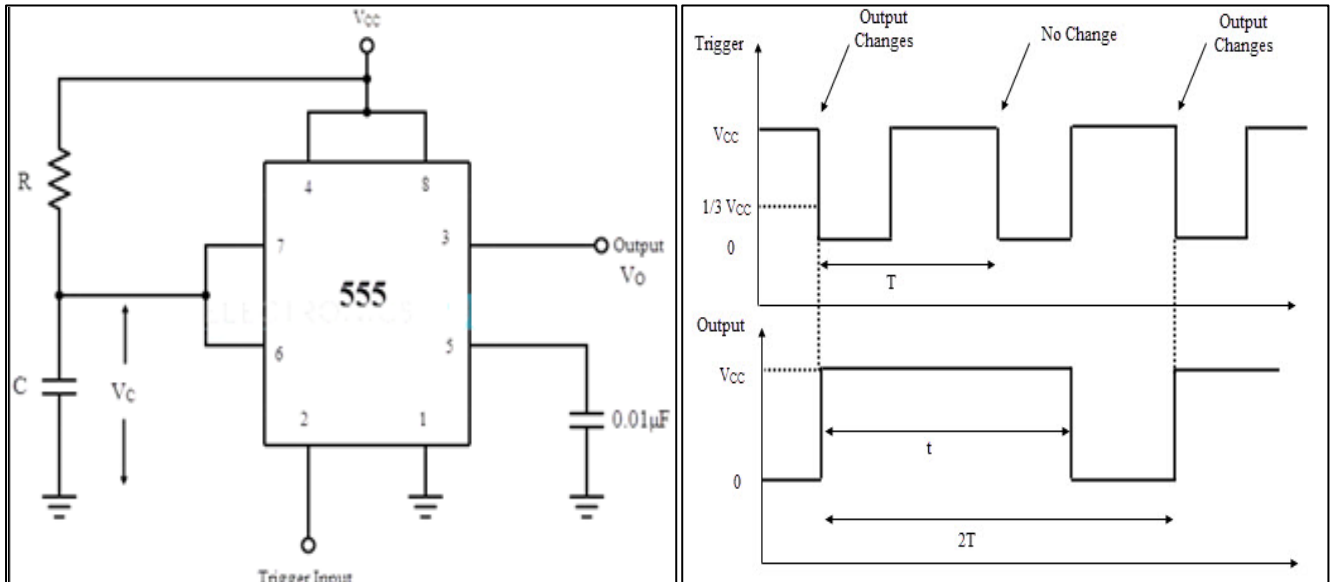
- The circuit shown above is a monostable multivibrator which is used as a frequency divider
- Corresponding to the first negative trigger pulse , the output of IC 555 goes high & this remain high for time period $T_{ON} = -1.1 R_A.C$
- The frequency divider operation is possible because the monostable multivibrator canot be triggered during T_{ON} time.

f) Draw the transfer characteristics of PLL & explain.
Ans: *(Diagram: 2Marks & Explanation: 2Marks)*
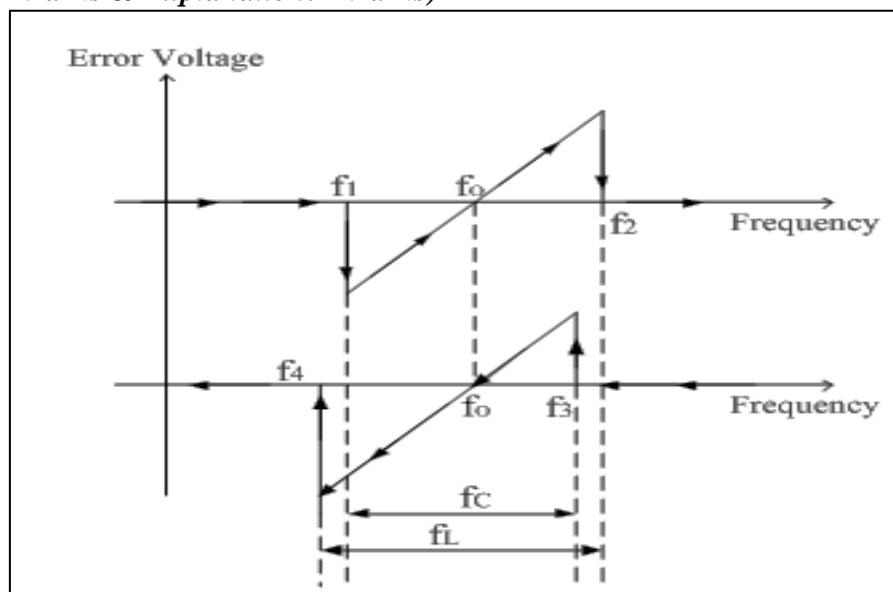
- Transfer characteristics shows the relationship between the error voltage / VCO output with the input signal frequency.
- The PLL does not respond to the increasing input frequency till it reaches a frequency f_1. This frequency is called as the lower edges of the capture range.

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- Again by increasing input frequency is $> f_1$, there is a sudden negative jump in the error voltage (V_O) which indicates $fs = f_1 < fo$.
  Ve α fs – fo , as fo is $<$ fs & therefore Ve is negative.
- As f_1 increases from f_1 to fo, the negative error voltage reduces & at $fs = fo$, the error voltage is zero.
- With further increase in fs up to f_2, the error voltage increases in the positive direction, when fs $> f_2$ then we get upper edge of lock range.
- When frequency decreases at f3, & $fs = f_3$ then we get the upper edge of capture range.
- Further when we decrease fs, the error voltage starts decreasing or starts going towards zero.& then the negative direction then when the fs reaches f_4 then we get lower edge of lock range.
- Therefore, capture range $= f_3 – f_1$
  .:Lock range $= f_2 – f_4$.

Q.6 Attempt any <u>FOUR</u> of the following: **16M**

a) **Draw the circuit diagram of square wave generator using IC 555. State the purpose the external diode used in the circuit & state expression of its output frequency.**

Ans:(*Diagram: 2Marks & purpose of the external diode: 1 mark & expression 1mark*)
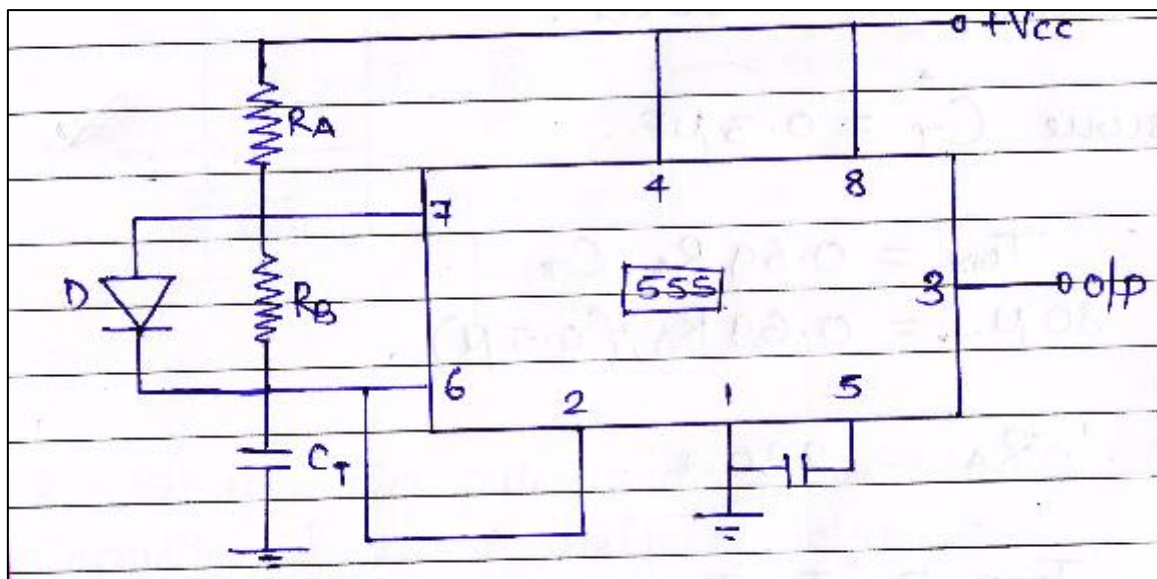

Purpose of external diode :

- Whenever user's needs; we can connect one diode across resistor R_B in astable multivibrator in such a way that anode is connected to upper terminal of R_B & cathode is connected to lower terminal of R_B ; So that during charging of capacitor , diode will be forward biased & therefore R_B will not have any effect on T_{ON} & therefore $T_{ON} = 0.69(R_A) (C_T)$.
 & T_{ON} becomes equal to $T_{OFF.}$

Output Frequency:
$$f = \frac{1}{0.693\ (R_A + R_B)C_T}$$

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b) Draw the circuit diagram of phase shift oscillator using IC741 state any two applications of it.
Ans: *(Diagram: 2Marks& Applications: 1marks of each)*
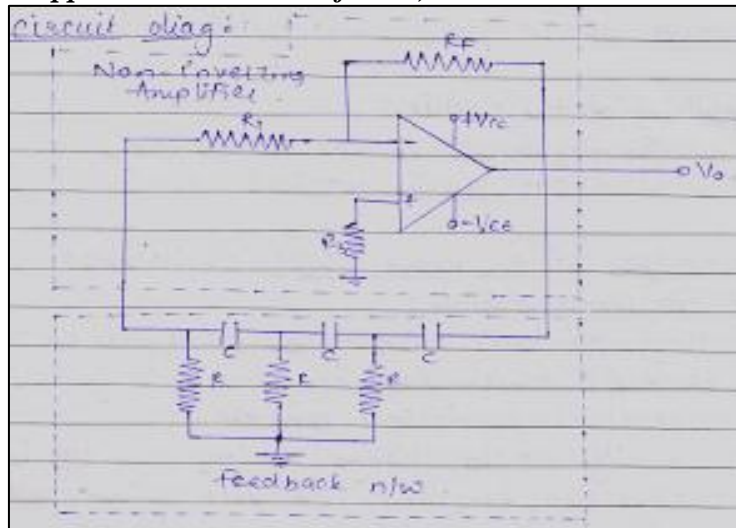
- Applicatons:-
  1. Used for range of frequencies from several hertz to several thousand kilo hertz.
  2. It is used in musical instruments.

c) Draw and describe the operation astable multivibrator using op-amp.
Ans:*(Diagram: 2Marks & Explanation: 2Marks)*
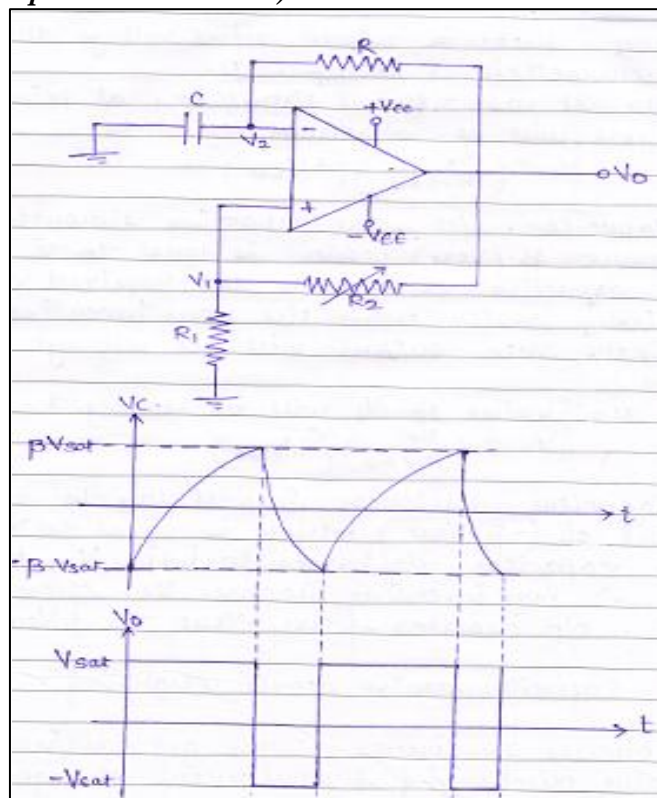
- Initially there is output offset voltage due to the characteristics of op-amp.
- Consider it as + Vsat, therefore at point V_1, the voltage is equal to ,

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$$V_1 = \left(\frac{R_1}{R_1 + R_2}\right)(+V_{sat})$$

- Therefore capacitor will start charging through R to the value $\beta\ (+V_{sat})$ which is equal to V_1
- When capacitor charges to the required value or slightly greater than the non inverting terminal, then output will get change to –Vsat.
- Now, at point V_1, the voltage is equal to ,

$$V_1 = \left(\frac{R_1}{R_1 + R_2}\right)(-V_{sat})$$

- Capacitor discharges & will try to reach value of $\beta\ (-V_{sat})$ which is equal to V_1
- When capacitor discharges below V_1 , then non inverting terminal becomes less than inverting terminal, then output will get change to +Vsat. Therefore capacitor starts charging.
- The process continues, so we get continuous charging & discharging of capacitor & thus output changes continuously.

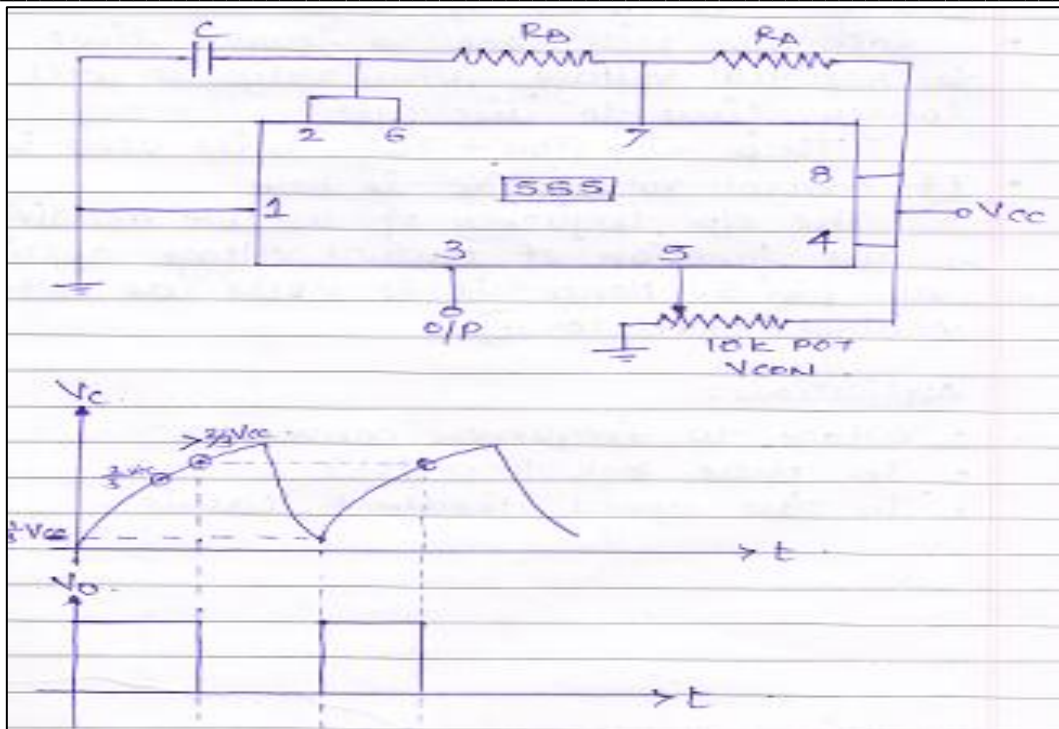**d) Design & draw Op-amp based Wein bridge Oscillator for frequency 1kHz.**
Ans: *(Diagram: 2Marks & Design: 2Marks)*
NOTE: students can assume any value of R so accordingly answer for C will change.
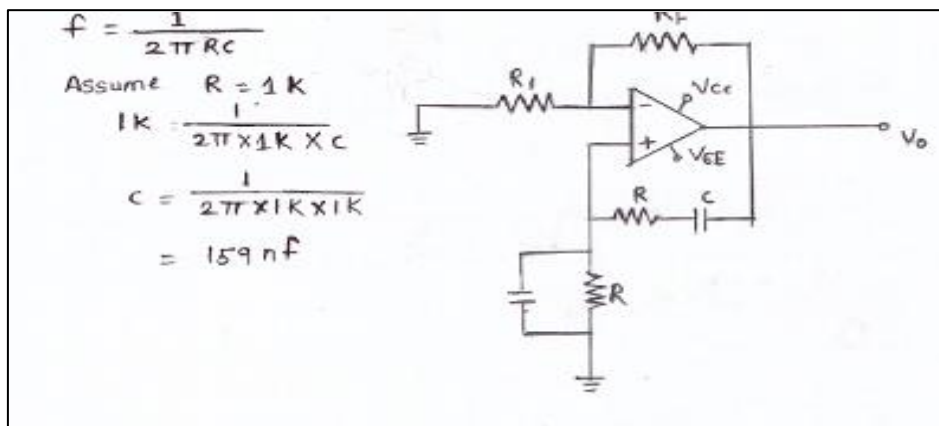
**e) Explain the working of IC555 as a voltage controlled oscillator (VCO).**
Ans: *(Diagram: 2Marks & Explanation: 2Marks)*

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- It is constructed using astable multivibrator by connecting one potentiometer to pin no.5, V_{CC}& ground.
- This circuit is also called as frequency converter or frequency changer.
- By connecting pot at pin no.5, the D.C voltage at this pin is not equal to 2/3 V_{CC}. But it is variable depending on position of pot wiper.
- If control voltage is increased above 2/3 V_{CC} then capacitor has to charge higher voltage to change the state of output.
- Therefore capacitors will take a longer time to change to required voltage. Similarly it will take longer time to discharge.
  Thus $T = T_{ON} + T_{OFF}$ will also increase.
- Therefore the output frequency of astable multivibrator is the function of control voltage applied at pin 5. Hence it works as voltage control oscillator.

f) **Explain the working of IC 555 as Schmitt trigger. Draw the circuit & sketch the output waveform.**
Ans:*(Sketch: 1Mark &Diagram: 1 Mark& Explanation: 2Marks)*

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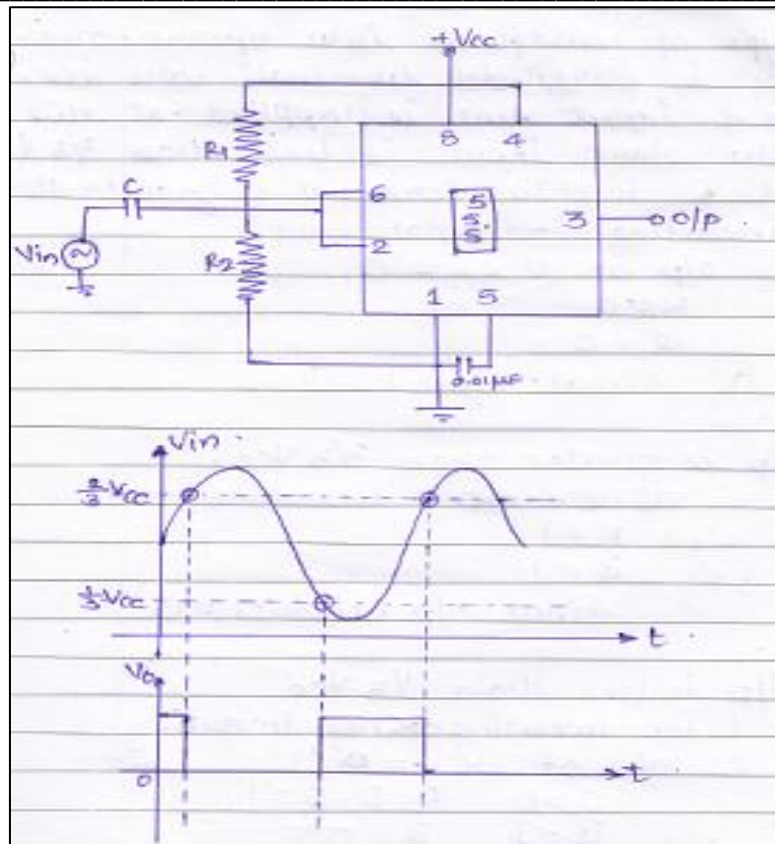
- Schmitt trigger is a circuit which converts any type of waveform into square wave.
- Trigger & threshold terminals are connected together & input sin is applied at this point.
- At the start input is less than $2/3 \ V_{CC}$.
  Therefore upper comparator inverting terminal is greater than non inverting terminal.
  So output of upper comparator becomes zero.
  $\therefore R = 0$
  $\overline{Q} = 0$
 $\therefore$ output of schmitt trigger becomes high.
- When input becomes greater than $2/3 \ V_{CC}$
  So output of upper comparator becomes high.
  $\therefore R = 1$
  $\therefore \overline{Q} = 1$ $\therefore$ output of schmitt trigger becomes low.
- When input is less than $1/3 \ V_{CC}$.
  Output of lower comparator goes high.
  $\therefore R = 0 \ \& \ S = 1$
  $\therefore \overline{Q} = 0$
$\therefore$ output of schmitt trigger goes high.