MODEL ANSWER

SUMMER– 17 EXAMINATION

Subject Title: Linear Integrated Circuit Subject Code: 17445

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

LIC 17445 Summer 17

1 a) Attempt any SIX of the following: 12

i) State ideal and typical values of:

1) Slew Rate 2) CMRR

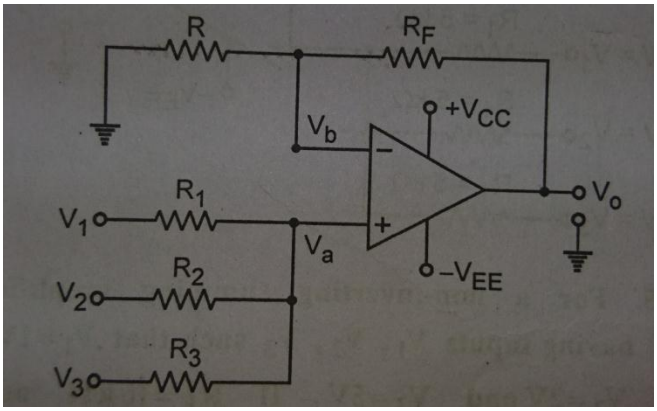
Ans:- (Ideal and typical value- ½ mks each)

Parameter	Ideal Value	Typical value
Slew rate	infinite	0.5V/ µsec
CMRR	infinite	90 dB

ii) Draw circuit diagram of non-inverting adder with 3 inputs.

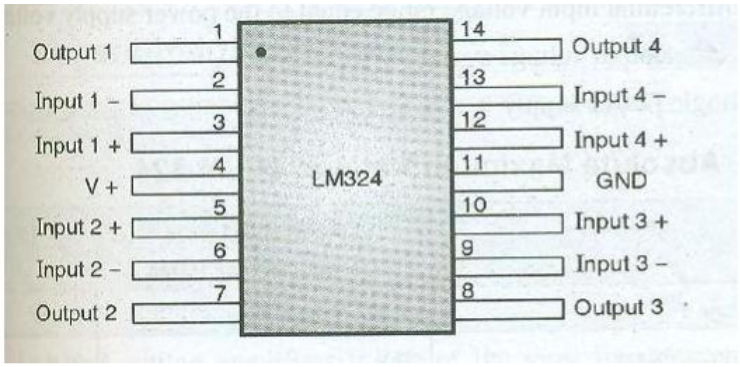
Ans:- (Proper relevant diagram – 2 mks)

3 inputs non inverting adder



iii) Draw pin diagram of IC LM 324.

Ans:- (Proper pin diagram- 2 mks)



iv) State the need of signal conditioning and signal processing.

Ans:-(Need – 2 mks)

Signal Conditioning and signal processing-

In an instrumentation system, a transducer is used for sensing various parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc.

However the transducer output cannot be used directly as an input to the rest of the instrumentation system.

In many applications, the signal needs to be conditioned and processed. The signal conditioning can be of different types such as rectification, clipping, clamping etc. Sometimes the input signal needs to undergo certain processing such as integration, differentiation, amplification etc.

v) State basic difference between active filter and passive filter.

Ans:- (Proper relevant answer- 2 mks)

A filter is an electronic device that can remove specific ranges of frequencies from a signal. A filter could be active or passive. The **main difference** between active and passive filters is that **passive filters cannot cause a power gain** (i.e. they **cannot bring energy into the circuit**). Nor can passive filters regulate the current. An **active filter can add energy into the circuit and also control current**.

The passive filter consists of combination of only passive components such as resistor, inductor and capacitor, while an active filter consists of active element such as transistor, Op-amp, etc. along with passive components resistor and capacitor.

vi) Draw the pin diagram of IC 555.

Ans:- (IC pin diagram- 2 mks)

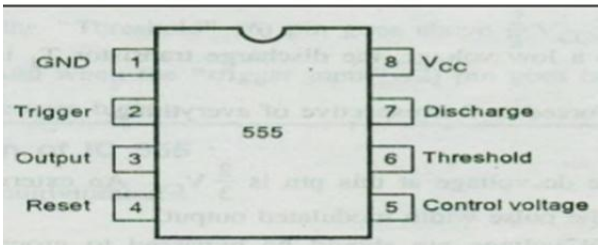


Fig: Pin diagram of IC -555

vii) Define multivibrator and gives its classification.

Ans:- (Definition- 1 mks, classification- 1 mks)

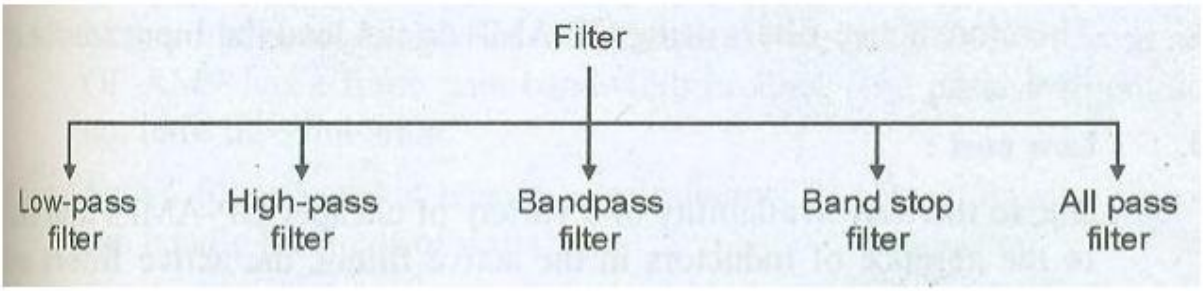
Multivibrator: An electronic circuit in which the output continuously changes between two states i.e. stable and unstable state is known as multivibrator.

Depending upon number of stable or unstable states, there are three types of multivibrator:

i. Astable multivibrator.
ii. Monostable multivibrator.
iii. Bistable multivibrator.

viii) Classify filters based on frequency response.

Ans:- (Proper classification- 2 mks)



b) Attempt any TWO of the following: 8

i) Draw block diagram of OPAMP and state the function of DC level shifting stage and output stage.

Ans:- (Block diagram- 2 mks,, functions- 1 mks each)

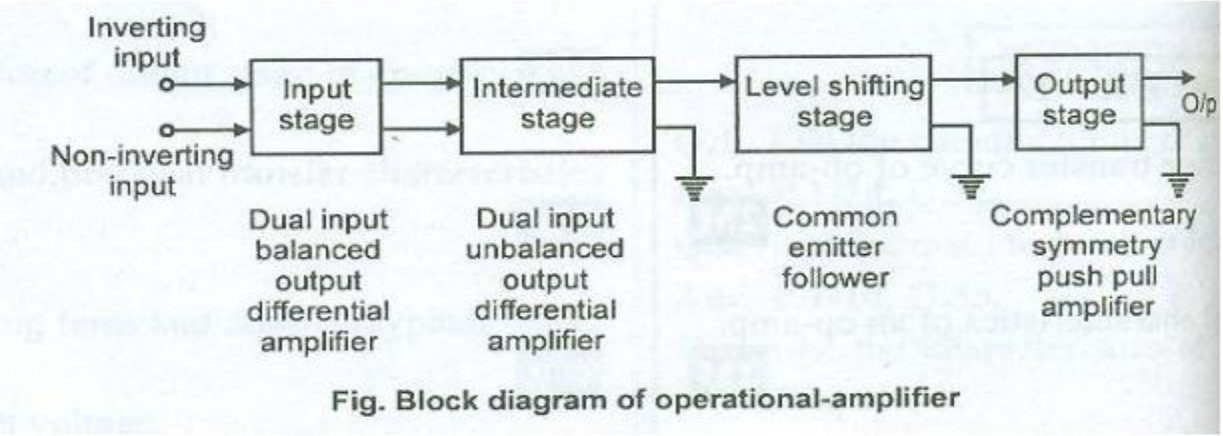


Fig. Block diagram of operational-amplifier

Level shifting stage: In this stage common emitter follower circuit is used. If the output of intermediate stage is shifted above or below the DC level, the level shifter stage brings back the signal to its original position.

Output stage: This stage uses complementary symmetry push pull amplifier. This stage provides low output resistance and hence increases the current supplying capability of op-amp and also this stage increases the output voltage swing.

ii) Draw dual input balanced output differential amplifier and describe the operation of it.

Ans:- (Diagram- 2 mks, operation- 2 mks)

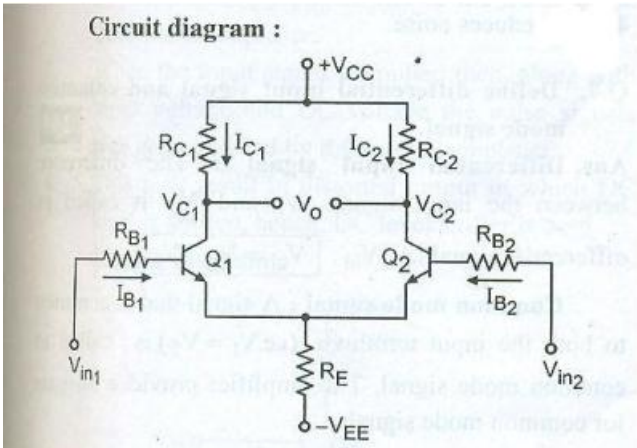


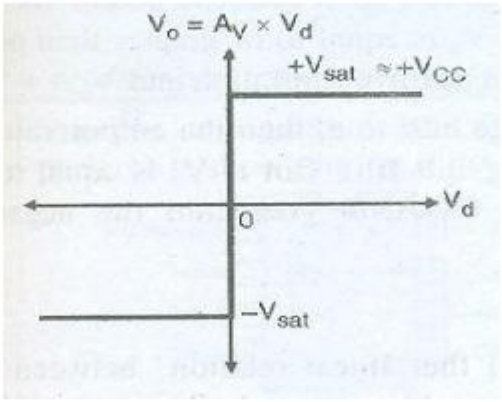
Fig. Dual input balanced output differential amplifier

Differential amplifier is a two input transistor amplifier which amplifies the difference between the two input signals V_{in1} and V_{in2}.

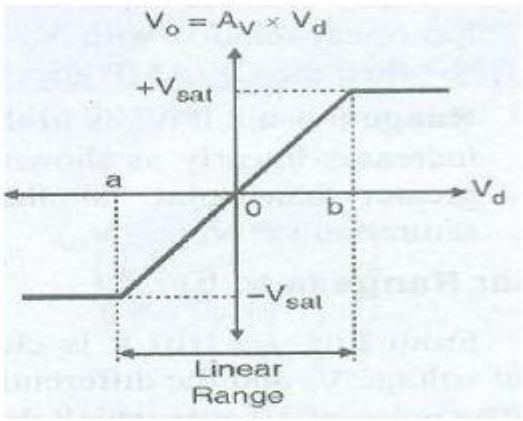
- The circuit is in the form of bridge and is excited by $+V_{CC}$ and $-V_{EE}$ and output V_o= I $V_{C1} - V_{C2}$
- When supply voltages are applied then Q_1 and Q_2 turns ON. As the circuit is symmetrical
- Therefore $I_{B1} = I_{B2}$.
  $I_{C1} = I_{C2}$
- By applying KVL at the output, we get,
  $V_{C1} = V_{CC} - I_{C1} R_{C1}$
  $V_{C2} = V_{CC} - I_{C2} R_{C2}$
  As,
  $I_{C1} = I_{C2}$, $R_{C1} - R_{C2}$, therefore, $V_O = 0$
- As null output is obtained, the bridge is said to be balanced.

iii) Draw ideal and practical voltage transfer characteristics of OP-AMP.

Ans:- (Both characteristics- 2 mks each)



Ideal voltage transfer characteristics of an ideal OP- AMP



Voltage transfer curve of practical OP- AMP

2. Attempt any FOUR of the following: 16

a) Draw closed loop inverting amplifier using OPAMP and derive expression for it's gain.

Ans:- (Diagram- 2 mks, derivation- 2 mks)

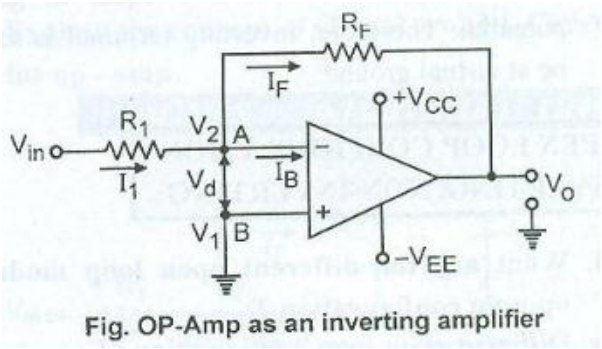
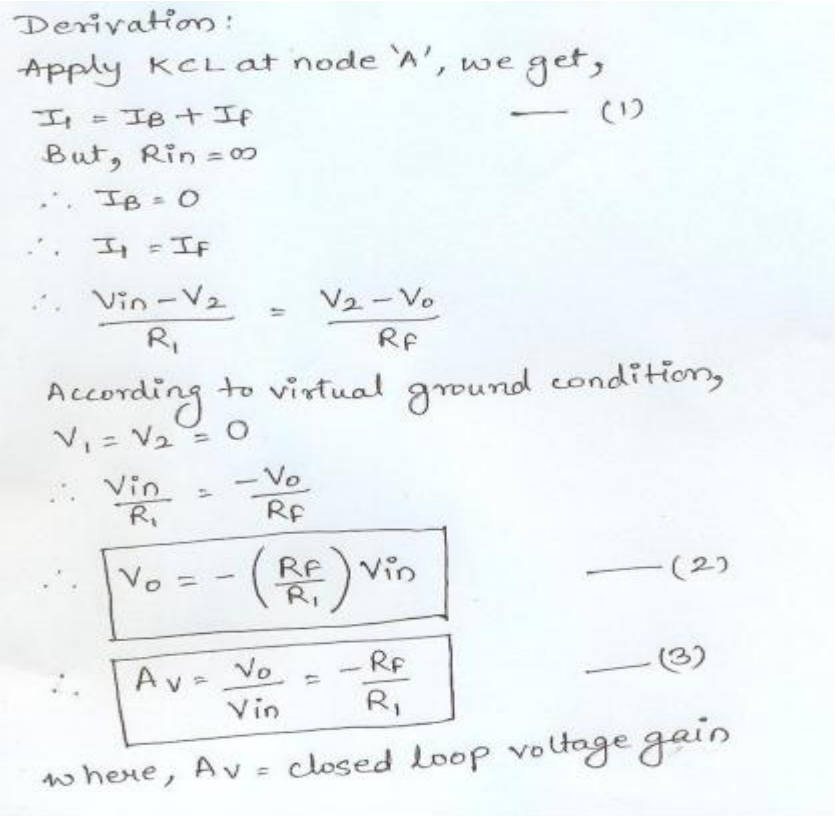


Fig. OP-Amp as an inverting amplifier

V_o= output voltage, V_{in}= input voltage, R_F= Feedback resistor, R_1= Input resistor

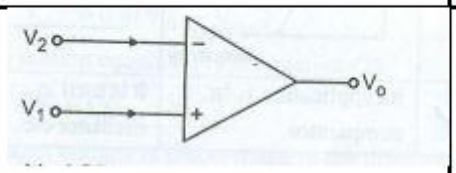
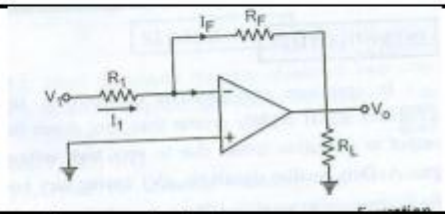
1. As input signal V_{in} is applied to inverting input, hence it is called as inverting amplifier and non inverting terminal is grounded.
2. The phase difference between input and output is 180^0
3. A negative feedback is provided from output to inverting terminal through R_F (Feedback resistor)



b) Compare open loop and closed loop configuration of OP-AMP with respect to :

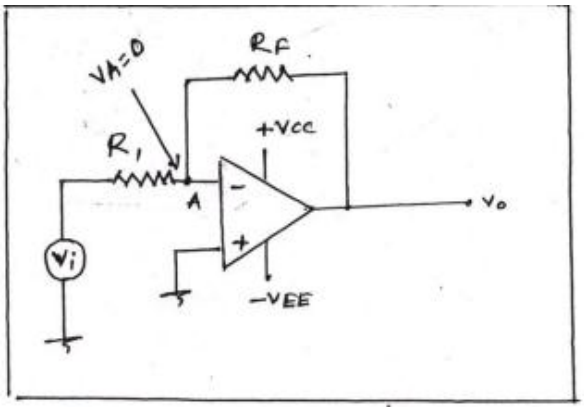
(i) Circuit diagram
(ii) Gain
(iii) Bandwidth
(iv) Application

Ans:- (Proper comparison -1 mks each)

Sr. No	Parameters	Open loop	Closed Loop
1	Circuit Diagram		
2	Gain	Voltage gain is very high	Voltage gain is low as compared to open loop.
3	Bandwidth	Bandwidth is low	Bandwidth is high
4	Application	Comparator	It is used in amplifier, oscillator etc.

c) Describe virtual ground and virtual short concept with reference to OP-AMP.

Ans:- (Diagram- 2 mks, description- 2 mks)



Description-

In circuit point V_A is virtual ground. Figure shows inverting amplifier using op-amp. In this circuit non-inverting terminal is connected to the actual ground. Due to this potential of inverting terminal become zero. Thus, inverting terminal is not actually connected to the ground. There after its potential is zero. Thus point V_A is known as virtual ground point. This phenomenon of having zero potential without actually grounding is known as virtual ground concept.

op-amp show virtual short during negative feedback and not positive feedback.

We have an op-amp working in inverting mode. Here we design it for say a gain of 5. Therefore, if our input is say 20 milli volts then our output will be 100 millivolts but OUT OF PHASE WITH INPUT (inverting mode). So when we feed back this voltage via Feedback resistor, it attenuates 100mV to nearly 20mV by dropping rest of voltage across it. Hence at the inverting input we have 20 mV input and -20 mV feedback (minus as it is completely out of phase) ,so the sum is nearly zero! For positive feedback we need the two voltage add up as they are in phase hence no zero potential.

d) Draw the circuit of basic differentiator. Draw output waveforms for sine and square wave input.

Ans:- (Diagram- 2 mks, proper waveforms- 2 mks)

Diagram-

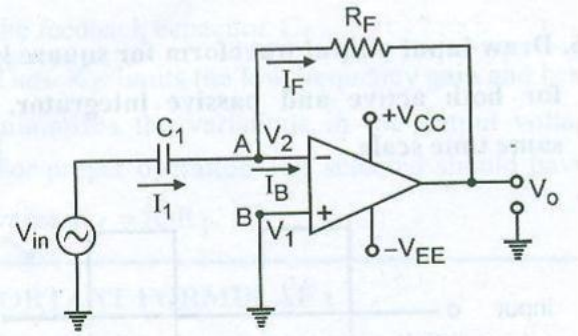
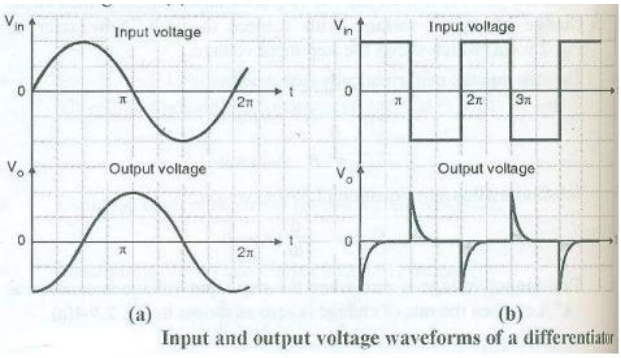


Fig. Circuit diagram of differentiator

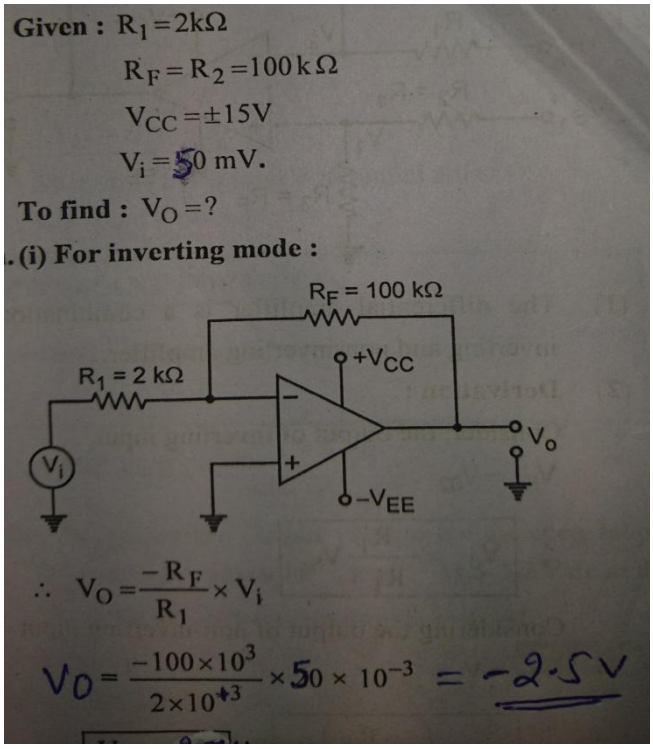
Waveforms



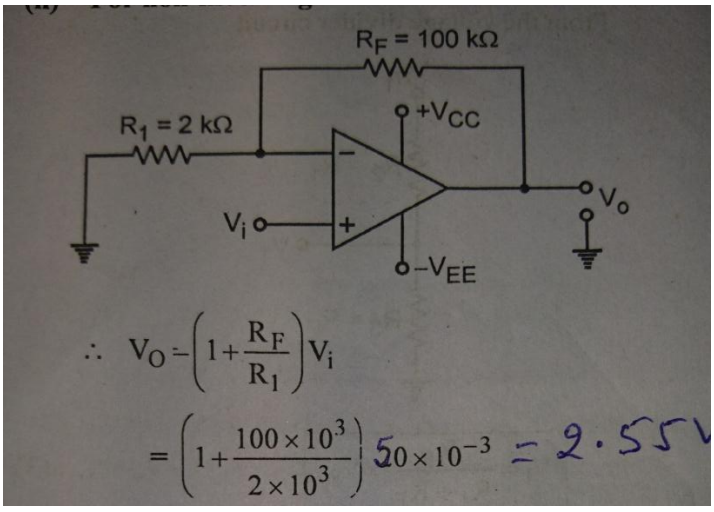
Input and output voltage waveforms of a differentiator

e) If R1 = 2KΩ, RF = 100KΩ, V cc = ± 15V and rms input voltage Vi = 50 mV. Calculate output voltage in inverting and non- inverting mode.

Ans:-(Both o/p voltage value- 2 mks each)



ii) For NINV amplifier-



f) Using OPAMP, draw the circuit to show the output V0 = 5(V1 – 4V2) Where V1 and V2 are input voltages.

Ans:- (Proper design-4 mks)

Sol:-

$V_0 = 5(V_1 - 4V_2)$

$= 5V_1 - 20V_2$

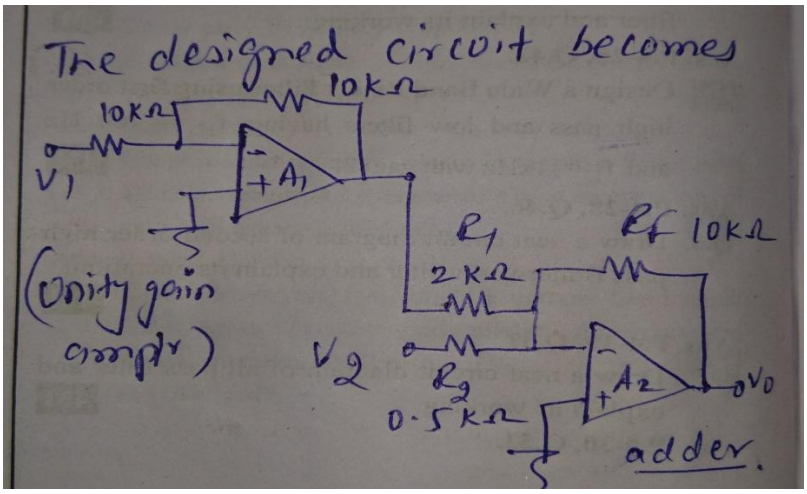
$= -(-5V_1 + 20V_2)$

$= -[5(-V_1) + 20V_2)]$

use unity gain amplifier A_1 to invert V_1 and use inverting adder A_2 to add V_2 with -

$\frac{Rf}{R_1} = 5$ and $\frac{Rf}{R_2} = 20$.

Let $Rf = 10K\Omega$, so $R_1 = 2K\Omega$ and $R_2 = 0.5K\Omega$



3. Attempt any FOUR of the following:

a) Describe the operation of Instrumentation amplifier using 3 – Op Amps with neat circuit diagram.

Ans:-(Diagram- 2 mks, description- 2 mks)

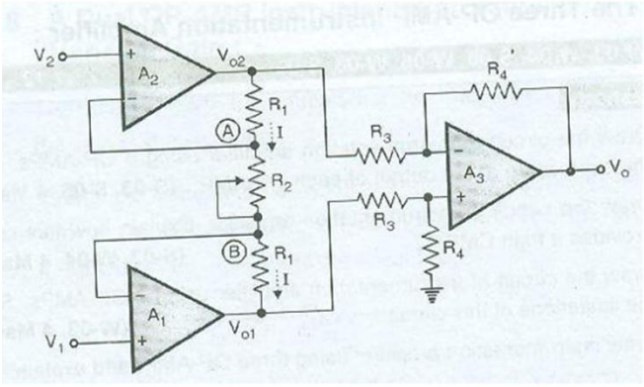


Fig: Instrumentation amplifier using three Op-Amp

Description-

(1) The Op-Amp A_1 and A_2 are connected in non-inverting configuration. The inverting terminals of both Op-Amps (A_1 & A_2) are connected to resistor R.

(2) **Derivation :**

Applying KCL at the output of A_1 & A_2

$$\therefore \quad I=\frac{V_o'-V_1}{R_1}=\frac{V_1-V_2}{R}=\frac{V_2-V_o''}{R_1}$$

Equating : $$\frac{V_o'-V_1}{R_1}=\frac{V_1-V_2}{R}$$

$$\therefore \quad V_o'=V_1\left(1+\frac{R_1}{R}\right)-V_2\left(\frac{R_1}{R}\right)$$

Similarly equating :

$$\frac{V_1-V_2}{R}=\frac{V_2-V_o''}{R_1}$$

$$\therefore \quad V_o''=V_2\left(1+\frac{R_1}{R}\right)-V_1\left(\frac{R_1}{R}\right)$$

The final O/p i.e. $$V_o=\frac{R_F}{R_2}\left[V_o''-V_o'\right]$$

[as A_3 is differential amplifier]

$$\therefore \quad V_o=\frac{R_F}{R_2}\left[\begin{array}{l}\left\{V_2\left(1+\frac{R_1}{R}\right)-V_1\left(\frac{R_1}{R}\right)\right\}\\ \qquad -V_1\left(1+\frac{R_1}{R}\right)+V_2\frac{R_1}{R}\end{array}\right]$$

$$\therefore \quad V_o=\frac{R_F}{R_2}\left(1+\frac{2R_1}{R}\right)(V_2-V_1)$$

$$\therefore \text{ Overall gain, } A_V=\frac{V_o}{V_2-V_1}=\frac{R_F}{R_2}\left(1+\frac{2R_1}{R}\right)$$

b) Draw and explain the circuit of V to I converter with floating load using OP-AMP.

Ans:- (Diagram- 2 mks, explanation/derivation-2 mks)

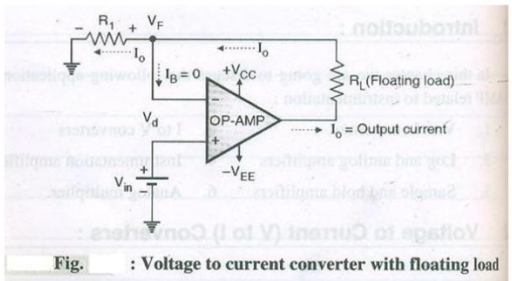


Fig. : Voltage to current converter with floating load

Description-

The input voltage is applied to the non-inverting (+) input terminal of the OP- AMP. Load resistance R_L is connected in place of the feedback resistor R_F (in the conventional non-inverting amplifier)
This circuit is also called as current series negative feedback amplifier.
This is because the feedback voltage across R_1 is proportional to the output current I_o and appears in series with the input voltage.
Apply KVL to the input loop

$V_{in} = V_d + V_f$

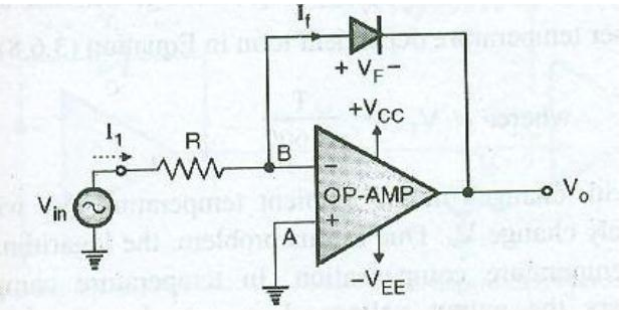
But as the open loop gain A_v of this OP- AMP is very large $V_d \approx 0$
Therefore $V_{in} = V_F$

But $V_{in} = R_1 \times I_o$ .....(as $I_B \approx 0$)

Therefore $I_o = V_{in} / R_1$

c) Describe the operation of logarithmic amplifier with neat circuit diagram.

Ans:- (Diagram- 2 mks, Operation- 2mks)



Description-(with derivation)

A p-n junction diode is connected in the feedback path. Therefore the output voltage is nothing but the voltage across this diode.

Therefore $V_o = -V_F$ --------1

Due to high impedance of OP- AMP the current going into the inverting terminal is zero

Therefore $I_1 = I_F = V_{in}/R$--------2

$$V_o = -\eta V_T [\log_e (I_f) - \log_e (I_o)]$$

$$= -\eta V_T [\log_e (V_{in}/R) - \log (I_o)]$$

Thus $V_o = -\eta V_T \log_e \left[\frac{V_{in}}{R \cdot I_o}\right]$

$\therefore V_o = -\eta V_T \log_e \left[\frac{V_{in}}{V_{ref}}\right]$

where $V_{ref} = R \cdot I_o$ = Fixed dc voltage.

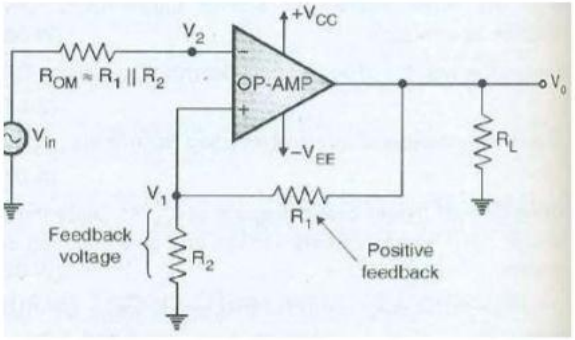
The output voltage is proportional to the logarithm of input voltage.

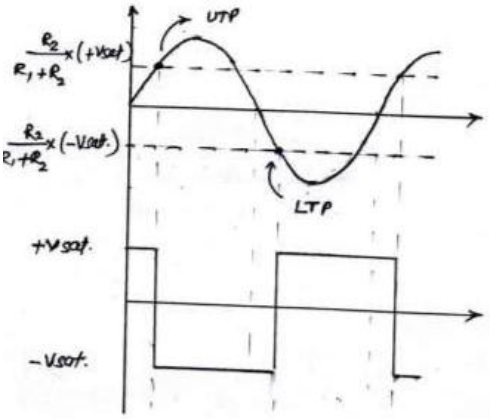
The output is in terms of natural log i.e. $\log_e$. If we want the output to be in terms of $\log_{10}$ then we should use the following conversion equation:

$\log_{10} V_i = 0.434 \log_e (V_i)$

d) Describe the operation of OP-AMP based Schmitt trigger for sine to square wave conversion with the help of circuit diagram.

Ans:- (Diagram- 2 mks, description- 1 mks, waveforms- 1 mks)





Operation-

Figure shows an inverting comparator with positive feedback. The circuit converts an irregular shaped waveform to a square wave or pulse. This circuit is known as Schmitt trigger.

The input voltage triggers the output, every time it exceeds certain voltage level called upper threshold voltage V_{ut} and lower threshold voltage V_{lt}.

The threshold voltage is obtained by the divider circuit $R_1 - R_2$. The voltage across R_1 is variable reference threshold voltage, that depends on the value and polarity of the output voltage V_o.

When $V_o = +V_{sat}$ the voltage across R_1 is called the upper threshold voltage V_{ut}. The input V_{in} is greater than V_{lt} and this causes V_o to switch from $+V_{sat}$ to $-V_{sat}$. As long as

$V_{in} < V_{ut}$, V_o is $+V_{sat}$ and

$$V_{ut} = \frac{R_1}{R_1 + R_2}(+V_{sat})$$

On the other hand, when $V_o = -V_{sat}$, the voltage across R_1 is referred to as lower threshold voltage V_{lt}. V_{in} must be slightly more negative than V_{lt} in order to cause V_o to switch from $-V_{sat}$ to $+V_{sat}$. Hence for $V_{in} > V_{lt}$, $V_o = -V_{sat}$ and

$$V_{lt} = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

Thus, if the threshold voltage V_{ut} and V_{lt} are made larger than the input voltages, the positive feedback will eliminate the false output transition. Also, the positive feedback, because of its regenerative action, will make V_o switch faster between $+V_{sat}$ and $-V_{sat}$ and $ROM = R_1 \| R_2$ compensate the offset voltage.

e) Explain working of active negative peak detector with neat circuit and waveforms.
Ans:- (Diagram- 2 mks, explanation- 1 mks, waveforms- 1 mks)

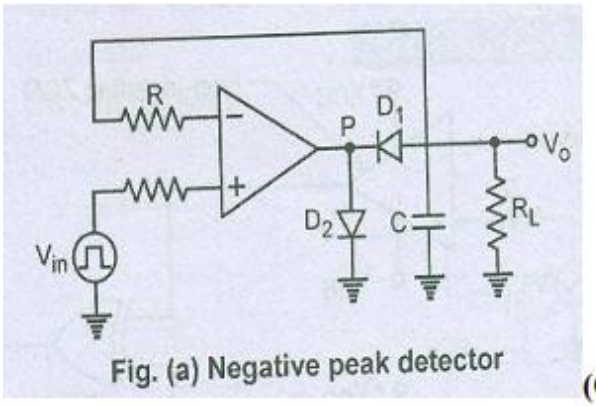
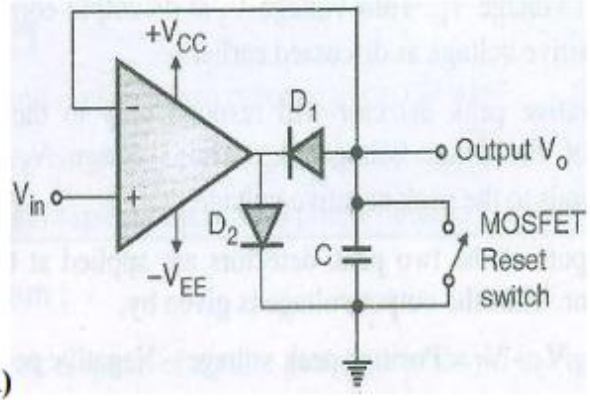


Fig. (a) Negative peak detector

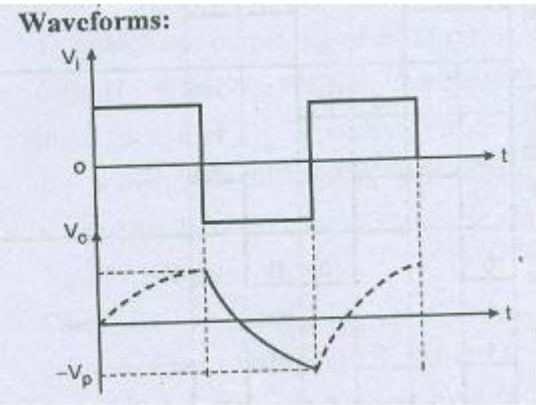
(OR)



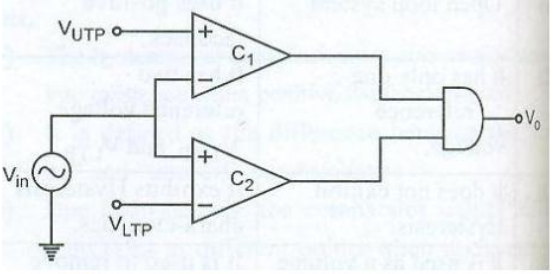
Operation-

During the positive half cycle, the potential B at point P is positive.
Hence, Diode D_1 is reverse biased and D_2 is forward biased.
Hence D_2 by passes the positive voltage towards ground and capacitor C remains un-charged.
During negative half cycle, potential P becomes negative, hence D_1 is forward biased.
Now, capacitor C starts charging for negative half cycle. And it charges up till the negative peak value.
As, the capacitor charges for the negative half cycle, hence, it is called as negative peak detector.

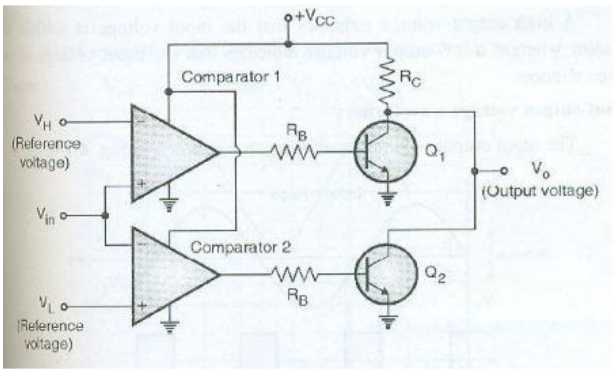
The MOSFET switch connected across the capacitor is to reset the circuit. By turning on this switch momentarily, we can discharge the capacitor completely.



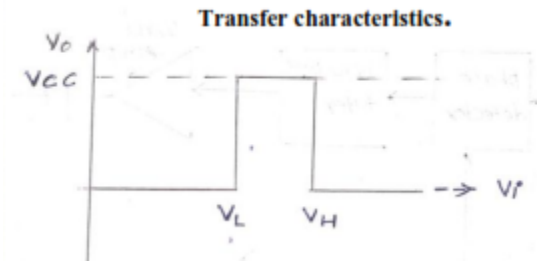
f) Draw the circuit of window detector. Describe its operation with waveform.
Ans:- (Diagram- 2 mks, explanation- 1 mks, waveforms- 1 mks)
Diagram-



OR



Waveform



Description-

- The window detector uses two comparator C_1 and C_2.
- The reference voltage of inverting comparator C_1 is V_{UTP} and the reference voltage of the non-inverting comparator C_2 is V_{LTP}. Assume $V_{LTP} < V_{UTP}$
- Case I: When $V_{in} < V_{UTP}$ then the differential voltage of C_2 is negative. Hence output of C_2 is low. V_{in} is also less than V_{UTP}. Hence output of C_1 is high and output V_o of AND gate is low.
- Case II: When $V_{in} > V_{UTP}$, then the differential input voltage of C_2 is high. The differential input voltage of C_1 is negative. The differential input voltage of C_1 is negative. Hence output of C_1 is low and output V_o of AND gate is low.
- Case III: When $V_{LTP} < V_{in} < V_{UTP}$, the differential input voltage of C_1 and C_2 is positive and output is high. The output of AND gate is high.

4. Attempt any FOUR of the following: 16

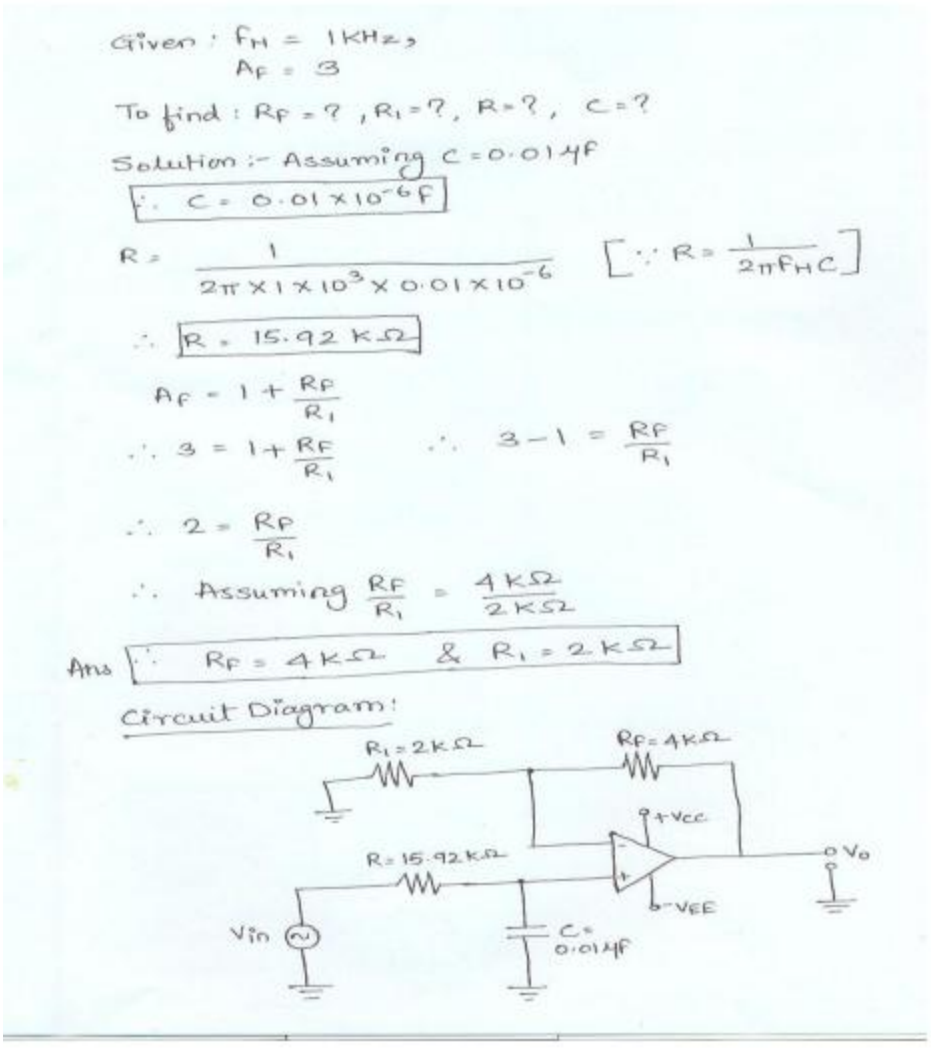
a) Write the comparison between comparator and Schmitt trigger.(four points)
Ans:-(4 relevant points- 4 mks)

Sr. No.	Parameter	Comparator	Schmitt trigger
1	**Definition**	It compares the two input voltages.	It converts any wave shape into square waves.
2	**Feedback**	In Comparator, open loop system	It uses positive feedback
3	**Hysteresis**	It does not exhibit hysteresis	It exhibit hysteresis
4	**External reference voltage.**	It has only one reference voltage	It has two reference voltage V_{UTP}

b) Design first order low pass filter with 1 KHz cut off frequency and pass band gain 3.

Ans:- (Proper design -2 mks, diagram- 2 mks)

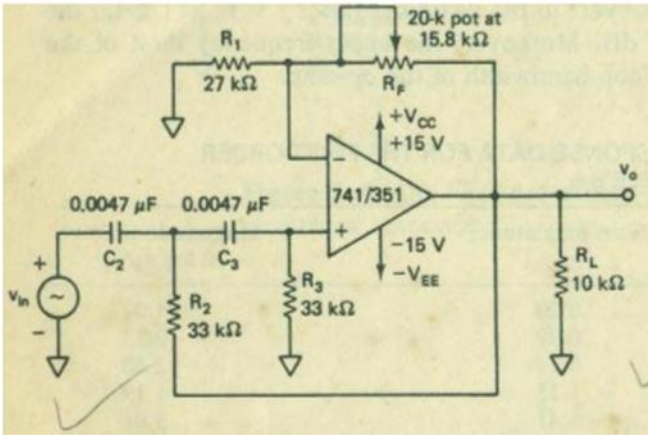
Value of R= 1M, Value of R_F& R_1= 1M, Design= 2M



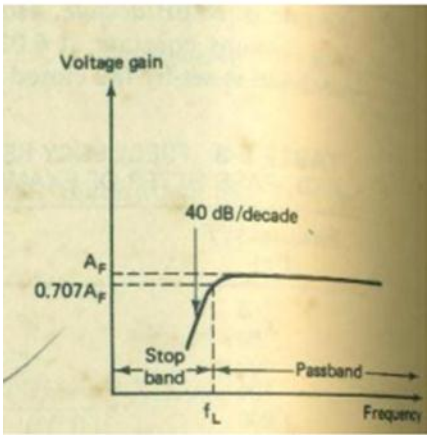
c) Draw the second order high pass filter and describe its operation.

Ans:- (Diagram-2 mks, description- 1 mks, frequency response- 1 mks)

Diagram



Frequency Response



Description-

The frequency response of the second order filter. It shows that the gain increases at a rate of 40 db/ decade in the attenuation band. This is doubled the rate of first order filter. This makes the frequency the frequency response sharper.

The second order filters are important because they can be used for designing the higher order filters.

- The resistors R_1 and R_F will decide the gain of the high pass filter. The gain can be made variable by keeping R_F variable.

The cut-off frequency f_c is determined by R_2, R_3, C_2 and C_3 as follows:

$$f_c = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

- The voltage gain magnitude is given by,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{VF}}{\sqrt{1+(f_c/F)^4}}$$

$A_{VF} = 1 + \frac{R_F}{R_1}$ = Passband gain of the filter.

d) Draw the circuit and frequency response of wide band reject filter and narrow band reject filter.

Ans:- (Each circuit- 1 mks, each frequency response- 1 mks)

wide band reject filter

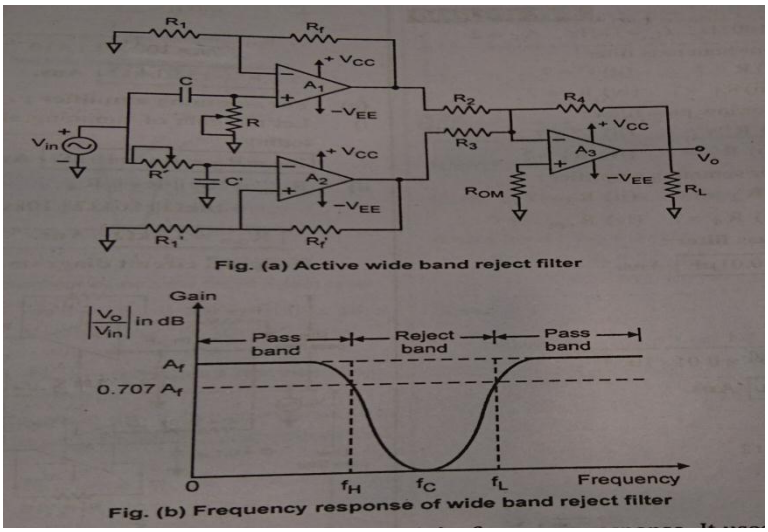


Fig. (a) Active wide band reject filter

Fig. (b) Frequency response of wide band reject filter

Narrow band reject filter.

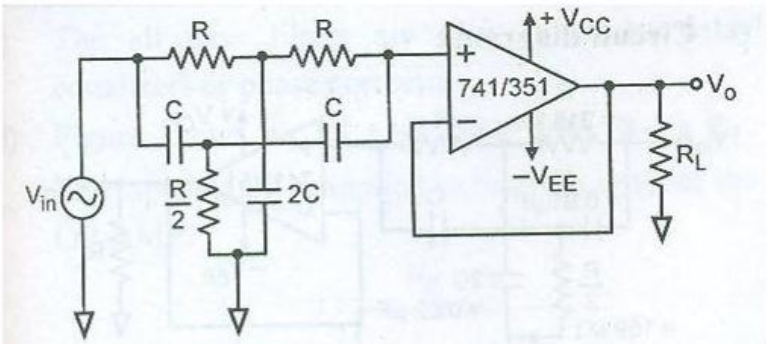


Fig. (a) Narrow band reject filter

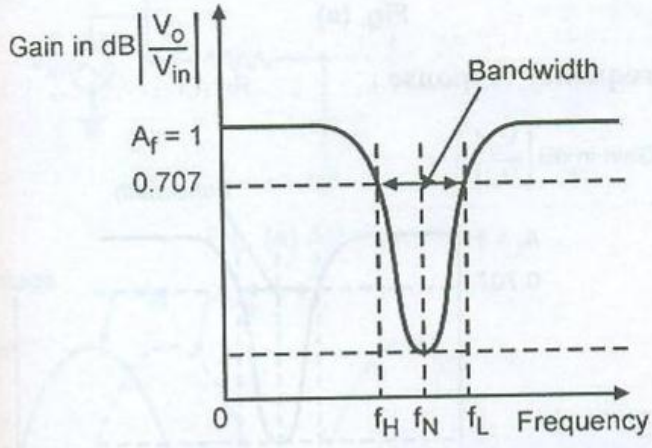
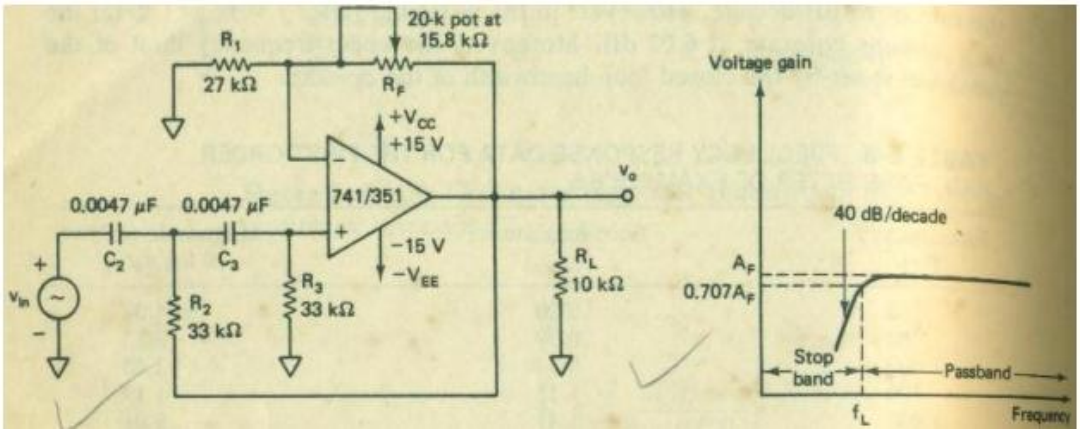


Fig. (b) Frequency response of narrow band reject filter

e) Draw the circuit diagram of second order high pass Butterworth filter with frequency response. Give expression for cut off frequency and gain.

Ans:- (Diagram- 1 mks , frequency response- 1 mks , expression- 1 mks each)

Diagram and frequency response



Expressions-

Cut-off Frequency $f_L = \frac{1}{2\pi \sqrt{R_2 C_2 R_3 C_3}}$

Gain $A_f = 1 + \frac{R_f}{R_1}$

f) Draw the circuit diagram of OPAMP based filter circuit which fulfill following response. Refer Figure No. 1.

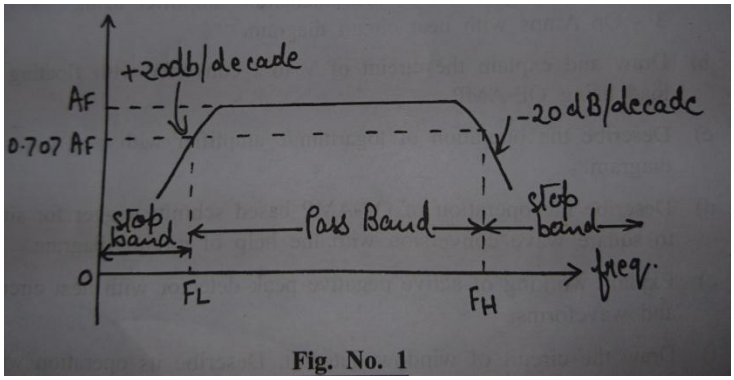


Fig. No. 1

Ans f. **(Naming of circuit – 1 mark, circuit diagram – 3 marks)**

- The given diagram is the frequency response of Wide Bandpass Filter.

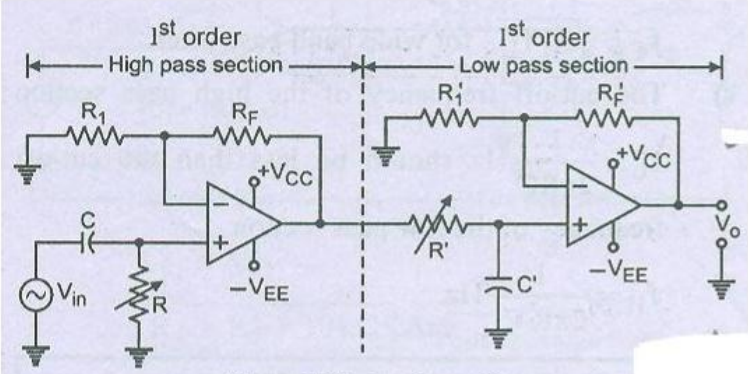


Fig. Wide band pass filter.

5 . Attempt any FOUR of the following: 16

a) Draw the functional block diagram of timer IC 555. State the function of internal PNP transistor in IC 555.

Ans:- (Functional diagram- 3 mks, function of PNP transistor – 1 mks)

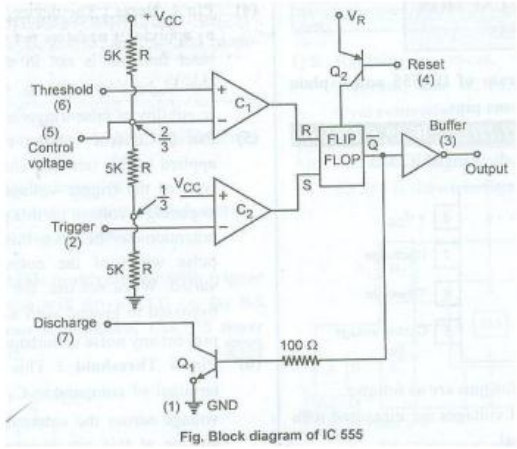
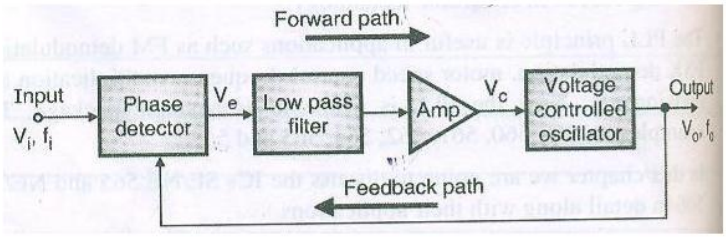


Fig. Block diagram of IC 555

Function of PNP transistor- The PNP transistor , also called as reset transistor is used to reset the timer IC. When a negative pulse is applied to pin 4 (reset pin) PNP transistor becomes on and resets the o/p of IC timer 555.For normal operation of IC 555, this pin 4 is connected to +Vcc.

b) Draw the block diagram of PLL and describe the function of each block.

Ans :- (Block diagram -2 mks, description-2 mks)



Phase locked loop consists of:

- A phase detector or phase comparator
- A low pass filter
- An error amplifier
- A voltage controlled oscillator (VCO)

Phase detector or phase comparator:

- The two points to a phase detector or comparator are the input voltage V_s at frequency f_s and the feedback voltage from a voltage controlled oscillator (VCO) at the frequency f_o

- The phase detector compares these two signals and produces a dc voltage V_e which is proportional to the phase difference between f_s and f_o. The output voltage V_e of the phase detector is called as error voltage.
- This error voltage is then applied to a low pass filter.

Low pass filter:

- The low pass filter removes the high frequency noise present in the phase detector output and produces output and produces a ripple free dc voltage.
- This dc voltage is amplified to an adequate level by the amplifier and applied to a voltage controlled oscillator (VCO). The dc amplifier output voltage is called as the control voltage V_C.

Voltage controlled oscillator (VCO):

- The control voltage V_C is applied at the input of a VCO.
- The output frequency of VCO is directly proportional to the dc control voltage V_C. The VCO frequency f_o is compared with the input frequency f_s by the phase detector and it (VCO frequency) is adjusted continuously until it is equal to the input frequency f_s i.e. $f_o = f_s$

The three states of operation through which the VCO undergoes are:

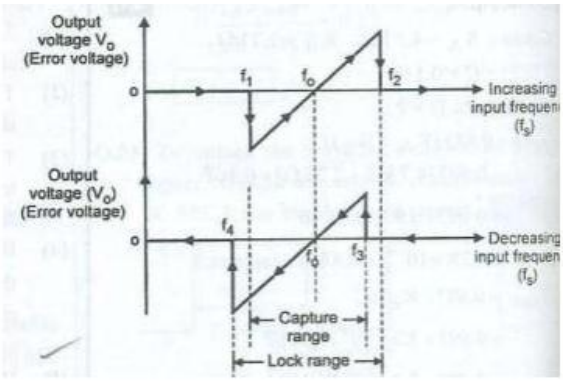
- Free running: There is no control on VCO output frequency f_o
- Capture: The comparison of f_o and f_s begins. The control voltage V_c starts adjusting f_o to bring it closer to f_s.
- Phase lock: When f_o is exactly equal to f_s the PLL is said to be phase locked. Once locked. One locked $f_o = f_s$ except for a finite phase difference φ

c) Draw transfer characteristics of PLL. Define:

(i) Lock range and

(ii) Capture range of PLL

Ans:- (transfer characteristics – 2 mks, each definition- 1 mks)



Lock in range: The range of frequencies over which the PLL can maintain the pahse lock with the incoming signal is defined as the lock in range.

$$\text{Lock range} = f_L - 2\,\Delta f_L$$

$$\text{Where } f_L = 8\, f_0 / V$$

Capture range: Capture range of PLL is defined as the range of frequencies over which the PLL can acquire lock with the input signal

$$\text{Capture range} = 2\,\Delta f_c$$

$$\text{Where } f_c = f_L / (2\pi * 3.6 * 10^3 * C)$$

d) Draw the circuit diagram of touch plate switch using IC 555 and describe its operation.

Ans:- (Diagram – 2 mks, description – 2 mks)

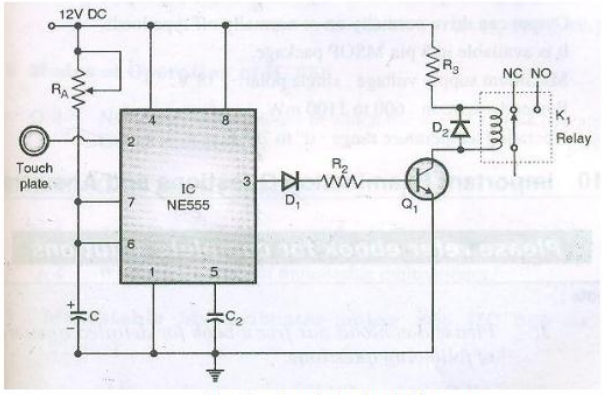


Fig: Touch switch circuit diagram

OR

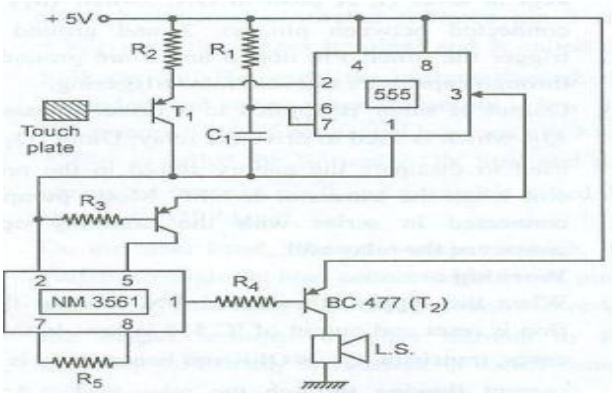


Fig : Touch Plate Switch using IC 555

Description-

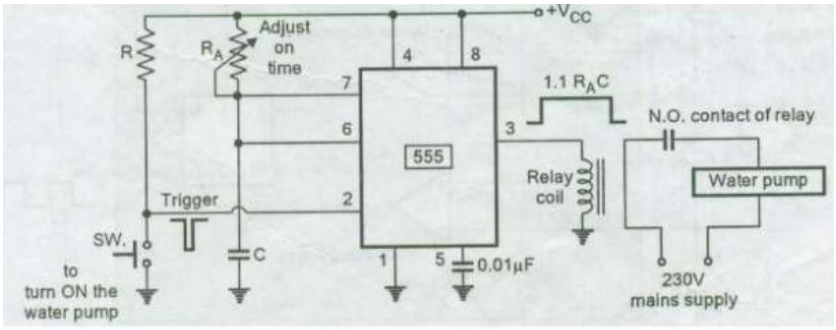
A touch plate (push to ON) is used to turn on the timer and active the relay.

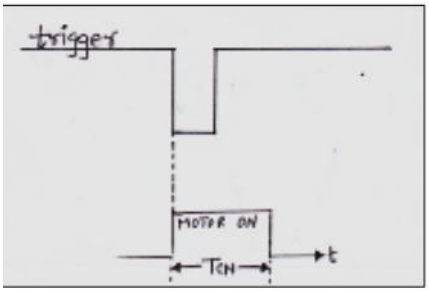
As soon as touch plate is switched ON (pushed), a trigger pulse is produced and applied to pin no. 2 of IC 555, and the output of IC 555 goes high.

It will remain high for a period of T_{ON}= 1.1 R_AC. The high output of IC 555 activates the transistor Q_1 which in turn energize the relay coil, and closes the N.O (Normally open) contact of the relay.

e) Draw and describe the operation of water level controller using IC 555.

Ans:- (Diagram – 2 mks, description – 2 mks)





In water level controller, IC 555 is used in the monostable multivibrator mode.
As soon as switch is ON, a trigger pulse is produced & applied to pin no 2 of IC 555 & the output of IC 555 goes high.
It will remain high for time period $T_{ON} = 1.1R_A.C$
The high output of IC 555 will energize the relay coil & close the normally open (N.O) contact of the relay to connect the 230 volt ac supply to the water pump motor.
The motor will remain on for the on for the ON time of monostable circuit. $T_{ON}=1.1.R_A.C$
The on time can be adjusted as per requirement by varying the resistance R_A.

f) Describe with the help of block diagram the operation of FM demodulator using PLL.

Ans:- (Diagram – 2 mks, description – 2 mks)

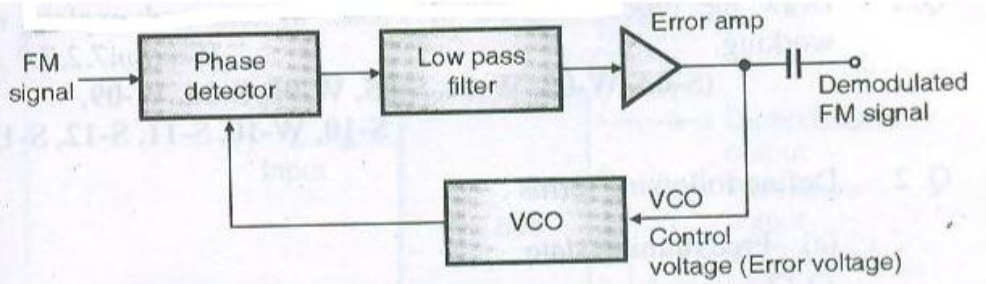


Fig. : PLL used as FM demodulator

Operation:

- The FM signal which is to be demodulated is applied at the input of the PLL.
- the PLL is locked to the FM
- The error voltage produced at the output of the amplifier is proportional to the deviation of the input frequency from the center frequency of FM. Thus, the at component of the error voltage represents the modulating signal. Thus at the error amplifies output we get demodulated
- The FM demodulator using PLL ensures a high Linearity, between the instantaneous input frequency and VCO control voltage (error amplifier output)

6 . Attempt any FOUR of the following: 16

a) Describe the working of voltage controlled oscillator using IC 741.

Ans:- (Diagram – 2 mks, description – 2 mks)

Note: If candidate attempted VCO by using IC555, can be considered. Reward appropriate marks to the candidate.

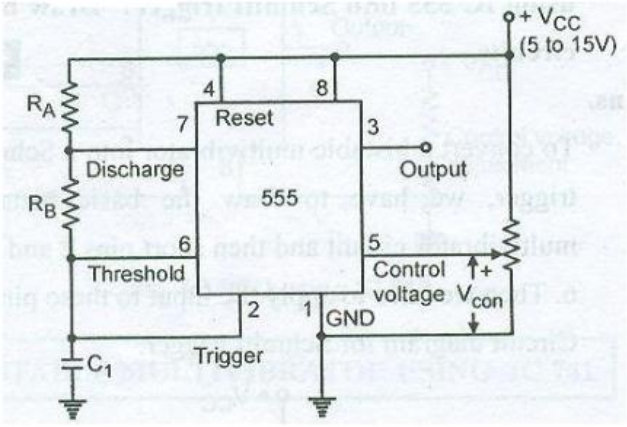


Fig: Circuit diagram of VCO using IC 555

Operation-

The constant current source/ sink block is used to charge and discharge the externally connected timing capacitor C_T linearly.

The value of charging and discharging current is dependent on the control voltage V_C applied at pin number (5) modulating input.

This current can also be changed by varying the external timing resistor R_T.

The potential difference between pins (5) and (6) I almost zero. That means these pins are equipotential.

Therefore if we increase the modulating voltage V_C at pin number (5), the voltage at pin number (6) will increase with the same amount.

This reduces the voltage drop across R_T and reduces the charging current.

The voltage across the capacitor is thus triangular wave. This triangular wave is applied to a buffer A_1.

The buffer is connected in order to avoid to avoid any possible loading of the capacitor.

The buffer output is taken out at pin number (4) as triangular wave output.

The buffer output is also applied to a Schmitt trigger A_2, which converts the triangular wave into square waveform.

Resistors R_a and R_b is a potential divider generating the reference levels for the upper and lower trigger voltages. This square wave is inverted by inverter A_3 and made available at pin number (3).

b) Draw the circuit diagram of Wein bridge oscillator using IC 741 and give expression for frequency of oscillations.

Ans:- (Diagram – 3 mks, Frequency expression- 1 mks)

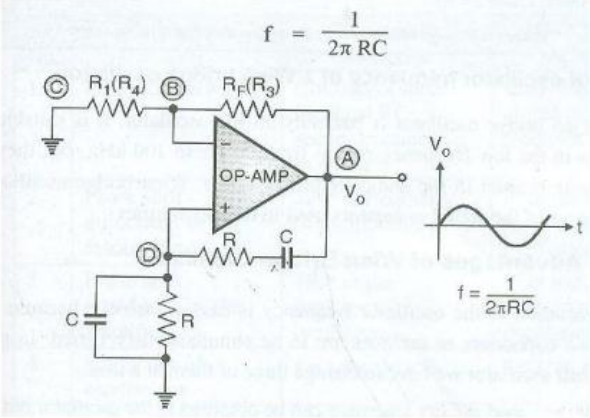


Fig: Wein bridge oscillator using OP-AMP

Frequency of Oscillation-

$$f = \frac{1}{2\pi RC}$$

c) Design and draw monostable multivibrator using IC 555 with Tp = 1ms.

Ans:- (Design steps- 2 mks, diagram- 2 mks)

Given- Tp= 1 ms

For Monostable multivibrator-

Tp=1.1 RC

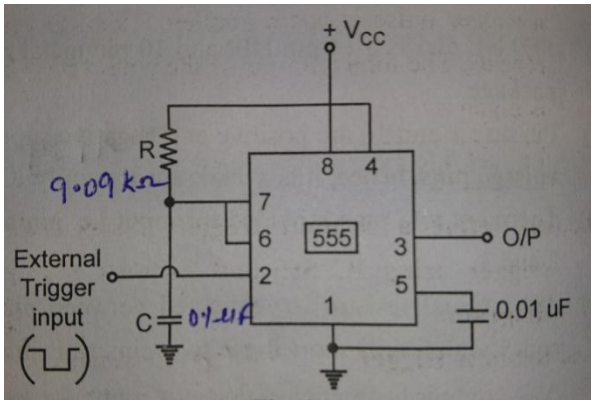
Assume C= 0.1 µf

Therefore-

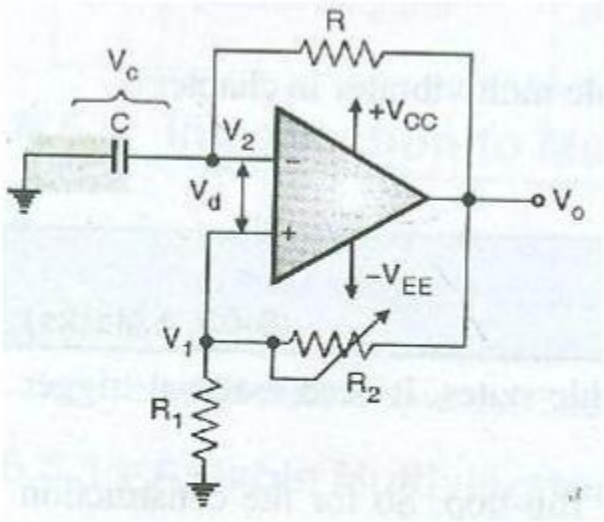
$1* 10^{-3}= 1.1* R* 0.1* 10^{-6}$

R= 9.09 KΩ

Diagram-



d) Draw and describe operation of astable multivibrator using OPAMP.
Ans:- (Diagram- 2 mks, description – 2 mks)



- The time period the output waveform is given by,

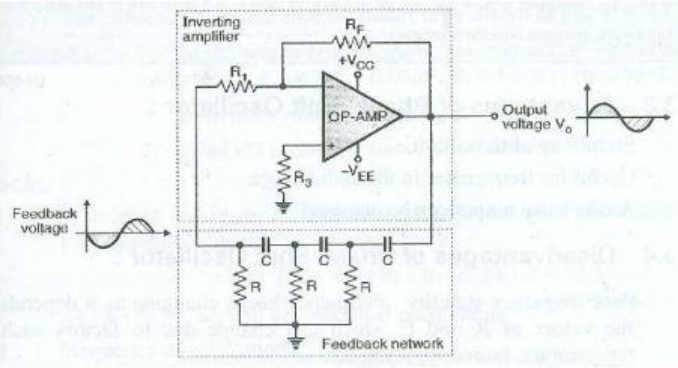
$$T = 2RC \log_e \left[\frac{2R_1 + R_2}{R_2}\right]$$

- The expression for output frequency is given by,

$$f_o = \frac{1}{T} = \frac{1}{2RC \log_e [(2R_1 + R_2)/R_2]}$$

- If we substitute $R_2 = 1.16R_1$ then the above equations becomes
  $f_o = 1/2RC$

e) Draw and explain the working of phase shift oscillator using IC 741.
Ans:- (Diagram- 2 mks, explanation- 2mks)



Description-

The OP- AMP is used as an inverting amplifier. Therefore it introduces a phase shift of 180^0 between its input and output.

The output of the inverting amplifier is applies at the input of the RC phase shift network. As discussed earlier, this network will introduce a phase shift of 180^o. This feedback network attenuates the signal at its input and feeds it to the amplifier input. The level of attenuation is decided by the feedback factor β.

The gain of the inverting amplifier is decided by the values of R_F and R_1. This gain is adjusted in such a way that the product Aβ is slightly greater than 1.

It can be proved that the value of feedback factor β at the frequency of oscillations is β=1/29. For sustained oscillations, the loop gain $A\beta \geq 1$. Therefore, in order to make the loop gain $A\beta \geq$, the gain of the inverting amplifier A should be greater than or equal to 29.

Gain of the inverting amplifier is given by,

$A= R_F/ R_1$

Therefore: $R_F/R_1 \geq 29$ or $R_f \geq 29R_1$

These values of R_F and R_1 will insure sustained oscillations.

The expression for frequency of oscillations of an RC phase shift oscillation using OP_ AMP is given by,

$$f_o = 1/ 2\pi \sqrt{6} RC$$

f) Define:

i) Q factor of filter

ii) Pass band of filter

Give the relation between roll off rate and order of filter.

Ans:- (Each definition- 1 mks, relation table- 2 mks)

i) Q factor-It is defined as the ratio of centre frequency to the bandwidth and given as-

Q=Fc/BW

ii) Pass band of filter- It is the band or range of frequencies which is passed through the filter freely.

Relation between roll off rate and order of filter

Order of Filter	Roll off Rate
1	20dB/ decade
2	40dB/ decade
3	60dB/ decade
4	80 dB/ decade