Unit - IV

INVERTERS

INVERTERS :-

A device that converts dc power into ac power at desired output voltage and frequency is called an Inverter.

Applications of inverter :-

* Adjustable ac drives
* Battery driven vehicles
* HVDC transmission lines
* UPS
* Stand by air craft power supplies.

CLASSIFICATION OF INVERTERS :-

I BASED ON METHOD OF COMMUTATION :-

1) Line commutated inverters :-

In case of ac circuits, when current in SCR goes through natural zero, the device is turned OFF. Inverters working on this principle are called as line commutated inverters.

2) Forced commutated inverters :-

In case of dc circuits, since the supply voltage does not go through zero point, some external components are required to turn OFF the device. Inverters working on this principle are called as forced commutated inverters.

II BASED ON THE CONNECTION:-

Based on the way in which the SCR and the commutating components are connected they are classified as

(i) Bridge inverter
(ii) series inverter
(iii) Parallel inverter.

III BASED ON TYPE OF INPUT:-

(i) Voltage source Inverter (VSI) (or) Voltage fed inverter (VFI) (or) Voltage driven inverter

* A VSI is one in which the dc source has small or negligible impedance. It has stiff dc Voltage source at its input terminals.

(or)

* A VSI is one in which the input voltage of the inverter is maintained constant.

(ii) Current source Inverter (CSI) (or) current fed inverter (CFI) (or) current driven inverter

* A CSI is one in which the dc source has high input impedance (or)

* A CSI is one in which the input current of the inverter is maintained constant.

(iii) Variable dc linked inverter:-

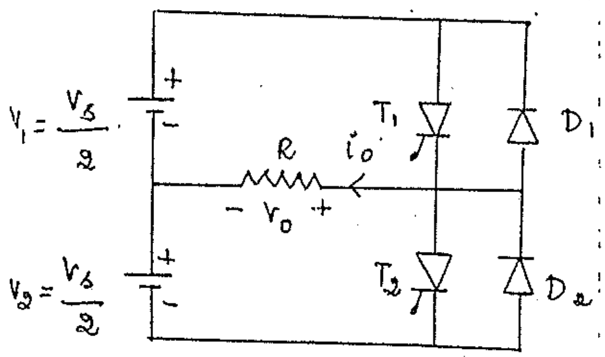
If the input voltage of the inverter is controllable it is called as variable - dc linked inverter.

BRIDGE TYPE 1φ VSI (Vge source inverter) :-

(i) single phase half bridge inverter
(ii) Single phase full bridge inverter

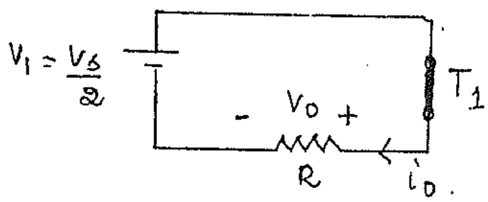
(i) 1φ HALF BRIDGE VSI :-

(a) with R load :-



* For R load D_1, D_2 does not conduct.
* Output current is constant.
* Output waveforms are drawn on the assumption that SCRs conduct for the duration its gate pulse is present and is commutated as soon as the pulse is removed.

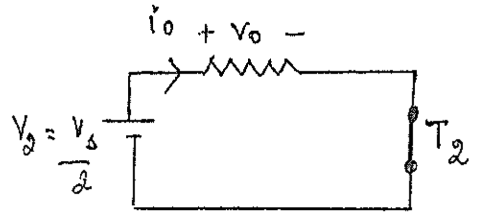
Mode 1 :- T_1 ON :-



* At $t = 0$, SCR T_1 is turned ON, T_2 is OFF.
* $V_0 = V_1 = \frac{V_s}{2}$
* $i_0 = \frac{V_0}{R} = \frac{V_s}{2R}$

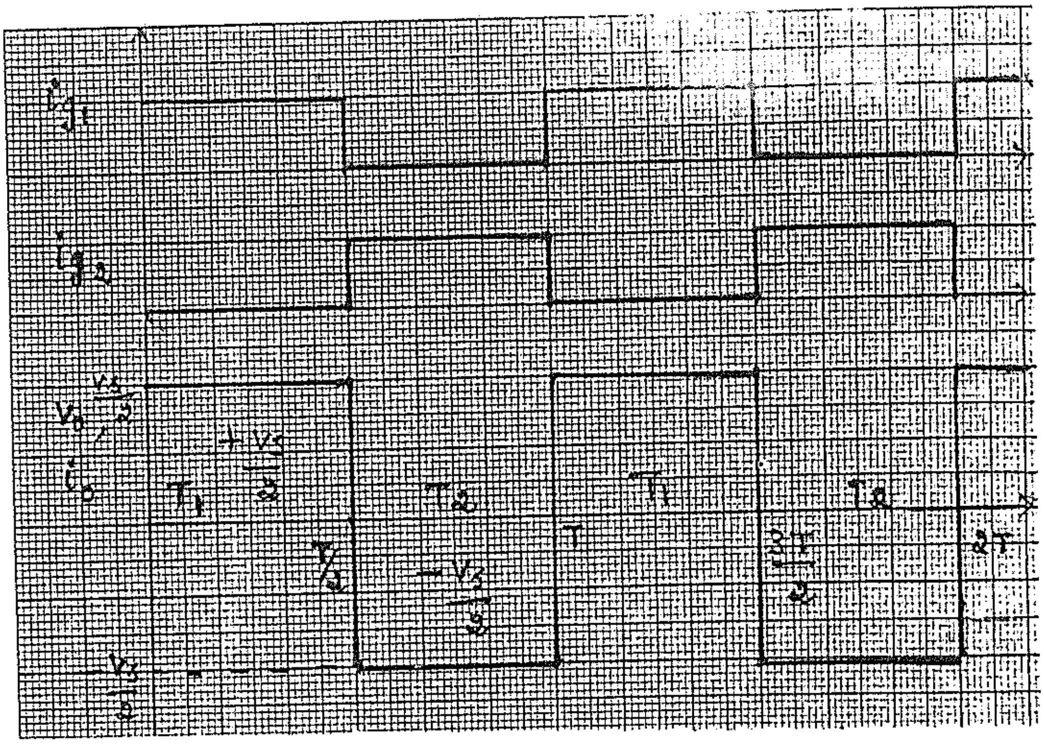
* At $t = T/2$ SCR T_1 is turned OFF and T_2 is turned ON.

Mode 2 :- T_2 is ON :-

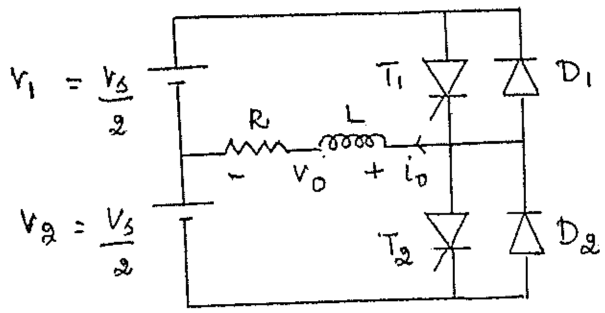


* At $t = T/2$ SCR T_2 is turned ON, T_1 is OFF
* direction of i_0 and V_0 is reversed.
* $V_0 = -V_2 = -\frac{V_s}{2}$, $i_0 = \frac{V_0}{R} = \frac{-V_s}{2R}$

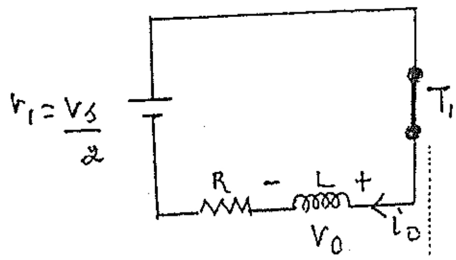
* At $t = T$ SCR T_2 is turned OFF and T_1 is turned ON.



b) with R-L load :-



T_1 ON :-



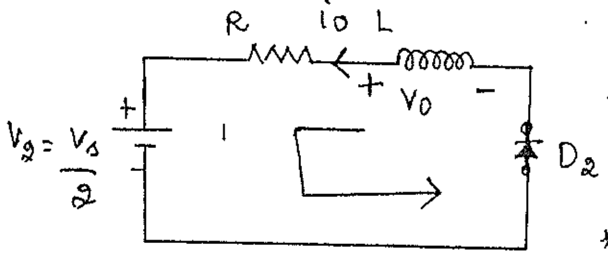
* Say at time $t = t_1$ SCR T_1 is turned ON
* V_0, i_0 is in +ve direction.
* $V_0 = V_1 = \frac{V_s}{2}$
* i_0 increases slowly to maximum value due to the RL load.
* At time $t = t_2$ T_1 is turned OFF and gate pulse is given to SCR T_2.

* At time $t = t_2$; when SCR T_1 is turned OFF, the gate Pulse is given to SCR T_2.

* when T_1 is OFF, the voltage polarity across the inductor is reversed. This reverse voltage across the inductor reverse biases the SCR T_2. ∴ even if the gate pulse is available SCR T_2 does not turn ON.

* The voltage across the inductor forward biases the diode D_2. ∴ the diode D_2 conducts till all energy stored in L is dissipated (or) till i_0 reaches zero.

D_2 is ON at $t = t_2$:-



* D_2 is ON

* Output Voltage is the Voltage across the inductor

* ∵ polarity of voltage in inductor is reversed ∴ $V_0 = -\frac{V_s}{2}$

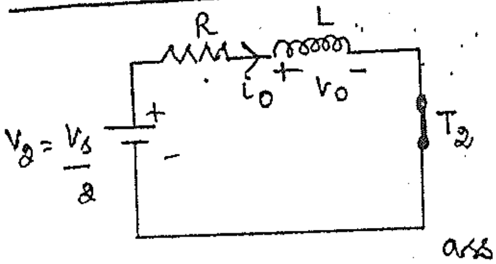
* But the output current i_0 is maintained in the same direction. V_0 is -ve; i_0 is +ve.

* Load current now flows from load to source (regeneration). (i_0 ↓es)

* Now when the energy stored in the inductor is freewheeled through diode D_2, the current reaches zero.

* Now when the current i_0 decreases and reaches zero at $t = t_3$ diode D_2 is OFF. At the same time SCR T_2 is turned ON since the gate Pulse is already available across T_2.

T_2 is ON at $t = t_3$:-



* At $t = t_3$; when D_2 is OFF, SCR T_2 is turned ON
* Now v_0, i_0 are opposite to the assumed positive direction.

∴ V_0, i_0 is −ve.

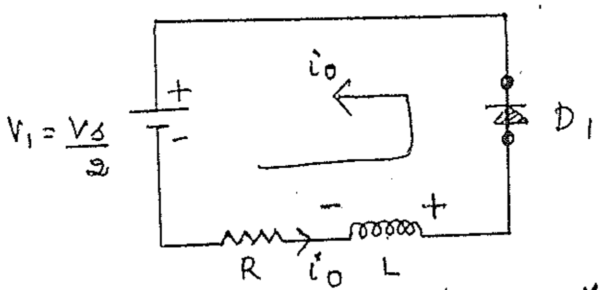
* ∴ $V_0 = -\frac{V_s}{2}$
* i_0 increases slowly in the reverse direction.

Now at time $t = t_4$; SCR T_2 is turned OFF and gate pulse is given to SCR T_1.

* when T_2 is OFF the voltage across the inductor is reversed. This reverse vge across the inductor reverse biases T_1. ∴ T_1 cannot turn ON even when the gate pulse is given.

* But the voltage across the inductor forward biases diode D_1. ∴ at $t = t_4$. D_1 is ON. till i_0 reaches zero.

D_1 is ON at $t = t_4$:-

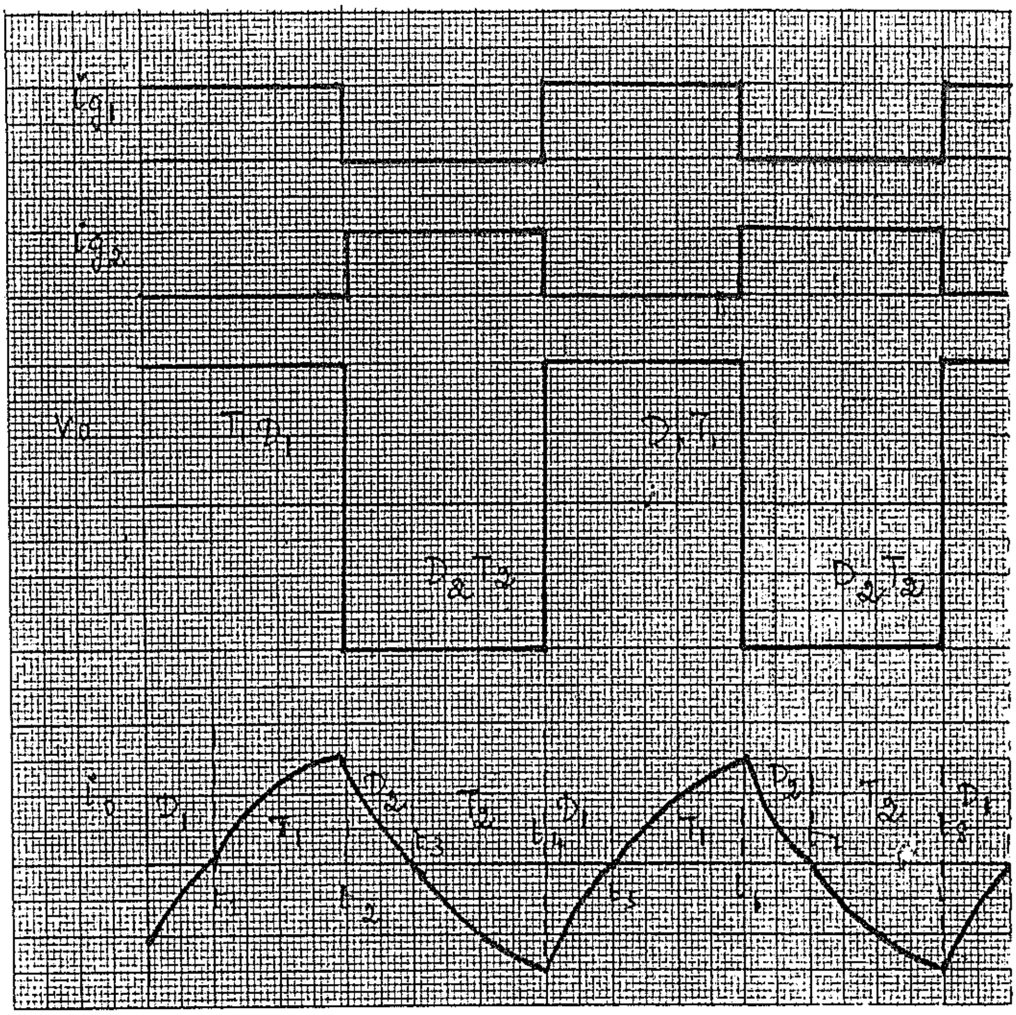


* D_1 is ON
* current is maintained in same direction.
* i_0 decreases slowly in −ve direction
* But vge is +ve.

$V_0 = +\frac{V_s}{2}$

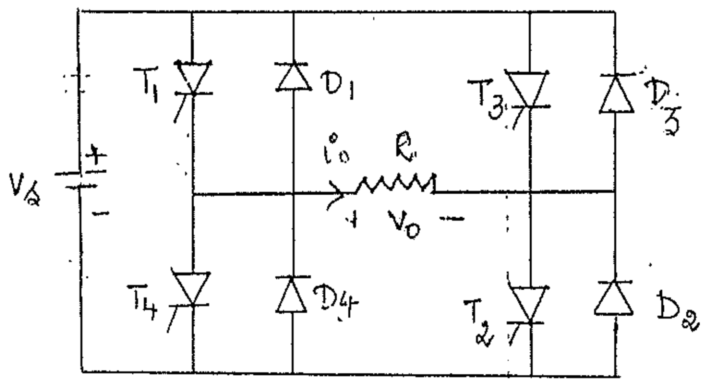
* $i_0 = -ve$; V_0 is +ve.

* At $t = t_5$; i_0 decreases to zero, ∴ D_1 is OFF
* when D_1 is OFF, T_1 is ON because already gate pulse is available across T_1. ∴ again mode 1 will continue.



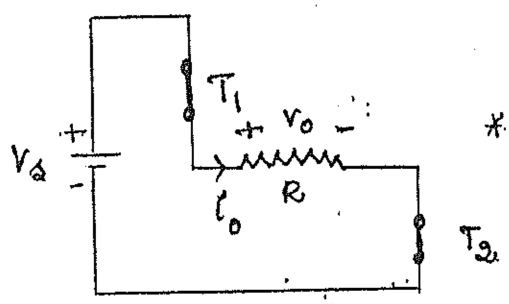
(ii) 1ϕ FULL BRIDGE INVERTER :-

a) with R load :-



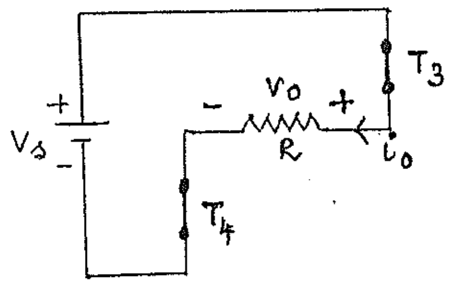
* For R load, the diodes D_1, D_2, D_3, D_4 does not conduct.

T_1 and T_2 ON :-



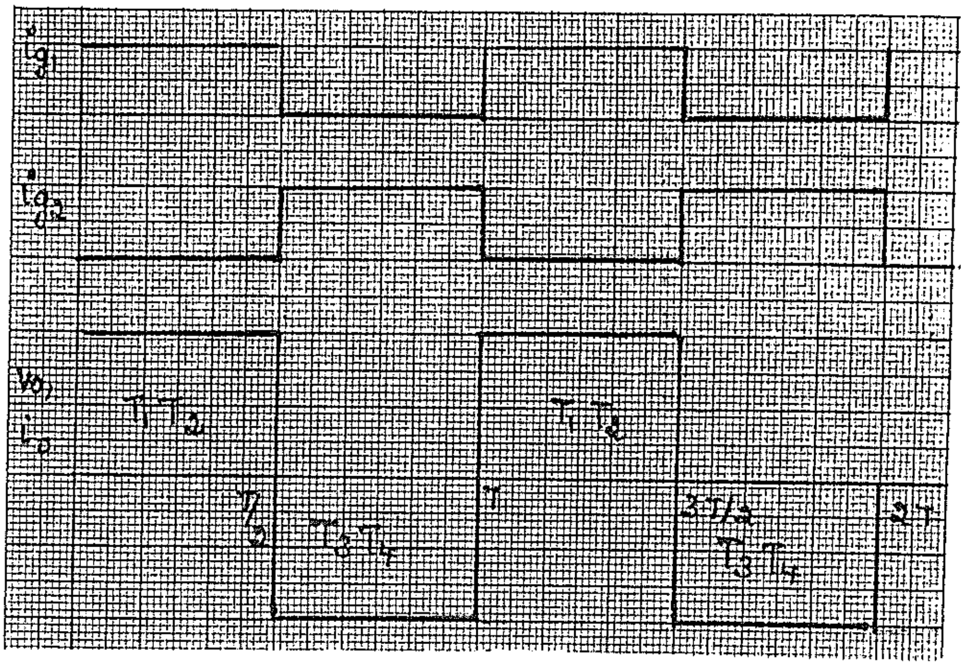
* At time $t = 0$; SCR T_1 and T_2 are turned ON by giving gating Pulses.
* Now V_0, i_0 is +ve.
* $V_0 = V_s$; $i_0 = \frac{V_0}{R} = \frac{V_s}{R}$
* At $t = T/2$; T_1, T_2 are turned OFF

T_3 and T_4 ON :-

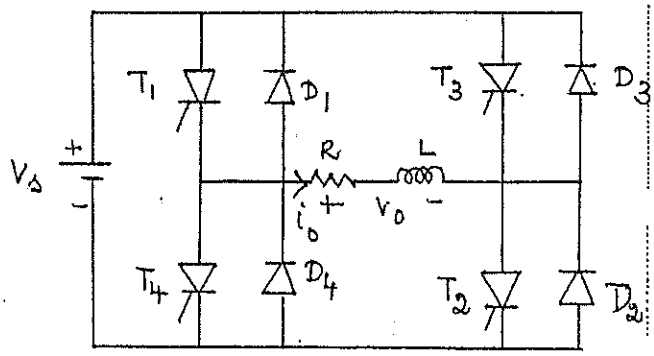


* At $t = T/2$; T_3, T_4 are turned ON by giving gate pulses.
* V_0 and i_0 are opposite to assumed +ve direction.
* $\therefore$ V_0, i_0 are −ve.
* $V_0 = -V_s$; $i_0 = \frac{V_0}{R} = \frac{-V_s}{R}$

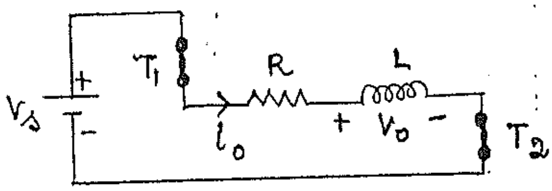
At $t = T$; $T_3 T_4$ is turned OFF and $T_1 T_2$ ON.



b) with RL load :-



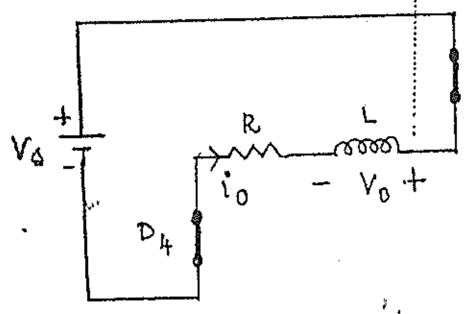
T_1 and T_2 ON :-



* At time $t = t_1$, SCR T_1 and T_2 are turned ON.
* V_0, i_0 are +ve.
* $V_0 = V_s$

* i_0 slowly increases in +ve direction.
* At time $t = t_2$; SCR T_1 and T_2 are turned OFF and gate pulse is given to SCR T_3 and T_4.
* when T_1 and T_2 is turned OFF, the polarity of vge across the inductor is reversed. This vge across the inductor reverse biases SCR T_3 and T_4. ∴ even if the gate pulse is available they are not turned ON.
* The voltage across inductor forward biases the diode D_3 and D_4. ∴ D_3 & D_4 conduct till i_0 reaches zero.

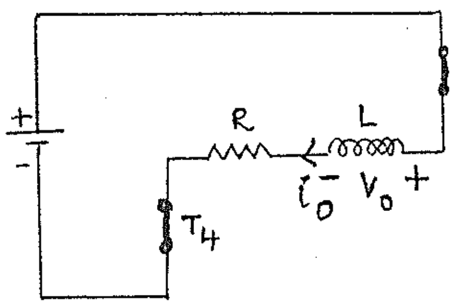
D_3 and D_4 ON at $t = t_2$:-



* D_3 and D_4 is ON
* Output Voltage is -ve, since the Voltage in the load (L) is reversed.
* $V_0 = -V_s$.
* But the output current i_0 is maintained in the same direction. i_0 is +ve.
* Load current i_0 decreases (or) freewheels through D_3, D_4. i_0 decreases in +ve direction.
* Now when the current i_0 ↓es and reaches zero, the diodes D_3 and D_4 is reverse biased and turned OFF, at time $t = t_3$.

At time $t = t_3$, when D_3 and D_4 is OFF, SCRs T_3 and T_4 turn ON (∵ gate pulse is already available across them).

T_3 and T_4 ON :-

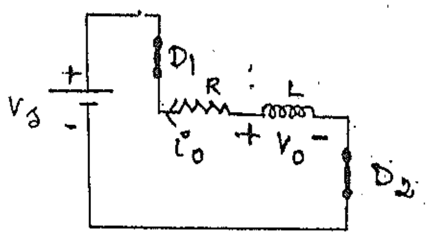


* At $t = t_3$, T_3 and T_4 are ON.
* V_0, i_0 are opposite to assumed +ve direction.
* ∴ V_0, i_0 is -ve.
* ∴ $V_0 = -V_s$
* i_0 increases slowly in the reverse direction.
* Now at time $t = t_4$, SCR T_3 & T_4 are turned OFF and gate pulse is given to SCR T_1 and T_2.

* when T_3 and T_4 is OFF, the voltage across the inductor is reversed. This vge reverse biases T_1 and T_2.
∴ T_1 and T_2 cannot turn ON even if gate is given.

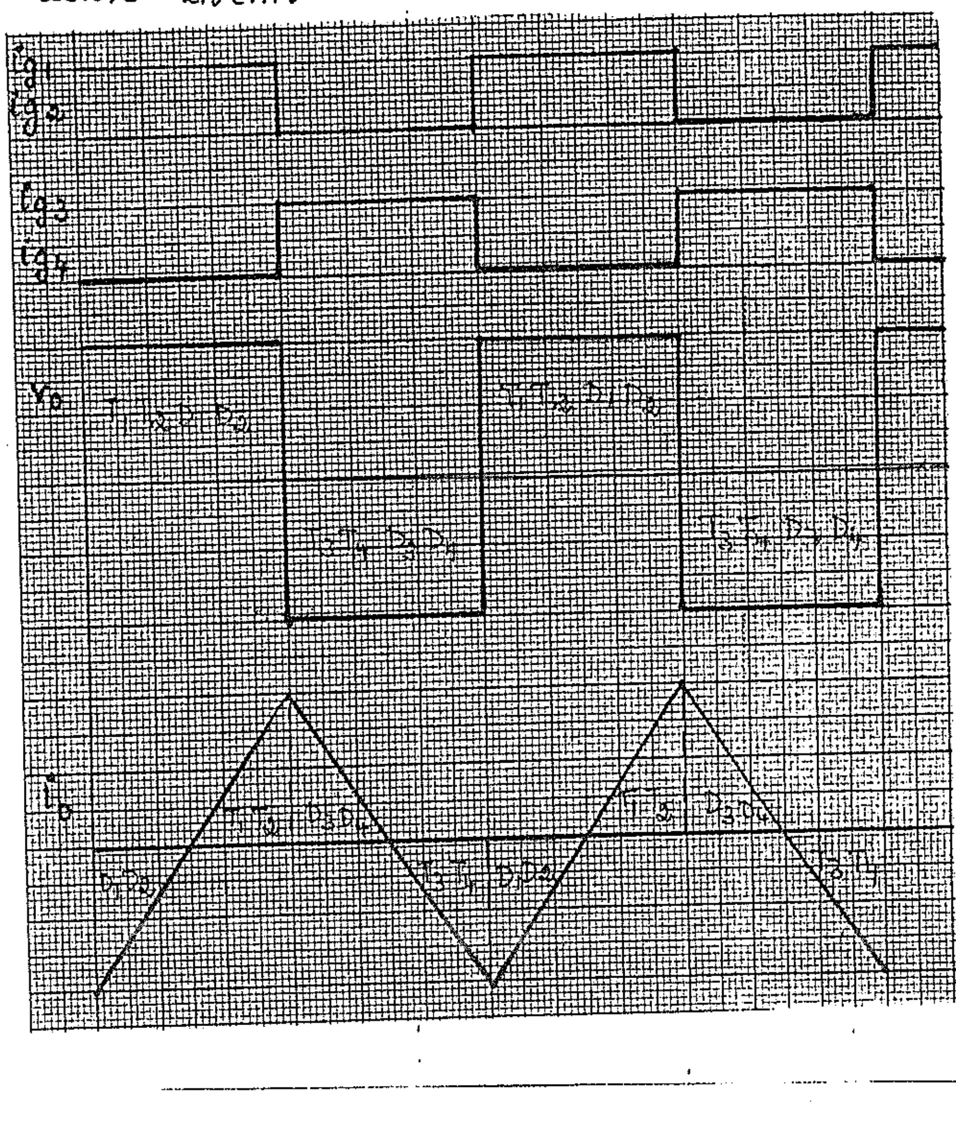
* But this vge forward biases diode. D_1 and D_2. D_1, D_2 conduct till i_0 is zero.

D_1 and D_2 ON at $t = t_4$:-



* D_1 and D_2 is ON
* current is maintained in same direction
* i_0 decreases slowly in -ve direction
* Vge is +ve ; $V_0 = V_s$
* i_0 is -ve.

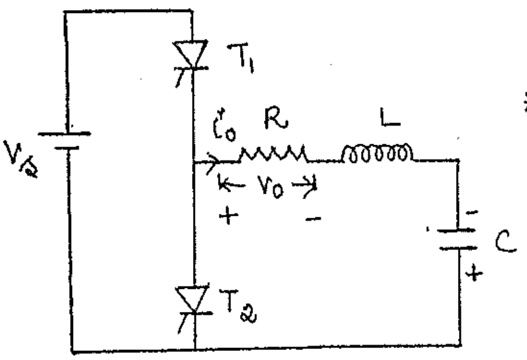
* At $t = t_5$; $i_0 = 0$ ∴ D_1, D_2 is OFF. As D_1, D_2 is turned OFF SCR T_1 and T_2 are turned ON since gate pulse is available across them.



(ii) SERIES INVERTER:

* An inverter in which the commutating components (L and C) are connected in series with the load is called as series inverter.

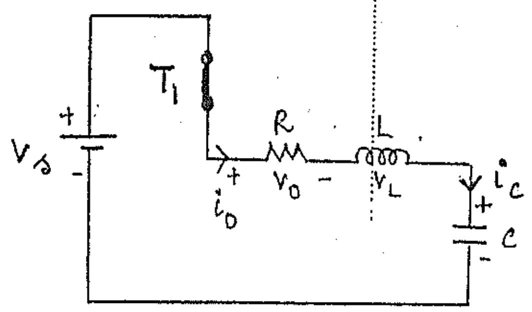
* As current attains zero value naturally, due to the nature of the series circuit, the inverter is also called as self commutated (or) load commutated inverters.



* It consists of load resistance 'R'
* commutating components L and C are connected in series with load 'R'
* SCR T_1 and T_2 are turned ON so that o/p voltage of desired frequency can be obtained.

* Capacitor C is precharged with upper plate negative and lower plate positive. $V_C = -V_s$

Mode 1 :- SCR T_1 ON :-



* SCR T_1 is ON at time $t=0$.
* current i_0 flows in the circuit through R – L – C
* ∵ capacitor is precharged the Vge is $V_c = -V$;
* $V_s = V_L + V_c$.

$i_0 = i_c$

* Due to current i_0 capacitor C is charged to upper plate +ve and lower plate –ve; ∴ $V_c = +V$.

w.k.T when current is max, $V_c = 0$ at $t = t_1$
zero, $V_c = +V$ at $t = t_2$

* when capacitor charges from $+V_s$ to $-V_s$ the current is zero.

* when current goes through zero SCR T_1 is turned OFF.

* Similarly when $i_0 \uparrow$ vge across L ↑es. and when $i_0 \downarrow$ vge across L ↓. ($V_L = V_{..}$)

[Already seen in Unit - I RLC circuit]

$V_0 = V_R$; $i_0 = \frac{V_0}{R}$ (V_0, i_0 is +ve)

Mode II :-

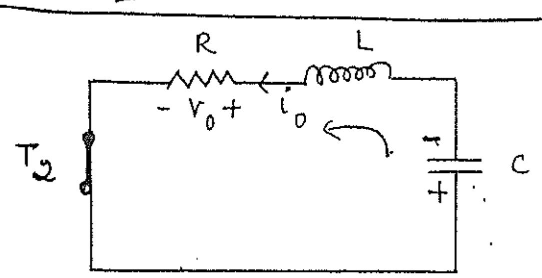
*SCR T_2 is not triggered immediately after T_1 is OFF.

* If T_2 is triggered immediately, then T_1 and T_2 will short the supply V_s.

* This time delay between the conduction of T_1 and T_2 is called dead band. (from t_2 to t_3)

* During the dead band $V_R = 0$; $V_L = 0$; $V_C = +V$.

Mode III :- T_2 is ON.



* SCR T_2 is triggered at time $t = t_3$

* The capacitor discharges through L, R and T_2.

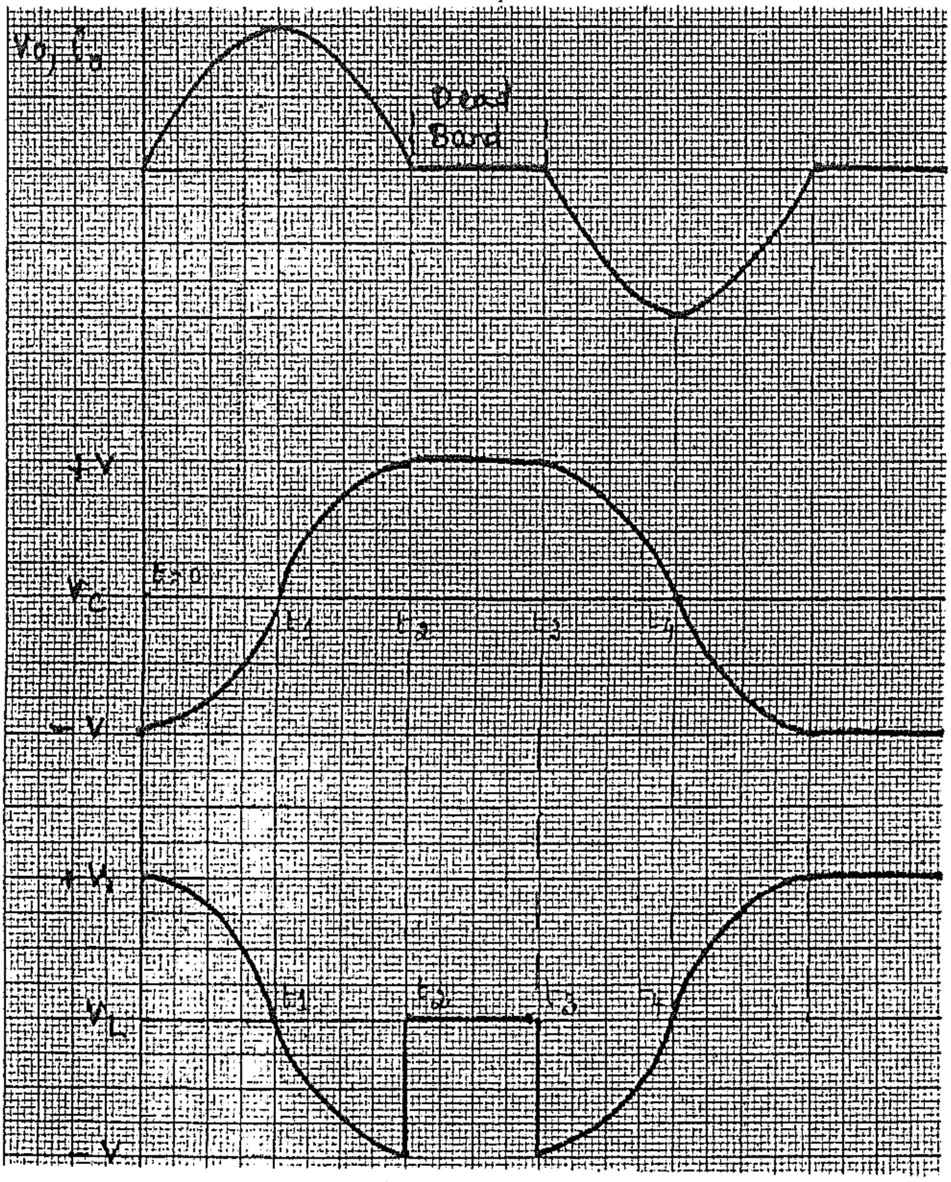
* V_0, i_0 in R are opposite to assumed positive direction. ∴ V_0, i_0 are -ve. $i_0 = i_c$.

* At $t = t_4$ i_c is max and $V_C = 0$.

* At $t = t_4$ i_c decreases to zero and $V_C = -V_s$.

* At $t = t_4$ $i_c = 0$, ∴ current thro T_2 is zero and ∴ SCR T_2 is turned OFF.

* After some dead band SCR T_1 is again turned ON.

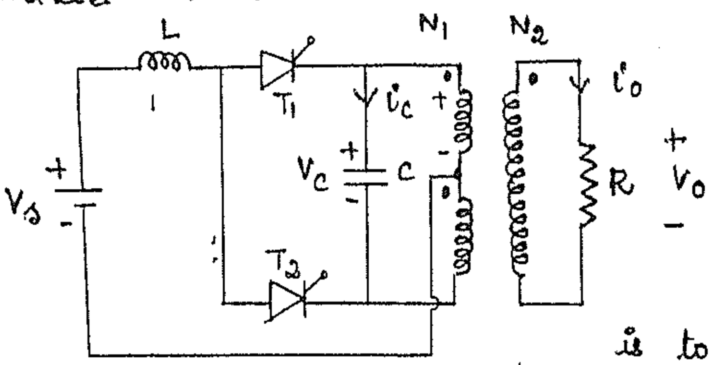


<u>Disadvantages of series inverter :-</u>

* Battery is used only during +ve half cycle.
* Output voltage has harmonics due to dead band.

(iii) PARALLEL INVERTER:-

* An inverter in which the commutating component is parallel to the load is called as a parallel inverter.

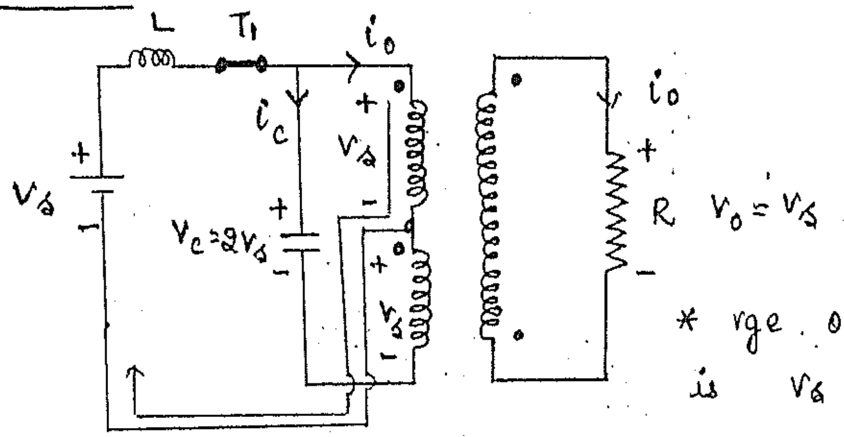


* It uses two SCRs T_1, T_2.
* C is the commutating component.
* Function of inductor L is to make the source current constant.

* Assumed +ve direction for vge and current is shown in figure.

* Transformation ratio from each primary half to secondary winding is assumed to be unity.

Mode 1:-

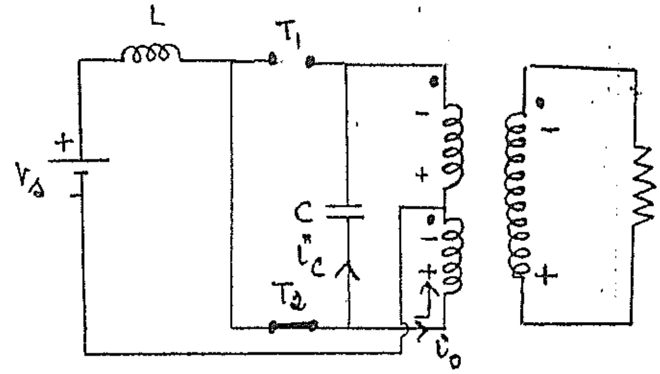


At t=0
* SCR T_1 is ON
* current flows in upper half of primary.
* vge on upper half of py is V_s.

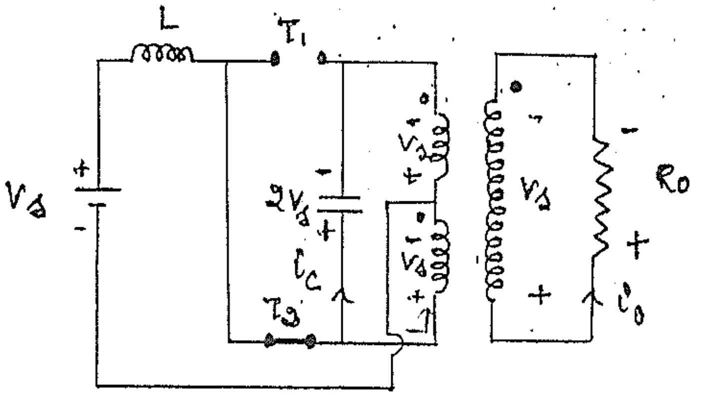
* ∴ the magnetic flux links the lower half of py wdg also the vge in the lower half is also V_s.

* ∴ voltage across primary = $2V_s$
* This vge charges the capacitor with upper plate +ve to a vge $V_c = +2V_s$. This vge V_c forward biases SCR T_2

Mode 2:-

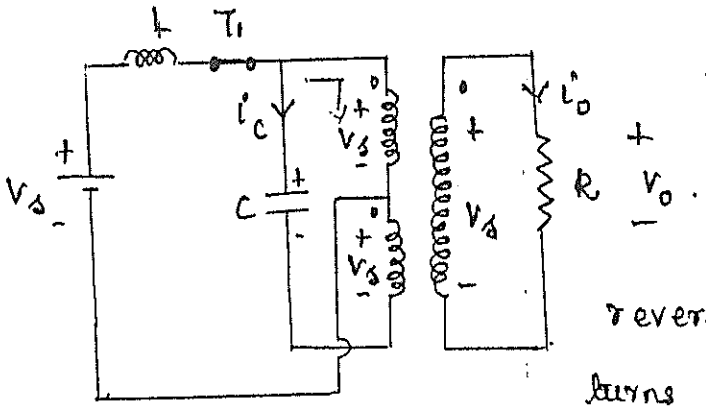


* At $t = t_1$, SCR T_2 is turned ON.
* At this time the capacitor voltage $2V_s$ applies a reverse bias across SCR T_1 and turns it OFF.
* When T_2 is ON current i_0 flows in lower half of primary. Vge in primary lower half is $-V_s$. Due to flux linking an equal vge $-V_s$ is induced in upper half of primary.
* Vge in secondary is also $= -V_s$.
* Now the current through capacitor is in the opposite direction.
* This current i_c charges the capacitor with lower plate +ve and upper plate -ve.



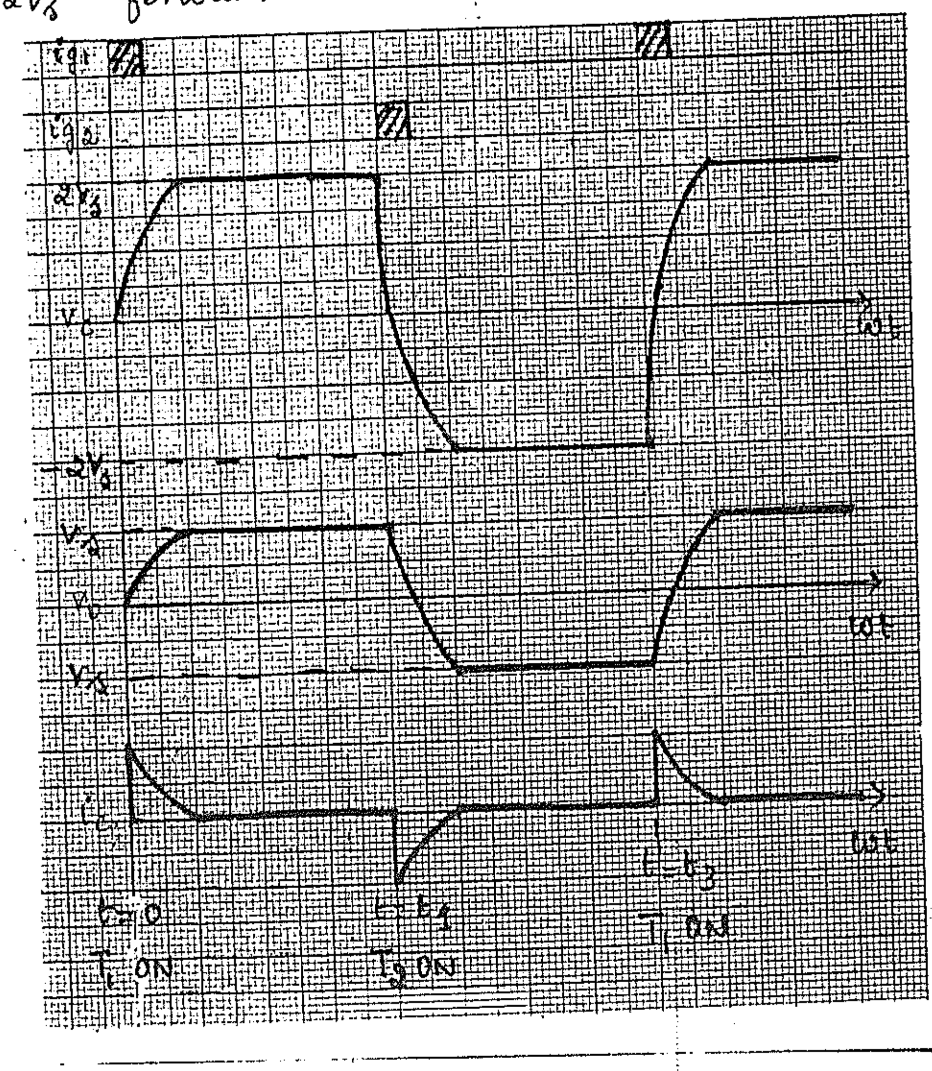
* At $t = t_2$ $V_c = -2V_s$.
* This vge V_c forward biases the SCR T_1

Mode 3 :-

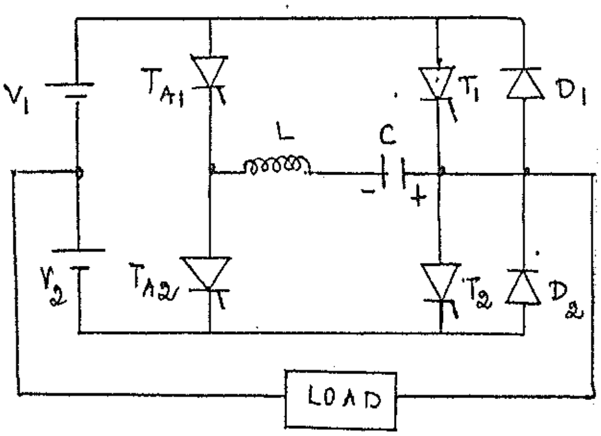


* If say at $t = t_3$ SCR T_1 is triggered the capacitor voltage $V_c = -2V_s$ reverse biases SCR T_2 and turns it OFF.

* Now capacitor current i_c is +ve.
* Vge V_s is induced in upper half and lower half of Py. Total vge in py = $2V_s$.
* current i_c charges capacitor with upper plate +ve to value $V_c = 2V_s$.
* $V_c = 2V_s$ forward biases SCR T_2. Again mode 2 will continue.



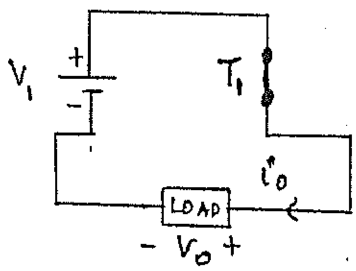
Mc-MURRAY INVERTER (Voltage source inverter):-



* T_1 and T_2 are main SCRs
* T_{A1}, T_{A2} are auxiliary SCRs to commutate the main SCRs.
* L and C are the commutating components.
* Capacitor is precharged with left side of plate -ve and right side +ve.
* Load current i_0 is constant.

Mode 1:-

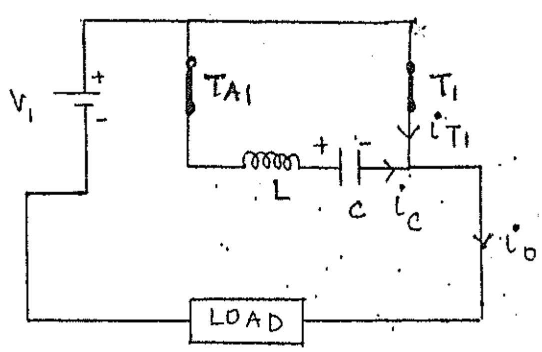
* SCR T_1 is ON at time $t=0$.



* Constant load current i_0 flows through load.

Mode 2:-

* At $t = t_1$ SCR T_A is ON.



* SCR TA_1, L, C, T_1 forms a ringing circuit.
* $i_0 = i_c + i_{T_1}$

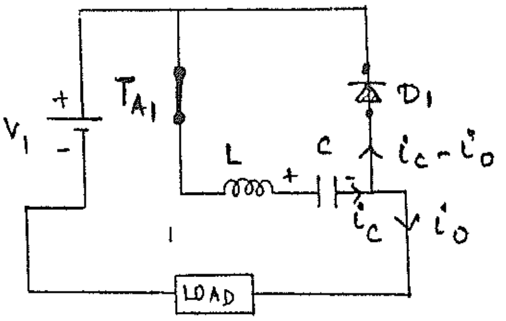
$i_{T_1} = i_0 - i_c$.

* Capacitor current i_c ↑es. At $t = t_2$ $i_c = i_0$.

when $i_c = i_0$; $i_{T_1} = i_0 - i_c = i_0 - i_0 = 0$., $\therefore i_{T_1} = 0$

* ∴ when current through SCR T_1 reduces to zero SCR T_1 is turned OFF
* ∴ at $t = t_2$ SCR T_1 is OFF.

Mode 3 :-



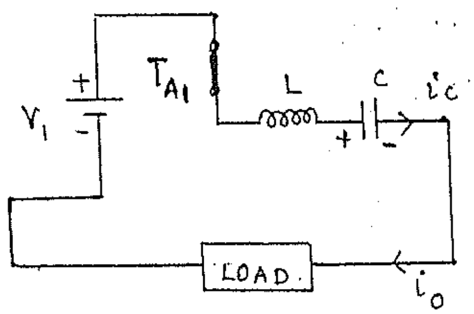
* After SCR T_1 is turned OFF, the capacitor current i_c increases further.
* ∵ i_0 is constant, the current $i_c - i_0 = i_{D_1}$ flows thro' diode D_1 and so diode D_1 is forward biased.

* Capacitor current increases and reaches a maximum value and then decreases.
* As i_c decreases, at time $t = t_3$ the current $i_c = i_0$. ∴ current thro' diode D_1 equals to zero

∵ $i_{D_1} = i_c - i_0 = i_0 - i_0 = 0$.

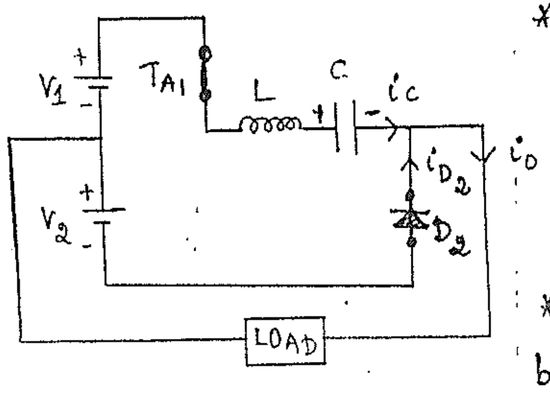
∴ at $t = t_3$ when $i_{D_1} = 0$ diode D_1 is turned OFF.

Mode 4 :-



* After D_1 is turned OFF, load current flows through capacitor.
* $i_0 = i_c$
* Now the capacitor is charged with the constant load current i_0.

Mode 5 :-



* Now due to constant load current i_0 the capacitor is slightly over charged. ie V_c is slightly greater than V_s. at $t = t_4$.
* ∴ the diode D_2 gets forward biased.

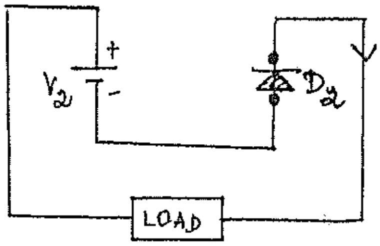
Now $i_0 = i_c + i_{D_2}$.

* The diode current increases while the capacitor current decreases.

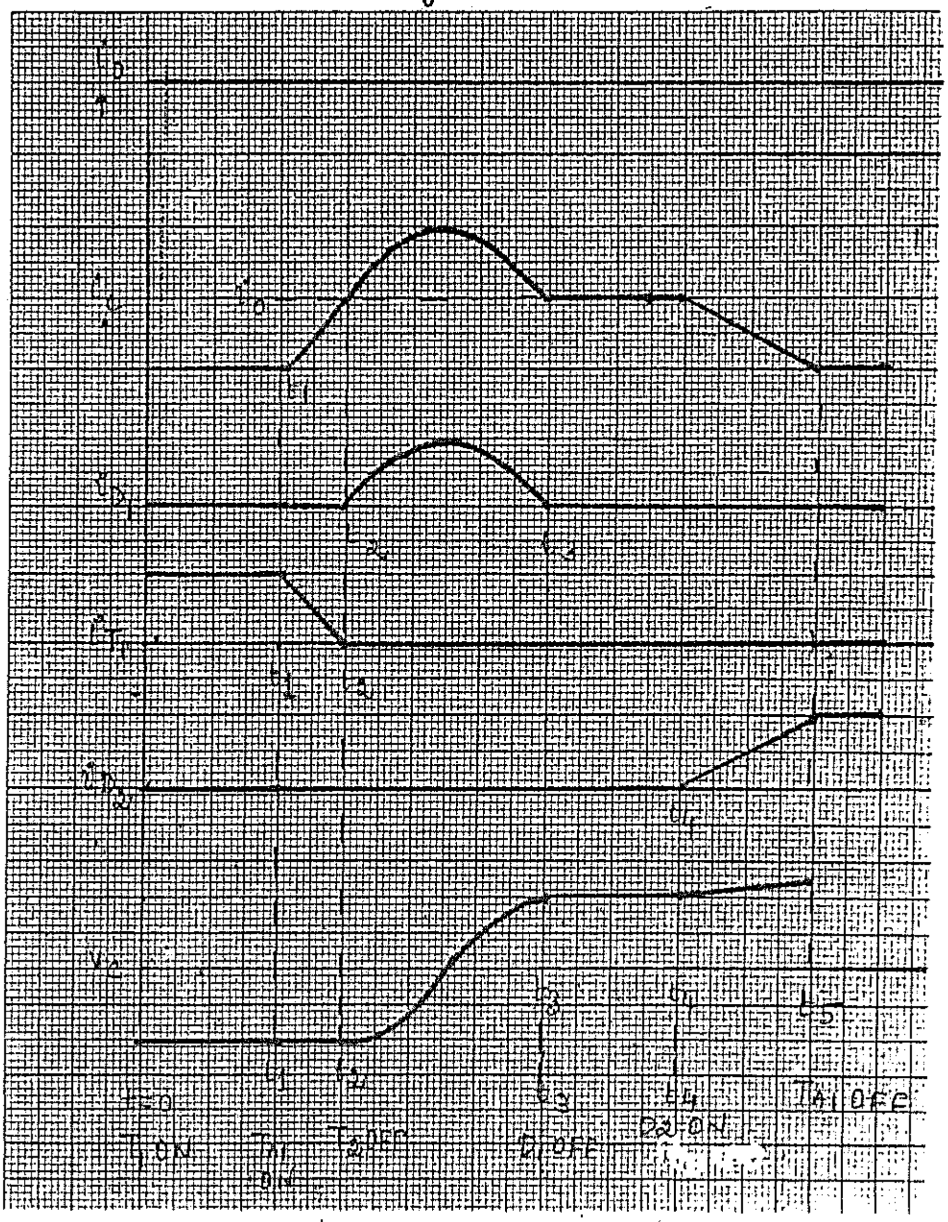
* At $t = t_5$ capacitor current $i_c = 0$, and diode current $i_{D_2} = i_0$. As $i_c = 0$, SCR T_{A1} is turned OFF.

∴ at $t = t_4$ SCR T_{A1} is turned OFF.

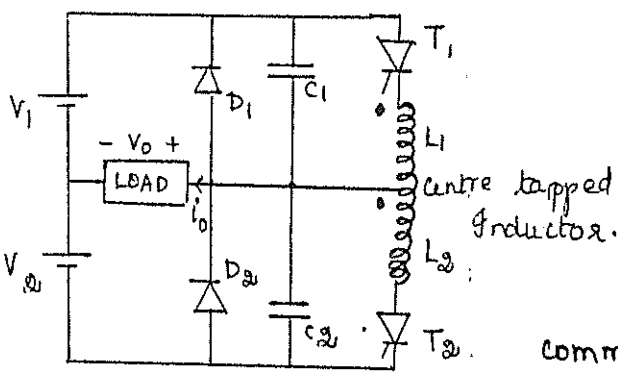
<u>Mode 6:-</u>



* D_2 conducts and $i_{D_2} = i_0$.
* After $i_{D_2} = 0$, diode D_2 turns OFF
* After which SCR T_2 is turned ON.
* similar cycles repeat.

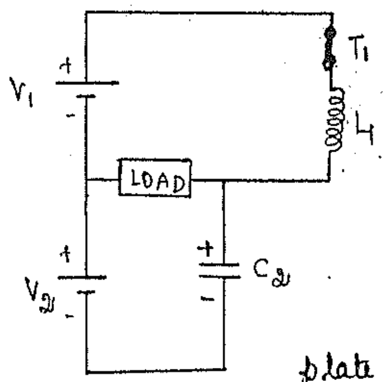


MC-MURRAY BEDFORD INVERTER:- (VSI)



* $L_1 = L_2 = L$ $(V_1 = V_2 = V)$
* $C_1 = C_2 = C$
* It has two SCRs T_1, T_2
* Turning ON of one SCR commutates the other. So this type is also called as complementary commutated inverter.

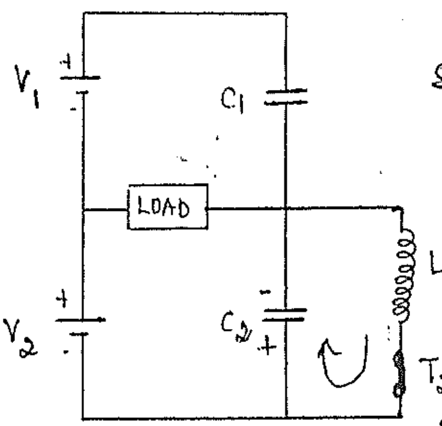
Mode 1:-



* SCR T_1 is ON at time $t=0$.
* constant current flows through T_1, L_1.
* Vge across $L_1 = 0$ $\left(V_{L_1} = L_1 \cdot \frac{di}{dt} = 0\right)$ since constant current flows through it
* capacitor C_2 charges with upper plate +ve and lower plate -ve to a voltage

$V_{C_2} = V_1 + V_2 = 2V$.

Mode 2:-



* SCR T_2 is turned ON to commutate SCR T_1
* when T_2 is ON, the vge across C_2 $(V_{C_2} = 2V)$ appears across L_2.
* ∴ Vge across $L_2 = 2V$
* By transformer principle an equal value of vge is induced in L_1

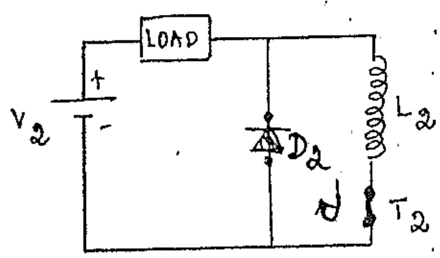
∴ Vge across $L_1 = 2V$.

* Now the anode of SCR T_1 is at 2V and the cathode is at 4V. Since the cathode vge is greater than anode vge SCR T_1 is reverse biased and is turned OFF.

* Now the current is transferred from T_1 to T_2.

* This current flows through capacitor C_2 in the opposite direction and charges it with lower plate +ve and upper plate −ve.

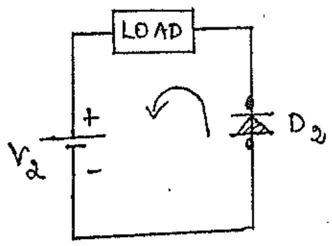
Mode 3 :-



* when capacitor is completely charged with lower plate +ve and upper plate −ve then diode D_2 is forward biased.
* Since D_2 is ON; C_2 is shorted by D_2.

* Energy stored in L_2 dissipates through T_2 and D_2.
* when all energy is dissipated (i.e.. when current is zero) SCR T_2 is turned OFF.

Mode 4 :-



* Now due to energy stored in load the diode D_2 is forward biased.
* Current flows from load to source.
* D_2 conducts till all energy stored in the load is dissipated.

* T_2 is again triggered for the −ve cycle.

VOLTAGE CONTROL IN SINGLE PHASE INVERTERS:-

* AC loads may require a constant or variable voltage at their input terminals.

* when the load is fed by inverters, they should be controlled to fulfill the requirements of the load. The requirements are

* AC load may require a constant voltage. ∴ the dc input vge must be adjusted in order to get the constant ac output. (or it may require a variable vge)

* Various methods for control of output voltage of inverters are

(a) External control of ac output voltage.

(b) External control of dc input voltage

(c) Internal control of inverter.

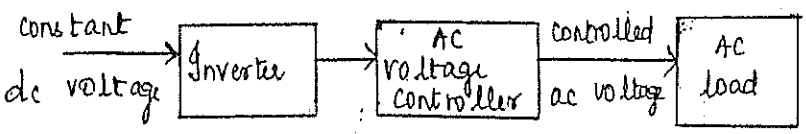
(a) EXTERNAL CONTROL OF AC OUTPUT VOLTAGE:-

This is done by two methods

(i) AC voltage control

(ii) Series - Inverter control.

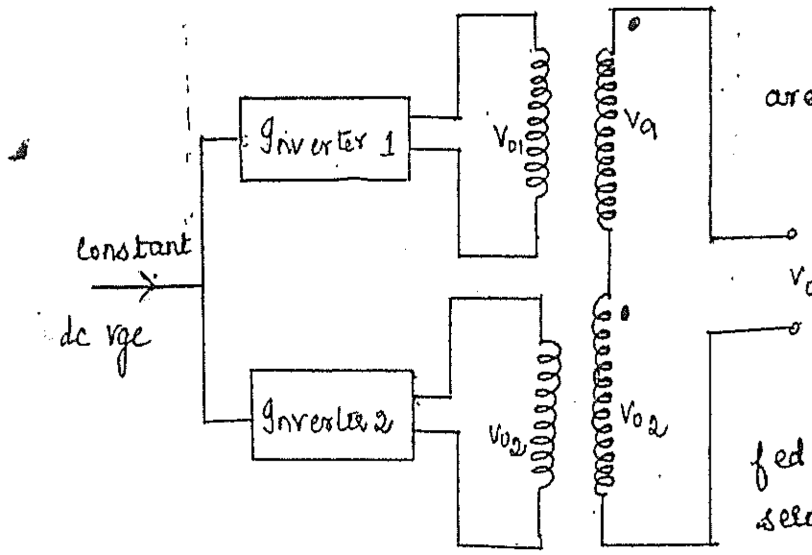
(i) AC VOLTAGE CONTROL:-



* Here an ac vge controller is inserted between the inverter and the load.

* Output of inverter is given to ac vge controller, and converted to a variable ac vge and given to load.

(ii) SERIES INVERTER CONTROL:-



* Here, two or more inverters are connected in series.

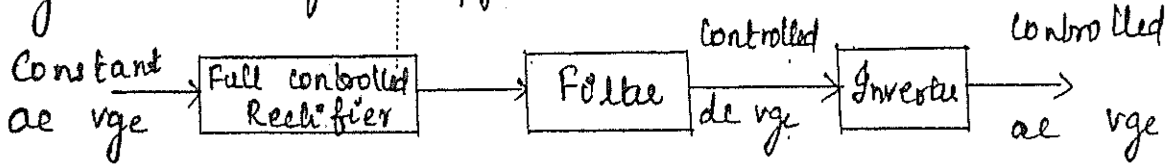
* Output of the inverter is fed to two transformers whose secondaries are connected in series.

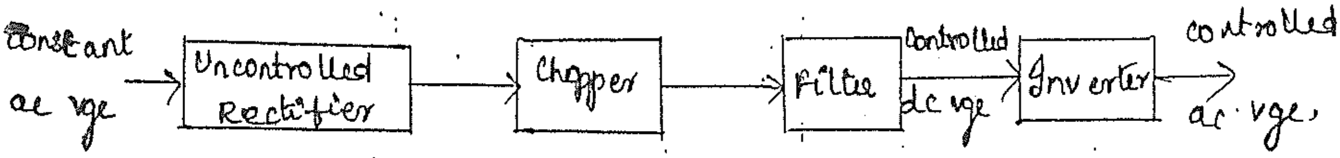
* output voltage of two inverters is summed up with the help of transformer to get variable ac voltage.

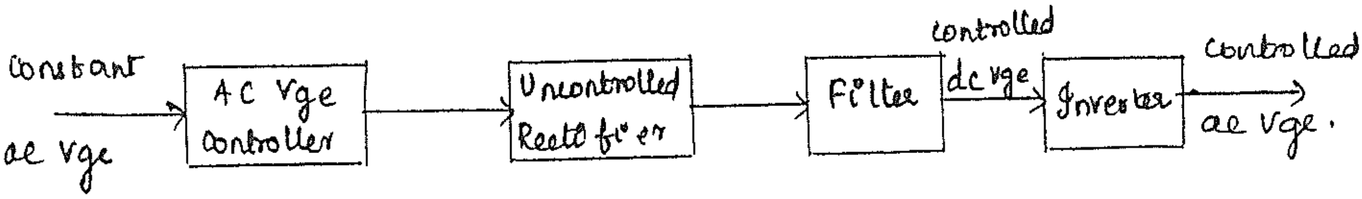
b) EXTERNAL CONTROL OF DC INPUT VOLTAGE:-

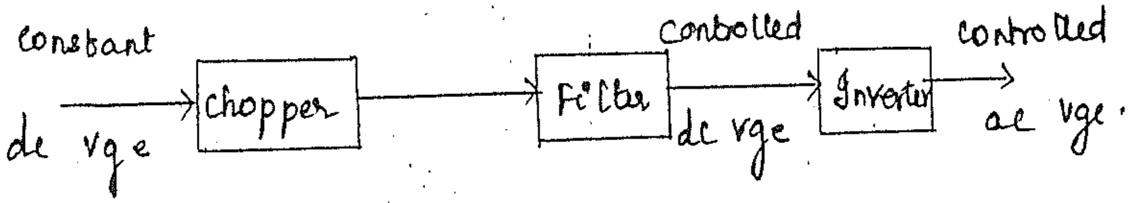
* In this method, if the available voltage is ac then the dc i/p to the inverter is controlled through a
  * fully controlled rectifier (or)
  * an Uncontrolled rectifier and chopper (or)
  * an ac vge controller and an Uncontrolled rectifier

* If the available vge is dc then it is controlled by means of chopper.









(c) INTERNAL CONTROL OF INVERTER:-

* Output voltage from an inverter can also be adjusted by doing a control inside the inverter itself.
* The most commonly used method is Pulse width modulation (PWM).

PWM control:-

* Here the output vge is controlled by adjusting the ON/OFF periods of the switches in the inverter.

Advantages:-

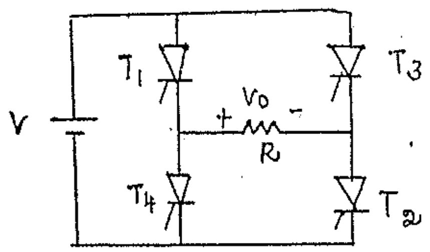
* o/p vge is controlled without any additional components.
* Lower order harmonics are eliminated.

PWM INVERTERS :

Various PWM techniques are

(i) Single pulse modulation.
(ii) Multiple pulse modulation.
(iii) Sinusoidal pulse modulation.
(iv) Modified sinusoidal PWM.

(i) single PWM.

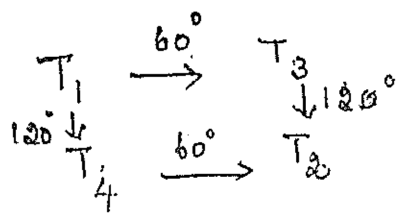


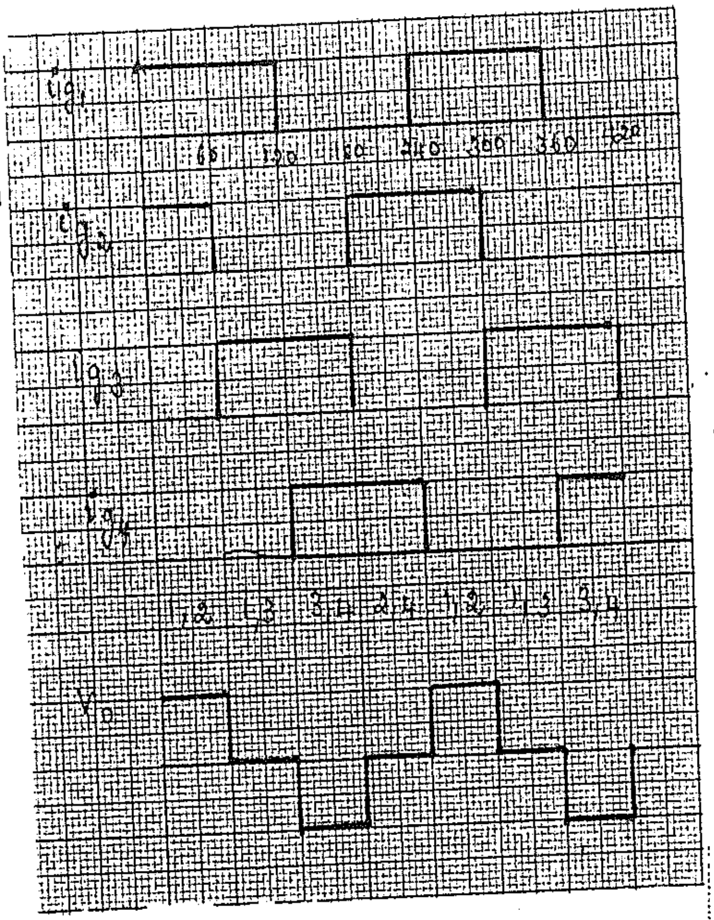
* T_1, T_3 are SCRs of +ve group.
* T_2, T_4 are SCRs of -ve group.
* Every SCR conducts for 120°.

* SCRs of same group conduct with a delay of 60°
  ie T_3 conducts 60° after T_1 and
  T_2 conducts 60° after T_4.

* SCRs from different groups conduct with delay of 120°.
  ie T_4 conducts 120° after T_1
  T_2 conducts 120° after T_3.

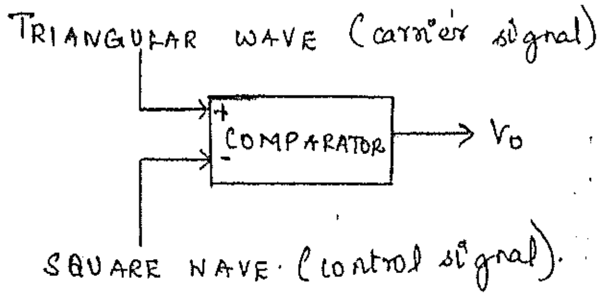
∴ T_1 is ON at $\omega t = 0$; T_3 is ON at $\omega t = 60°$
T_4 is ON at $\omega t = 120°$, T_2 is ON at $\omega t = 180°$





* Based on the firing pulses available across the SCRs, it is found which SCR conducts.
* for ex, during first 60° T_1, T_2 conduct. Then V_0 is +ve.
* when $T_1 T_3$ conduct the load is shorted ∴ $V_0 = 0$.
* when $T_3 T_4$ conduct V_0 is -ve.

(ii) MULTIPLE PWM :-



Let

V_T = Triangular wave

V_c = Square wave

V_0 = Output

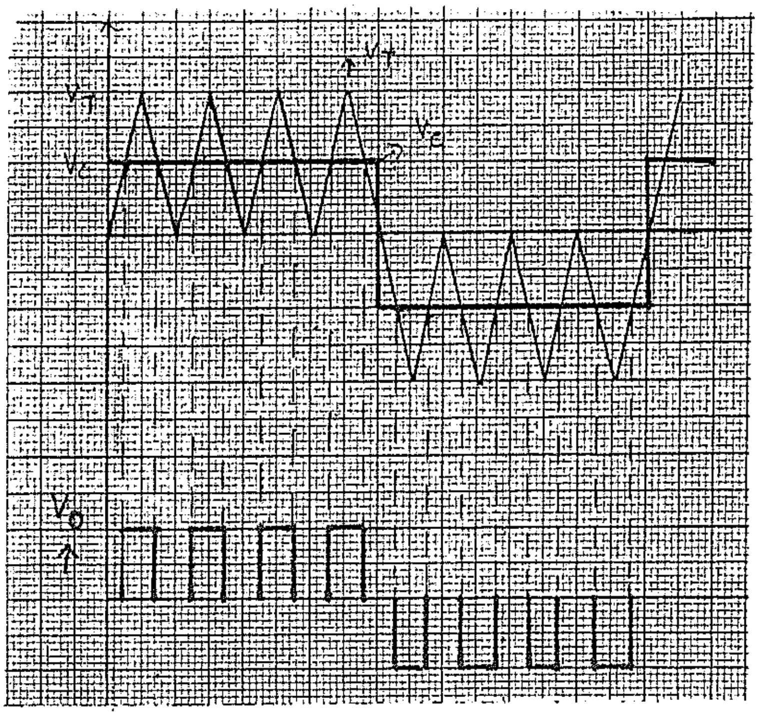
* A triangular (V_T) signal is compared with a Square wave form (V_c).

* Output of the comparator is high when V_T is > V_c. ∴ an o/p pulse is produced.

* Output of comparator is low when $V_T < V_c$. ∴ no o/p pulse.

∴ The output of comparator has a train of pulses

∴ Multiple PWM has multiple pulses per cycle.



THREE PHASE BRIDGE INVERTER:- (3ϕ VSI)

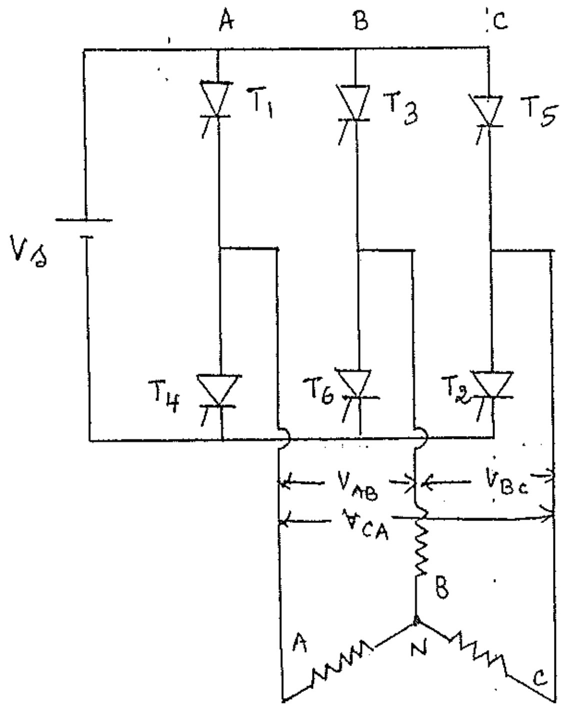
* 3ϕ inverter is a 6 step bridge inverter.
* It has 6 SCRs.
* A step is defined as a change in firing from one SCR to the next SCR in proper sequence.
* 3ϕ inverter generates a 3ϕ output.
* For one 360° cycle, 6 SCRs conduct.

∴ $\frac{360}{6} = 60°$. ∴ every SCR is triggered with a delay of 60°.

There are two types of VSI

* 180° conduction
* 120° conduction.

(i) 180° conduction mode 3ϕ VSI :-



* A 3ϕ inverter has 6 SCRs.

$T_1, T_3, T_5 \Rightarrow$ +ve group SCRs

$T_4, T_6, T_2 \Rightarrow$ −ve group SCRs.

* A 3ϕ star connected load is used.
* Let A, B, C be the 3 phases.

$T_1 T_4$ are connected in A

$T_3 T_6$ are connected in B

$T_5 T_2$ are connected in C

∴

A	B	C
T_1	T_3	T_5
T_4	T_6	T_2

* In 180° conduction mode every SCR conducts for an interval of 180°.

* Every SCR is triggered with a delay of 60°

∴ $\frac{180}{60} = 3$; ∴ during every instant 3 SCRs conduct.

* SCRs are triggered in the sequence T_1, T_2, T_3, T_4, T_5 and T_6 with a delay of 60° between each.

i.e., $T_1 \xrightarrow{60^\circ} T_2 \xrightarrow{60^\circ} T_3 \xrightarrow{60^\circ} T_4 \xrightarrow{60^\circ} T_5 \xrightarrow{60^\circ} T_6$

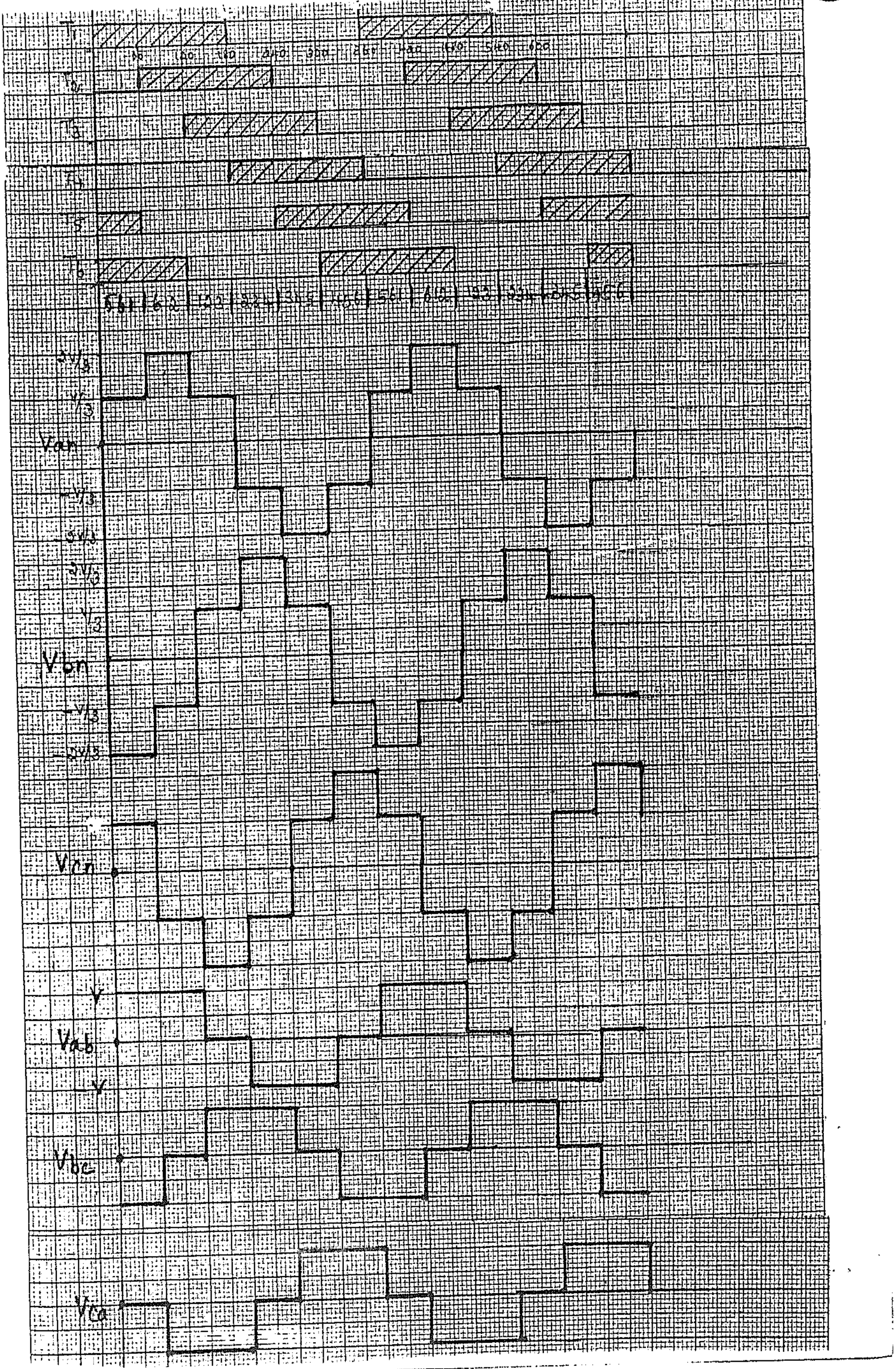
If T_1 is ON at $\omega t = 0$;
then T_2 is ON at $\omega t = 60$
T_3 is ON at $\omega t = 120$
T_4 is ON at $\omega t = 180$
T_5 is ON at $\omega t = 240$
T_6 is ON at $\omega t = 300$

After being turned ON each SCR will conduct for 180° and it will be OFF for another 180°

The triggering sequence is as follows (from graph)

561, 612, 123, 234, 345, 456, 561 - - - -

During every instant Two SCRs from +ve group and One SCR from −ve group conduct. (OR) Vice Versa.


T1
T2
T3
T4
T5
T6
2V/3
V/3
Van
-V/3
-2V/3
2V/3
V/3
Vbn
-V/3
-2V/3
Vcn
V
Vab
V
Vbc
Vca

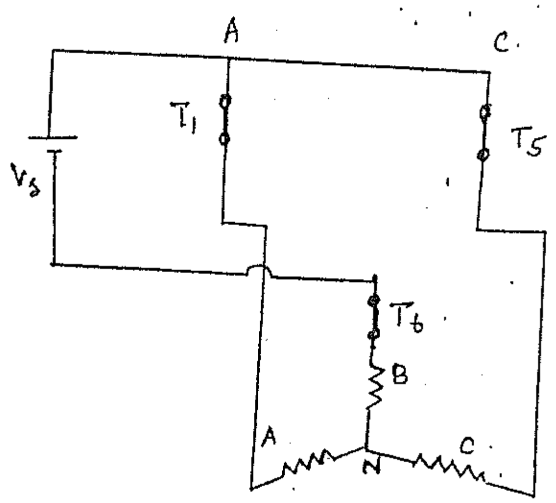
* For the first sequence 5 6 1.

SCRs T_5, T_6, T_1 conduct.

T_1 T_5 are SCRs from +ve group

T_6 is SCR from −ve group.

Now the equivalent circuit is



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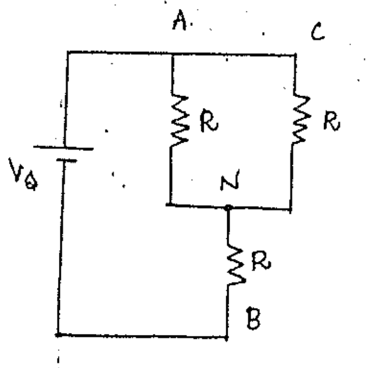
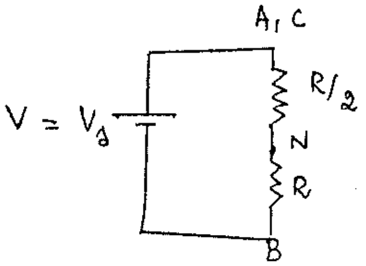


R_{AN} and R_{CN} are in parallel. $\therefore R_{eq} = \frac{R * R}{R + R} = \frac{R^2}{2R} = \frac{R}{2}$



$V_{AN} = V_{CN}$

let $V_s = V$

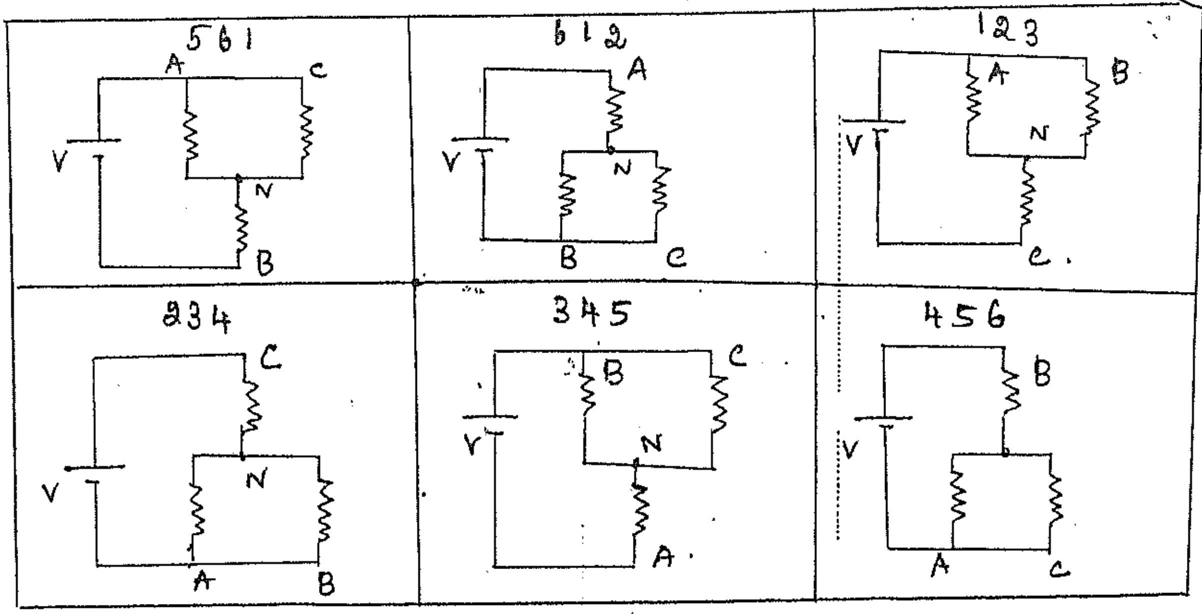
By vge division technique

$$V_{AN} = V_{CN} = \frac{V * R/_2}{R + R/_2} = \frac{V}{3}$$

$$V_{BN} = \frac{V * R}{R + R/_2} = \frac{2}{3} V$$

From this if 2 SCRs of same group conduct their load resistance is in parallel and $V_{ge} = V/_3$ (+ve if +ve group SCR conduct, −ve if −ve " " ")

For the single SCR from other group the load will be in series with other phase loads resistance and $V_g = 2V/_3$
(+ve if +ve group SCR conduct, −ve " −ve " " ")



conducting SCRs	V_{AN}	V_{BN}	V_{CN}	V_{AB}	V_{BC}	V_{CA}
5 6 1	$V/3$	$-\frac{2}{3}V$	$V/3$	V	$-V$	0
6 1 2	$\frac{2}{3}V$	$\frac{-V}{3}$	$-V/3$	V	0	$-V$
1 2 3	$V/3$	$V/3$	$-2V/3$	0	V	$-V$
2 3 4	$-V/3$	$2V/3$	$-V/3$	$-V$	V	0
3 4 5	$-2V/3$	$V/3$	$V/3$	$-V$	0	V
4 5 6	$-V/3$	$-V/3$	$2V/3$	0	$-V$	V

$$V_{AB} = V_{AN} - V_{BN}$$

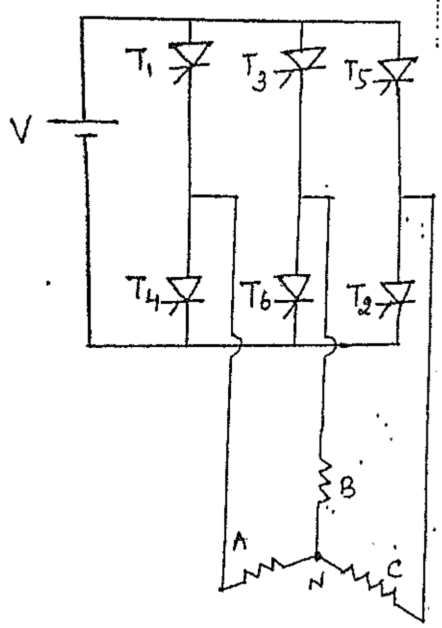
$$V_{BC} = V_{BN} - V_{CN}$$

$$V_{CA} = V_{CN} - V_{AN}$$

V_{AN}, V_{BN}, V_{CN} = Phase vge (stepped wave)

V_{AB}, V_{BC}, V_{CA} = Line vge (quasi square wave)

(ii) 120° conduction mode VSI :-



* It has 6 SCRs.
* T_1, T_3, T_5 → +ve group SCRs
* T_4, T_6, T_2 → -ve group SCRs
* A, B, C be the 3 phases.
* T_1 T_4 is connected in phase A
* T_3 T_6 " " " B
* T_5 T_2 " " " C

* In 120° conduction mode every SCR conducts for an interval of 120°
* Every SCR is triggered with a delay of 60°

∴ $\frac{120}{60} = 2$. ∴ during every instant 2 SCRs conduct.

* SCRs are triggered in sequence $T_1, T_2, T_3, T_4, T_5, T_6$ with a delay of 60° between each.

$T_1 \xrightarrow{60°} T_2 \xrightarrow{60°} T_3 \xrightarrow{60°} T_4 \xrightarrow{60°} T_5 \xrightarrow{60°} T_6$

T_1 is ON at $\omega t = 0$, T_2 is on at $\omega t = 60°$, T_3 is ON at $\omega t = 120°$
T_4 is ON at $\omega t = 180°$, T_5 is ON at $\omega t = 240°$, T_6 is ON at $\omega t = 300°$.

After being turned ON each SCR will conduct for 120° and will be OFF for another 240°.

* The triggering sequence is as follows.

61, 12, 23, 34, 45, 56, 61, 12 - - - -

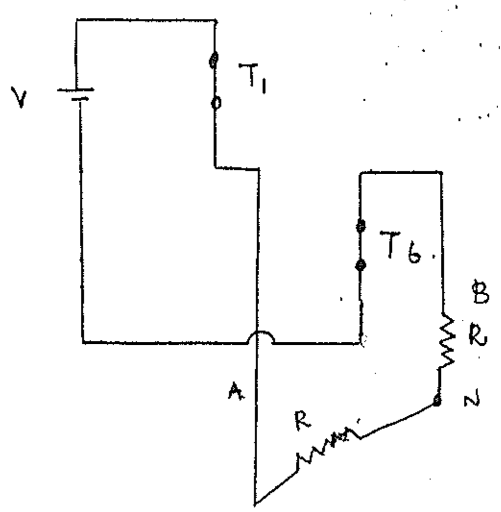
* During every instant one SCR from +ve group and one SCR from -ve group conduct.

* Now for the sequence 61, SCR T_6, T_1 conduct.

T_1 is +ve group SCR in phase A

T_6 is -ve group SCR in phase B.

Now the equivalent circuit is :-



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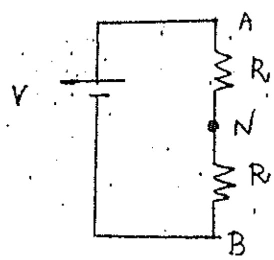


$V_{AN} = V_{BN} = V/2$

(∵ vge is equally divided)

$V_{CN} = 0$ ∵ SCR in C phase is not ON.

From this if SCR in +ve group conducts the vge is $= +V/2$

and if SCR of -ve group conduct the voltage is $= -\frac{V}{2}$.

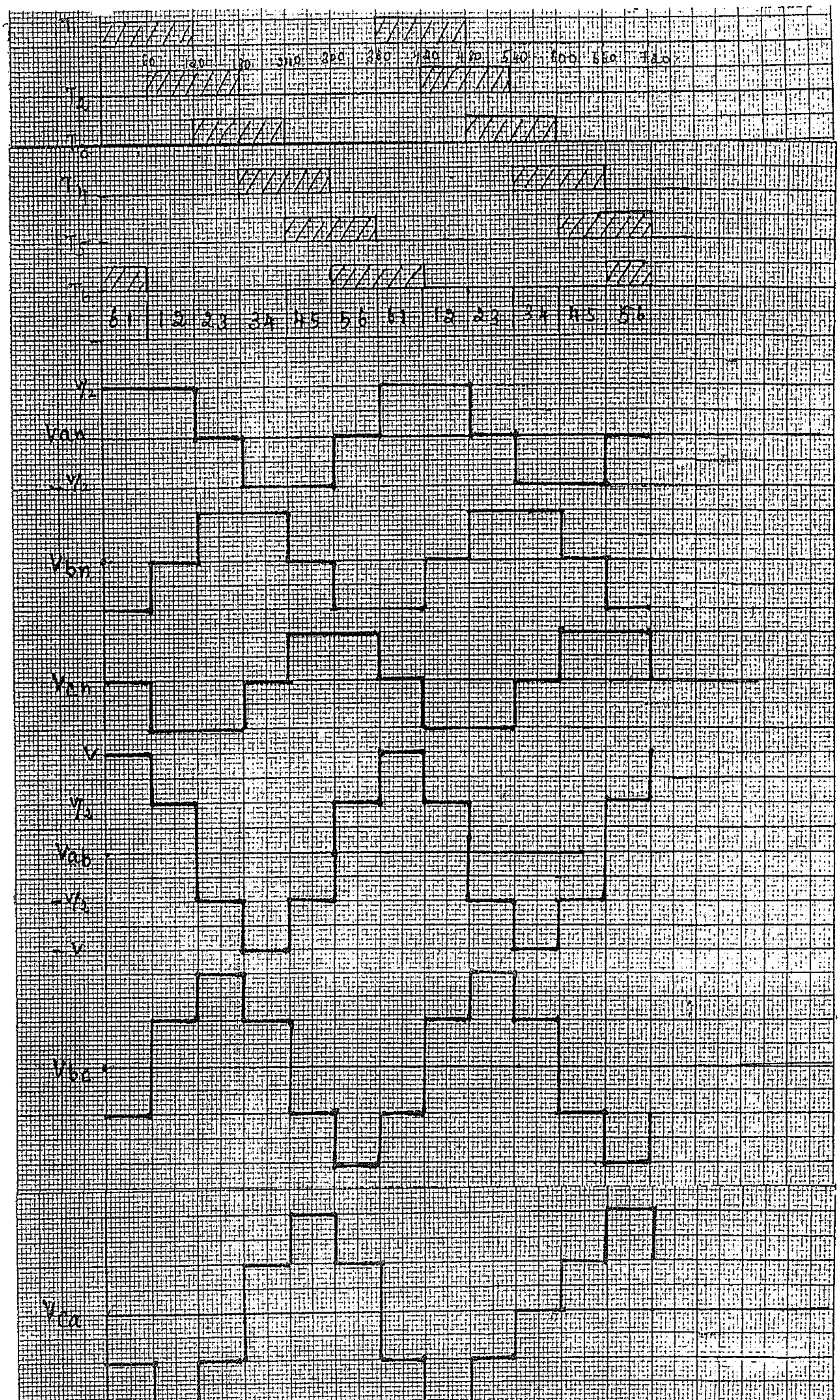
$V_{AB} = V_{AN} - V_{BN}$

$V_{BC} = V_{BN} - V_{CN}$

$V_{CA} = V_{CN} - V_{AN}$

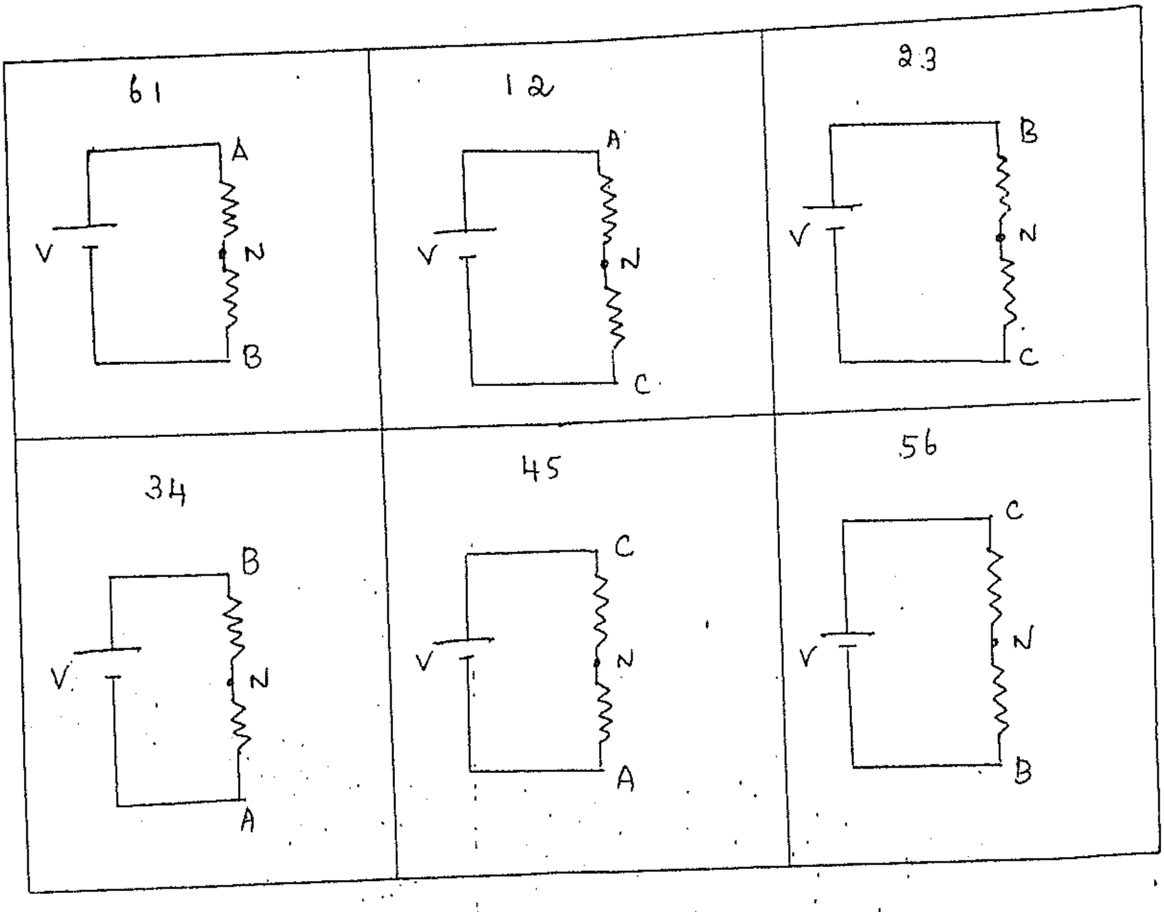
V_{AN}, V_{BN}, V_{CN} : Phase vge (quasi square wave)

V_{AB}, V_{BC}, V_{CA} : Line vge (stepped wave)



T1
60 120 180 240 300 360 420 480 540 600 660 720
T2
T3
T4
T5
T6
61 12 23 34 45 56 61 12 23 34 45 56
V/2
Van
-V/2
Vbn
Vcn
V
V/2
Vab
-V/2
-V
Vbc
Vca

Conducting SCRs	V_{AN}	V_{BN}	V_{CN}	V_{AB}	V_{BC}	V_{CA}
61	$V/2$	$-V/2$	0	V	$-V/2$	$-V/2$
12	$V/2$	0	$-V/2$	$V/2$	$V/2$	$-V$
23	0	$V/2$	$-V/2$	$-V/2$	V	$-V/2$
34	$-V/2$	$V/2$	0	$-V$	$V/2$	$V/2$
45	$-V/2$	0	$V/2$	$-V/2$	$-V/2$	V
56	0	$-V/2$	$V/2$	$V/2$	$-V$	$V/2$



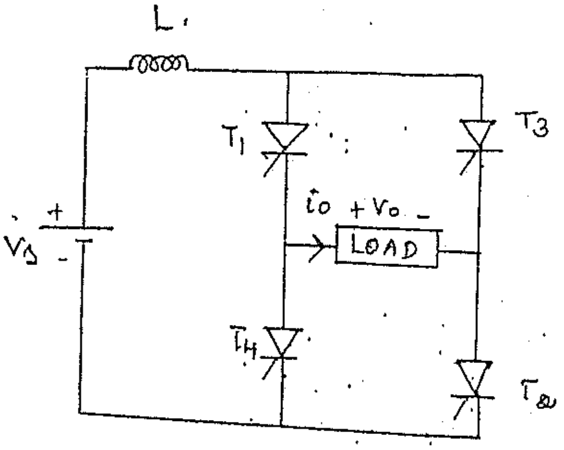
CURRENT SOURCE INVERTER:- (CSI)

* It is one in which the input voltage is maintained constant.

(i) 1ϕ current source inverter

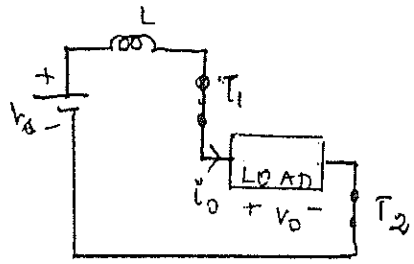
(ii) 3ϕ current source inverter.

(i) 1ϕ CSI :-



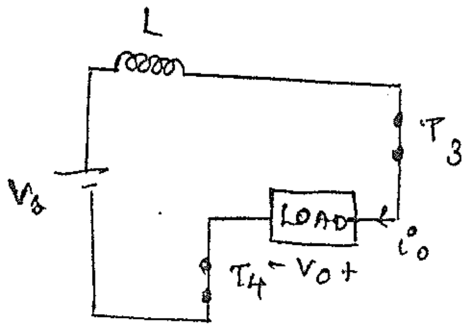
* Inductor L in series with the vge source, is to maintain the current constant.

* when $T_1 T_2$ ON:-



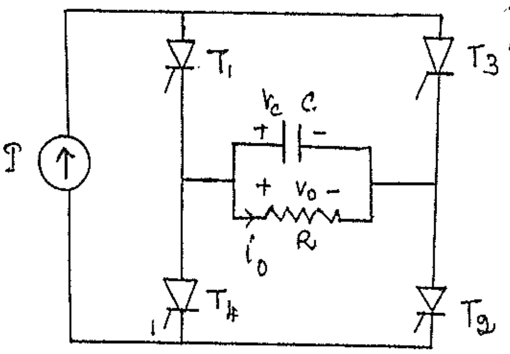
* V_o, i_o is +ve when T_1, T_2 is ON.

* when $T_3 T_4$ ON



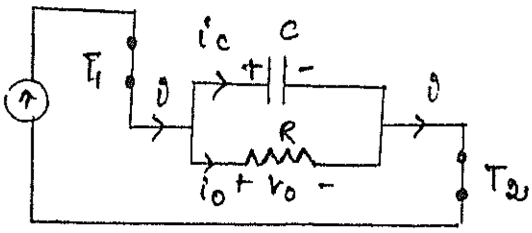
* V_o, i_o is -ve when T_3 T_4 is ON.

(ii) 1φ capacitor commutated CSI :- (with R load):-



* Capacitor is connected parallel to load
* It has 4 SCRs.

(i) T_1, T_2 ON :-



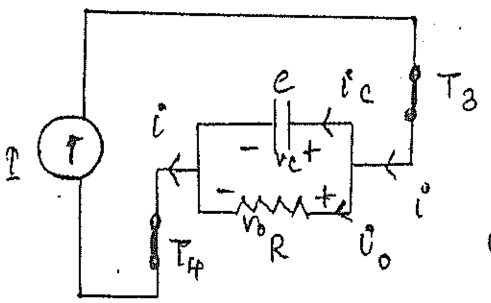
* T_1, T_2 are ON at time $t=0$.
* current i flows through SCR T_1, T_2
* current i_0 flows thro' load
* current i_c flows thro' 'c'

* ∵ R, C and in parallel $V_0 = V_c$.
* Capacitor C charges with left plate +ve and right side plate -ve to $V_c = V_s$, ∴ $V_0 = V_c = +V_s$.

* Now when at time $t = t_1$, SCR T_3, T_4 are turned ON then the vge across 'c' reverse biases T_1, T_2 and turns it OFF.

(ii) T_3, T_4 ON :-

* when T_3, T_4 is ON at $t = t_1$, current i flows thro' T_3 & T_4.

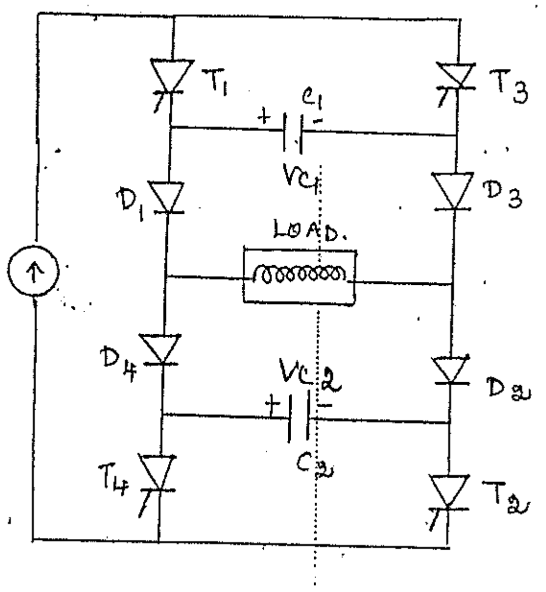


* i_c flows thro' c.
* i_0 flows thro' R
* i_c charges c with left plate -ve and right plate +ve. ∴ $V_c = -V_s$

$$V_0 = V_c = -V_s.$$

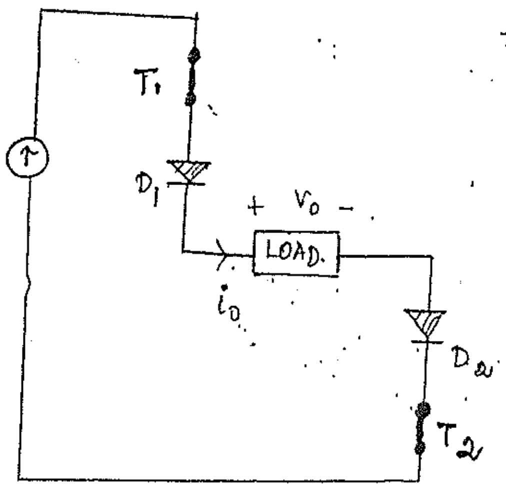
* Now at $t = t_2$ when T_1, T_2 are turned ON the capacitor vge reverse biases T_3, T_4 and turns them OFF.

(iii) 1φ Auto sequential commutated Inverter (1φ ASCI):



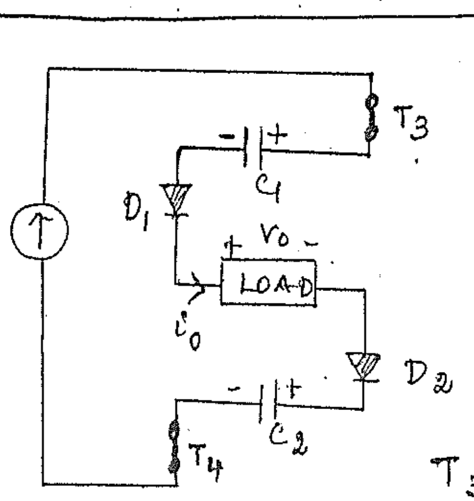
* capacitors are precharged with left plate +ve.

(i) when T_1 and T_2 are ON:-



* when SCR T_1, T_2 are turned ON.
* Load current flows through $T_1 - D_1 -$ load $- D_2 - T_2$
* V_0, i_0 is +ve.

(ii) when T_3 & T_4 are ON:-



* when T_3 & T_4 are ON, the capacitor Voltage V_{C1} and V_{C2} apply a reverse bias across SCR T_1 & T_2 respectively and turns them OFF.
* Now load curnt flows through $T_3 - C_1 - D_1 -$ load $- D_2 - C_2 - T_4$

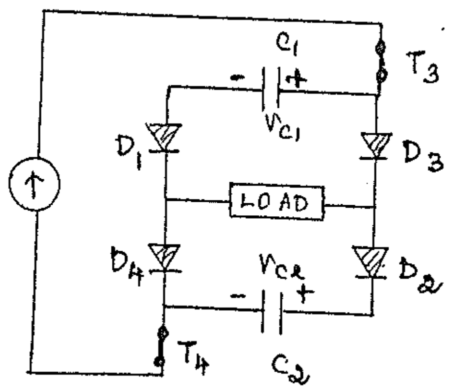
* Due to current flowing thro' C_1 and C_2 they are charged with right plate +ve and left plate −ve.

* This increasing polarity on the capacitors forward biases diodes D_3 and D_4.

* D_1 and D_2 are already ON.

Now all diode D_1, D_2, D_3 and D_4 are ON.

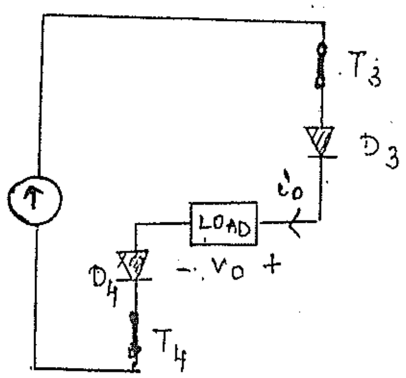
(iii) when D_1, D_2, D_3, D_4 ON:-



* Here all four diodes are ON.

* Now when the capacitors is completely charged with right side plate +ve the diodes D_1 and D_2 are reverse biased by V_{C1} and V_{C2} and they are turned OFF.

(iv) Diodes D_1, D_2 turned OFF:-

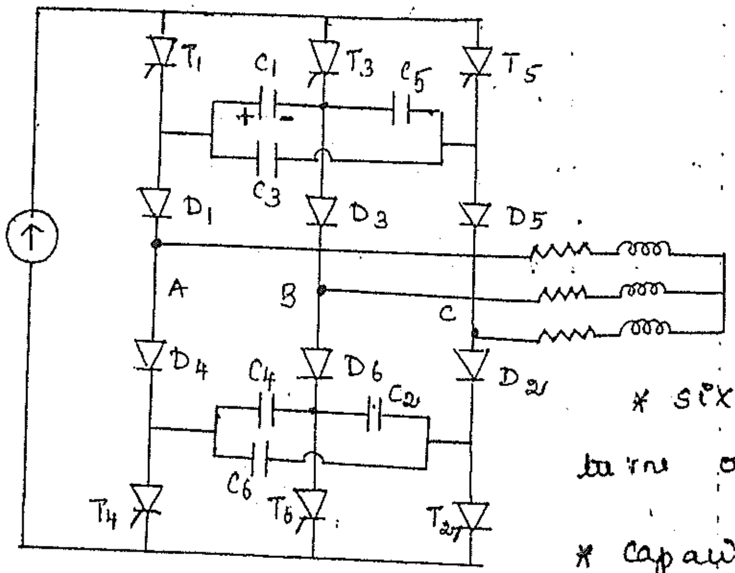


* Now when D_1, D_2 is OFF, the current i_0 flows through $T_3 \rightarrow D_3 \rightarrow$ load $\rightarrow D_4 \rightarrow T_4$

* Now V_0, i_0 is −ve.

* To turn OFF SCR T_3, T_4, SCR T_1, T_2 are turned ON.

3 ϕ CURRENT SOURCE INVERTERS:-



* It uses voltage commutation.

* Operates in 120° conduction mode.

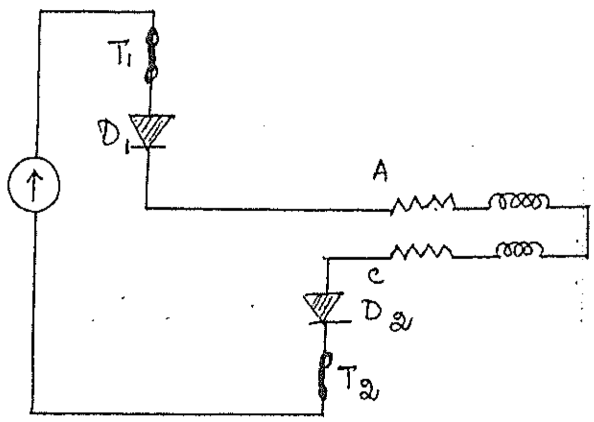
* six capacitors are used to turn of 6 SCRs.

* capacitor C_1 is charged with left side plate +ve and right plate -ve.

* SCRs are triggered in the sequence 12, 23, 34, 45, 56, 61, 12 and so on.

Let us consider the the change over from SCR 12 to 23.

(i) when T_1, T_2 is turned ON:- T_1 on at $\omega t = 0$
T_2 on at $\omega t = 60°$

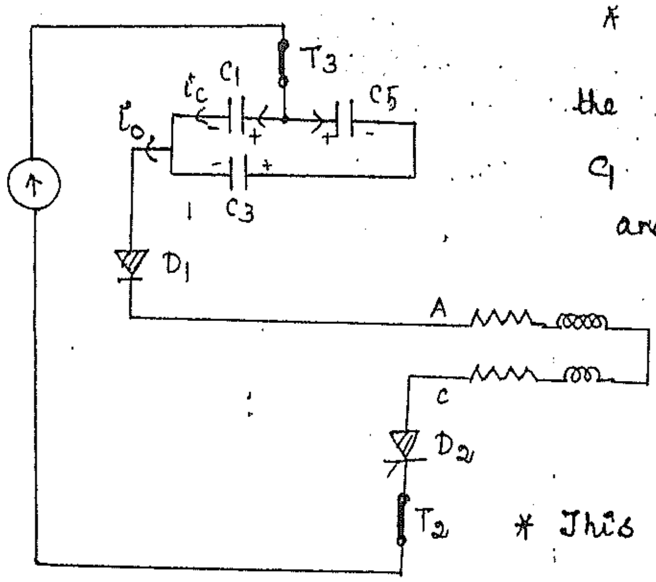


* Here T_1, T_2 are ON

* I_0 flows through
$T_1 - D_1 -$ load $- D_2 - T_2$

* After 60° SCR T_2, T_3 should conduct.

(ii) SCR T_3 is turned ON:-

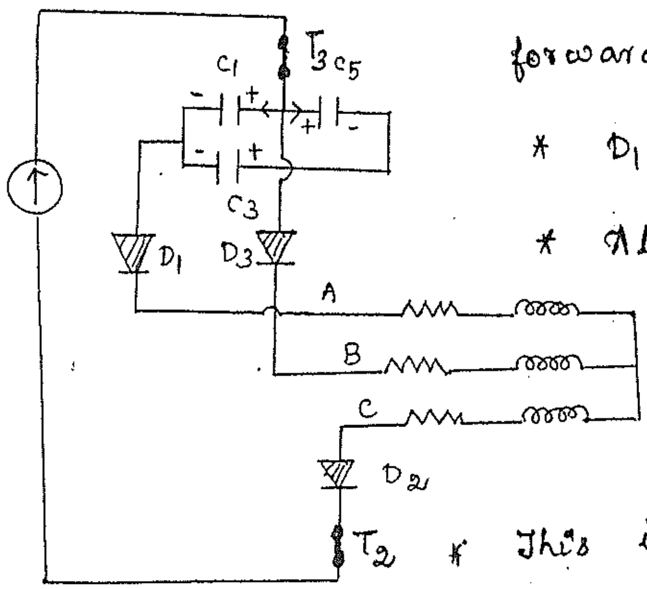


* When T_3 is turned ON, the Voltage across the capacitor C_1 reverse biases the SCR T_1 and turns it OFF.

* Now load cuut flows through $T_3 - C_1 - D_1 -$ load $- D_2 - T_2$.

* This current i_C flowing through capacitor C_1 charges it with left plate -ve and right plate +ve.

(iii) D_3 ON:-



* Increasing vge on capacitor forward biases diode D_3.

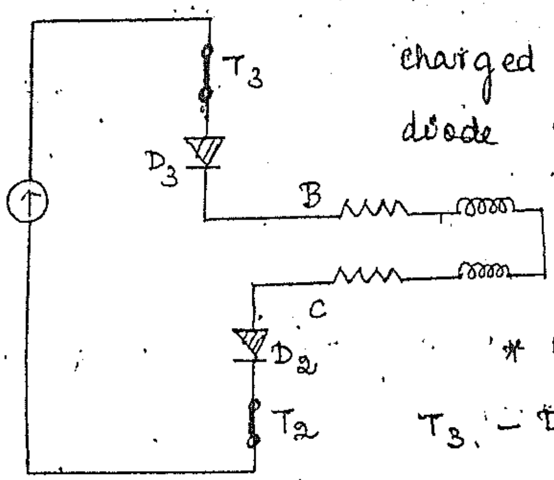
* D_1 and D_2 are already ON.

* All three diodes are ON.

* In this mode all three loads are energised.

* This is called the period of overlap.

(iv) Diode D_1 is OFF :-



* when capacitor is completely charged with left plate -ve, the diode D_1 is reverse biased and turns OFF.
* D_1 is OFF.
* Now load current flows through T_3 - D_3 - load - D_2 - T_2.

Similar modes follow for other sequences.

Difference between

vge source inverter	current source inverter.
1. Input vge is constant	Input current is constant.
2. current waveform depends on load	voltage waveform depends on load.
3. Short circuit can damage the circuit	Short circuit cannot damage the circuit.
4. Freewheeling diodes are required in case of inductive loads.	4. Freewheeling diodes are not required.

— x ——— x ——— x ———