SUBJECT: LINEAR IC's & APLLICATIONS

IA MARKS: 25 SUBJECT CODE: 10EC46

EXAM HOURS: 3 EXAM MARKS: 100

HOURS / WEEK: 4 TOTAL HOURS: 52

PART - A

UNIT 1:

Operational Amplifier Fundamentals: Basic Op-Amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations; Op-Amps as DC Amplifiers- Biasing Op-Amps, Direct coupled -Voltage Followers, Non-inverting Amplifiers, Inverting amplifiers, Summing amplifiers, Difference amplifier.

UNIT 2:

Op-Amps as AC Amplifiers: Capacitor coupled Voltage Follower, High input impedance - Capacitor coupled Voltage Follower, Capacitor coupled Non-inverting Amplifiers, High input impedance - Capacitor coupled Non-inverting Amplifiers, Capacitor coupled Inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled Difference amplifier, Use of a single polarity power supply.

UNIT 3:

Op-Amps frequency response and compensation: Circuit stability, Frequency and phase response, Frequency compensating methods, Band width, Slew rate effects, Z_{in}Mod compensation, and circuit stability precautions.

UNIT 4:

OP-AMP Applications: Voltage sources, current sources and current sinks, Current amplifiers, instrumentation amplifier, precision rectifiers, Limiting circuits.

PART – B

UNIT 5:

More applications: Clamping circuits, Peak detectors, sample and hold circuits, V to I and I to V converters, Log and antilog amplifiers, Multiplier and divider, Triangular / rectangular wave

generators, Wave form generator design, phase shift oscillator, Wein bridge oscillator.

UNIT 6:

Non-linear circuit applications: crossing detectors, inverting Schmitt trigger circuits, Monostable&Astablemultivibrator, Active Filters –First and second order Low pass & High pass filters.

UNIT 7:

Voltage Regulators: Introduction,Series Op-Amp regulator, IC Voltage regulators, 723 general purpose regulator, Switching regulator.

UNIT 8:

Other Linear IC applications: 555 timer - Basic timer circuit, 555 timer used as astable and monostablemultivibrator, Schmitt trigger; PLL-operating principles, Phase detector / comparator, VCO; D/A and A/ D converters – Basic DAC Techniques, AD converters.

TEXT BOOKS:

1. **"Operational Amplifiers and Linear IC's",** David A. Bell**,** 2nd edition, PHI/Pearson, 2004

2. **"Linear Integrated Circuits",** D. Roy Choudhury and Shail B. Jain**,** 2nd edition, Reprint 2006, New Age International

REFERENCE BOOKS:

1. **"Op - Amps and Linear Integrated Circuits",** Ramakant A. Gayakwad,4th edition, PHI,

2. **"Operational Amplifiers and Linear Integrated Circuits",** Robert. F. Coughlin &Fred.F. Driscoll**,** PHI/Pearson, 2006

3. **"Op - Amps and Linear Integrated Circuits",** James M. Fiore**,** Thomson Learning, 2001

4. **"Design with Operational Amplifiers and Analog Integrated Circuits",** Sergio Franco**,** TMH, 3e, 2005

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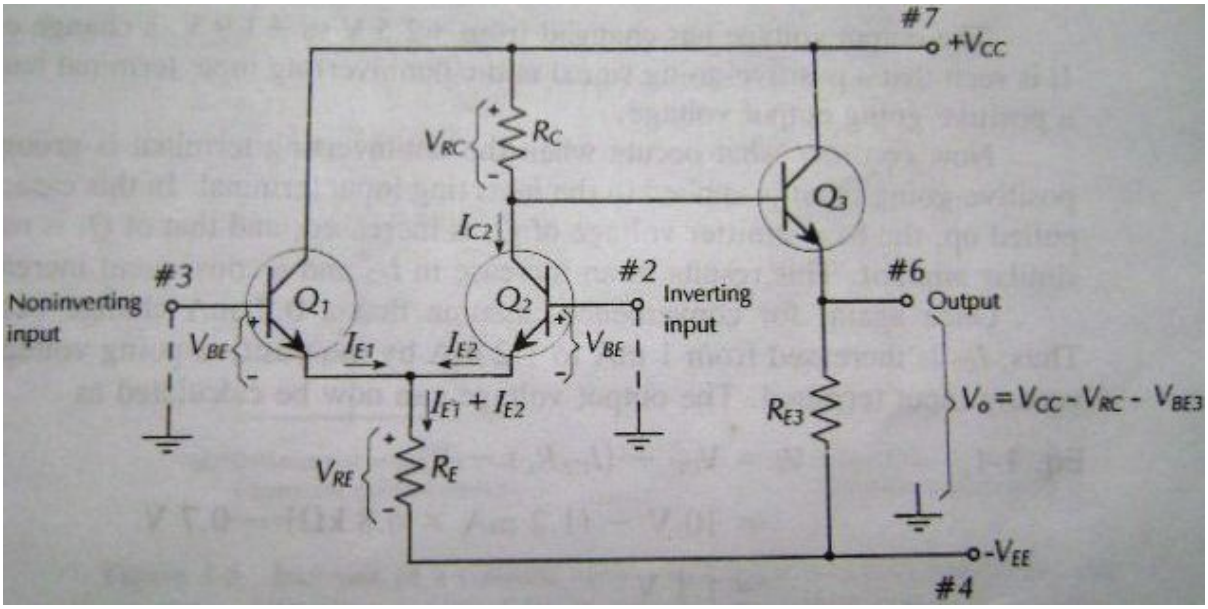
UNIT - 1

OPERATIONAL AMPLIFIER FUNDAMENTALS

1.1 Basic operational amplifier circuit-



The basic circuit of an operational amplifier is as shown in above fig. has a differential amplifier input stage and an emitter follower output. Supply voltages $+V_{cc}$ and $-V_{cc}$ are provided. Transistors Q_1 and Q_2 constitute a differential amplifier, which produces a voltage change as the collector of Q_2 where a difference input voltage is applied to the bases of Q_1 and Q_2. Transistor Q_2 operates as an emitter follower to provide low output impedance.

$$V_o = V_{cc} - V_{RC} - V_{BE3}$$

$$= V_{cc} - I_{C2}R_c - V_{BE}$$

Assume that Q_1 and Q_2 are matched transistors that are they have equal V_{BE} levels and equalcurrent gains.

With both transistor bases at ground level, the emitter currents are equal and both I_{E1} and I_{E2} flow through the common emitter resistor R_E.

The emitter current is given by:-

$$I_{E1} + I_{E2} = V_{RE}/R_E$$

With Q_1 and Q_2 bases grounded,

$$0 - V_{BE} - V_{RE} + V_{EE} = 0$$

$$V_{EE} - V_{BE} = V_{RE}$$

$$V_{RE} = V_{EE} - V_{BE}$$

$$I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E}$$

$V_{cc} = 10$ V, $V_{EE} = -10$ V, $R_E = 4.7$ K, $R_c = 6.8$ K, $V_{BE} = 0.7$,

$$I_{E1} + I_{E2} = (10 - 0.7)/4.7 \text{ K} + 2 \text{ mA}$$

$$I_{E1} = I_{E2} = 1\text{mA}$$

$$I_{c2} = I_{E2} = 1 \text{ mA}$$

$$V_o = 10 - 1\text{mA} \times 6.8 \text{ K} - 0.7$$

$$V_o = 2.5 \text{ V}$$

If a positive going voltage is applied to the non-inverting input terminal, Q_1 base is pulled up by the input voltage and its emitter terminal tends to follow the input signal. Since Q_1 and Q_2 emitters are connected together, the emitter of Q_2 is also pulled up by the positive going signal at the non-inverting input terminal. The base voltage of Q_2 is fixed at ground level, so the positive going movement at its emitter causes a reduction in its base-emitter voltage (V_{BE2}). The result of the reduction in V_{BE2} is that its emitter current is reduced and consequently its collector current is reduced.

Positive going input at the base of Q_1 reduces I_{c2} by 0.2 mA (from 1mA to 0.8mA)

VO = 10 – (0.8 mA x 6.8 KΩ) – 0.7 = 3.9 V

It is seen that a positive going signal at pin 3 has produced a positive going output voltage

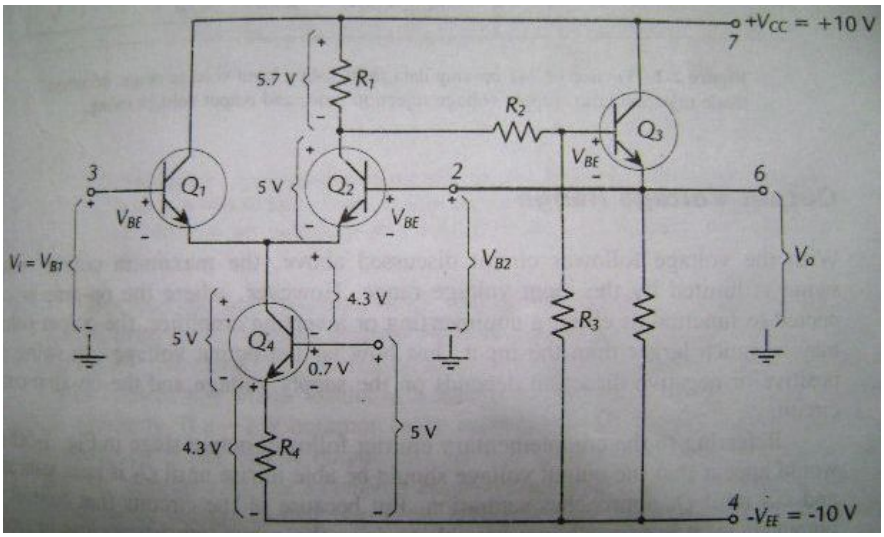
A basic operational amplifier circuit consists of a differential amplifier stage with two input terminals and a voltage follower output stage. The differential amplifier offers high impedance at both input terminals and it produces voltage gain. The output stage gives the op-amp low op output impedance. A practical op-amp circuit is much more complex than the basic circuit.

1.2 OPERATIONAL AMPLIFIER PARAMETERS

INPUT VOLTAGE RANGE

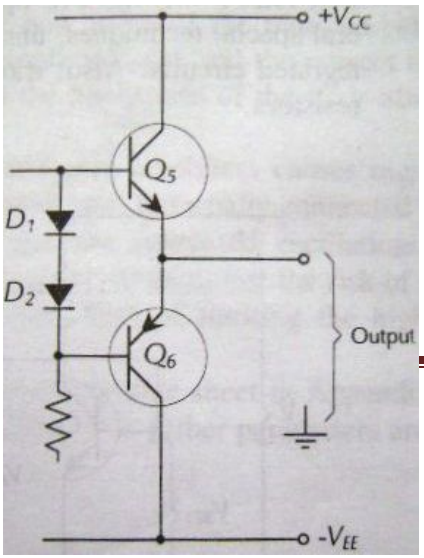
The circuit is designed to have a V_{CE} of 5V across Q2 and Q4. With a ±10 V supply and the bases of Q1 and Q2 at ground level, the voltage drops across R1 and R4 is 5.7 V and 4.3 V respectively. If the input voltage at Q1 base goes down to -4 V, the output terminal and Q2 base also goes down to -4 V as the output follows the input.

This means that the emitter terminals of Q1 and Q2 are pushed down from -0.7 to -4.7 V. Consequently, the collector of Q4 is pushed down by 4 V, reducing V_{CE4} from 5 V to 1 V. Although Q4 might still be operational with a V_{CE} of 1 V, it is close to saturation. It is seen that there is a limit to the negative going input voltage that can be applied to the op-amp if the circuit is to continue to function correctly.



There is also a limit to positive going input voltages. Where V_{B1} goes to +4 V, the voltage drop across resistor R1 must be reduced to something less than 1 V, in order to move V_{B2} and V_{E3} up by 4 V to follow the input. This requires a reduction in I_{c2} to a level that makes Q2 approach cutoff. The input voltage cannot be allowed to become large enough to drive Q2 into cutoff.

The maximum positive going and negative going input voltage that may be applied to an op-amp is termed as its input range.



OUTPUT VOLTAGE RANGE

The maximum voltage swing is limited by the input voltage range. The output voltage can swing in a positive or negative direction depends on the supply voltage and the op-amp output circuitry. Referring to the complementary emitter follower output stage in fig., it would appear that the

output voltage should be able to rise until Q5 is near saturation and fall until Q6 approaches saturation.

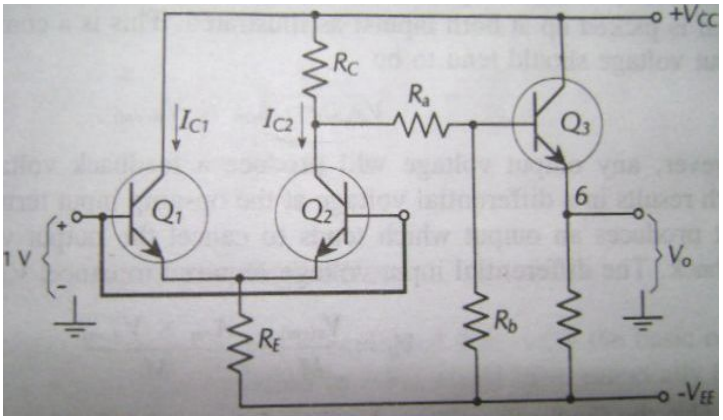
But because of the circuits that control the output stage, is normally not possible to drive the output transistors close to saturation levels.

A rough approximation for most op-amps is that the maximum output voltage swing is approximately equal to 1 V less than the supply voltage.

For the 741 op-amp with a supply of ±15 V, the data sheet lists the output voltage swing as typically ±14 V.

COMMON MODE AND SUPPLY REJECTION

Common mode rejection:-



When the same voltage is applied to both the input terminals of op-amp, the voltage is called 'Common Mode Voltage V_{in}', and the op-amp is said to be operating in the ' Common Mode Configuration '. Both input terminals are at the same potential, so ideally the output should be zero. Because the base voltages of Q_1 and Q_2 are biased to 1 V above ground, the voltage drop across emitter resistor R_E is increased by 1 V and consequently, I_{C1} and I_{C2} are increased. The increased level of I_{C2} produces an increased voltage drop across R_C , which results in a change in the output voltage at the emitter of Q_3.

The common mode gain is given by,

$$A_{cm} = \frac{V_{ocm}}{V_{icm}}$$

The success of the op-amp rejecting common mode inputs is defined in the common mode rejection ratio (CMRR). This is the ratio of the open loop gain A to the common mode gain A_{cm}.

$$CMRR = A/A_{cm}$$

It is expressed in decibel, CMRR = 20 log A/A_{cm}dB. The typical value of 741 is 90 dB.

Significance:

The CMRR expresses the ability of an op-amp to reject a common mode signal. Higher the value of CMRR, better is its ability to reject a common mode signal. Thus any unwanted signals such as noise or pick-

up would appear as common to both the input terminals and therefore the output due to this signal would be zero. Hence no undesirable noise signal will be amplified along with the desired signal.

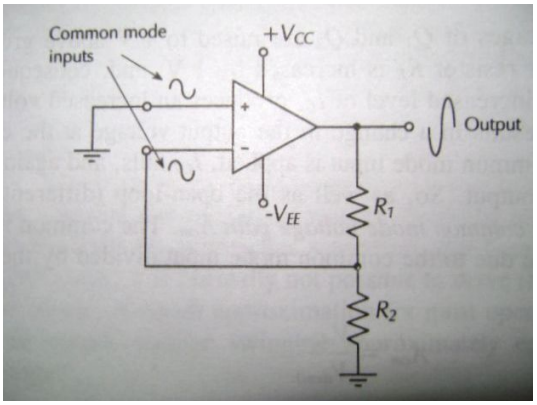
Consider the non-inverting amplifier circuit as shown below, with the input terminal grounded. The circuit output should also be at ground level. Now, suppose a sine wave signal is picked up at both inputs, this is a common mode input. The output voltage should tend to be,

$$V_{o\,cm} = A_{cm} \times V_{i\,cm}$$

Any output voltage will produce a feedback voltage across resistor R_i, which results in a differential voltage at the op-amp input terminals. The differential input produces an output which tends to cancel the output voltage that caused the feedback. The differential input voltage required to cancel $V_{o\,cm}$ is,

$$V_d = \frac{Vo\,cm}{A} = A_{cm} \times \frac{Acm \times Vi\,cm}{A}$$

V_d is the feedback voltage developed across R_1



$$V_{dc} = \frac{R1}{R1+Ri} \times V_{ocm}$$

$$\frac{R1}{R1+Rf} \times V_{o(cm)} = \frac{Acm \times Vi\,cm}{A}$$

$$V_{o(cm)} = \frac{Acm \times Vi\,cm}{A} \times \frac{R1}{R1+Ri}$$

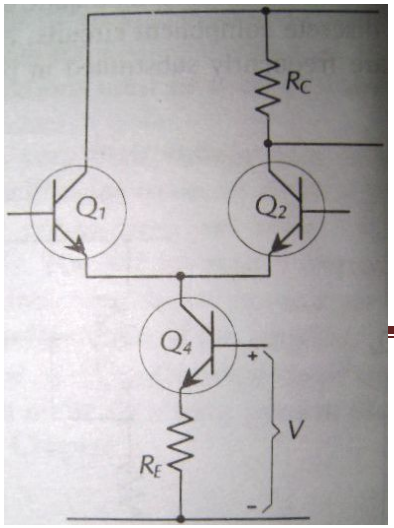
$$V_{o(cm)} = \frac{Vi\,cm}{CMRR} \times A_f$$

Problem

A 741 op-amp is used in a non-inverting amplifier with a voltage of 50. Calculate the typical output voltage that would result from a common mode input with a peak level of 100mV.

Solution

Typical value of CMRR for 741 op-amp = 90 dB.



$$CMRR = \text{antilog}\frac{90\,db}{20} = 31623$$

We have, $$V_{ocm} = \frac{Vi\,cm}{CMRR} \times A_f$$

$$= \frac{100\ mV}{CMRR} \times 50$$

Therefore, $V_{ocm} = 158\ \mu V$

POWER SUPPLY VOLTAGE REJECTION:

Any change in $-V_{EE}$ would produce a change in the voltage drop across R_E. This would result in an alteration in I_{E1}, I_{E2} and I_{C2}. The change in I_{C2} would alter V_{RC} and thus affect the level of the dc output voltage. The variation in $-V_{EE}$ would have an effect similar to an input voltage.

This can be minimized by replacing the emitter resistor with constant current circuit (or constant current tail) as shown in fig below.

A constant voltage drop is maintained across resistor R_E by providing a constant voltage V at Q_4 base. Now, any change in supply voltage is developed across the collector-emitter terminal of Q_4 and the emitter currents of Q_1 and Q_2 are not affected. Even with such circuitry, variations in V_{CC} and V_{EE} do produce some changes at the output. The Power Supply Rejection Ratio (PSRR) is a measure of how effective the op-amp is in dealing with variations in supply voltage.

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If a variation of 1V in V_{CC} or V_{EE} causes the output to change by 1V, then the supply voltage rejection ratio is 1V/V. If output changes by 10mV when one of the supply voltages changes by 1V, then SVRR is 10mV/V. In 741 op-amps it is 30 mV/V.

Problem

A 741 op-amp uses a ± 15 V supply with 2 mV, 120 Hz ripple voltage superimposed. Calculate the amplitude of the output voltage produced by the power supply ripple.

$$V_o(rip) = Vs\ (rip) \times PSRR$$

$$= 2mV \times 30\mu V/V$$

$$= 60\ nV$$

OFFSET VOLTAGE AND CURRENTS:

Input offset voltage

Basic operational circuit connected to function as a voltage follower as shown in fig 2. The output terminal and the inverting terminal follow the voltage at the non-inverting input.

For the output voltage to be exactly equal to the input voltage, transistors Q1 and Q2 must be perfectly matched. The output voltage can b e calculated as,

$$V_o = V_i - V_{BE} + V_{BE2}$$

With $V_{BE1} = V_{BE} \rightarrow V_o = V_i$

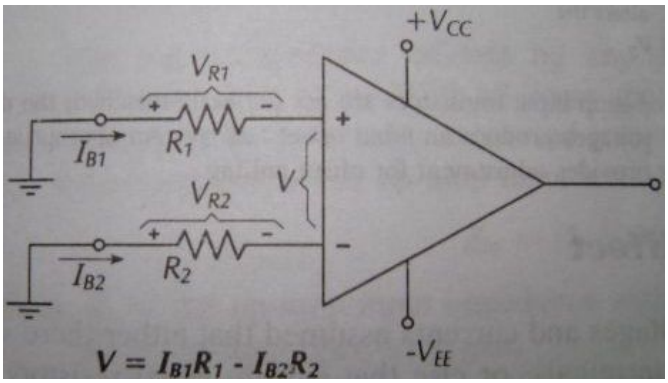
If the input voltage is zero then output voltage is also zero. i.e., $V_o = V_i$.

Suppose that the transistors are not perfectly matched and that V_{BE1} = 0,7 V while V_{BE2} = 0.6 V with the input at ground level,

$$V_o = 0 - 0.7V + 0.6V = -0.1V$$

This unwanted output is known as 'Output Offset Voltage'. To set V_o to ground level the input would have to be raised to + 0.1V (i.e. the input voltage applied to reduce the output offset voltage to zero) is known as 'Input Offset Voltage'. Although transistors in integrated circuits are very well matched, there is always some input offset voltage. The typical offset voltage is listed as 1 mV on 741 data sheet (max –5 mV).

Input Offset Current



If the input transistors of an op-amp not being perfectly matched, as well as the transistor base-emitter voltages being unequal, the current gain of one transistor may not be exactly equal to that of the other. Thus, when both transistors have equal levels of collector current, the base current may not be equal. So, the algebraic difference between these input currents (base currents) is referred as 'Input Offset Current (I_{OS}) '.

$$I_{OS} = | I_{B1} - I_{B2} |$$

I_{B1} = Current in the non-inverting input

I_{B2} = Current in the inverting input

This typical value for 741 op-amps is 20 nA (min) and the max is 200 nA.

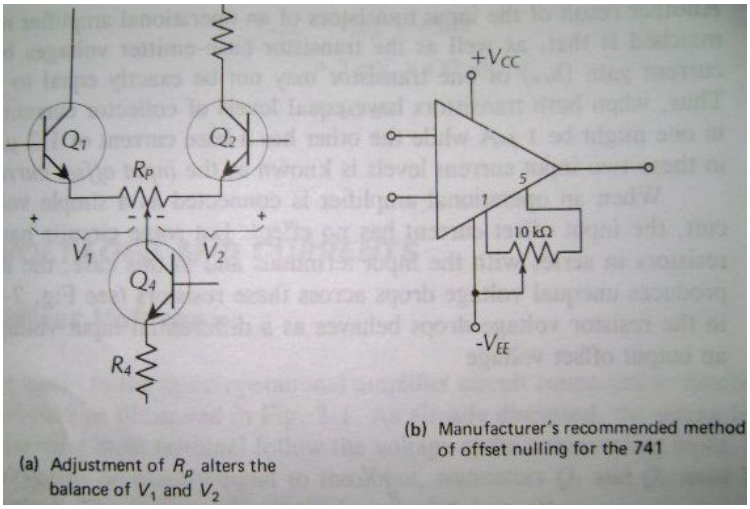
Input Bias Current (I_B)

Input bias current is the average of the currents that flow in to the inverting and non-inverting input terminals of the op-amp.

$$I_B = \frac{IB1 + IB2}{2}$$

Typical value of input bias current I_B for 741 op-amps is 80 nA and max is 600 nA.

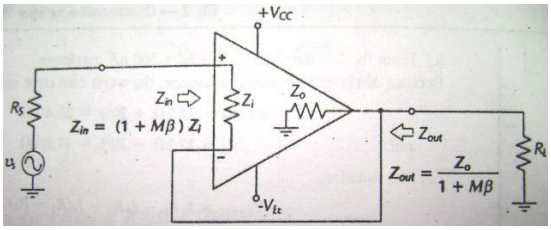
Offset Nulling



One method of dealing with input offset voltage and current is as shown in fig below, which shows a low resistance potentiometer (R_P) connected at the emitters of Q1 and Q2. Adjustment of RP alters the total voltage drop from each base to the common point at the potentiometer moving contact, because an offset voltage is produced by the input offset current. This adjustment can null the effects of both input offset current and input offset voltage.

INPUT AND OUTPUT IMPEDANCE

Input Impedance :



The input impedance offered by any op-amp is substantially modified by its application. From negative feedback theory, the impedance at the op-amp input terminal becomes,

$$Z_{ip} = (1 + A\beta)\, Z_i$$

Z_i = the op-amp input impedance without negative feedback.

A = op-amp open loop gain, typical value for 741 op-amp is 50000

β = Feed back factor

R_i= Input impedance, typical value for 741 op-amp is 0.3 MΩ

Output impedance:

The typical output resistance specified for the 741 op-amp is 75Ω. Any stray capacitance in parallel with this is certain to have a much larger resistance than 75Ω. So 75Ω is also effectively the amplifier output impedance.

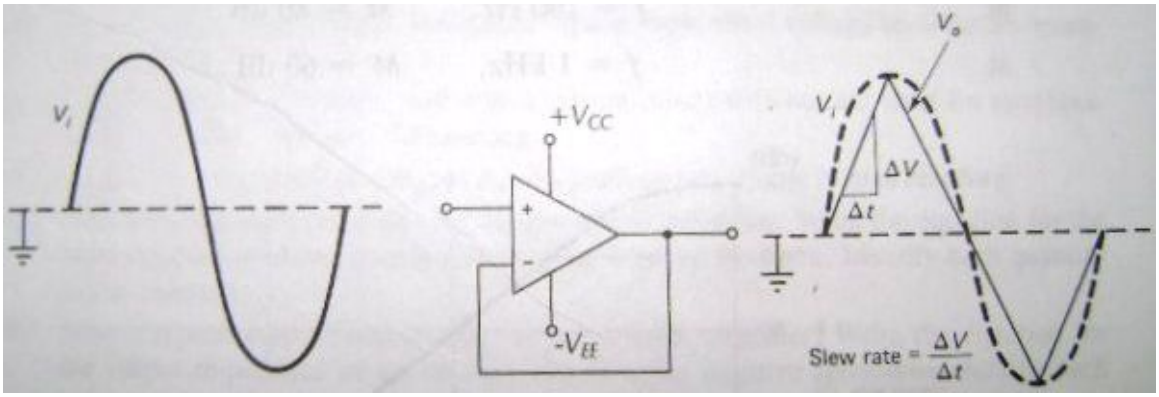
The output impedance of the op-amp is affected by negative feedback.

$$Z_{out} = \frac{Z_o}{(1 + A\beta)}$$

Z_o = op-amp output impedance without negative feedback

Slew Rate

The slew rate (S) of any op-amp is the maximum rate at which the output voltage can change. When the slew rate is too slow for the input, distortion results. This is illustrated in fig below, which shows a sine wave input to a voltage follower producing a triangular output waveform. The triangular wave results because the op-amp output simply cannot fast enough to follow thee sine wave input.



$$S = \frac{\Delta V_o}{t}$$

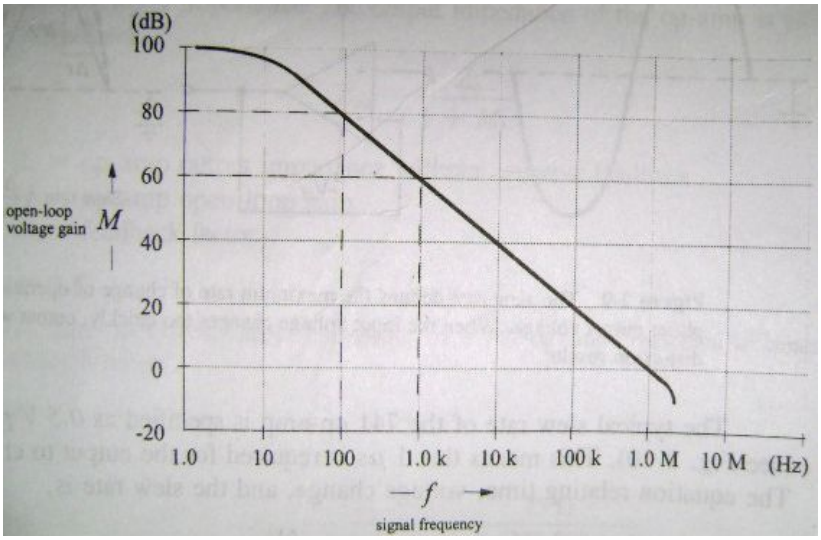
The typical slew rate of the 741 op-amp is 0.5 V/μs. This means that 1μs is required for output to change by 0.5 V

Frequency limitations

Fig below shows the graph of open loop gain (A) plotted versus frequency (f) for a 741 op-amp.

f = 100 Hz, A = 80 dB

f = 1 KHz, A = 60 dB



The open loop gain (A) falls by 20 dB when the frequency increases from 100 Hz to 1 KHz. The ten times increase in frequency is termed a decade. So, the rate of the gain is said to be 20 dB per decade. Where internal gain equals to or greater than 80 dB is required for a particular application, it is available with a 741 only for signal frequencies up to ≈100 Hz. A greater than 20 dB is possible for signal frequencies up to ≈ 90 kHz. Other op-amp maintains substantial internal gain to much higher frequencies than the 741.

1.3 OP-AMP AS DC AMPLIFIERS: Biasing op-amps

Bias Current Paths :

Op-amps must be correctly biased if they are to function properly. The inputs of most op-amps are the base terminals of the transistors in a differential amplifier. Base currents must flow into these terminals for the transistors to be operational.

One of the two input terminals is usually connected in some way to the op-amp output to facilitate negative feedback. The other input might be biased directly to ground via a signal source.

From the fig given below, current I_{B1} flows into the op-amp via the signal source while I_{B2} flows from the output terminal. The next fig shows a situation in which resistor R1 is added in series with inverting terminal to match signal source resistance Rs in series with the non-inverting terminal.

Op-amp input currents produce voltage drops I_{B1} x R_s and I_{B2} x R_1 across the resistors. Rs and R1 should be selected as equal resistors so that the resistor voltage drops are approximately equal. Any difference in these voltage drops will have the same effect as an input offset voltage.

Maximum Bias Resistor Values :

If very small resistance values are selected for Rs and R1 in the circuit the voltage drops across them will be small. On the other hand, if Rs and R1 are very large the voltage drops IB1 x Rs and IB2 x R1 might be several volts. For good bias stability the maximum voltage drop across these resistors should be less than the typical forward biased V_{BE} level for the op-amp input transistors.

Usually the resistor voltage drop made at least ten times smaller than $V_{BE.}$

$I_{B(max)} \times R_{(max)} \approx V_{BE}/10 \approx 0.07$ V

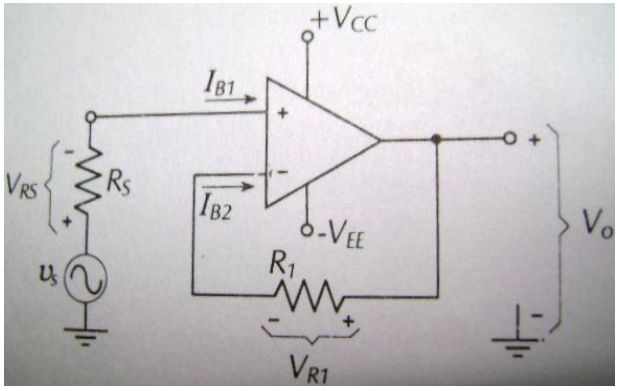
From the 741 data sheet $I_{B(max)} = 500$nA.

Therefore, $R_{(max)} \approx 0.07/500\text{nA} \approx 140$ kΩ.

This is a maximum value for the bias resistors for a 741 op-amp. R(max) can be calculated using the specified I_B(max)for the particular op-amp.

$$R(max) \approx 0.1\ V_{BE}/I_B(max)$$

1.4 Direct – Coupled Voltage Followers

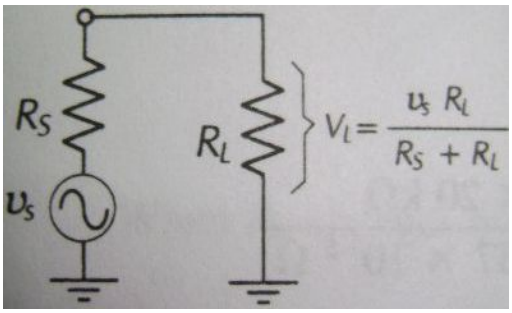


As shown in the figure the resistor R1 is frequently included in series with the inverting terminal to match the source resistance Rs in series with the non-inverting terminal.

The input and output impedances of the voltage follower are

$$Z_{in} = (1+A)\ Z_i \quad \text{and} \quad Z_{out} = Z_o \backslash (1+A)$$

The voltage follower has very high input impedance and very low output impedance. Therefore, it is normally used to convert a high impedance source to low output impedance. In this situation it is said to be used as a 'buffer' between the high impedance source and the low impedance load. Thus, it is termed a 'buffer amplifier'.



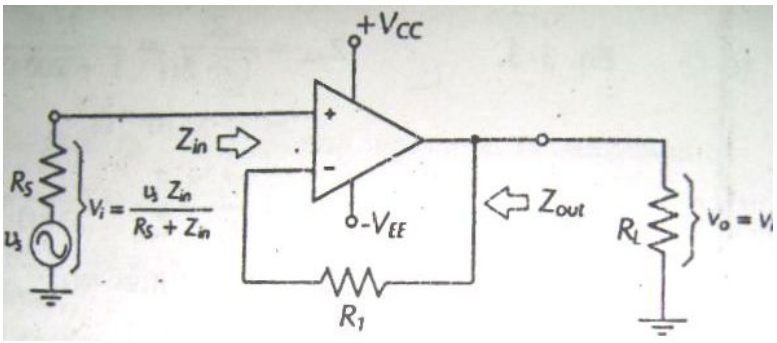
From the fig, a signal voltage is potentially divided across $R_s$and R_L when connected directly to a load. But when the load and source are joined by the voltage follower, it presents its very high impedance to the signal source. Because Z_{in} is normally very much larger than Rs, there is virtually no loss at this point and effectively all the input appears at the op-amp input.

The voltage follower output is

$V_d = \frac{V_i}{A}$ And $V_o = V_i - V_d$

$$\therefore V_o = V_i - \frac{V_i}{A}$$

$$\Rightarrow V_o = V_i\left(1 - \frac{1}{A}\right)$$



The output voltage can be thought of as being divided across RL and the voltage follower output impedance Z_{out}. But Z_{out} is much smaller than any load resistance that might be connected. So, there is effectively no signal loss and all V_i appears as V_o at the circuit output.

Example:

1. A voltage follower using a 741 op-amp is connected to a signal source via a 47kΩ. Select a suitable value for resistor R1. Also calculate the maximum voltage drop across each resistor and the maximum offset voltage produced by the input offset current.

$R_1 = R_s = 47k\Omega$

From a 741 data sheet $I_{B(max)} = 500nA$ and $I_{i(offset)} = 20nA$

$I_{B(max)1} \times R_s = I_{B(max)2} \times R_s$

$= 500nA \times 4.7k\Omega$

$= 23.5mV$

$V_{i(offset)} = I_{i(offset)} \times (R_s or R_1)$

$= 20nA \times 47k\Omega$

$= 0.94mV$

Problem 2

The voltage follower in the above problem has a 1V signal and a 20kΩ load. Calculate the load voltage

(a) When the load is directly connected to the source.
(b) When the voltage follower is between the load and the source.

Solution: (a) $V_L = \frac{V_i R_L}{R_s + R_L} = \frac{1 \times 20k}{(20k + 47k)} = 298mV$

(b) For 741 op-amp, $A = 2 \times 10^5$, $Z_{in} = 2M\Omega$, $Z_{out} = 75\Omega$

$$Z_{inf} = (1 + A)Z_{in} = (1 + 2 \times 10^5) \times 2M$$

$$= 4 \times 10^{11}\Omega$$

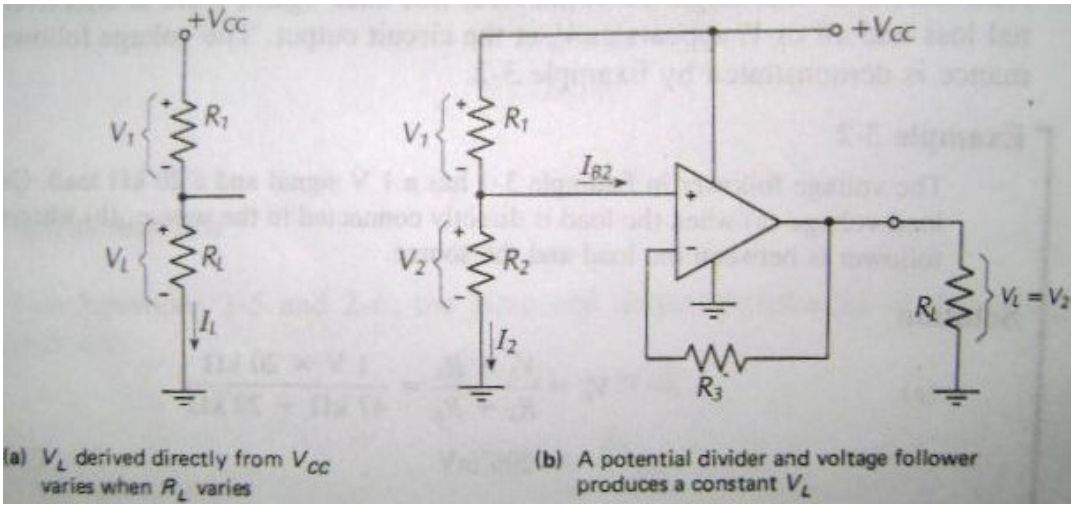
$$V_i = \frac{V_s \times Z_{inf}}{Z_{inf} + R_s} = \frac{1 \times 4 \times 10^{11}}{4 \times 10^{11} + 47k} \approx 1V effectively$$

$$V_o = V_i\left(1 - \frac{1}{A}\right) = 1\left(1 - \frac{1}{200000}\right) = 1V effectively$$

$$Z_{outf} = \frac{Z_o}{1 + A} = \frac{75}{1 + 200000} = 37 \times 10^{-5}\Omega$$

$$V_L = \frac{V_o \times R_L}{R_L + Z_{outf}} = \frac{1 \times 20k}{20k + 37 \times 10^{-5}} \approx 1V$$

When the voltage follower is used with a potential divider to produce a low impedance dc voltage source, as in fig (a), load resistor R_L is directly connected in series with R_1 to derive a voltage V_L from the supply V_{CC}. This simple arrangement has the disadvantage that the V_L varies if the load resistance changes. In fig (b), the presence of the voltage follower maintains the VL constant regardless of the load resistance.



(a) V_L derived directly from V_{CC} varies when R_L varies

(b) A potential divider and voltage follower produces a constant V_L

Example:

A 1 kΩ load resistor is to have 5V developed across it from a 15V source. Design suitable circuits as shown above circuit fig (a) and (b) and calculate the load voltage variation in each case when the load resistance varies by -10%. Use a 741 op-amp.

Solution: For circuit in fig. (a)

$$I_L = \frac{V_L}{R_L} = \frac{5}{1k} = 5mA$$

$$V_1 = V_{cc} - V_L = 15 - 5 = 10V$$

$$R_i = \frac{V_1}{I_L} = \frac{10}{5m} = 2k\Omega$$

When R_L changes by -10%

$$V_L = \frac{V_{cc} \times (R_L - 10\%)}{(R_L - 10\%) + R_f} = \frac{15 \times (1k - 10\%)}{(1k - 10\%) + 2k} = 4.66V$$

For circuit in fig. (b) $V_2 = V_L = 5V and V_1 = V_{cc} - V_2 = 10V$

For 741 $I_{B(max)} = 500nA and I_2 = 100I_{B(max)} = 50\mu A$

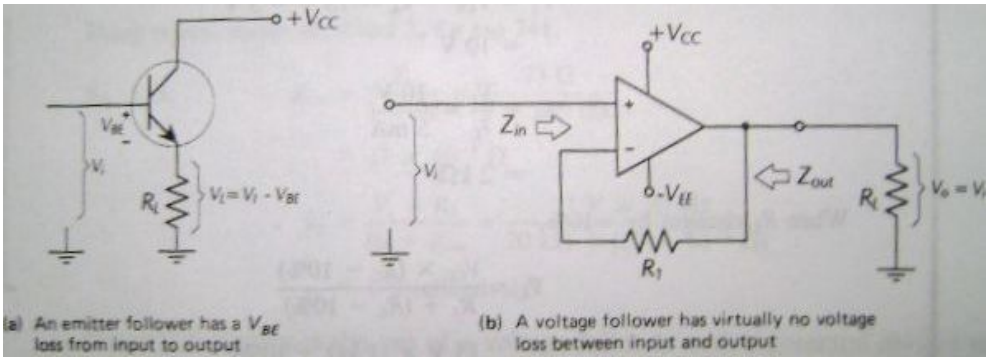
$$R_2 = \frac{V_2}{I_2} = \frac{5}{50\mu} = 100k\Omega$$

$$R_1 = \frac{V_1}{I_2} = \frac{10}{50\mu} = 200k\Omega$$

When R_L changes by -10%

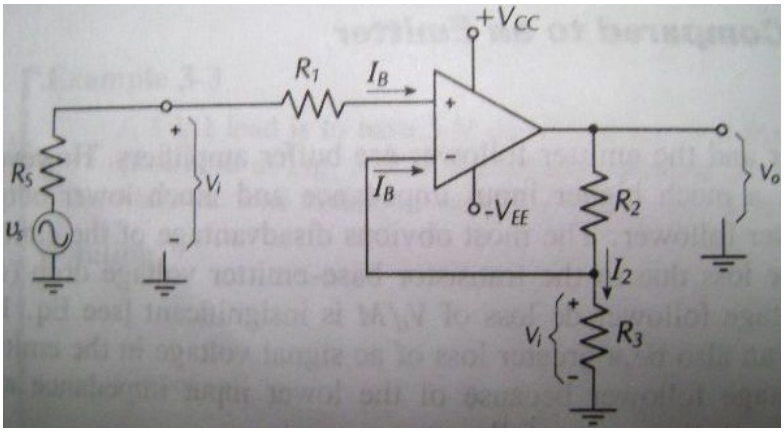
$V_L = V_2 = 5V effectively$

Voltage Follower compared to an Emitter Follower



- Both voltage follower and the emitter follower are buffer amplifiers.
- The voltage follower has a much higher input impedance and much lower output impedance than the emitter follower.
- The disadvantage of the emitter follower is the dc voltage loss due to the transistor base-emitter voltage drop. But the voltage follower dc loss of V_i/A is insignificant.
- There can also be a greater loss of ac signal voltage in the emitter follower than in the voltage follower because of the lower input impedance and higher output impedance with the emitter follower.

1.5 Direct coupled non-inverting amplifiers:



The voltage gain of a non-inverting amplifier,

$$A_f = 1 + \frac{Rf}{R2}$$

As always with a bipolar op-amp, design commences by selecting the potential divider current (I_2) very much larger than the maximum input bias current I_B(max).

Because $V_{R2} = V_i$ (virtual short)

$R_2 = V_i/I_2$

And V_o appears across $(R_2 + R_f)$.

So, $R_2 + R_f = V_o/I_2$

Finally, to equalize the I_BR voltage drops at the op-amp input, R1 is calculated as

$R_{com} \approx R2 \text{ ll } R3$

If R1 is not very much larger than the source resistance,

$Rs + R_{com} \approx R2 \text{ ll } R3$

Example

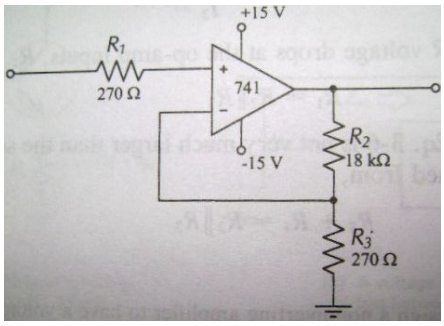
Using a 741 op-amp design a non-inverting amplifier to have a voltage gain of approximately 66. The signal amplitude is to be 15mV.

Solution :

$I_{B(max)} = 500nA \therefore I_2 = 100 \times I_{B(max)} = 50\mu A$

$$R_2 = \frac{V_i}{I_2} = \frac{15m}{50\mu} = 300\Omega$$

$V_o = A_v \times V_i = 66 \times 15m = 990mV$



$$R_2 + R_f = \frac{V_o}{I_2} = \frac{990m}{50\mu} = 19.8k\Omega$$

$$R_f = (R_2 + R_f) - R_2 = 19.5k\Omega$$

$\therefore R_{com} = R\_2 \parallel R\_f \approx 295\Omega$

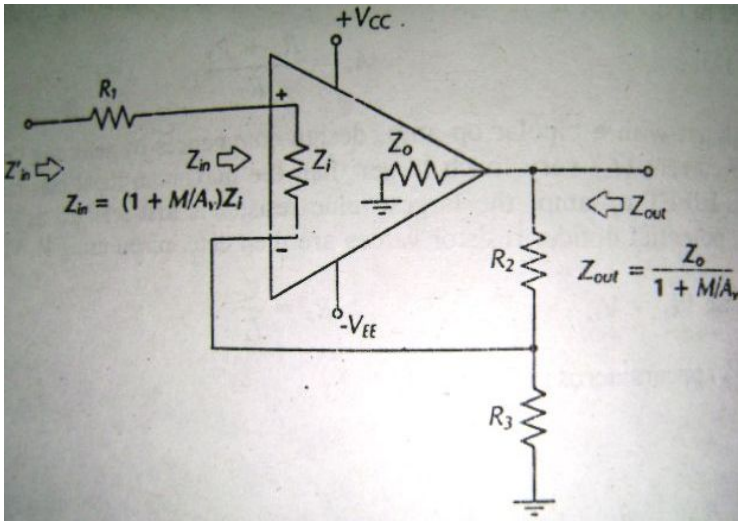
Performance

The input impedance of the op-amp circuit is,1

$$Z_{inf} = (1 + A\beta)Z_{in}$$

$$\beta = \frac{R_1}{R_1 + R_f} = \frac{1}{A_f}$$

$$\therefore Z_{inf} = \left(1 + \frac{A}{A_f}\right)Z_{in}$$



The impedance seen from the signal source is,

$$Z'_{inf} = R_{com} + Z_{inf}$$

Since Z_{inf} is always much larger than R_{com} in a non-inverting amplifier, the inclusion of R1 normally makes no significant difference.

The output impedance of the op-amp circuit is,

$$Z_{outf} = \frac{Z_{out}}{1 + A\beta}$$

$$\because \beta = \frac{1}{A_f} \therefore Z_{outf} = \frac{Z_{out}}{1 + \frac{A}{A_f}}$$

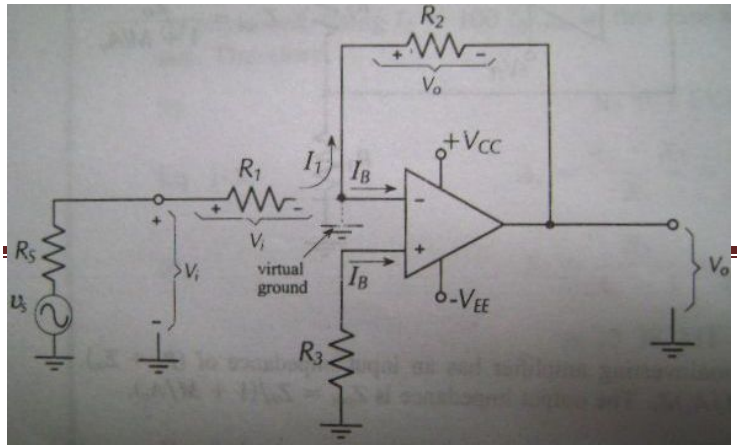
Problem

Calculate the input impedance of the non-inverting amplifier as shown below . Use the typical parameters for the LF 353 op-amp.

Solution: For LF 353 A=100000 and $Z_{in} = 10^{12}\Omega$

$$\because Z_{inf} = \left(1 + \frac{A}{A_f}\right)Z_{in} \approx 1.5 \times 10^{15}\Omega$$

$$and\, Z'_{inf} = R_{com} + Z_{inf} \approx 1.5 \times 10^{15}\Omega$$



1.6 Direct - Coupled Inverting Amplifier:

Resistor R_{com} is included at the non-inverting terminal to equalize the dc voltage drops due to the input bias currents approximately equal

resistance should be 'seen' when 'looking out' from input terminal of the op-amp .

Therefore, $R_{com} \approx R_1 \| R_f$

And if R_f is not very much larger than the source resistance, then

$R_{com} \approx (R_1 = R_s) \| R_f$

As with other bipolar op-amp circuits, the resistor current (I_1) is first selected very much larger than the maximum input bias current ($I_{B\,max}$).

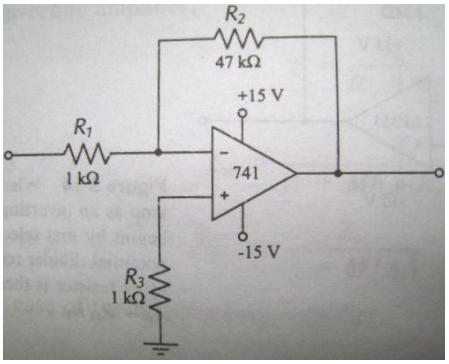
$$R_1 = \frac{V_i - V_2}{I_1} = \frac{V_i}{I_1} [\because V_2 = 0]$$

Since op-amp input terminal does not draw any current so, I_1 flows to feedback resistance.

$R_f = V_o/I_1$

Example

Design an inverting amp using a 741 op-amp. The voltage gain is to be 50 and the output voltage amplitude is to be 2.5 V

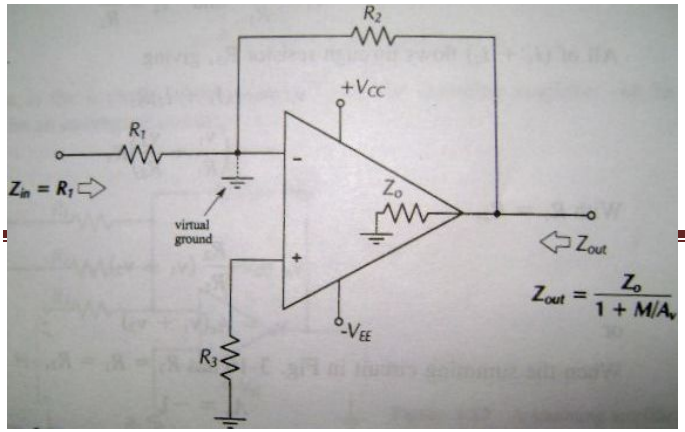


Solution:

$$I_{B(max)} = 500nA \therefore I_2 = 100 \times I_{B(max)} = 50\mu A$$

$$V_i = \frac{V_o}{A_f} = \frac{2.5}{50} = 50mV$$

$$R_1 = \frac{V_i}{I_1} = \frac{50m}{50\mu} = 1k\Omega$$



Performance

$Z_{inf} = R_1$

The output impedance of the inverting amplifier is determined exactly as for any other op-amp circuit.

$$Z_{outf} = \frac{Z_{out}}{1 + A\beta} and \beta = \frac{R_1}{R_1 + R_f}$$

$$Z_{outf} = \frac{Z_o}{\left(1 + \frac{AR_1}{R_1 + R_f}\right)}$$

$$when R_f \gg R_1 Z_{outf} = \frac{Z_{out}}{1 + \frac{A}{A_f}}$$

1.7 Summing Amplifiers:

Inverting Summing Circuit:

Fig below shows a circuit that amplifies the sum of two or more inputs and since inputs are applied to the inverting input terminal, hence the amplifier is called 'Inverting Summing Amplifier'.
V_a,V_b and V_c are three inputs applied to the inverting terminal through resistors R_a ,R_b and R_c.
Applying Kirchoff's law at node V2

$$I_a + I_b + I_c = I_f$$

$$\Rightarrow \frac{V_a - V_2}{R_a} + \frac{V_b - V_2}{R_b} + \frac{V_c - V_2}{R_c} = \frac{V_2 - V_o}{R_f}$$

Because of Virtual Ground, V_2=0

$$\Rightarrow \frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = \frac{-V_o}{R_f}$$

$$\Rightarrow V_o = -R_f\left(\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c}\right)$$

$$If R_a = R_b = R_c = R then V_o = \frac{-R_f}{R}(V_a + V_b + V_c) \Rightarrow V_o = A_f(V_a + V_b + V_c)$$

$$Also if R_f = R, then V_o = (V_a + V_b + V_c)$$

$$And if \frac{R_f}{R} = \frac{1}{n} where n is the no. of inputs. \ Here n = 3$$

$$\therefore \frac{R_f}{R} = \frac{1}{3} \Rightarrow V_o = -\frac{(V_a + V_b + V_c)}{3}$$

Here the output voltage is equal to the average of all the three inputs. Hence this can be used as an 'Averaging Circuit'.

Non-Inverting Summing Circuit:

Here the three inputs are connected to the non-inverting input through resistors of equal value R. The voltage V_1 is determined using superposition theorem. Let V_b and V_c are grounded and let V_{1a} be at V_1 due to V_a, corresponding voltage.

$$V_{1a} = \frac{V_a \times R\backslash 2}{R + R\backslash 2}$$

Similarly when V_a and V_c are grounded, then

$$V_{1b} = \frac{V_b \times R\backslash 2}{R + R\backslash 2}$$

When V_a and V_b are grounded, then

$$V_{1c} = \frac{V_c \times R\backslash 2}{R + R\backslash 2}$$

$$V_1 = V_{1a} + V_{1b} + V_{1c} = \frac{V_a}{3} + \frac{V_b}{3} + \frac{V_c}{3}$$

The output voltage is $V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_a + V_b + V_c}{3}\right)$$

$$If \left(1 + \frac{R_f}{R_1}\right) = 3 \quad ie. the no. of inputs$$

$$then V_o = V_a + V_b + V_c$$

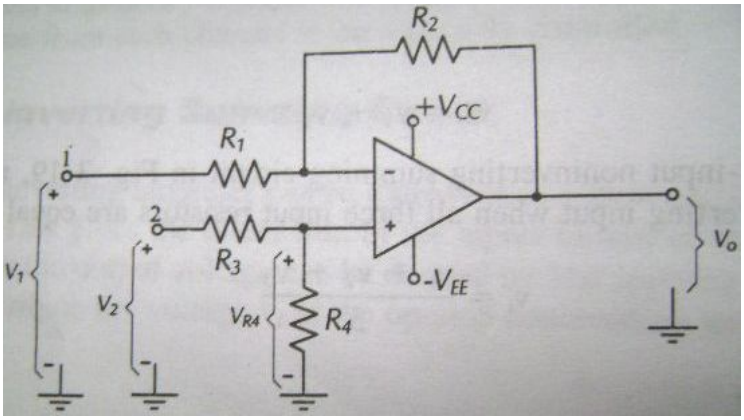
Output voltage is equal to the sum of all the three input voltages.

If the gain of the amplifier is 1 I.e. $\left(1+\frac{R_f}{R_1}\right)=1$, then the output is,

$$Vo = \frac{(Va + Vb + Vc)}{3}$$

1.8 Difference Amplifier:

A difference amplifier or a differential amplifier amplifies the difference between two input signals. A differential amplifier is a combination of inverting and non-inverting configurations. V_y and V_x are two inputs applied to inverting and non-inverting input terminals respectively. Apply superposition theorem to determine the output voltage Vo.



When V_x = 0, the configuration becomes an inverting amplifier and hence the output is

$V_{oy} = -\frac{RF}{R1} V_y$

When V_y = 0, the configuration is a non-inverting amplifier. Hence the output is,

$$V_{ox} = \left(1+\frac{R_f}{R_1}\right) V_1$$

$$V_1 = \frac{R_3}{R_2+R_3} V_x$$

$$\Rightarrow V_{ox} = \left(\frac{R_3}{R_2+R_3}\right)\left(1+\frac{R_f}{R_1}\right) V_x$$

$$Let R_{23} = R_1 and R_f = R_3, then V_{ox} = \frac{R_f}{R_1} V_x$$

∴The total output voltage is,

$$V_o = V_{oy} + V_{ox}$$

$$= \frac{R_f}{R_1} V_x - \frac{R_f}{R_1} V_y$$

$$\Rightarrow V_o = \frac{R_f}{R_1}(V_x - V_y)$$

When RF and R1 are equal value resistors, the output is the direct difference of the two inputs. By selecting RF greater than R1 the output can be made an amplified version of the input difference.

Input Resistance

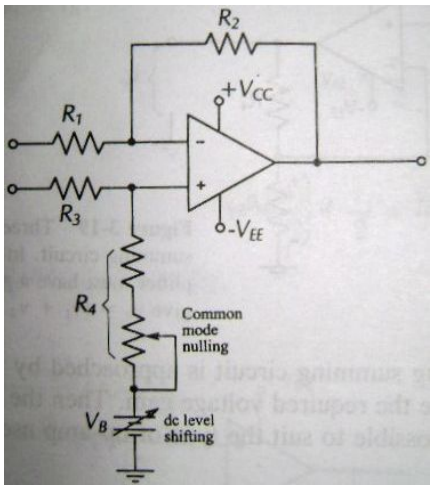
Problems with selecting the difference amplifier resistors as R1 = R2 and RF = R3 is that the two input resistances are unequal. The input resistance for voltage at inverting terminal is R1 as in the case of an inverting amplifier. At the op-amp non-inverting input terminal, the input resistance is very high, as it is for a non-inverting amplifier.

From the output voltage equation it is shown that the same result would be obtained if the ratio RF/R1 is the same as R3/R2 instead of making RF = R3 and R1 = R2.
Therefore, when the resistance of R1 has been determined, R2 = R3 can be made equal to R1, as long as the ratio of the resistance is correct. This will give equal input resistances at the two input terminals of the circuit.

There are two types of differential input resistance $(R_{i(diff)})$ and common mode input resistance (R_{icom}).

The differential input resistance is the resistance offered to a signal source which is connected directly across the input terminals. It is the sum of the two input resistances.

$R_{i(diff)} = R_1 + R_2 + R_3$



The common mode input resistance is the resistance offered to a signal source which is connected between the ground and both input terminals, that is, the parallel combination of the two input resistances.

$R_{i(cm)} = R_1 \parallel (R_2 + R_3)$

Common Mode Voltage

If the ratio R_F/R_1 and R_3/R_2 are not exactly equal, one input voltage will be amplified by a greater amount than the other. Also, the common mode voltage at one input will be amplified by a greater amount than that at the other input. Consequently, common mode voltages will not be completely cancelled. One way of minimizing the common mode input from a difference amplifier is as shown in the fig below.

R_3 is made up of a fixed value resistor and a much smaller adjustable resistor . This allows the ratio R_3/R_2 to be adjusted to closely match R_F/R_1 in order to null the common mode output voltage to zero.

Output Level Shifting

R_3 is connected to a VB instead of grounding it in the usual way. To understand the effect of V_B, assume that both input voltages are zero. The voltage at the op-amp non-inverting input terminal will be $V_f = \frac{V_B \times R_2}{R_1 + R_2}$

The voltage at the op-amp inverting input terminal will be ,

$$V_- = V_+$$

The output will be, $Vo = \left(\frac{R_1 + R_F}{R_1}\right) V_+$

Substituting for V+ and using the resistor relationships ($\frac{RF}{R1} = \frac{R3}{R2}$), the output voltage is ,

$$V_o = V_B$$

Therefore, if VB is adjustable, the dc output voltage level can be shifted as desired.

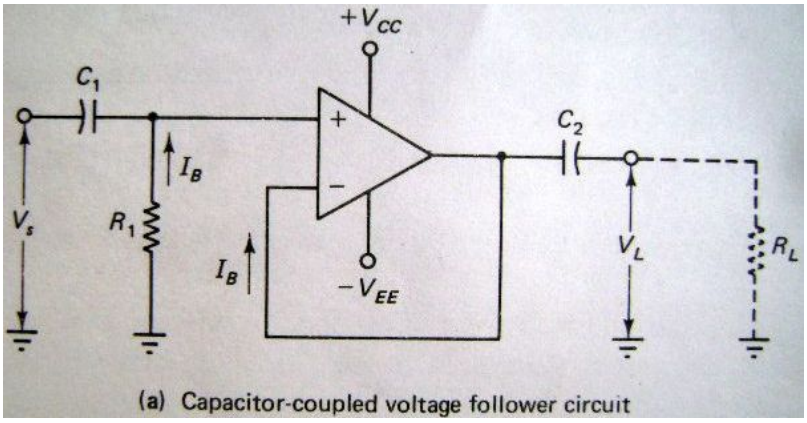
UNIT – 2

OP-AMPS AS AC AMPLIFERS

2.1 CAPACITOR-COUPLED VOLTAGE FOLLOWER

When a voltage follower is to have its input and output capacitor-coupled, the non-inverting input terminal must be grounded via a resistor. The resistor is required to pass bias current to the amplifier non-

inverting input terminal. A resistor equal to R_1 might be included in series with the non-inverting terminal to equalize the I_BR_B voltage drop and thus minimize the output offset voltage. However in the case of a circuit with its output capacitor coupled, small dc offset voltage is unimportant because they are blocked by the capacitor.

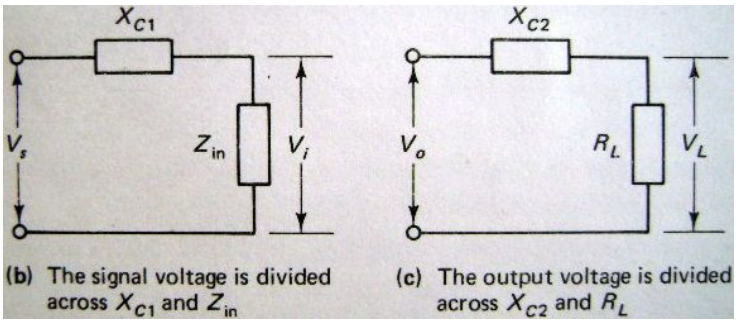


(a) Capacitor-coupled voltage follower circuit

Design of a capacitor coupled voltage follower as in figure involves calculation of R_1, C_1 and C_2. As always, the largest possible values are normally selected to ensure minimum circuit power dissipation and minimum current demand from the power supply. The smallest possible capacitor values are normally used for their small physical size and low cost. We have the maximum value for R1 for a bipolar op-amp as $(0.1\ V_{BE})/I_B$.

The circuit input impedance is $R_1 \parallel Z_i'$, where Z_i' is the input impedance at the op-amp non-inverting input terminal, $[Z_i' = Z_i(1 + M\beta)]$. But, with 100% negative feedback employed in a voltage follower circuit, Z_i' is always much larger than R1. Consequently, for the circuit $Z_{in} = R_1$.

Load resistor R_L normally has a lower resistance then R_1. Therefore, because each capacitor value is inversely proportional to the resistance in series with it, C_2 is usually much larger than C_1. At the circuit low 3dB frequency (f_1), the impedance of C_1 should be much smaller than Z_{in}, so that there is no significant division of the signal across X_{C1} and Z_{in}, as in figure (b). In this case, C_1 will have no effect on the circuit low 3dB frequency. Thus, C_1 is calculated from



(b) The signal voltage is divided across X_{C1} and Z_{in} (c) The output voltage is divided across X_{C2} and R_L

$$X_{C1} = \frac{Z_{in}}{10} at f_1$$

$$giving C_1 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)}$$

As illustrated in figure (c), the circuit output voltage v_o is divided across X_{C2} and R_L to give the load voltage V_L. The equation for V_L is

$$V_L = \frac{v_o \times R_L}{\sqrt{(R_L^2 + X_{C2}^2)}}$$

$$When X_{C2} = R_L, \qquad V_L = \frac{v_o \times R_L}{\sqrt{(2R_L^2)}} = \frac{v_o}{\sqrt{2}}$$

$$= 0.707\ v_o = v_o - 3dB$$

Or, the circuit 3dB frequency (f_1) occurs when $X_{C2}=R_L$. Therefore, C_2 is calculated from

$$X_{C2} = R_L at f_1$$

$$which gives C_2 = \frac{1}{2\pi f_1 R_L}$$

The above design approach gives the smallest possible capacitor values. When selecting standard value components, the next larger standard size should be chosen to give capacitive impedances slightly smaller than calculated.

In the unusual situation where R_1 is smaller than R_L, C_1 would be larger capacitor than C_2. To give the smallest capacitor values in this case, it is best to letC_1determine the low 3dBfrequency, by making $X_{c1}=R_1$ at f_1. Then, $X_{c2}=R_L/10$ at f_1.

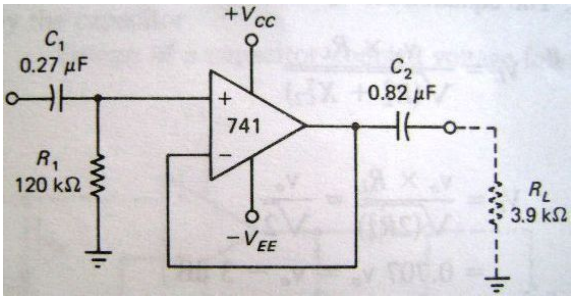
Example 1:

Design a capacitor-coupled voltage follower using a 741 operational amplifier. The lower cutoff frequency for the circuit is to be 50 Hz and the load resistance is RL=3.9kΩ.

Solution

$$R_{1(max)} = \frac{0.1\ V_{BE}}{I_{B(max)}} = \frac{0.1 \times 0.7}{500n} \approx 140\ k\Omega$$

$$And X_{C1} = \frac{R_1}{10} at f_1$$



$$or, \quad C_1 = \frac{1}{2\pi f_1 \left(\frac{R_1}{10}\right)} = \frac{1}{2\pi \times 50 \times \left(\frac{240k}{10}\right)} = 0.27\ \mu F$$

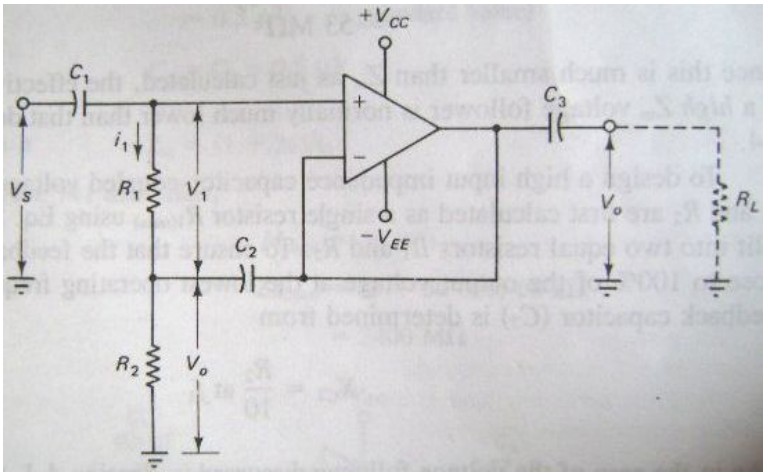
$$And X_{C2} = R_L at f_1$$

$$or, \quad C_2 = \frac{1}{2\pi f_1 R_L} = \frac{1}{2\pi \times 50 \times 3.9k} \approx 0.82\ \mu F$$

The circuit supply voltages should normally be ±9V to ±18V or within whatever range is specified on the op-amp data sheet.

2.2 HIGH Z_{in} CAPACITOR COUPLED VOLTAGE FOLLOWER

The input impedance of the capacitor-coupled voltage follower discussed previously is set by the value of the resistor R_1. This gives much smaller input impedance than the direct-coupled voltage follower. Figure shows a method by which the input impedance of the capacitor-coupled voltage follower can be substantially increased.



Capacitor C_2 in figure couples the circuit output voltage to the junction of resistors R_1 and R_2. C_2 behaves as an ac short circuit so that v_o is developed across R_1 is

$$v_1 = v_s - v_o$$

$$= v_s - Av_1$$

$$giving v_1 (1 + A) = v_s$$

$$or v_1 = \frac{v_s}{1 + A}$$

$$and i_1 = \frac{v_1}{R_1} = \frac{v_s}{(1 + A)R_1}$$

$$input resistance Z_{in} = \frac{v_s}{i_1}$$

$$or, \quad Z_{in} = (1 + A)R_1$$

The above equation shows that this circuit indeed has very high input impedance. For example, with an open loop gain of 200000 and a 47 kΩ resistor for R_1, the circuit input impedance would be

$$Z_{in} \approx 200000 \times 47\ k\Omega$$

$$= 9.4 \times 10^9 \Omega$$

This extremely high input impedance is unrealistic when it is remembered that some stray capacitance is always present. If the stray capacitance (C_2) between the circuit input and ground is 3pF (which is quite possible), the impedance of C_2 at 1 kHz is

$$X_{Cs} = \frac{1}{2\pi \times 1k \times 3p}$$

$$= 53\ M\Omega$$

Since this is much smaller than Z_{in} as just calculated, the effective input impedance of a *high* Z_{in} voltage follower is normally much lower than that determined from the above equation.

To design a high input impedance capacitor coupled voltage follower, resistors R_1 and R_2 are first calculated as a single resistor $R_{1(max)}$. Then, $R_{1(max)}$ is split into two equal resistors R_1 and R_2. To ensure that the feedback voltage remains close 100% of the output voltage at the lower cutoff frequency, the required feedback capacitor (C_2) is determined from

$$X_{C2} = \frac{R_2}{10} at f_1$$

As in the case of the voltage follower discussed previously, the output capacitor can be used to set the lower 3dB frequency for the high-input impedance voltage follower.

$$X_{C3} = R_L at f_1$$

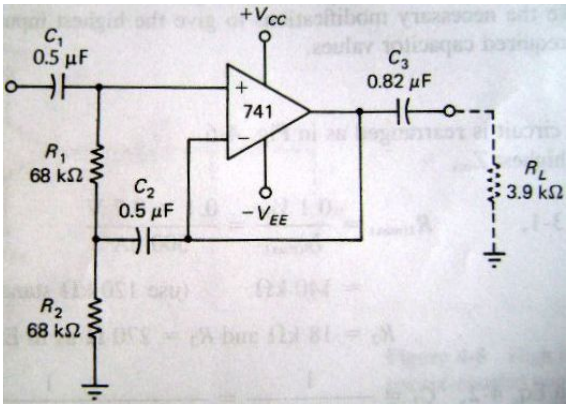
The impedance of input capacitor C_1 should theoretically be determined as $X_{C1} = Z_{in}/10$. However, as the previous discussion of input impedance shows, the actual input impedance is affected by stray capacitance. Also, simply selecting C1 as much larger than the likely stray capacitance can cause a peaking effect in the circuit frequency response. Therefore, a reasonable rule-of-thumb for the circuit is to

select $X_{C1} = R_1/10$ at f_1. With R_1=R_2, X_{C1} =X_{C2}, and C_1=C_2.

A resistor could be included in series with the op-amp inverting input terminal in the circuit to equalize the voltage drops, but as already explained, this is not usually necessary when the output is capacitor-coupled. If such a resistor is to be used, it should be equal to (R_1 + R_2) and it should be connected between the inverting input terminal and the junction of C_2 and the op-amp output. In other words, it should not be in series with C_2.

Example 2:

Modify the circuit in Example 1 to make it a high input impedance voltage follower. Also, determine the minimum theoretical input impedance of the circuit.



Solution

$$R_1 + R_2 = R_{1(max)} = 140\ k\Omega$$

$$\therefore R_1 + R_2 = \frac{140}{2} = 70\ k\Omega$$

$$Also C_3 = \frac{1}{2\pi f_1 R_L} = 0.82\ \mu F$$

$$And C_2 = \frac{1}{2\pi f_1 \left(\frac{R_2}{10}\right)} = \frac{1}{2\pi \times 50 \times \left(\frac{68k}{10}\right)}$$

$$\approx 0.5\ \mu F$$

$$\therefore C_1 = C_2 = 0.5\ \mu F$$

$$Now Z_{in} = (1 + A)R_1$$

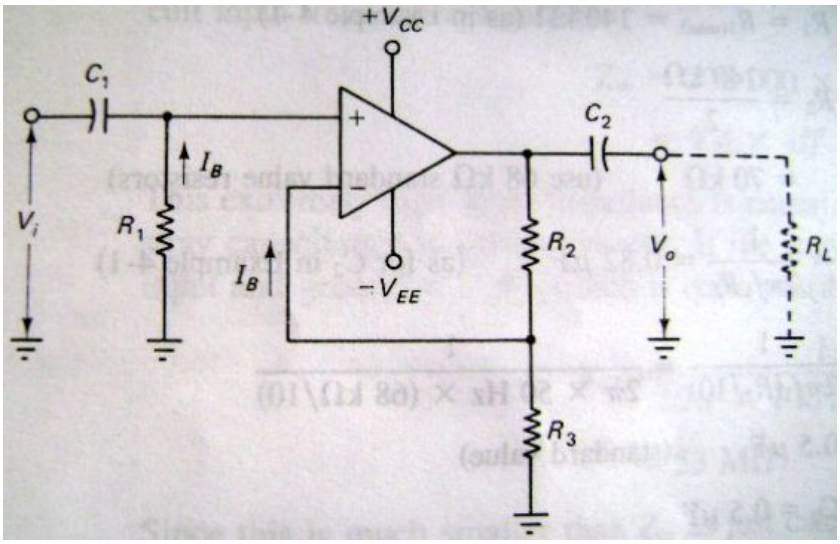
$$From datasheet of\ 741, \quad M_{min} = 50000$$

$$\therefore Z_{in(min)} = (1 + 50000) \times 68k$$

$$= 3400\ M\Omega$$

2.3 CAPACITOR-COUPLED NON-INVERTING AMPLIFIER

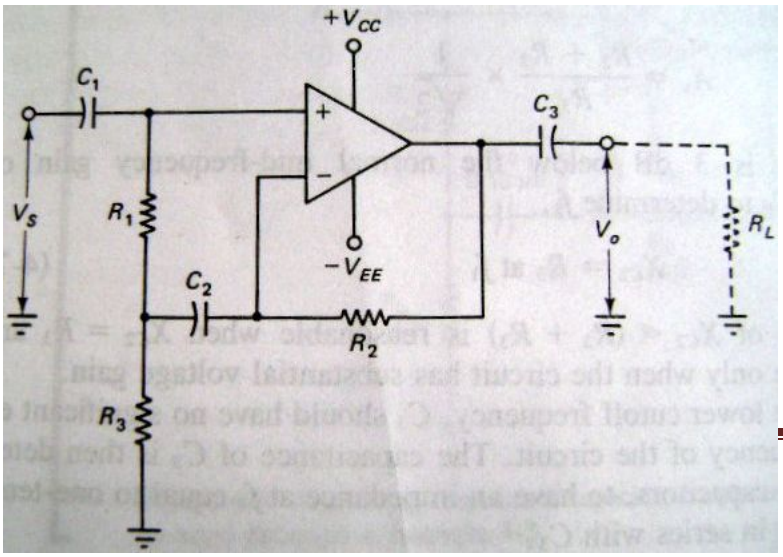
When the input of a non-inverting amplifier is to be capacitor coupled, the non inverting input terminal must be grounded via a resistor to provide a path for the input bias current. Figure shows the arrangement. R_1 may be equal to $R_2 \parallel R_3$ as in the direct-coupled case. However, as already explained, dc offset is unimportant when the output is capacitor coupled, so any reasonable value of R_1 is chosen within the limit set by $R_{1(max)}$.



As in the case of the capacitor coupled voltage follower, $Z_{in} = R_1$ for a capacitor coupled non inverting amplifier also. Resistors R_2 and R_3 are calculated in the same way as for the capacitor coupled voltage follower.

2.4 HIGH Z_{in} CAPACITOR COUPLED NON-INVERTING AMPLIFIER

The input impedance of the non inverting amplifier in figure is improved in the same way as for the high Z_{in} voltage follower. Here, the voltage fed back form the output to the input via R_2, C_2 and R_3 is not 100%, but is potentially divide by a factor β, where



$$\beta = \frac{R_3}{R_2 + R_3}$$

Substituting this quantity into the analysis for Z_{in} gives

$$Z_{in} = (1 + A\beta) \times R_1$$

The values of resistors R_2 and R_3 for the high Z_{in} circuit are determined exactly as for a

direct coupled non inverting amplifier. Then, for equal I_BR_B voltage drop

$$R_1 + R_3 = R_2$$

$$Whichusuallygives, \quad R_1 \approx R_2$$

Alternatively, for the highest input impedance (without equalizing the I_BR_B voltage drops)

$$R_1 + R_3 = R_{max}$$

$$= \frac{0.1\ V_{BE}}{I_{B(max)}}$$

The capacitor values can be exactly as for the high Z_{in} voltage follower. An alternative to this for a circuit which might have a variable load is to use C_2 to determine the low 3dB frequency for the circuit. With C_2 in the circuit, the voltage gain is

$$A_v = \frac{R_2 + R_3 - jX_{C2}}{R_3 - jX_{C2}}$$

$$If X_{C2} \ll (R_2 + R_3), \quad A_v \approx \frac{R_2 + R_3}{\sqrt{(R_3^2 + X_{C2}^2)}}$$

$$and when X_{C2} = R_3, \quad A_v = \frac{R_2 + R_3}{R_3} \times \frac{1}{\sqrt{2}}$$

Or, when $X_{C2} = R_3$, A_v is 3dB below the normal mid-frequency gain of $(R_2 + R_3)/R_3$. Thus, for C_2 to determine f_1

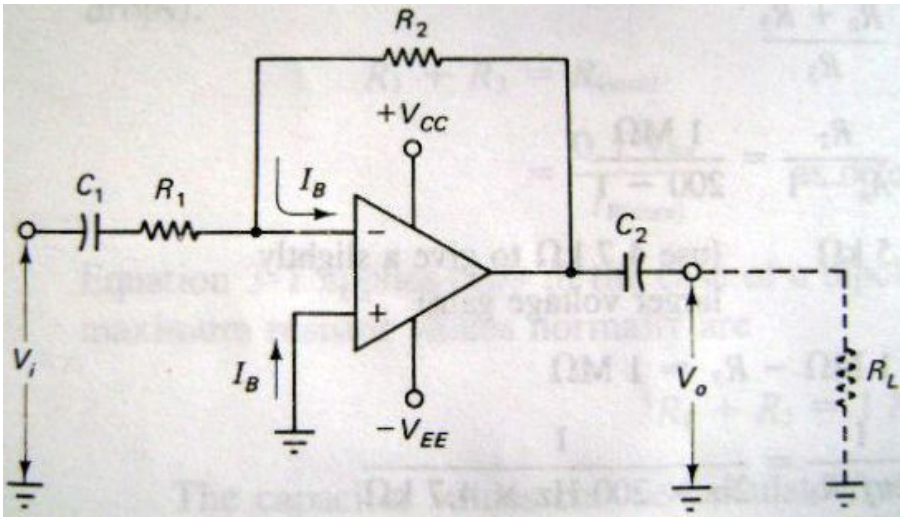
$$X_{C2} = R_3 at f_1$$

Note that the assumption of $X_{C2} \ll (R_2 + R_3)$ is reasonable when $X_{C2} = R_3$ and $R_3 \ll R_2$, which is the case only when the circuit has substantial voltage gain.

When C_2 is to set the lower cutoff frequency, C_3 should have no significant effect on the low 3dB frequency of the circuit. The capacitance of C_3 is then determined, like other coupling capacitors, to have impedance at $_{fl}$ equal to one-tenth of the minimum resistance in series with C_3.

2.5 CAPACITOR-COUPLED INVERTING AMPLIFIER

A capacitor-coupled inverting amplifier is the figure. In this case, bias current to the op-amp inverting input terminal flows via resistor R_2, so coupling capacitor C_1 does not interrupt the input bias current. No resistor is included in with the non inverting input terminal, because a small dc offset is unimportant with a capacitor-coupled output. If it is desired to equalize the I_BR_B voltage drops, the resistance in series with the non inverting input should equal R_2 because R_2 is not part of the bias current path at the inverting input terminal.

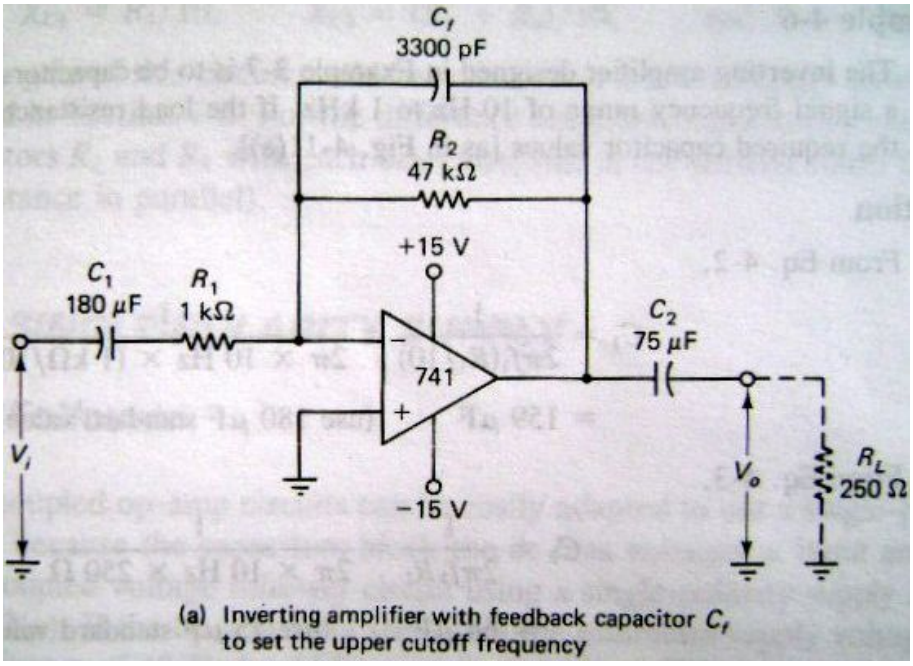


The resistor values are determined as for a direct-coupled inverting amplifier circuit. Then C_1 and C_2 are calculated to give$X_{c1} = R_1/10\,at f_1$, and$X_{c2} = R_L at f_1$, as in the case of a capacitor-coupled non inverting amplifier.

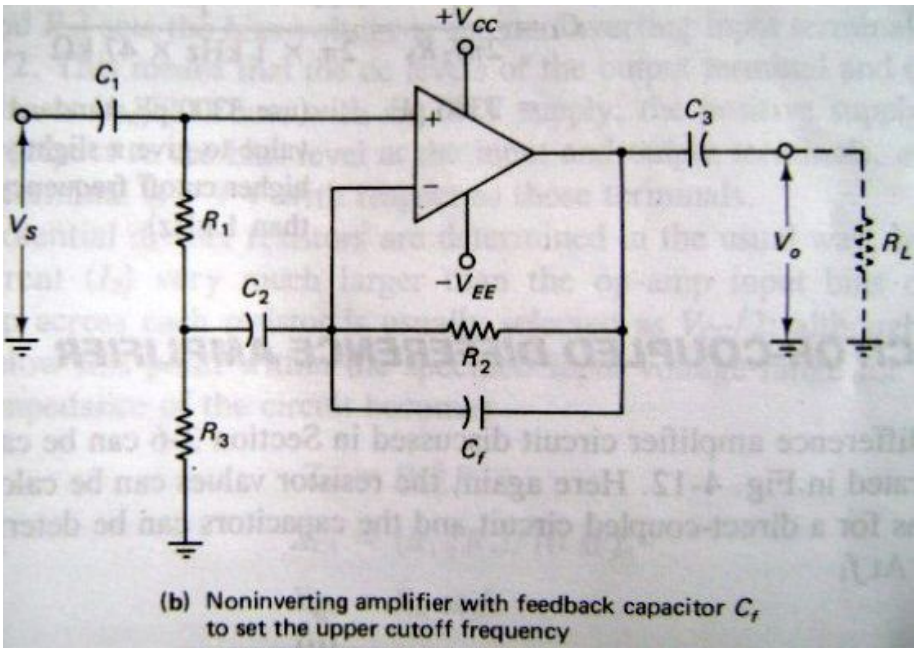
SETTING THE UPPER CUTOFF FREQUENCY

The highest signal frequency that can be processed by an op-amp circuit depends on the op-amp selected. In some circumstances, the upper cutoff frequency may be higher than desired. One example this is where very low frequency signals are to be amplified and unwanted high frequency noise voltages are to be excluded. In this case, the circuit voltage gain should be made to fall off just above highest desired signal

frequency. The usual method is to connect a feedback capacitor C_f from the op-amp output to its inverting input terminal as illustrated in figures (a) and (b).



(a) Inverting amplifier with feedback capacitor C_f to set the upper cutoff frequency



(b) Noninverting amplifier with feedback capacitor C_f to set the upper cutoff frequency

For the inverting amplifier in the figure (a), the voltage gain is

$$A_v = \frac{R_2 \parallel C_{Cf}}{R_1}$$

$$or, \quad A_v = \frac{1}{R_1\sqrt{\left(\frac{1}{R_2}\right)^2 + \left(\frac{1}{X_{Cf}}\right)^2}}$$

$$When X_{Cf} = R_2, \quad A_v = \frac{1}{\sqrt{2}}\left(\frac{R_2}{R_1}\right)$$

Or A_v is 3dB below the normal voltage gain of R_1/R_2. Thus, the upper cutoff frequency for the circuit can be set at the desired frequency (f_2) by making

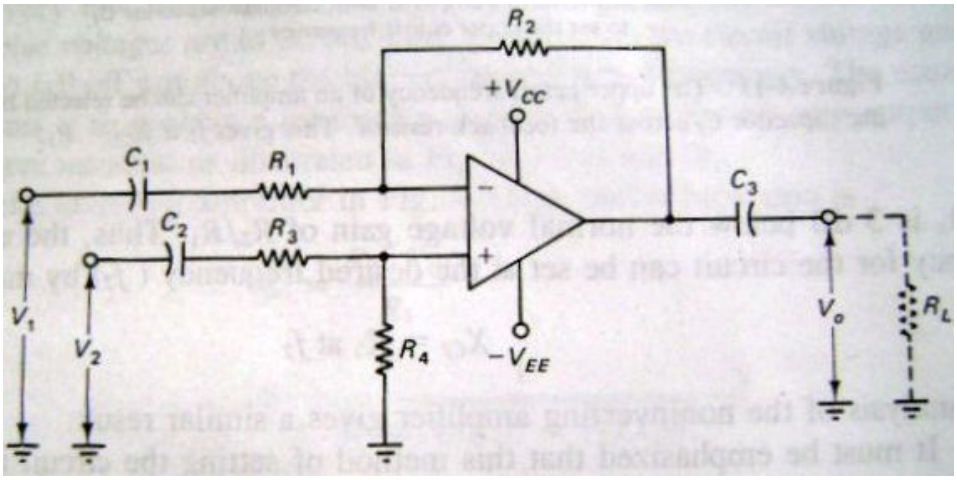
$$X_{Cf} = R_2 at f_2$$

An analysis of the non inverting amplifier gives a similar result.

It must be emphasized that this method of setting the circuit upper cutoff frequency is applicable only the op-amp has a much higher cutoff frequency. The op-amp cutoff frequency must be greater than the circuit cutoff frequency multiplied by the amplifier closed-loop gain.

2.6 CAPACITOR-COUPLED DIFFERENCE AMPLIFIER

The difference amplifier circuit can be capacitor-coupled as illustrated in the figure. The resistor values can be calculated in the same way as for a direct-coupled circuit and the capacitors can be determined in the usual way. At



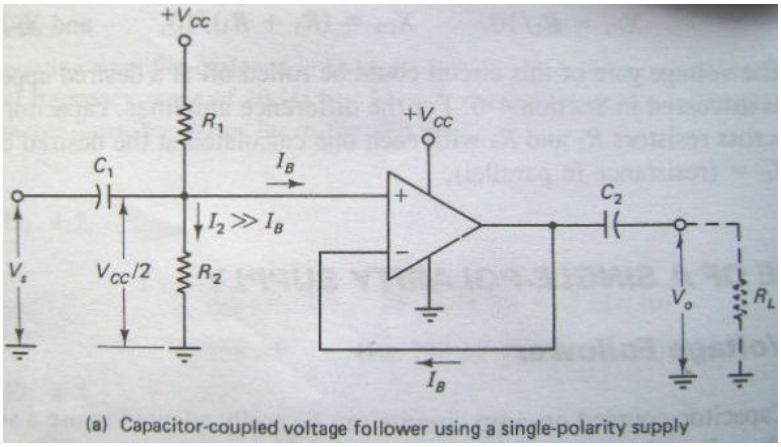
$$X_{C1} = \frac{R_1}{10}, \qquad X_{C2} = \frac{R_3 + R_4}{10}, \qquad and X_{C3} = R_L$$

The voltage gain of this circuit could be rolled off at a desired upper cutoff frequency. For the difference amplifier, capacitors should be placed across resistors R_2 and R_4 with each one calculated at the desired cutoff frequency as X_c = (resistance in parallel).

2.7 USE OF A SINGLE-POLARITY SUPPLY

Voltage follower

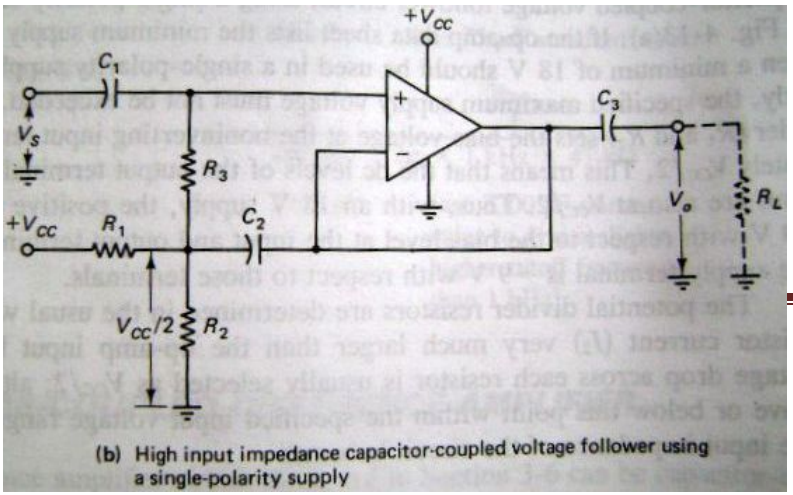
Capacitor-coupled op-amp circuits can be easily adapted to use a single-polarity supply voltage because the capacitors block the DC bias voltages at input and output. A capacitor- coupled voltage follower circuit using a single-polarity supply is illustrated in figure (a). If the op-amp data sheet lists the minimum voltage supply voltage as 9V, then a minimum of 18 V should be used in a single-polarity supply situation. Similarly, the specified maximum supply voltage must not be exceeded. The potential divider (R_1 and R_2) sets the bias voltage at the non inverting input terminal as approximately$Vcc/2$. This means that the dc levels of the output terminal and the inverting input are also at$Vcc/2$. Thus, with an 18V supply, the positive supply terminal is +9 V with respect to the bias level at the input and output terminals, and the negative supply terminal is -9 V with respect to those terminals.



(a) Capacitor-coupled voltage follower using a single-polarity supply

The potential divider resistors are determined in the usual way, by choosing a resistor current (I_2) very much larger than the op-amp input bias current. The voltage drop across each resistor is usually selected as$Vcc/2$; although it could be above or below this point within the specified input voltage range for the op-amp. The input impedance of the circuit becomes

$$Z_{in} = R_1 \parallel R_2$$



(b) High input impedance capacitor-coupled voltage follower using a single-polarity supply

$$so as usual, \quad X_{C1} = \frac{R_1 \parallel R_2}{10} at f_1$$

$$and R_L at f_1$$

The figure (b) shows a high input impedance voltage follower using a single polarity supply.

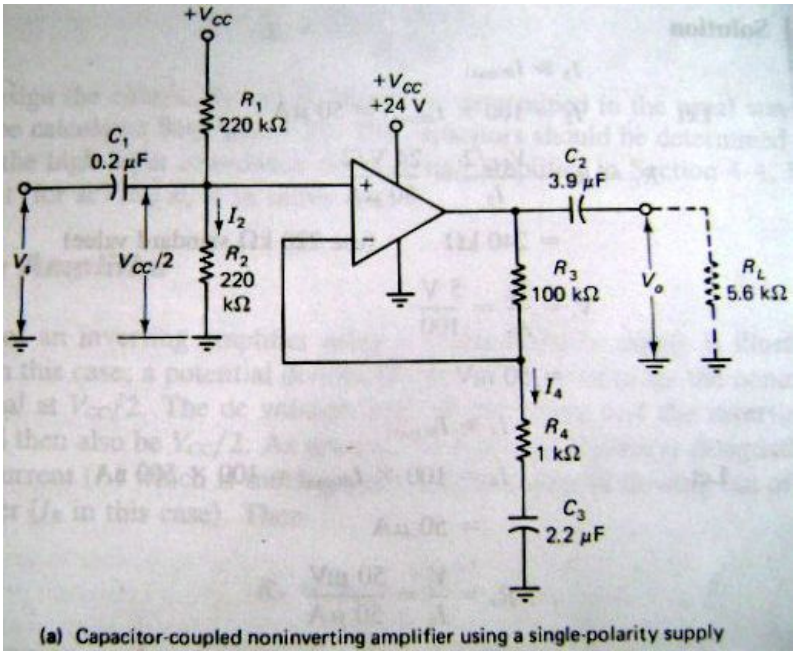
Potential divider R_1 and R_2 again serve to set the bias voltage at approximately$Vcc/2$. Resistor R_3 is now included so that its bottom end may be pushed up and down by feedback via C_2 and thus offer an input impedance of (1+A) R_3. In this circuit, the resistance in series with C_2 is$R_1 \parallel R_2$because the top of R_1 is AC

grounded viaVcc. So, C_2 is calculated from

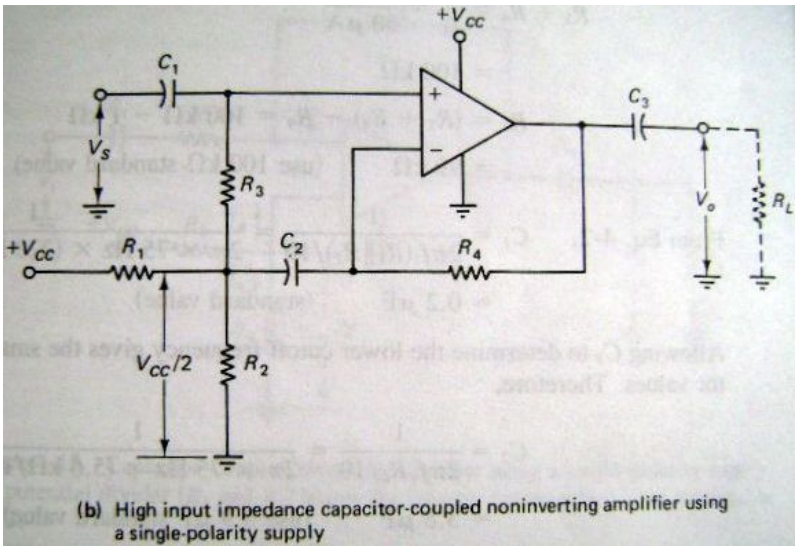
$$X_{C2} = \frac{R_1 \parallel R_2}{10} at f_1$$

Non-inverting amplifier

Figure (a) shows the circuit of a capacitor coupled non-inverting amplifier using a single polarity supply. Here again, the potential divider constituted by R_1 and R_2 biases the op-amp non-inverting input terminal at$Vcc/2$. The bottom of resistor R_4 is capacitor coupled to ground via capacitor C_3. If this point was directly grounded, the DC voltage at the op-amp output terminal would tend towards A_v × (bias level at the non-inverting input), or$A_v \times Vcc/2$. This would saturate the output at approximately$Vcc - 1V$. With C_3 in the circuit as shown, and R_3 connecting the inverting input terminal to the op-amp, the op-amp behaves as DC amplifier. The DC voltage level at the op-amp output terminal is the same as that at the non-inverting terminal ($Vcc/2$). For AC voltages, C_3 behaves as a short circuit, so that the AC voltage gain is $(R_3 + R_4)/R_4$.



(a) Capacitor-coupled noninverting amplifier using a single-polarity supply



(b) High input impedance capacitor-coupled noninverting amplifier using a single-polarity supply

ComponentsC$_1$, C$_2$, R$_1$ and R$_2$ are calculated exactly as for the voltage follower discussed above, and R$_3$ and R$_4$ are determined in the usual way for a non-inverting amplifier. Capacitor C$_3$ should be selected to have impedance very much smaller than R$_4$ at the low 3dB frequency of the circuit. As usual, let$X_{C3} = \frac{R_4}{10} at f_1$. An alternative is to have C$_3$ determined at lower cutoff frequency for the circuit. This might be desirable for a circuit that has a variable load. In this case$X_{C3} = R_4 at f_1, and X_{C2} = R_{L(min)} / 10\, at f_1$.

Example 3:

A capacitor coupled non-inverting amplifier is to have +24V supply, a voltage gain of 100, an output amplitude of 5V, a lower cutoff frequency of 75Hz, a minimum load resistance of 5.6 kΩ. Using a 741 op-amp, design a suitable circuit

Solution

$I_2 \gg I_{B\,(max)}$

$Let I_2 = 100 \times I_{B\,(max)} = 50\ \mu A$

$$R_1 = R_2 = \frac{\frac{V_{cc}}{2}}{I_2} = \frac{\frac{24}{2}}{50\mu}$$

$= 240\ k\Omega$

$$V_i = \frac{V_o}{A_v} = \frac{5}{100}$$

$= 50\ mV$

$I_4 \gg I_{B\,(max)}$

$Let I_2 = 100 \times I_{B\,(max)} = 50\ \mu A$

$$R_4 = \frac{V_i}{I_4} = \frac{50m}{50\mu}$$

$= 1\ k\Omega$

$$R_3 + R_4 = \frac{V_o}{I_4} = \frac{5}{50\mu}$$

$= 100\ k\Omega$

$R_3 = (R_3 + R_4) - R_4 = 100 - 1$

$= 99\ k\Omega$

$$Also, \quad C_1 = \frac{1}{2\pi f_1 \left(\frac{R_i || R_2}{10}\right)} = \frac{1}{2\pi \times 75 \times \left(\frac{220k || 220k}{10}\right)}$$

$\approx 0.2\ \mu F$

Allowing C_3 to determine the lower cutoff frequency gives the smallest possible capacitance value. Therefore,

$$C_2 = \frac{1}{2\pi f_1 \left(\frac{R_L}{10}\right)} = \frac{1}{2\pi \times 75 \times \left(\frac{5.6k}{10}\right)}$$

$\approx 3.8\ \mu F$

$$C_3 = \frac{1}{2\pi f_1 R_4} = \frac{1}{2\pi \times 75 \times 1k}$$

$\approx 2.12\ \mu F$

The high input impedance non-inverting amplifier with a single polarity supply in figure 4-14(b) is very similar to the high input impedance voltage follower in figure 4-13(b). The difference is that the resistor R_4 is included in the non-inverting amplifier circuit to give a voltage gain greater than 1. The voltage gain is

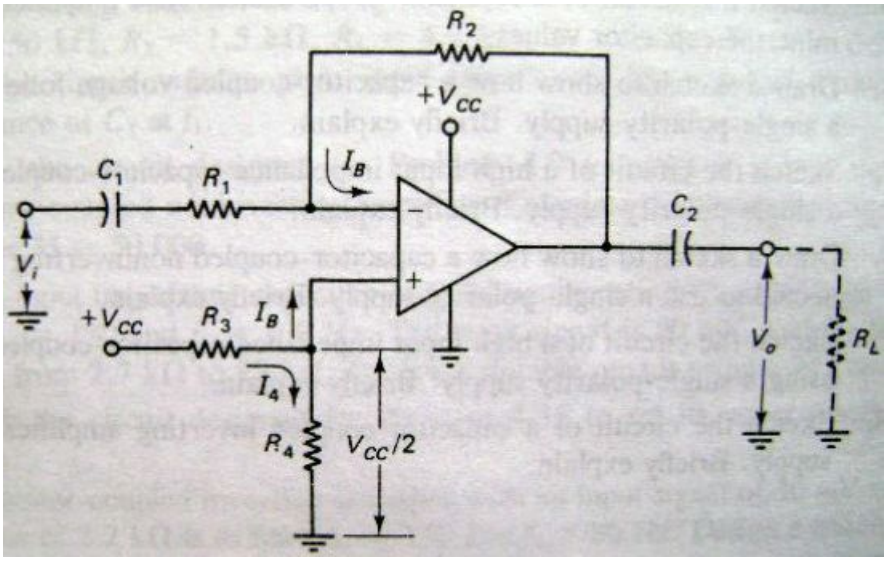
$$A_v = \frac{R_4 + (R_1 \parallel R_2)}{R_1 \parallel R_2}$$

To design the circuit, R_1 and R_2 should be determined in the usual way. Then R_4 should be calculated from equation 4-10. The capacitors should be determined as discussed for the high input impedance non-inverting amplifier in Section 4-4, bearing in mind that (for ac) $R_1 \| R_2$ is in series with C_2.

Inverting amplifier

The circuit of an inverting amplifier using a single-polarity supply is illustrated in the figure. In this case, a potential divider (R_3 and R_4) is used to set the non-inverting input terminal at $Vcc/2$. The dc voltage level of the output and the inverting input terminal will the also be $Vcc/2$. As always, the potential divider is designed by first selecting a current (I_4) which is much greater than the current flowing out of the potential divider (I_B in this case). Then

$$R_3 = R_4 = \frac{\frac{V_{cc}}{2}}{I_4}$$



Other components are determined as discussed as before.

UNIT 3

OP-AMP FREQUENCY RESPONSE AND COMPENSATION

CIRCUIT STABILITY:

When the op-amp is used in a circuit for amplification purposes(only ac),we should check whether the output ac signal is a small signal(below 1v peak) or large signal (above 1v peak).If only small ac output signals are present, the important op-amp characteristics that limit it's performance are noise and frequency response. If large ac signals are expected, the characteristics that would add to above told characteristics are slew rate limitation that would again distort the signal

EFFECT OF OPEN LOOP GAIN ON CLOSED LOOP GAIN OF AN AMPLIFIER.

Ideal closed loop gain of the amplifier is defined as that gain which is determined only by the external resistors. However the actual closed loop gain of the amplifier is determined both by the open loop gain of the op-amp and the external resistors. It is given by
Actual AcL=(Rf+Ri)/Ri/(1+(Rf+Ri)/AoLRi)).

Frequency and Phase response:

Most op-amps are internally frequency compensated and have an open-loop frequency response with a 20 dB/decade roll-off. A response of this kind, in principle, ensures that the op-amp will be closed-loop stable under all conditions of resistive feedback. However, it is important to be aware that the use of an internally frequency compensated op-amp does not always ensure closed-loop stability.

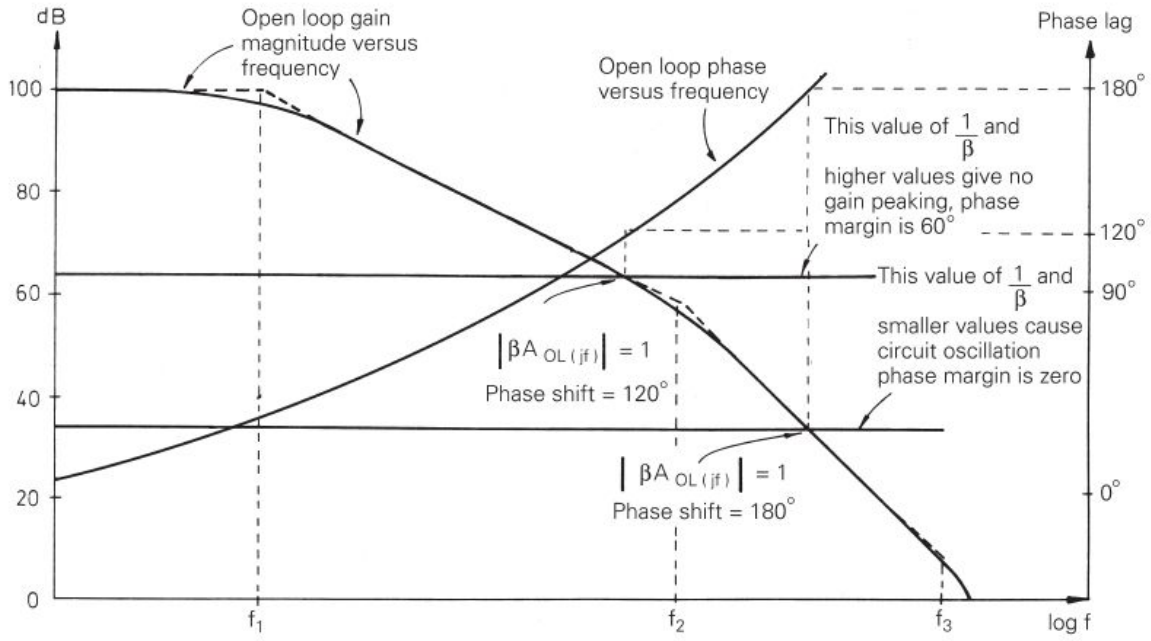
Capacitive loading at the output of an op-amp, or stray capacitance between the inverting input terminal and earth, can cause phase shifts leading to instability – even in resistive feedback circuits. In differentiator applications, in which the feedback fraction _ is deliberately made frequency dependent, an internally compensated op-amp exhibits instability.

Some op-amps exhibit a final roll-off in their open-loop frequency response of greater than 20 dB/decade; they are called externally frequency compensated op-amps. These fast roll-off op-amps are often used in circuits where both wide closed-loop bandwidth and greater than unity gain are required. They require the external connection of a capacitor to make them closed-loop stable. The closed-loop frequency response obtained with fast roll-off (externally frequency compensated) op-amps can be explained using Bode plots.

The response is related to the gain error caused by the decaying open-loop gain

and the associated phase shift. For example, consider an op-amp with a response that has three gain stages, each stage having a frequency response with a different cut-off point. The magnitude and phase characteristics of the open-loop gain are illustrated in Figure The magnitude and phase characteristics of the loop gain for a particular feedback fraction are obtained by superimposing a plot of 1/_ on the open loop frequency response plot. With resistive feedback, _ is frequency independent. The phase shift in the closed-loop gain is determined by the phase shift in the open-loop gain; this can be found by referring back to the graphs in Figure

Phase margin is the amount by which this phase shift is less than 180¬at the frequency at which the magnitude of the loop gain is unity (0 dB). Note that increasing _ results in successively smaller phase margins. Phase margins less than 60¬cause the closed-loop gain to peak up The gain peaking increases as the phase margin is reduced further until, at zero phase margin, the circuit breaks out into sustained oscillations

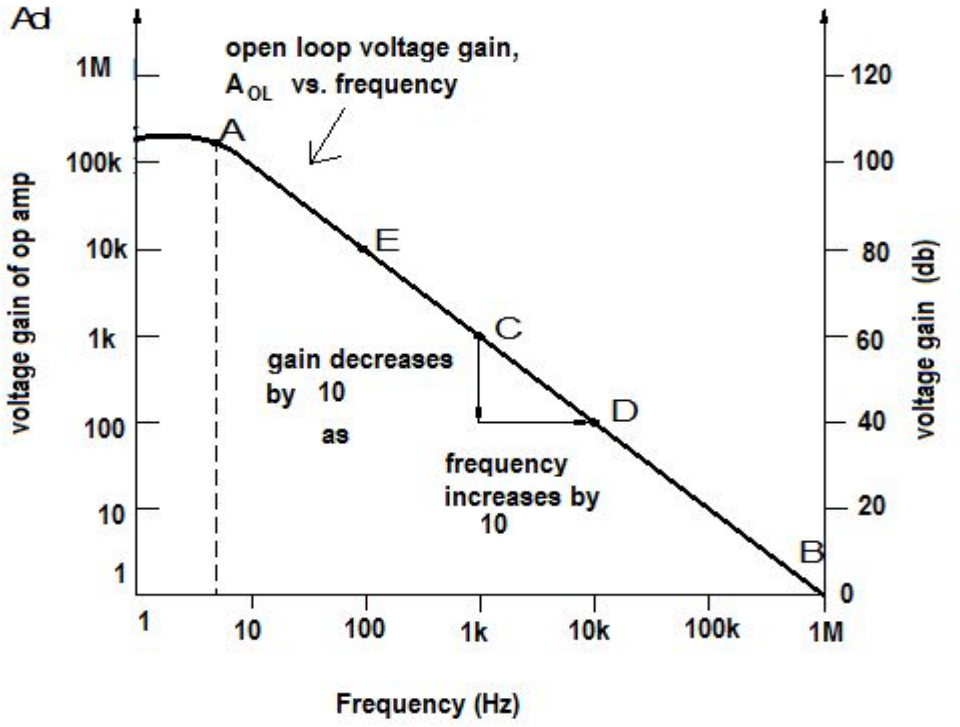


Gain magnitude and phase characteristics of op-amp with three-pole response

FREQUENCY RESPONSE OF THE OP-AMP:
INTERNAL FREQUENCY COMPENSATION.

Most of the general purpose op-amps are internally compensated by using a capacitor of the order of 30pF.The internal compensation helps in preventing the op-amp oscillating at higher frequencies. Otherwise at some higher frequencies if barkhaussean criteria is satisfied ,the op-amp may go to oscillating state. Thus op-amp is prevented from going in to oscillating state.

The typical frequency response of an internally compensated would be as shown above. Since the reactance of the capacitor=1/(2*pi*f*c),as the frequency increases by 10,the capacitor reactance decreases by 10.A change in frequency of 10 is called decade.In the above plot,A represents the break frequency at which the gain of the op-amp is 0.707 times the gain at the lower frequencies. Points C and D shows how gain decreases by 10 as the frequency increases by 10.Thus to express the slope of the response usually we use the term per decade. The right hand vertical axis in the plot shows the value of the gain in dB. The voltage gain decreases by 20 dB for every 1 decade increases in frequency, thus we say that the response is rolling off at 20dB/decade.



Frequency compensating methods:

Lead compensation and lead compensation:

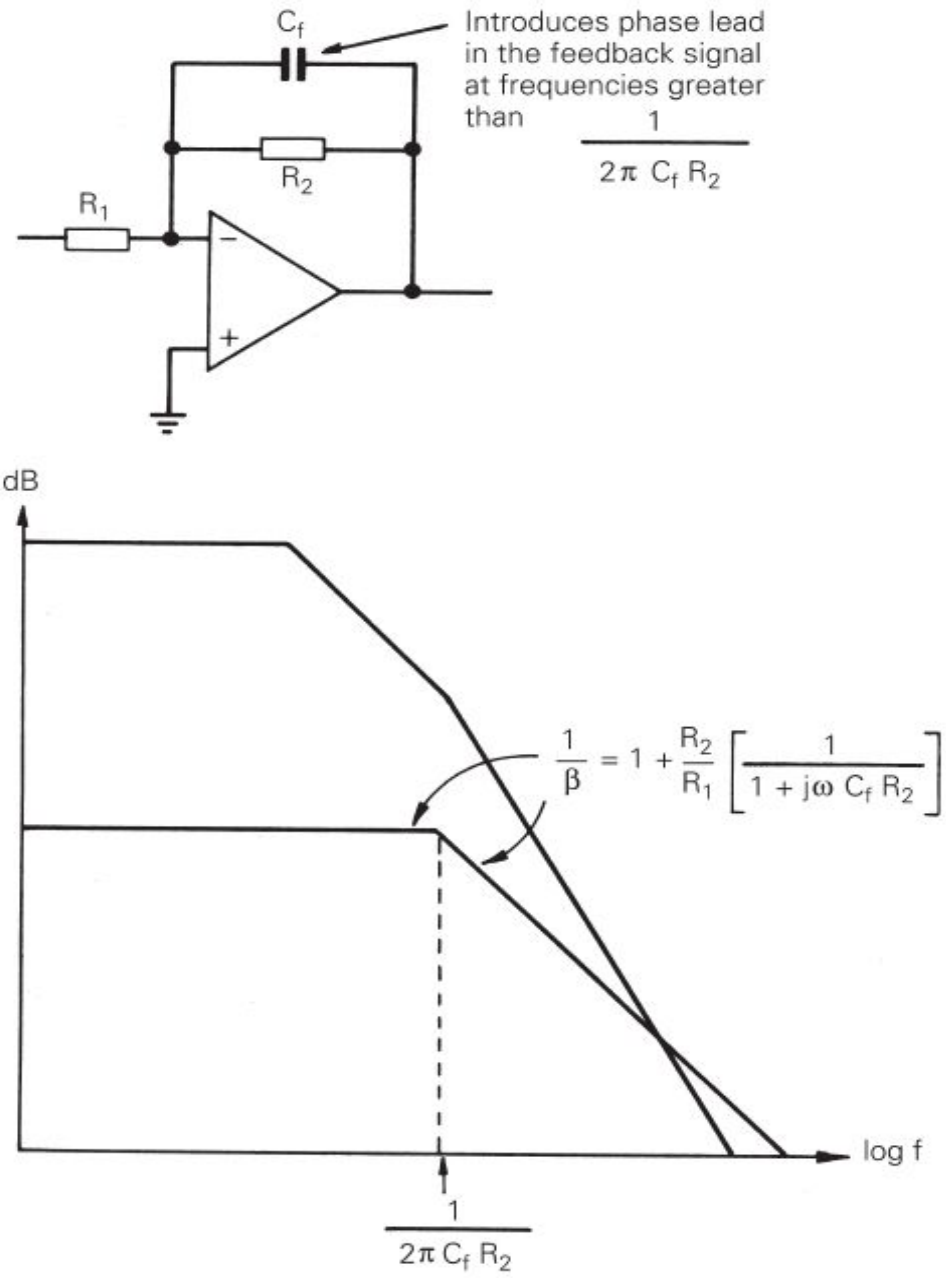
Lead frequency compensation is a technique used to increase the phase margin. A capacitor is included in a feedback loop to introduce a phase lead, compensating for the op-amp phase lag,

which would otherwise result in insufficient phase margin. A simple way of achieving this is to connect a capacitor *C*f in parallel with the feedback resistance. A circuit using this method of lead compensation is shown, together with its associated Bode plots, in Figure

We write

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1}\left(\frac{1}{1 + j\omega C_f R_2}\right) = \left[1 + \frac{R_2}{R_1}\right] 1 + \frac{1 + j\omega C_f (R_1 // R_2)}{1 + j\omega C_f R_2}$$

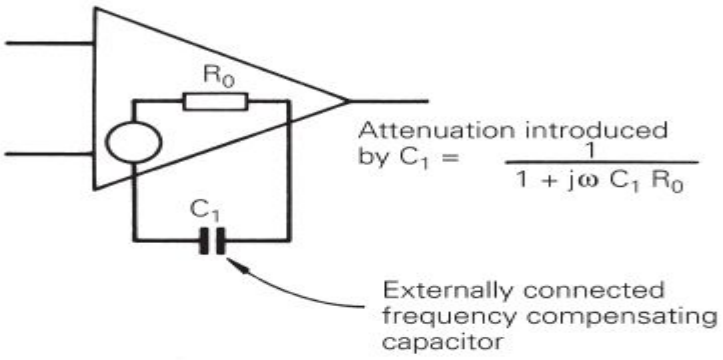
At frequencies greater than 1/2 *CfR*2 the capacitor introduces a phase lead in the feedback fraction, which approaches 90π. If *C*f is chosen so that the frequency 1/2 *CfR*2 is a decade below the frequency at which the 1/_ and open-loop response plots intersect, a phase margin of approximately 90π is obtained. Use of a lead capacitor in parallel with a feedback resistor is a convenient way of getting extra phase margin. It is also a technique that can be used to overcome the effect of stray capacitance between the op-amp's inverting input and earth .

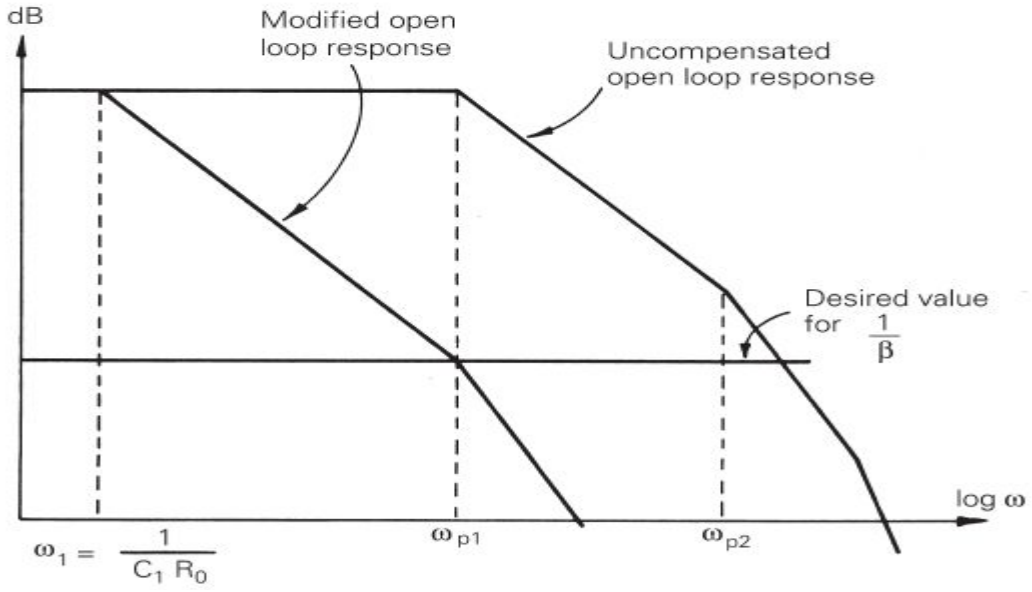


Lead compensation

Shunting a signal point with a capacitor resistor combination (a lag network) is an alternative technique that allows wider closed-loop bandwidths . At frequencies above 1/2 *C*1*R*1 (the break-back frequency) a network of this kind produces an attenuation *R*1/(*R*1 _ *R*o) but the phase shift returns to zero.

Previous sections have been concerned with factors influencing the small signal frequency response characteristics of op-amp feedback circuits. Attention is now directed to the factors influencing their behaviour in time, namely their transient behaviour in response to large and small input step or square-wave signals. Students may gain a greater understanding of op-amp transient behaviour, and the terminology used to describe it, by performing transient tests. Frequency compensating component magnitude, load capacitance, input capacitance and any stray feedback capacitance all influence closed-loop transient behaviour.





Simple lag compensation with single capacitor

UNITY GAIN BANDWIDTH.

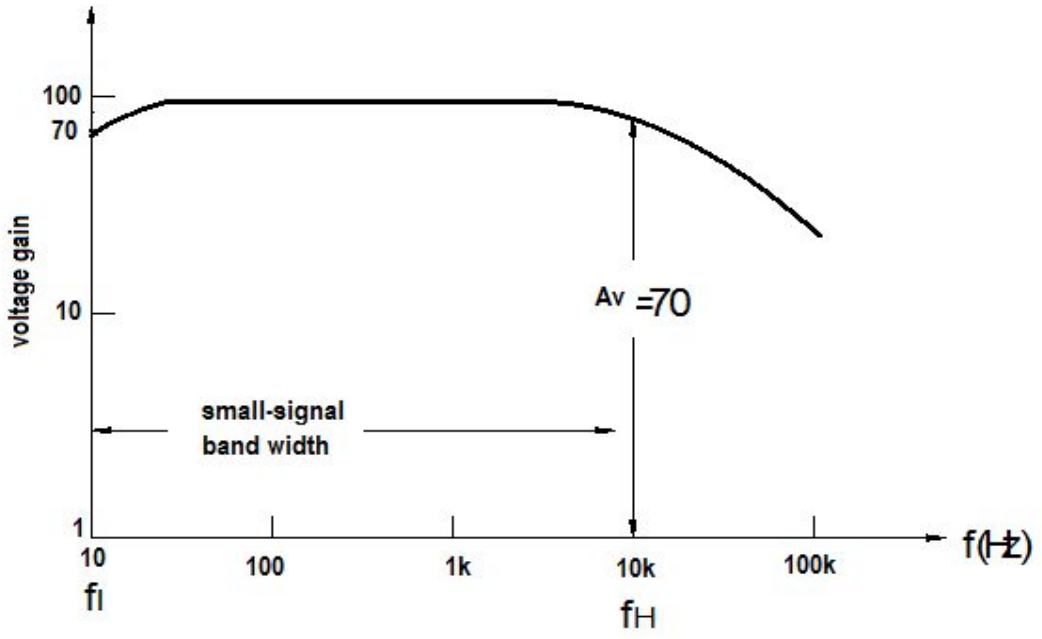
When we design amplifier circuits using op-amp and all, the frequency response does not depend upon the frequency response of the op-amp, instead it depends on the key characteristic i.e., the frequency at which the gain of the op-amp becomes unity. In the above figure point B is used to

represent the frequency at which the gain becomes unity. The corresponding bandwidth is called small signal unity gain bandwidth. It is usually denoted by B.
B can be easily calculated from the data sheet as B=0.35/(rise time),where the transient response time would be indicated in the data sheet prepared by the manufacturer.

RISE TIME

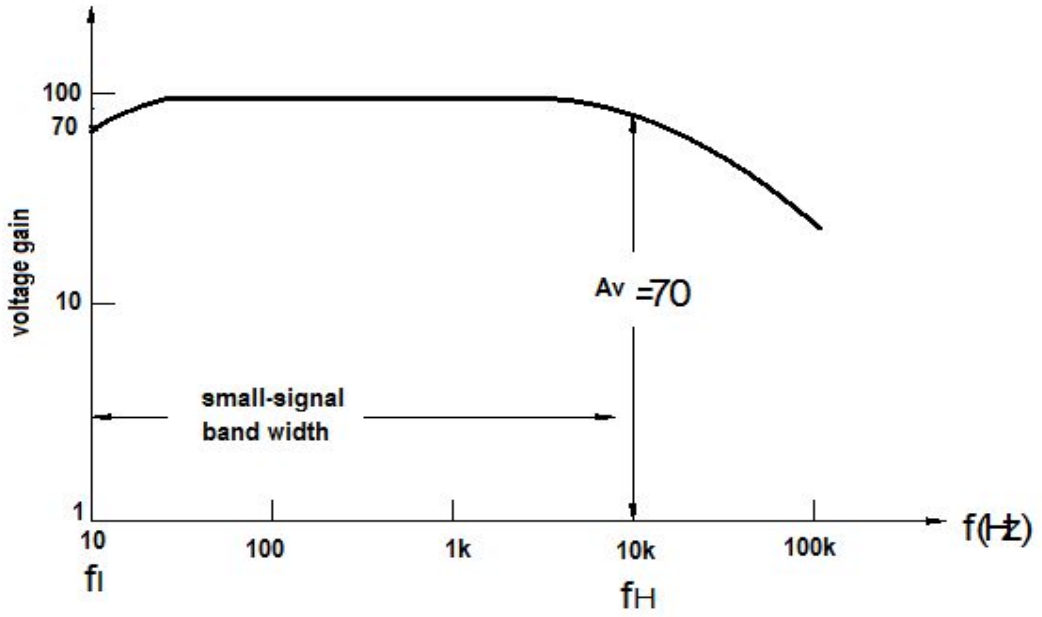
Rise time is defined as the time required by the output voltage to rise from 10% of it's final value to 90% of it's final value .e.g., Rise time is 0.35 ms would imply the output takes 0.35ms to rise it's value from 10% of it's final value to 90% of it's final value.

SMALL SIGNAL BANDWIDTH ,LOW AND HIGH FREQUENCY LIMITS



The useful frequency range of any amplifier is defined by a high frequency limit(fh) and a low frequency limit fL.AtfL and fh, the voltage gain is 0.707 times its maximum value in the middle of the useful frequency range. In terms of decibels, the voltage gain is 3dB at both fL and fh. Same thing is shown graphically in the above figure.

Small signal bandwidth is the difference between fLanffH. Usually for a dc amplifier, fL will be very less. So we can approximate the small signal bandwidth as fH.
Band width=fF-fL.
fH=B/((R1+Rf)/R1)



SLEW RATE

Slew rate of the op-amp gives us an idea of how fast the output of an op amp change .For example,if the slew rate is 0.2V/s which implies that the output of the op amp can change maximum by 0.2 volts for 1s.The specification depends on the amplifier gain,compensating capacitors,and even whether the output voltage is going positive or negative.It is usually specified at unity gain.

Usually there will be a capacitor connected required to prevent op amp going in to oscillation mode.The ratio of the maximum current to the corresponding capacitor C is termed as the slew rate.

Slew rate=(output voltage change)/(time).
If the output is changing at a rate greater than slew rate, output will be distorted. The maximum frequency for which output is undistorted is fmax=SR/(6.28 Vop).op-amps with more slew rate specification is termed as high speed operational amplifiers.

UNIT-4
OP-AMP APPLICATIONS

Instrumentation Amplifier:

Another differential amplifier configuration that is often used is shown in Figure This circuit has two stages: a differential input stage and a subtractor stage. The differential input stage presents high impedance to both inputs. Two coupled non-inverting amplifiers form the differential input stage. This stage produces a differential output voltage in response to a differential input signal. Assuming that the op-amps in the input stage take no current at their input terminals, the same current must flow through the three resistors (labelled$R1$ and $R2$). If we make the further usual assumption of negligible voltage between op-amp input terminals then this current

$$I = \frac{e_{o_1} - e_1}{R_2} = \frac{e_1 - e_2}{R_1} = \frac{e_2 - e_{o_2}}{R_2}$$

$$\text{Thus } e_{o_1} = \left(1 + \frac{R_2}{R_1}\right) e_1 - \frac{R_2}{R_1} e_2$$

$$\text{And } e_{o_2} = \left(1 + \frac{R_2}{R_1}\right) e_2 - \frac{R_2}{R_1} e_1$$

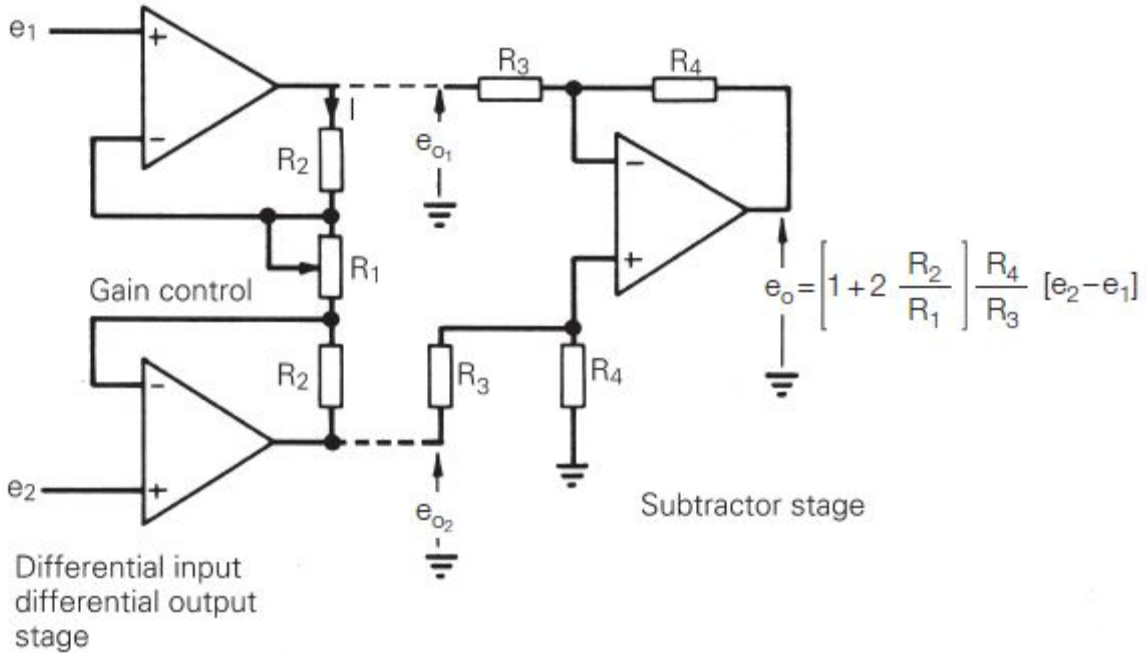
The input stage has a differential output, given by:

$$(e_{o_1} - e_{o_2}) = (e_1 - e_2)\left[1 + 2\frac{R_2}{R_1}\right]$$

Note that if $e1$ _ $e2$ _ $e$cm then eo1 _ eo2 _ $e$cm. The input stage passescommon mode input signals at unity gain. If the input stage used separatelyconnected follower circuits, these would pass both common mode *and* differentialsignals at the same gain. The advantage of a cross-connected differentialinput stage, which is configured to provide some voltage gain, is that itamplifies differential input signals but not common mode signals.An isolated load, such as a meter, can be driven directly by the differentialoutput from the input stage. This has atheoretically infinite CMRRunaffected by resistor tolerance and the possibility of gain setting by meansof a single resistor value ($R1$). In practice CMRR is not infinite, because ofdifferences in the internal common mode errors of the two op-amps. Dualop-amps can be used in this type of circuit, with the possibility of drift errorcancellation (if the temperature drift coefficient on the two op-amps matchesand tracks).

Monolithic dual op-amps have the advantage of maintaining both op-ampsat the same temperature. However, despite the monolithic construction, theop-amp parameters are not matched. Improved performance can be obtainedby using dual op-amp devices in which two

separately matched op-amp chipsare assembled into a single dual-in-line package.To drive an earth-referred load, a single ended output is required. Thedifferential output produced by the cross-coupled followers can be convertedinto a single ended output by using the differential amplifier circuit of Figure, which uses a single op-amp. The overall CMRR obtained with a circuitthat uses three op-amps is greater than that of the single op-amp circuit, bya factor equal to the differential gain of the input stage.The resistor values in the single op-amp circuit should be well matched,to give good common mode rejection. The input common mode range ofthe circuits of Figures is limited to that of the op-amps used inthe circuits. A differential input circuit configuration using two invertingamplifiers can be given a larger inputcommon mode range but with the disadvantage of lower input resistance inthe inverter configuration.In the presence of large or potentially dangerous common mode signals,consideration should be given to the use of an isolation amplifier.



Instrumentation Amplifier

Precision Rectifiers

Introduction to precision rectifiers The limitation of ordinary silicon diodes is that they cannot rectify voltages below 06V They can be grouped loosely into the following classifications They are

 Linear half-wave rectifiers The linear half-wave rectifiers circuit delivers an output that depends on the magnitude and polarity of the input voltageThe linear half-wave rectifier can be modified to perform a variety of signal processing applications The linear half-wave rectifier is also called *precision half-wave rectifier* and acts as an ideal diode

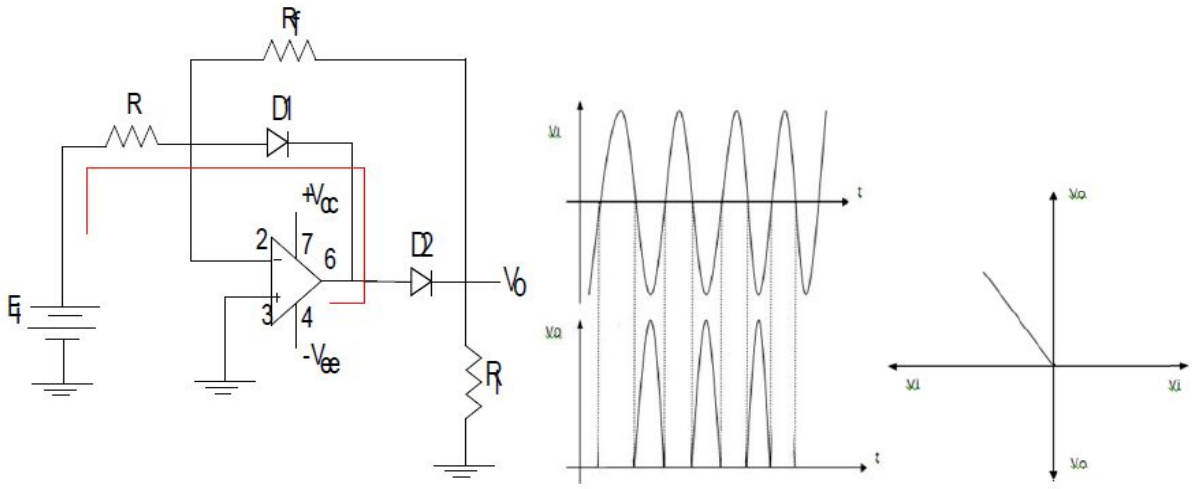
Precision full-wave rectifiers

The precision full-wave rectifier delivers an output proportional to the magnitude, but not the polarity of the input The precision full-wave rectifier is also called an absolute-value circuit Application of both linear half-wave and precision full-wave rectifiers

- Detection of amplitude modulated signals
- Dead-zone circuits
- Precision bound circuits of *clippers*
- Current switches
- Wave shapers
- Peak-value indicators
- Sample-and-hold circuits
- Absolute-value circuits
- Averaging circuits

- Signal polarity detectors
- Ac- to- dc converters

Linear half-wave rectifier *Inverting linear half-wave rectifier, positive output* The inverting amplifier is converted into an ideal half wave rectifier by adding 2 diodes as shown in fig a When Ei is positive in fig a , diode D1 conducts, causing the 0p amp's output voltage, VOA, to go negative by one diode drop 0 6V This forces diode D2 to be reverse biased The circuit's output voltage VO equals zero because input current I flows through D1 For all practical purposes, no current flows through Rf and therefore VO 0

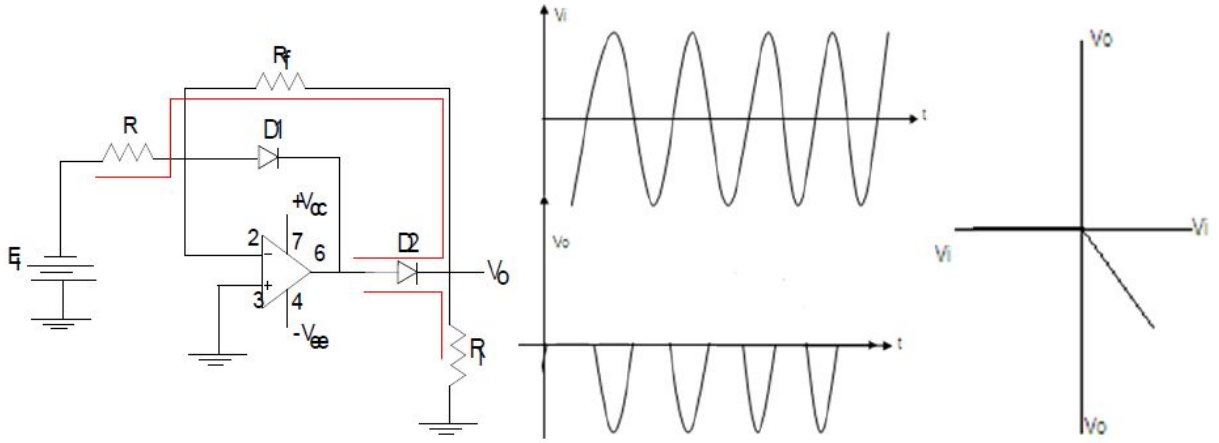


Note the load is modeled by a resistor RL and must always be resistive. If the load is a capacitor, inductor, voltage, or current source, then Vo will not equal zero

In fig (b), negative input Ei forces the op amp output VoA to go to positive. This causes D2 to conduct. The circuit then acts like an inverter, since Rf = Ri and Vo = (Ei) = +Ei. Since the ( ) input is at ground potential, diode D1 is

reverse biased Input current is set by EiRi and gain by -- RfRi This gain equation applies only for negative input, and VO can only be positive or zero Finally observe the wave shapes of op amp output VOA in fig c When Ei crosses 0V going negative , VOA jumps quickly from -0 6V to 0 6V as it switches from supplying the drop for D2 to supplying the drop for D1 This jump can be monitored by a differentiator to indicate the zero crossing During the jump time the op amp operates open loop

Inverting linear half wave rectifier, negative output The diodes in the fig a can be reversed as shown in fig 1 Now only positive input signals are transmitted and inverted The output voltage Vo equals 0V for all negative input Circuit operation is summarized by the plot of Vo and VOA verses Ei in graph below

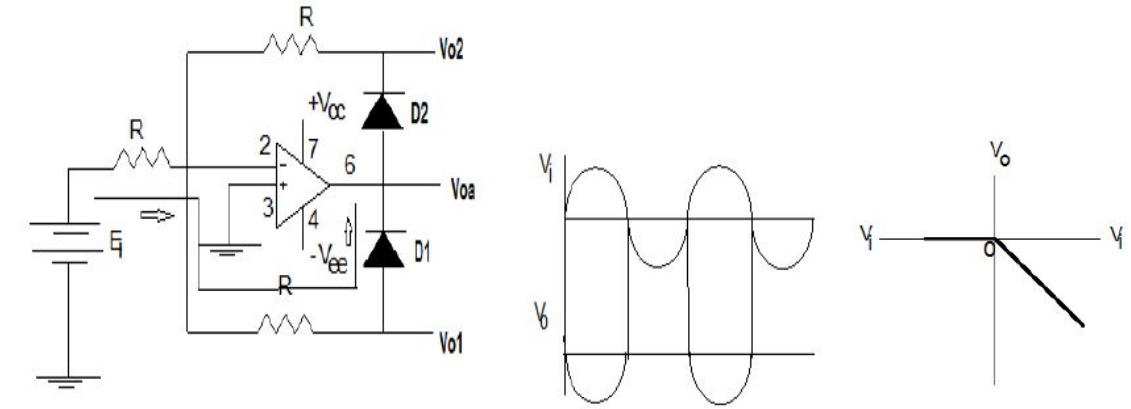


Signal polarity separator

The circuit diagram is the expansion of the circuit given in fig a and fig 1 When the input Ei is positive then the diode D1 conducts and diode D2 is reversed biased so it's open, the current flows through D1 via resistor R The circuit acts as the inverting circuit therefore the output voltage is same as that of the voltage across the feedback resistorBut as there is a diode in the path there will be a drop across it as well therefore the output voltage will be the sum of the drop across the resistor and the diode with a negative sign due to inverting circuitIeVoEi 06 When the

input voltage Ei isnegative diode D2 conducts and the diode D1 is reversed biased thus openIn the similar way output will be VoEi 06

A)



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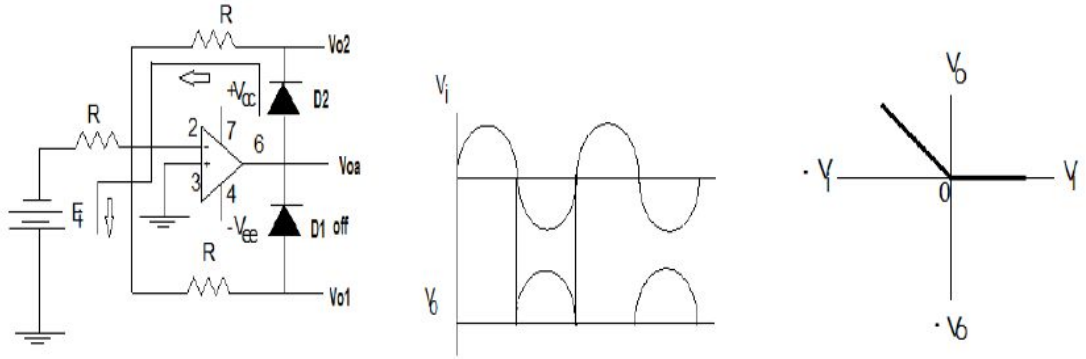


Precision rectifierThe absolute value circuit

The precision full wave rectifier transmits one polarity of the input signal and inverts the otherIt can rectify input voltages with millivolt amplitudeThe precision rectifier is also called an absolute value circuitThe absolute value of a number is equal to its magnitude regardless of its sign

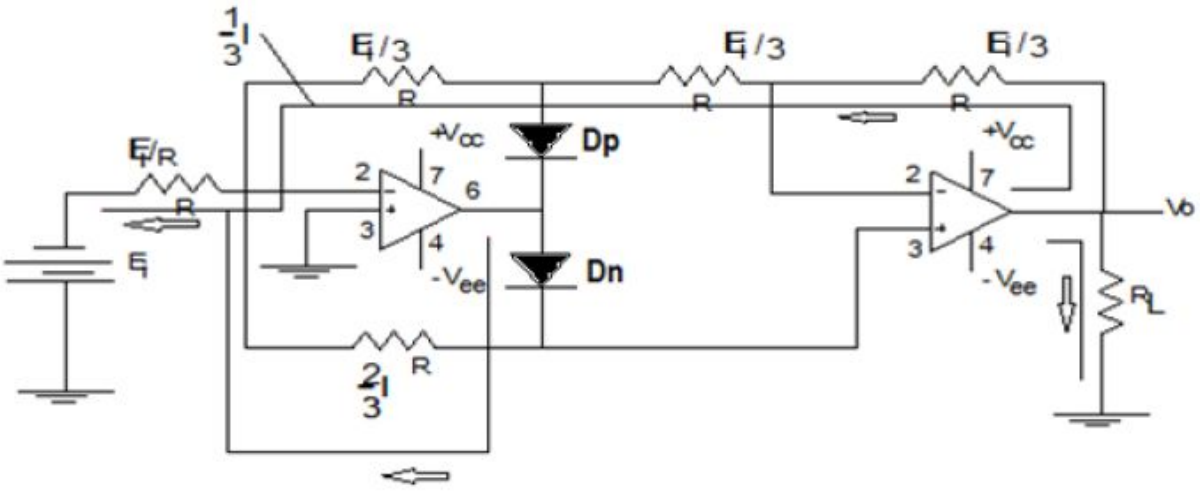
Types of precision full wave rectifier

There are 3 typesThe 1st is inexpensive because it uses 2 op amps, two diodes, and 5 equal resistorsUnfortunately, it does not have high input resistance, so a second type is given that does have high input resistance but requires resistors that are precisely proportional but not all

equalNeither type has a summing node at virtual ground potential, 3rd type is using a summing amplifier

Full wave precision rectifier with equal resistors

The circuit uses equal resistors and has an input resistance equal to RThe circuit shows the current directionFor positiveinput the diode Dp conducts and the diode DN is offDue to VG the pin 2 is at ground so the voltage across the resistor R is EiThe same current which flows through input resistor R flows through the feedback resistor as well, therefore the voltage is also same Ei but due to the inverting terminal the output of 1st op amp is –EiAgain the second op amp acts as an inverting amplifier so the output will be – -Ei, ieVOEi For Einegative input, D1 is off and D2 is on R1 is connected bw inverting input and the supply R2 and R3 are series because D1 is offThis series R2 R3combination is bw the inverting input of A1 and inverting input A2R4 is connected bw input of A1 and VOAVOA is connected to input of A2 due to VS voltage V2 of A1 is same as VOA that means R1 R3||R4 Hence current through R1 I , the current through R2 R3I and current through R4 I KCL at V2 of A1 I *I*R1 R VOAcurrent through R4X R4 I X R4 But R4 R X R Ei VOA is connected to input of A2 hence A2 is like non inverting amplifier with Ei as input R2 and R3 are series because D1 is off EiVOEi



Voltage scaling and buffer amplifier:

The great attraction of all op-amp circuits lies in the ability to set a precise operation with a minimum number of precise components. In Figures, closed-loop gain is determined by simply selecting two resistor values. The accuracy of this gain depends almost entirely upon the resistor value tolerance. The inverting circuit in Figure(a) can be given any gain from zero upwards. The lower limit of the gain for the non-inverting circuit Figure (b) is unity. In both configurations, the practical upper limit to the gain depends on the requirement for maintaining an adequate loop gain, so as to minimize gain error .Also, closed-loop bandwidth decreases with increase in closed-loop gain. If high closed-loop gains are required, it is often better to connect two op-amp

circuits in cascade rather than to use a single op-amp circuit. Both inverting and non-inverting amplifier circuits feature low output impedance. This is a characteristic of negative voltage feedback .

The main performance difference between them, apart from signal inversion, lies in their input impedance. In the case of the inverter, resistor *R*1 loads the signal source driving the circuit. The non-inverting amplifier presents very high input impedance, which ensures negligible loading in most applications.

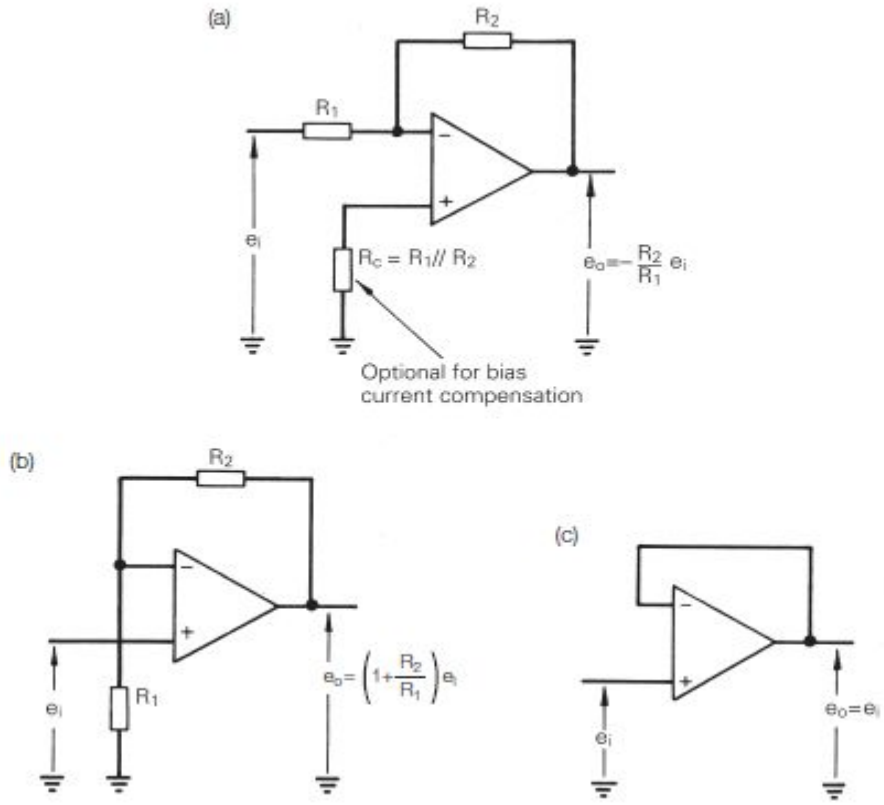
The main limitation of the inverting circuit is that its input impedance is effectively equal to the value of the input resistor *R*1. The application may require high input impedance, to minimize signal source loading. This demands a large value for the resistor *R*1 and an even larger value for *R*2, dependent upon the gain required. Large resistor values inevitably give increased offset errors due to op-amp bias current. Also, stray capacitance in parallel with a large feedback resistor limits bandwidth. For example, assume that it is required to use the inverting circuit with closed loop gain 100 and input resistance 1 M_. In Figure (a) *R*1 _ 1 M_ and *R*2 _ 100 M_ is required. Stray capacitance *C*s in parallel with *R*2 would limit the closed-loop bandwidth to a frequency *f* _ 1/(2_*C*s*R*2). With *C*s say 2 pF, the closed-loop bandwidth would be limited to 800 Hz – a severe restriction!

Stable very high value resistors are not freely available. If the inverting configuration must be used, the need for a very high value feedback resistor can be overcome by the use of a *T* resistance network as shown in Figure. This is at the expense of a reduction in loop gain and an increase in noise gain (1/_).

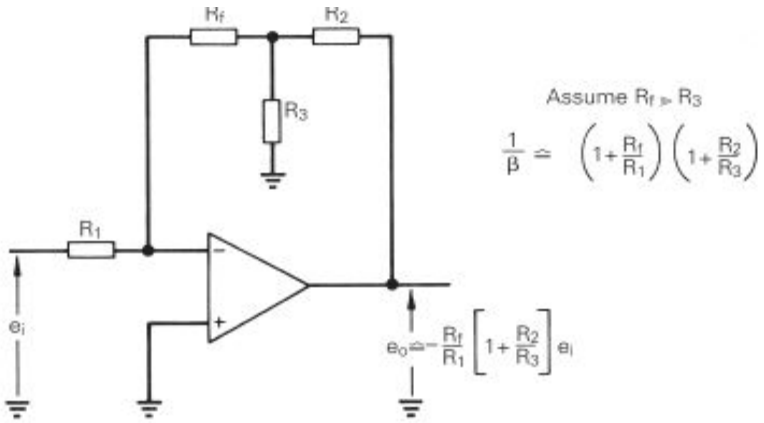
The non-inverting circuit achieves high input impedance without the use of large value resistors. This is an advantage in applications requiring wide bandwidth, since large value resistors and stray circuit capacitance interact to cause bandwidth limitations. The effective input impedance of the non inverting configuration was This was shown to be equal to the differential input impedance of the op-amp, multiplied by the loop gain in the circuit (*Z*in_*A*OL). Practical op-amps have their common mode input impedance *Z*cm between their non-inverting input terminal and earth. This shunts *Z*in_*A*OL and so reduces its value. The effective input impedance of the follower configuration is thus *Z*cm.

The high input impedance of the non-inverting circuit makes it a better choice than the inverting circuit for use in many applications. However, the non-inverting circuit is subject to common mode errors . Also, the voltage applied to the non-inverting input must not be allowed to exceed the maximum common mode voltage for the op-amp (since feedback will force both inputs to have the same potential). These points do not usually impose too serious a restriction.

The buffer circuit in Figure(c) has high input impedance and low output impedance. It is often used to prevent interaction between a signal source and load, e.g. for unloading potentiometers, or buffering voltage references. Buffers are used in Sallen and Key filter circuits to prevent interaction between filter stages and to allow simple design rules



Basic voltage scaling applications (a) Inverting amplifier. (b) Non-inverting amplifier. (c) Unity-gain follower (buffer)



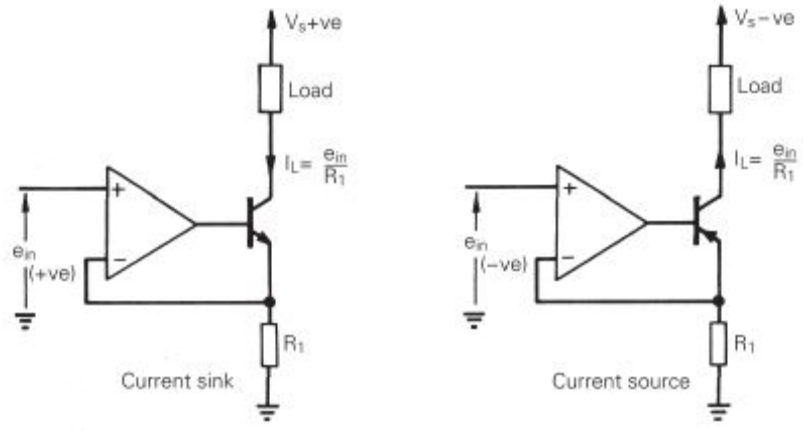
Inverter circuit using resistive T feedback network

CUEERNT SOURCES AND CURRENT SINKS:

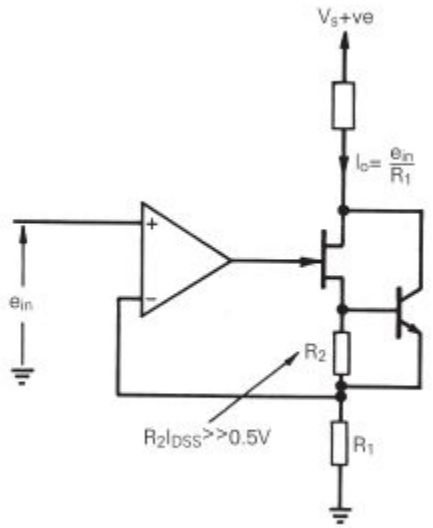
The voltage-to-current sources considered so far have provided a bi-directional output current. Unidirectional current sources can be formed using a simple circuit comprising a transistor, a resistor and an op-amp, as shown in Figure.

Resistor *R*1 is a current sensing resistor. Feedback around the op-amp forces the current through resistor *R*1 to take on a value such that *I*1*R*1 _ *e*in. The current *I*1 is the emitter current of the transistor, less the very small bias current of the op-amp. The collector current of the transistor, which is almost equal to its emitter current, forms the stable output current to the load. Output currents greater than the capability of the op-amp are possible, since the op-amp need only supply the output transistor's base current. A current limit is set by transistor saturation caused by the voltage that appears across the load. Departure from linearity in voltage-to-current conversion is likely at low current levels. This is because the gain of a bipolar transistor falls at low values of collector current. The linearity dependence on transistor current gain, exhibited by the current sources of Figure 4.20, can be overcome by using a FET in place of the bipolar transistor. However, output current is then limited to the *I*dss of the FET. The output current limit can be overcome by combining an n-channel FET and a bipolar npn transistor as shown in Figure.

In the circuit given in Figure , virtually all the current through the sensing resistor *R*1 flows as output current. The only error contributions being the very small gate leakage current and the op-amp bias current.



Current source and sinks



Precise current sink

PART-B

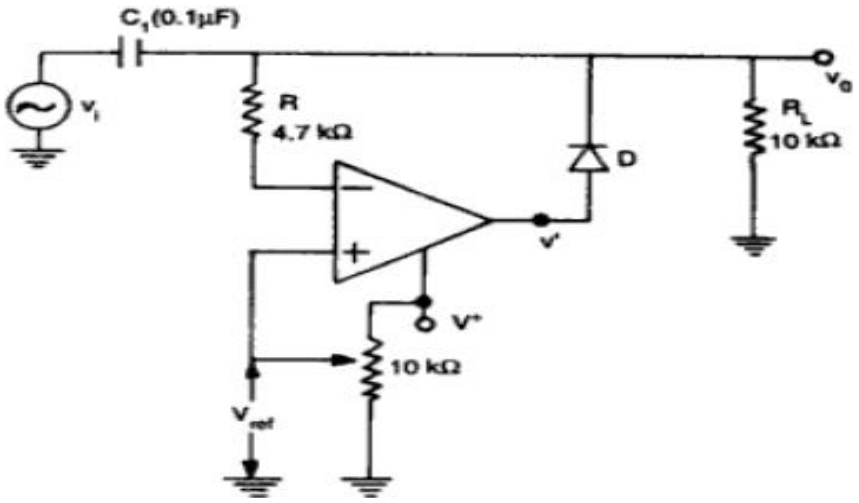
UNIT-5 MORE APPLICATIONS

5.1 Clamper

The clamper is also known as dc inserter or restorer. The circuit is used to add a desired dc level to the output voltage. In other words, the output is clamped to a desired dc level. If the clamped dc level is positive, it is called positive clamper. Similarly if the clamped dc level is negative, the clamper is called negative clamper.

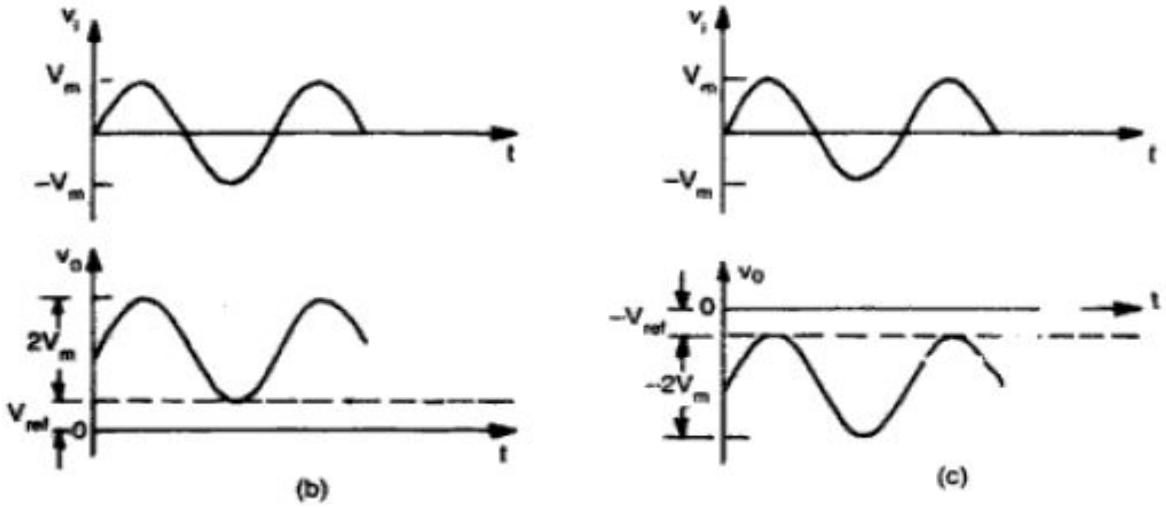
Figure 4.16 (a) shows a clamper with a variable positive dc voltage applied at the (+) input terminal. This circuit clamps the peaks of the input waveform and therefore is also called a peak clamper. The output voltage in the circuit is the net result of ac and dc input voltages applied to the (–) and (+) input terminals respectively. Let us first see the effect of V_{ref} applied at the (+) input terminal. For positive V_{ref}, the voltage v' is also positive, so that the diode D is forward biased. The circuit operates as a voltage follower and therefore output voltage $v_o = + V_{ref}$.

Now consider the ac input signal $v_i = V_m \sin \omega t$ applied at the (–) input terminal. During the negative half cycle of v_i, diode D conducts. The capacitor C_1 charges through diode D to the negative peak voltage V_m. However, during the positive half cycle of v_i, diode D is reverse biased. The capacitor retains its previous voltage V_m. Since this voltage V_m is in series with the ac input signal, the output voltage now will be $v_i + V_m$. The total output voltage is, therefore,



Peak clamper circuit

protecting the op-amp against excessive discharge currents from capacitor C_1 especially when the dc supply voltages are switched off.



5.2 Peak detector:

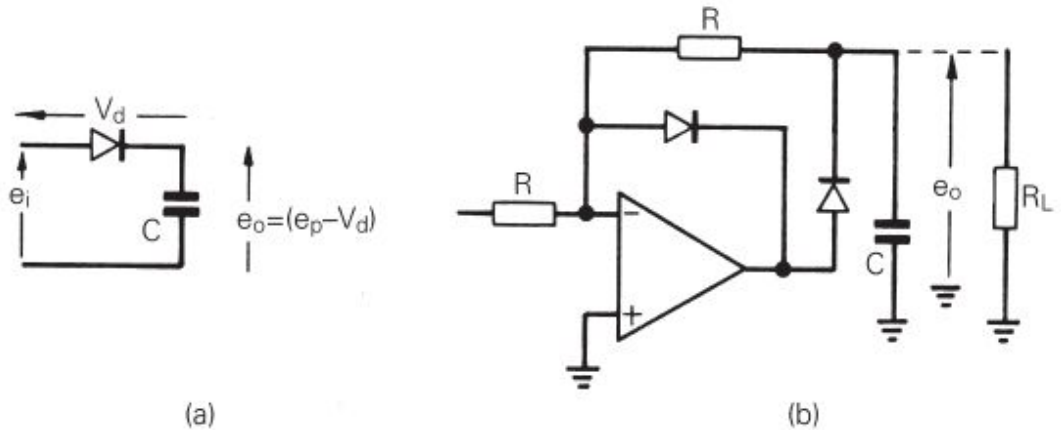
It is sometimes necessary to measure the maximum positive excursion (peak value) or negative excursion (valley value) of a waveform over a given time period. There may also be a requirement to capture and hold some maximum value of a positive or negative pulse. A circuit that performs this function is a peak detector.

A basic peak detector circuit consists of a diode and a capacitor connected as shown in Figure The capacitor is charged by the input signal through the diode. When the input signal falls, the diode is reverse biased and the capacitor voltage retains the peak value of the input signal. The

simple circuit has errors because of the diode forward voltage drop. Forward voltage drop errors can be removed by replacing the diode with a precise diode circuit as shown in Figure 8.

The circuit of Figure is useful in applications not requiring a long hold time, for example for measuring the peak value of a repetitive signal. In the hold mode, the voltage across the capacitor decays exponentially governed by the time constant

$$t = \frac{CRR_L}{R + R_L}$$

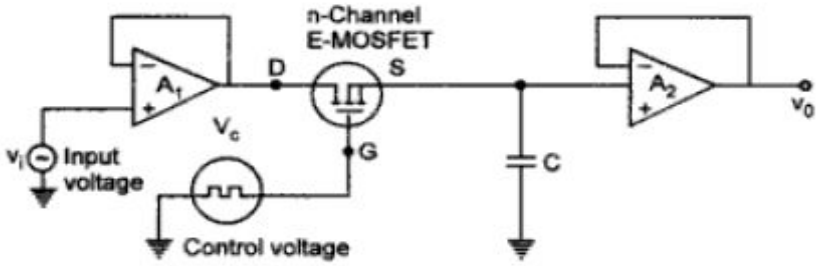


Peak detection. (a) Simple peak detector. (b) Precise diode peak detector

(b) Waveforms for + V_{ref} (c) Waveforms for – V_{ref}

5.3 SAMPLE AND HOLD CIRCUIT

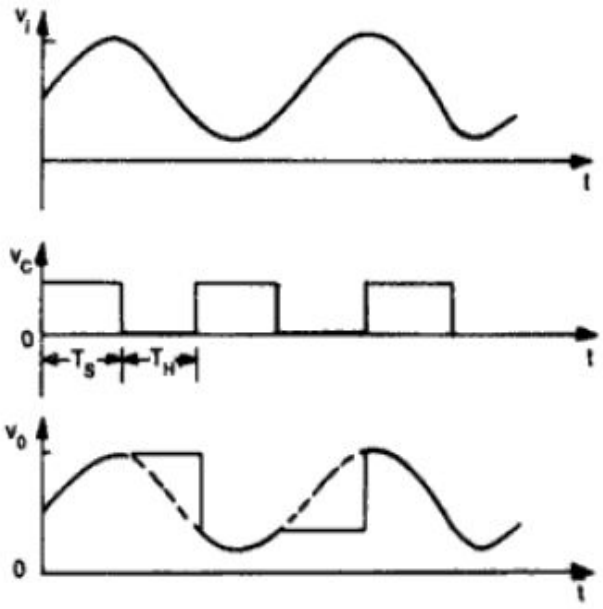
A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems. One of the simplest practical sample and hold circuit configuration is shown in Fig. 4.17 (a). The *n*-channel E-MOSFET works as a switch and is controlled by the control voltage v_c and the capacitor *C* stores the charge. The analog signal v_i to be



Sample and hold circuit

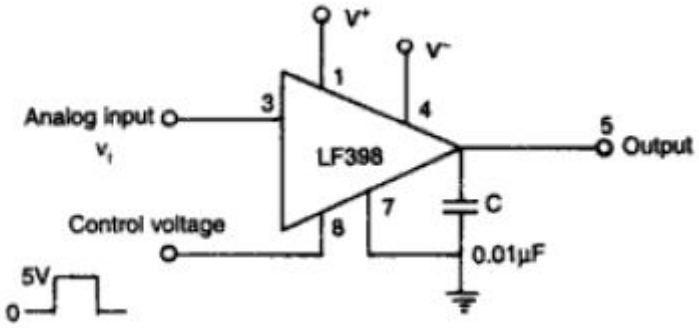
sampled is applied to the drain of E-MOSFET and the control voltage v_c is applied to its gate. When v_c is positive, the E-MOSFET turns ***on*** and the capacitor C charges to the instantaneous value of input v_i with a time constant $[(R_o + r_{DS}\ (on))]\ C$. Here R_o is the output resistance of the voltage follower A_1 and $r_{DS}\ (on)$ is the resistance of the MOSFET

when ***on***. Thus the input voltage v_i appears across the capacitor C and then at the output through the voltage follower A_2. The waveforms are as shown in Fig. 4.17 (b).



Input and output waveforms

During the time when control voltage v_c is zero, the E-MOSFET is *off*. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge. The capacitor holds the voltage across it. The time period T_S, the time during which voltage across the capacitor is equal to input voltage is called sample period. The time period T_H of v_c during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output waveform. A low leakage capacitor such as Polystyrene, Mylar, or Teflon should be used to retain the stored charge.



Typical connection diagram

Specially designed sample and hold ICs of make Harris semiconductor HA2420, National semiconductor such as LF198, LF398 are also available. A typical connection diagram of the LF398 is shown in Fig. 4.17 (c). It may be noted that the storage capacitor C is connected externally.

5.4 *V* TO *I* AND *I* TO *V* CONVERTER

Voltage to Current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuits possible.

V-I Converter with floating load
V-I Converter with grounded load

Figure 4.8 (a) shows a voltage to current converter in which load Z_L is floating. Since voltage at node 'a' is v_i, therefore,

$$v_i = i_L R_1 \qquad (\text{as } I_B^- = 0)$$

or,
$$i_L = \frac{v_i}{R_1}$$

That is the input voltage v_i is converted into an output current of v_i/R_1. It may be seen that the same current flows through the signal source and load and, therefore, signal source should be capable of providing this load current.

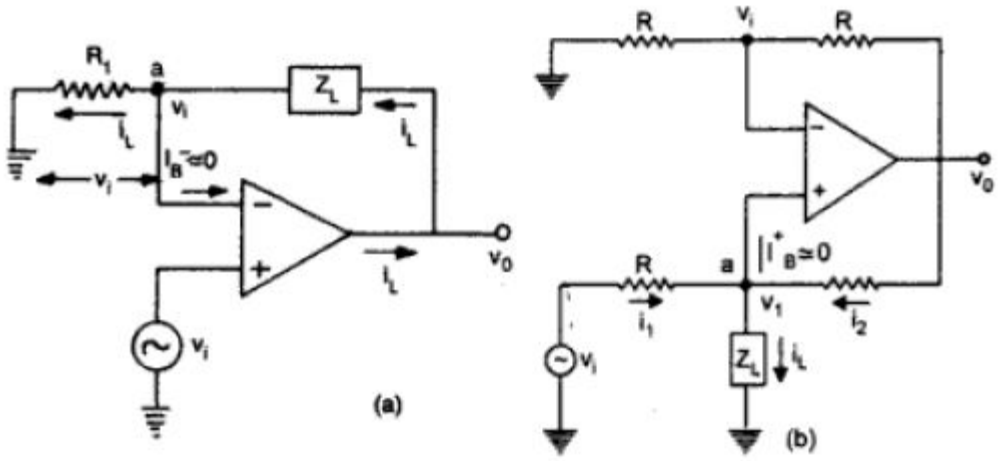
A voltage-to-current converter with grounded load is shown in Fig. 4.8 (b). Let v_1 be the voltage at node 'a'. Writing KVL, we get

$$i_1 + i_2 = i_L$$

or,
$$\frac{v_i - v_1}{R} + \frac{v_o - v_1}{R} = i_L$$

or,
$$v_i + v_o - 2v_1 = i_L R$$

Therefore,
$$v_1 = \frac{v_i + v_o - i_L R}{2}$$



Voltage to current converter with (a) floating load (b) grounded load

Since the op-amp is used in non-inverting mode, the gain of the circuit is $1 + R/R = 2$. The output voltage is,

$$v_o = 2\,v_1 = v_i + v_o - i_L R$$

that is, $$v_i = i_L R$$

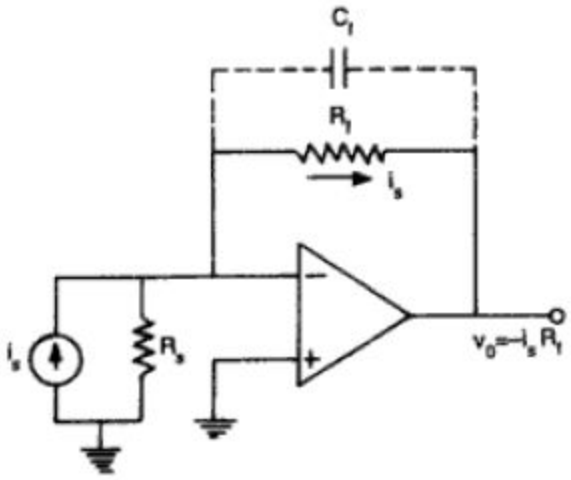
or, $$i_L = \frac{v_i}{R}$$

As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

Current to Voltage Converter (Transresistance Amplifier)

Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light or radiant energy incident on the photo-device can be measured.

Figure 4.9. shows an op-amp used as I to V converter. Since the (–) input terminal is at virtual ground, no current flows through R_s and current i_s flows through the feedback resistor R_f. Thus the output voltage $v_o = -i_s R_f$. It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current I_B of the op-amp. This means that μA741 (I_B = 3 nA) can be used to detect lower currents. The resistor R_f is sometimes shunted with a capacitor C_f to reduce high frequency noise and the possibility of oscillations.



Current to voltage converter

5.5 LOG AND ANTILOG AMPLIFIER

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or sinh x. These can be performed continuously with log-amps. One would like to have direct dB display on digital voltmeter and spectrum analyser. Log-amp can easily perform this function. Log-amp can also be used to compress the dynamic range of a signal.

Log Amplifier

The fundamental log-amp circuit is shown in Fig. 4.18 (a) where a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_s (e^{qV_E/kT} - 1)$$

Since, $I_C = I_E$ for a grounded base transistor,

$$I_C = I_s (e^{qV_E/kT} - 1)$$

I_s = emitter saturation current $\approx 10^{-13}$ A
k = Boltzmann's Constant
T = absolute temperature (in °K)

Therefore, $$\frac{I_C}{I_s} = (e^{qV_E/kT} - 1)$$

or, $$e^{qV_E/kT} = \frac{I_C}{I_s} + 1$$

$$\approx \frac{I_C}{I_s} \qquad [\text{as } I_s = 10^{-13} \text{ A}, I_C >> I_s]$$

Taking natural log on both sides, we get

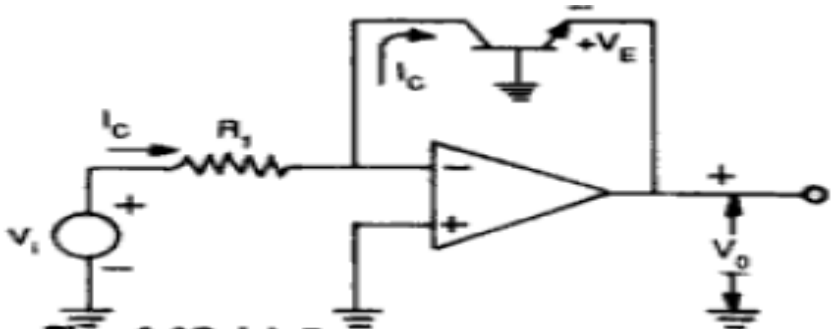
$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right)$$

Also in Fig. 4.18 (a), $I_C = \frac{V_i}{R_1}$

$$V_E = -V_o$$

so,
$$V_o = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

where
$$V_{ref} = R_1 I_s$$

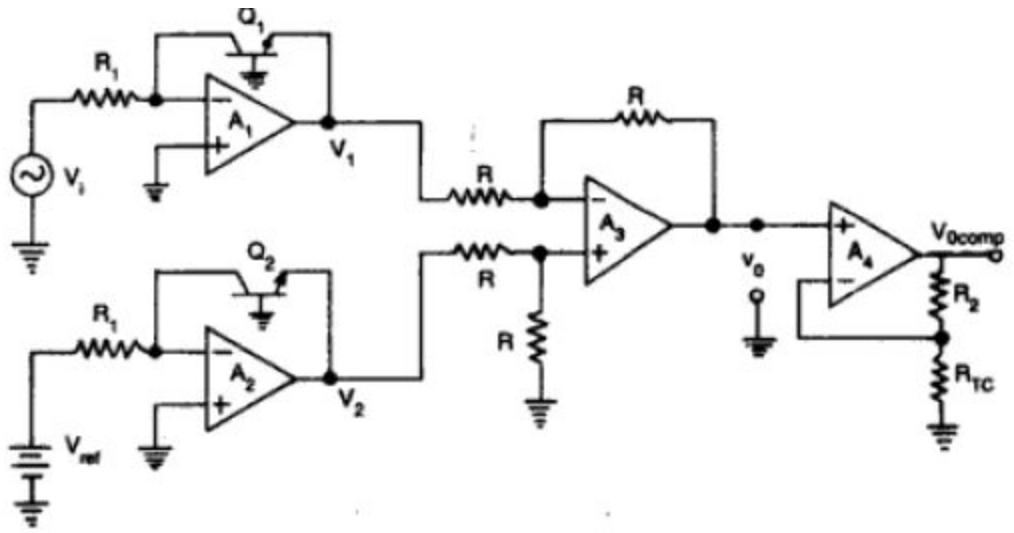


Fundamental log-amp circuit

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find $\log_{10}$ by proper scaling

$$\log_{10} X = 0.4343 \ln X$$

The circuit, however, has one problem. The emitter saturation current I_s varies from transistor to transistor and with temperature. Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by the circuit given in Fig. 4.18 (b). The input is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.



Log-amp with saturation current and temperature compensation

Assume, $I_{s1} = I_{s2} = I_s$

and then, $$V_1 = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right)$$

and $$V_2 = -\frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

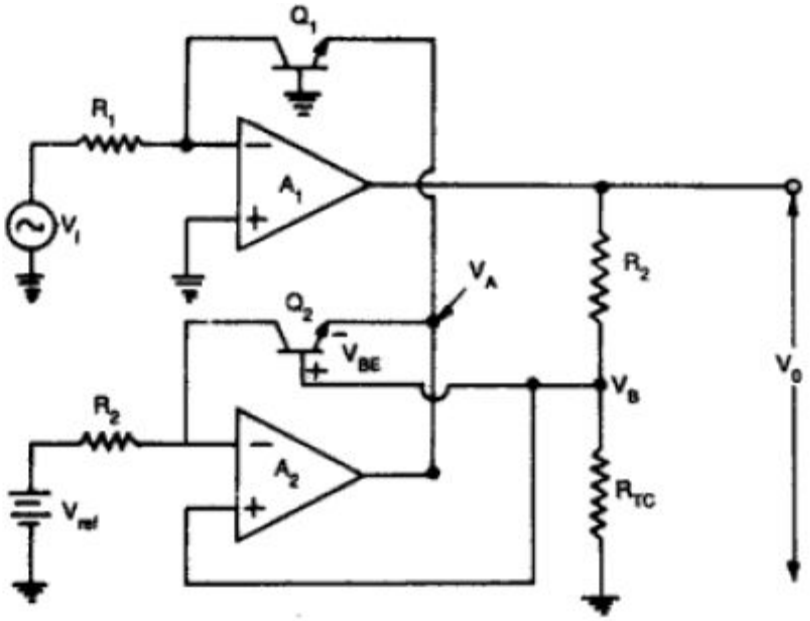
Now, $$V_o = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right]$$

or, $$V_o = \frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $(1 + R_2/R_{TC})$. Now, the output voltage is,

$$V_{o\ comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

where R_{TC} is a temperature-sensitive resistance with a positive coeffecient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.



Log-amp using two op-amps only

The circuit in Fig. 4.18. (b) requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output (with an inversion) can be obtained by the circuit of Fig. 4.18 (c) using two op-amps only.

Antilog Amplifier

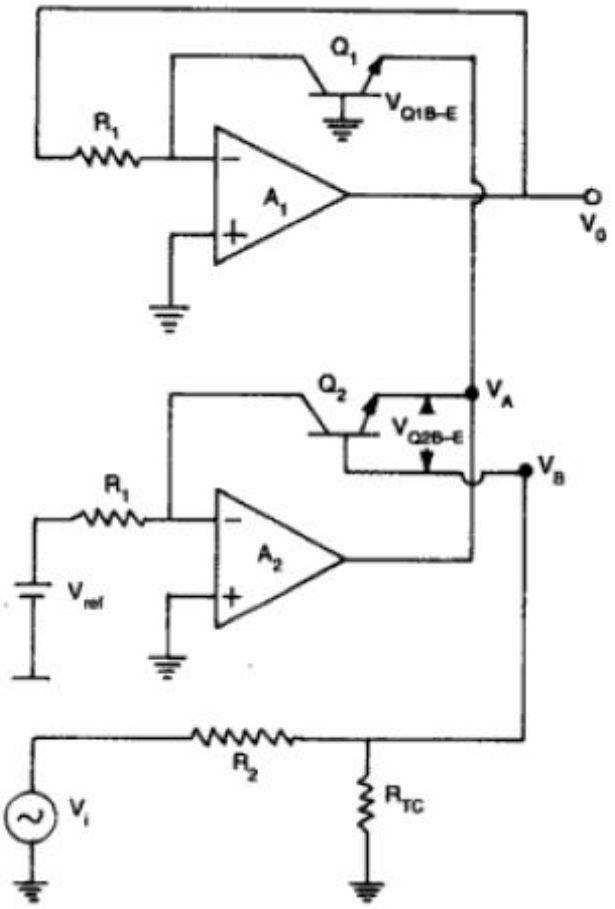
The circuit is shown in Fig. 4.19. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1. The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\ B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$

and $$V_{Q2\ B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

Since the base of Q_1 is tied to ground, we get

$$V_A = -V_{Q1\ B\text{-}E} = -\frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$



Antilog amplifier

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i$$

The voltage at the emitter of Q_2 is

$$V_{Q2\,E} = V_B + V_{Q2\,E\text{-}B}$$

or,
$$V_{Q2\,E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q2\,E}$$

or,
$$-\frac{kT}{q} \ln \frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_s}$$

or,
$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q}\left(\ln \frac{V_o}{R_1 I_s} - \ln \frac{V_{ref}}{R_1 I_s}\right)$$

or,
$$-\frac{q}{kT} \frac{R_{TC}}{R_2 + R_{TC}} V_i = \ln\left(\frac{V_o}{V_{ref}}\right)$$

Changing natural log, i.e., ln to $\log_{10}$ using Eq. (4.38)

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right)$$

or,
$$-K' V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

or,
$$\frac{V_o}{V_{ref}} = 10^{-K' V_i}$$

or,
$$V_o = V_{ref}\,(10^{-K' V_i})$$

where
$$K' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

Hence an increase of input by one volt causes the output to decrease by a decade. The 755 log/antilog amplifier IC chip is available as a

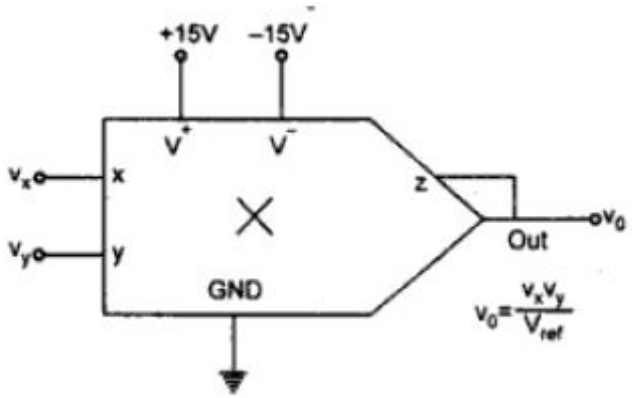
functional module which may require some external components also to be connected to it.

5.6 MULTIPLIER AND DIVIDER

Multiplier

There are a number of applications of analog multiplier such as frequency doubling, frequency shifting, phase angle detection, real power computation, multiplying two signals, dividing and squaring of signals. A basic multiplier schematic symbol is shown in Fig. 4.20 (a). Two signal inputs (v_x and v_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}.

$$v_o = \frac{v_x v_y}{V_{ref}}$$



Multiplier schematic symbol

Normally, V_{ref} is internally set to 10 volts. So,

$$v_o = \frac{v_x v_y}{10}$$

As long as

$$v_x < V_{ref}$$

and $$v_y < V_{ref}$$

the output of the multiplier will not saturate.

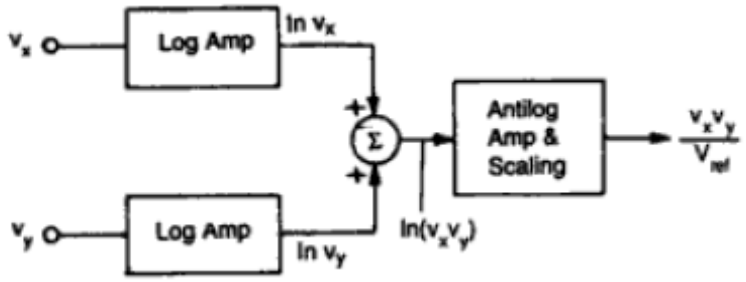
If both inputs are positive, the IC is said to be a one quadrant multiplier. A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative. If both inputs may be either positive or negative, the IC is called a four quadrant multiplier.

There can be several ways to make a circuit which will multiply according to Eq. (4.55). One commonly used technique is log-antilog method. The log-antilog method relies on the mathematical relationship

that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers.

$$\ln v_x + \ln v_y = \ln (v_x\, v_y)$$

Figure 4.20 (b) is a block diagram of a log-antilog multiplier IC. Log -amps require the input and reference voltages to be of the same polarity. This restricts log-antilog multipliers to one quadrant operation. A technique that provides four quadrant multiplication is transconductance multiplier. Some of the multiplier IC chips available are AD533 and AD534. We now discuss two applications of multiplier IC.



Block diagram of a log-antilog

Frequency Doubling

The multiplication of two sine waves of the same frequency, but of possibly different amplitudes and phase allows to double a frequency and to directly measure real power. Let

$$v_x = V_x \sin \omega t$$
$$v_y = V_y \sin (\omega t + \theta)$$

where θ is the phase difference between the two signals. Applying these two signals to the inputs of a four quadrant multiplier will yield an output as,

$$v_o = \frac{V_x \sin \omega t \, V_y \sin(\omega t + \theta)}{V_{ref}}$$

$$v_o = \frac{V_x V_y}{V_{ref}} \sin \omega t (\sin \omega t \cos \theta + \sin \theta \cos \omega t)$$

$$= \frac{V_x V_y}{V_{ref}} (\sin^2 \omega t \cos \theta + \sin \theta \sin \omega t \cos \omega t)$$

But $\sin^2 a = 1 - \cos^2 a$

and $\cos^2 a = 2\cos^2 a - 1$

so $\cos^2 a = \frac{1}{2} + \left(\frac{1}{2}\right)\cos 2a$

$$\sin^2 a = 1 - \frac{1}{2} - \left(\frac{1}{2}\right)\cos 2a = \frac{1}{2} - \left(\frac{1}{2}\right)\cos 2a$$

so $$v_o = \frac{V_x V_y}{V_{ref}} \left[\cos \theta \left(\frac{1}{2} - \left(\frac{1}{2}\right)\cos 2\,\omega t\right) + \sin \theta \sin \omega t \cos \omega t\right]$$

But, $\sin a \cos a = \left(\frac{1}{2}\right)\sin 2a$

Hence, $$v_o = \frac{V_x V_y}{2 V_{ref}} (\cos\theta - \cos\theta \cos 2\omega t + \sin\theta \sin 2\omega t)$$

or, $$v_o = \frac{V_x V_y}{2V_{ref}} \cos\theta + \frac{V_x V_y}{2V_{ref}} (\sin\theta \sin 2\,\omega t - \cos\theta \cos 2\,\omega t)$$

The first term is a DC and is set by the magnitude of the signals and their phase difference. The second term varies with time, but at twice the frequency of the inputs (2ω).

Divider

Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp's feedback loop. The output voltage from the divider in Fig. 4.20 (c) with input signals v_z and v_x as dividend and divisor respectively, is given by

$$v_o = -V_{ref}\frac{v_z}{v_x}$$

The result can be derived as follows. The op-amp's inverting terminal is at virtual ground. Therefore,

$$I_z = I_A$$

and

$$I_z = \frac{v_z}{R}$$

The output voltage V_A of the multiplier is determined by the multiplication of v_x and v_y

$$V_A = \frac{v_x v_y}{V_{ref}} = \frac{v_x v_o}{V_{ref}}$$

Again

$$V_A = -I_A R$$

so,

$$I_A = -V_A/R = -\frac{v_x v_o}{V_{ref} R}$$

As,

$$I_z = I_A$$

so,

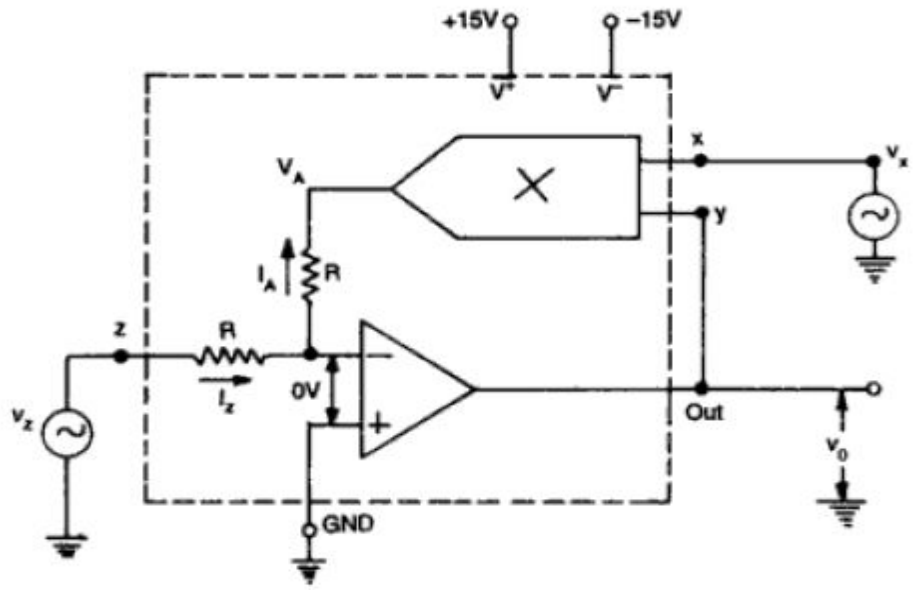
$$I_z = -\frac{v_x v_o}{V_{ref} R}$$

From Eq. (4.64), wt get

$$v_z = I_z R = -\frac{v_x v_o}{V_{ref}}$$

or,

$$v_o = -V_{ref}\frac{v_z}{v_x}$$



Multiplier IC configured as divider

Division by zero is, of course, prohibited. Multiplier IC can be used for squaring a signal. Similarly, divider circuit can be used to take the square root of a signal.

\

5.7 Triangular /Rectangular wave generator :

A basic circuit for a triangular square wave generator is given in Figure. It consists of an integrator and regenerative comparator connected in a positive feedback loop. Precise triangular waves are formed by integration of the square wave thatis fed back from the comparator's output to the integrator's input. With the comparator output at its positive saturation level, the integrator output ramps down at the rate

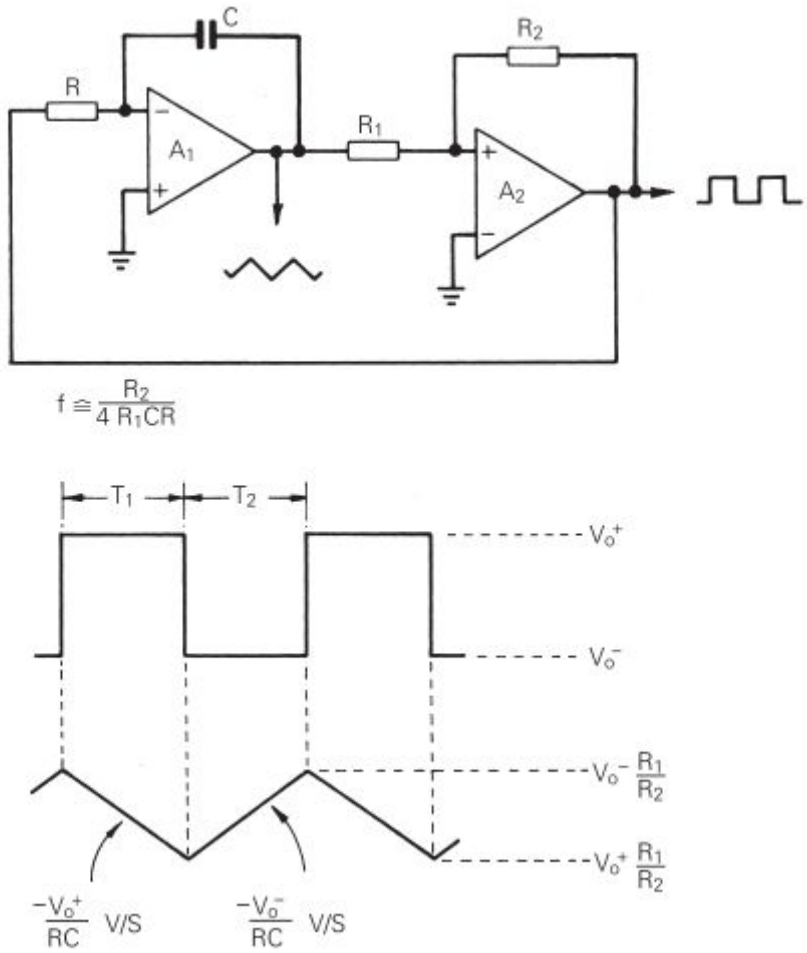
$$-\frac{V_o^+}{CR}\ \text{V/s}$$

until it reaches the lower trip point of the comparator:

$$-V_o^+\frac{R_1}{R_2}$$

The comparator output then switches rapidly to its negative saturation level *Vo* _ and the integrator output then ramps up at the rate

$$-\frac{V_o^-}{CR}\ \text{V/s}$$



Basic triangular square wave generator

When the integrator output reaches the upper trip point of the comparator:

$$-V_o^- \frac{R_1}{R_2}$$

the comparator again switches states and the process repeats. The waveform periods are determined by the relationships

$$T_1 = \frac{[V_o^+ - V_o^-]\frac{R_1}{R_2}}{-\frac{V_o^+}{CR}} \text{ s}$$

$$T_2 = \frac{[V_o^+ - V_o^-]\frac{R_1}{R_2}}{-\frac{V_o^-}{CR}} \text{ s}$$

If the comparator positive and negative output limits have the same magnitude, $V_o^+ = -V_o^-$, $T_1 = T_2$ and the frequency of the oscillations is determined by the relationship

$$f = \frac{1}{T_1 + T_2} = \frac{R_2}{4R_1 CR}$$

Equation 7.10 has been derived from the assumption of ideal op-amp action. The performance limits of a practical circuit are determined by comparator slew rate and integrator bandwidth at the higher frequencies and by integrator drift at the lower frequencies.

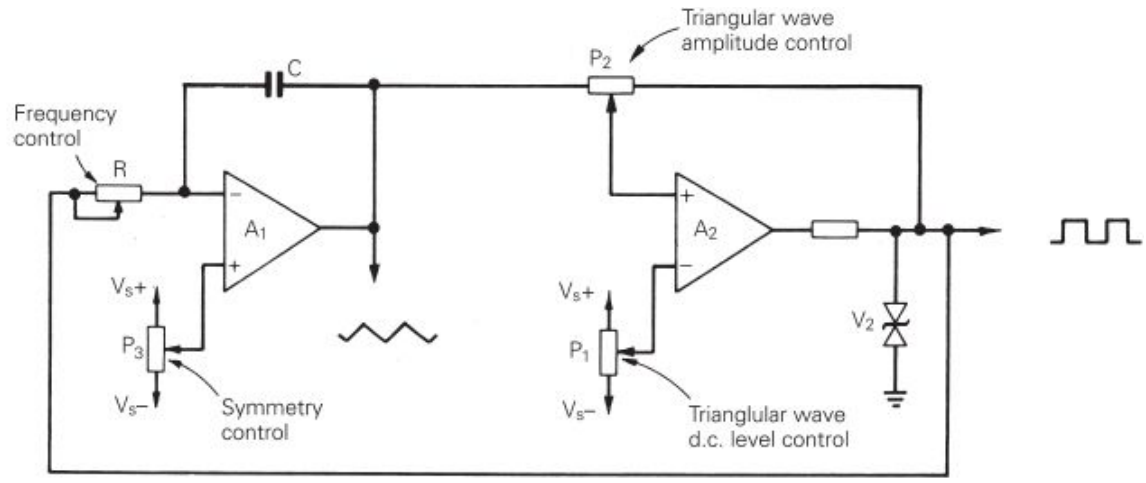
Bias current and input offset voltage give rise to an integrator output drift. This drift increases one integration rate and decreases the other as the output of the comparator changes polarity. The effect at low frequencies is to cause a lack of symmetry in the generator waveform.

The effect of bias current and input offset voltage on the performance of A_2 is to introduce an equivalent error voltage at the non-inverting input terminal. This error voltage shifts both comparator trip points an equal amount, which in turn shifts the DC level of the triangular wave but leaves its amplitude unchanged.

Varying the waveform characteristics of the basic generator

The waveform characteristics of the basic function generator system of Figure 7.21 can be varied during operation by using potentiometers. The circuit shown in Figure 7.22 gives one possible arrangement. This allows adjustment of frequency, waveform symmetry, triangular wave DC offset and triangular wave amplitude. The circuit includes a zener output limiting clamp on the comparator, which sets the square wave amplitude at $\pm V_Z$.

Adjustment of the timing resistor R controls the frequency and does not alter other waveform characteristics. Potentiometer P_1 applies a voltage V_1 to the inverting input of the regenerative comparator amplifier A_2. This shifts both comparator trip points by an amount V_1/β, where β is the positive



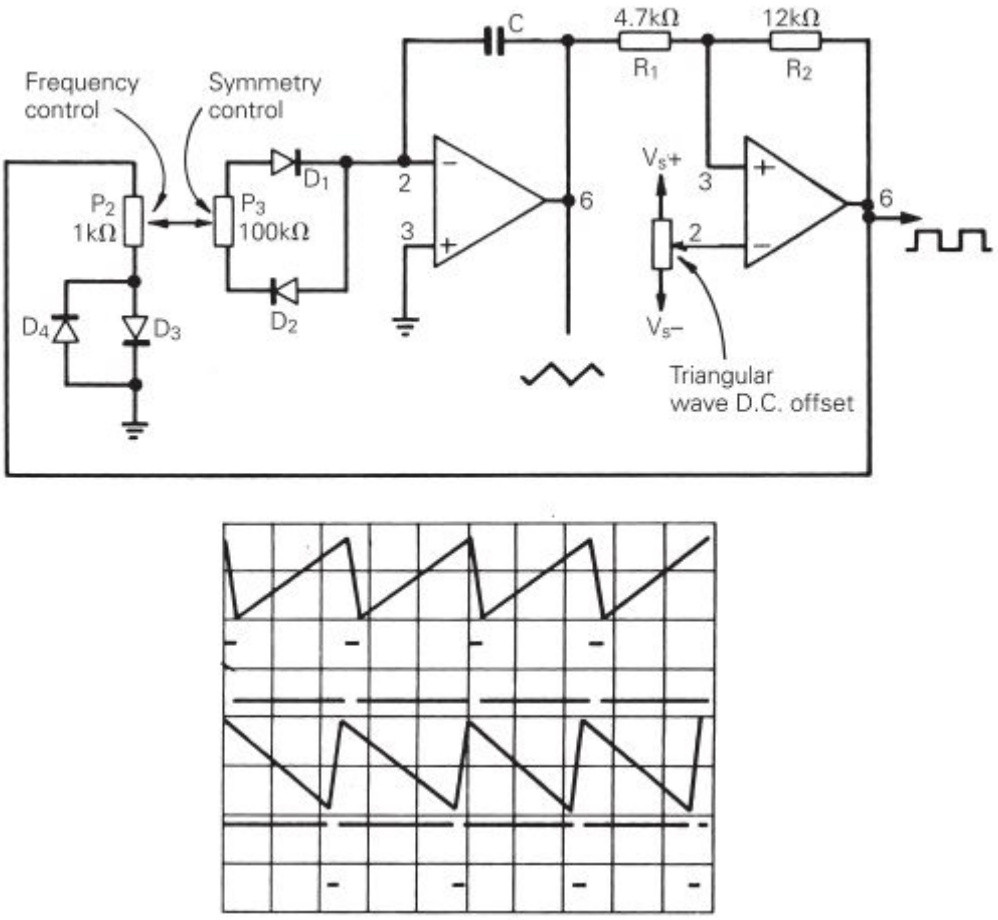
Waveform generator with control of waveform characteristics

feedback fraction determined by the setting of potentiometer P_2. The effect is to shift the DC level of the triangular wave by an amount V_1/β.

The setting of potentiometer P_2 determines the amount of hysteresis in the regenerative comparator. This controls the comparator trip points, and thus controls the triangular wave amplitude. Change of triangular wave amplitude is inevitably accompanied by a change in frequency. A decrease in triangular wave amplitude causes a proportional increase in frequency.

Potentiometer P_3 applies a DC offset to the integrator. This results in an increase in one timing period and a decrease in the other. This change of timing controls waveform symmetry, but it also affects the frequency.

In Figure 7.23 is an alternative circuit that allows control of waveform symmetry without altering the frequency. In the circuit, resistor values R_1 and R_2, which control the comparator trip points, are chosen so as to give a triangular wave of amplitude approximately 10 V peak-to-peak. This allows a single polarity triangular wave or ramp to be generated by adjustment of the triangular wave offset control potentiometer P_1. The traces as given in Figure 7.23 show the control of waveform symmetry obtained by adjusting the symmetry control potentiometer P_3.



Waveform generator with frequency unaffected by symmetry

Note that there is some interaction between the symmetry control potentiometer and the frequency control potentiometer, at the extreme settings of the symmetry control. This is due to unequal loading of the frequency control potentiometer on the run up and run down portion of the triangular wave. If this interaction is not tolerable, a follower can be used to buffer the output of the frequency control potentiometer.

Temperature dependence of the forward voltage drops of diodes D_1 and D_2, which can be expected to cause frequency instability at the lower levels of frequency, are compensated by diodes D_3 and D_4.

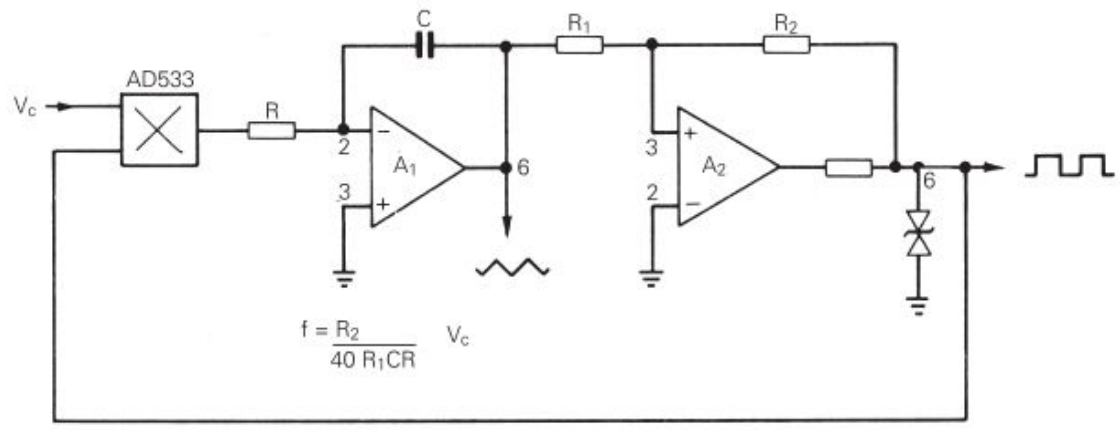
Waveform generator with voltage control of frequency

It is often convenient to be able to control, or modulate, the frequency of a waveform generator with a control voltage. To achieve this in the circuit of Figure 7.21, the magnitude of the current to the integrator must be varied in response to an externally applied control voltage. The sign of the integrator current must change during operation, to allow the integrator output to ramp both up and down.

A four-quadrant multiplier (see Chapter 5) could be connected between the comparator and the integrator. This is shown in Figure 7.24. The multiplier can be used for voltage control of the waveform generator's frequency. The multiplier may be thought of as acting as a voltage controlled potentiometer.

Assuming that the scaling factor of the multiplier is the normal 1/10, the square wave is multiplied by $V_c/10$ before being applied to the integrator. The equations for the waveform periods (equations 7.8 and 7.9) are in effect multiplied by $10/V_c$ and the expression for frequency (equation 7.10) is multiplied by $V_c/10$. If the comparator positive and negative output limits are equal in magnitude the frequency of oscillations given by the circuit in Figure 7.22 is thus:

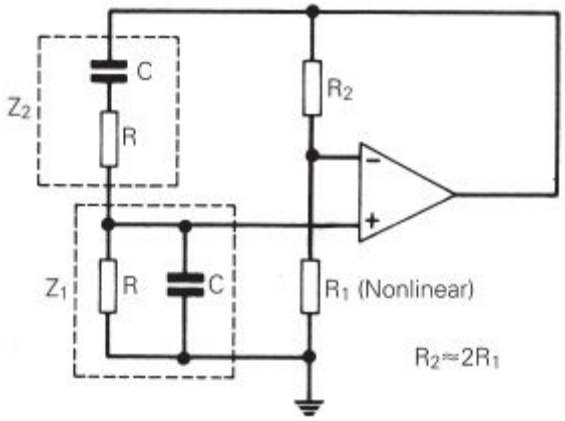
$$f = \frac{V_c}{10}\frac{R_2}{4R_1CR}$$



Four quadrant multiplier allows voltage control of frequency

5.8 Wein bridge oscillator:

The circuit shown in Figure 7.18 illustrates the use of an op-amp in a Wien bridge oscillator.



Wien bridge oscillator

In this circuit, feedback is applied between the output and the non-inverting input of the op-amp via the frequency dependent network Z_2, Z_1. The network produces zero phase change at a frequency

$$f_o = \frac{1}{2\pi CR}$$

Oscillations thus take place at this frequency since the feedback is positive. The output from the network

$$\left(\frac{Z_1}{Z_1 + Z_2}\right)$$

is one third that of the input at the frequency f_o. Negative feedback is applied to the amplifier via resistors R_2 and R_1 in order to reduce the loop gain to unity and so ensure a sinusoidal output waveform. If the amplifier had infinite open-loop gain, oscillations would just be maintained for values of R_2 and R_1 such that

$$\frac{R_1}{R_1 + R_2} = \frac{1}{3}$$

In a practical circuit, in order to maintain stable oscillation amplitude, a non-linear resistor is normally used for R_1. The non-linear resistor should have a positive temperature coefficient so that it increases its resistance with increasing current. This effect can be used to make the loop gain depend upon the amplitude of oscillations. An increase in the amplitude of oscillations causes an increase in the current through R_1, which results in an increase in the value of R_1. An increase in the magnitude of R_1 means a greater amount of negative feedback and a consequent reduction in loop gain and signal amplitude.

The impedances Z_2, Z_1, R_2, R_1, in fact form the arms of a bridge network (a Wien bridge). The imbalance voltage from the bridge is applied between the differential input terminals of the op-amp. Analysis of the bridge network shows that when $R_2 = 2 \times R_1$ the bridge is balanced at a frequency

$$f_o = \frac{1}{2\pi CR}$$

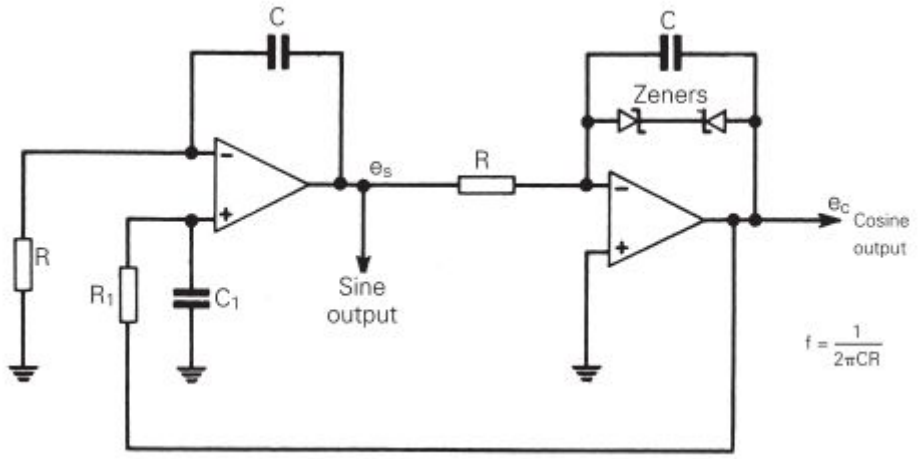
In practice a small imbalance must always exist but the greater the open-loop gain of the amplifier the closer is the bridge to balance and the greater is the frequency stability of the oscillator.

The circuit illustrated in Figure 7.19 shows an alternative method of ensuring amplitude stability. A field effect transistor (FET) is used in place of the non-linear resistor R_1.

For small values of drain source voltage (below 'pinch-off'), an FET behaves very much like a linear resistor. The resistance between the FET's drain and source (R_{DS}) is determined by the voltage applied between the FET's gate and source. In this circuit the oscillator output voltage is rectified by the diode D, filtered by R_5 and C_2, and applied via potentiometer R_6 to the gate of the FET. The arrangement ensures that R_{DS} takes on that value just necessary to maintain the required amplitude of oscillation. The signal amplitude applied to the bridge must be small enough to ensure that the FET is working in the linear resistance region.

5.9 Phase shift (Quadrature phase) oscillator:

The circuit illustrated in Figure 7.20 may be used to generate two sinusoidal signals in quadrature.



Quadrature oscillator

The circuit uses two amplifiers: one acts as a non-inverting integrator, the other as an inverting integrator (see Chapter 6). The two amplifiers are connected in cascade to form a feedback loop. The feedback loop is represented by the differential equations

$$RC\frac{de_S}{dt} = e_C \quad RC\frac{de_C}{dt} = -e_S$$

The solution is represented by a sinusoidal oscillation of frequency

$$f_o = \frac{1}{2\pi CR}$$

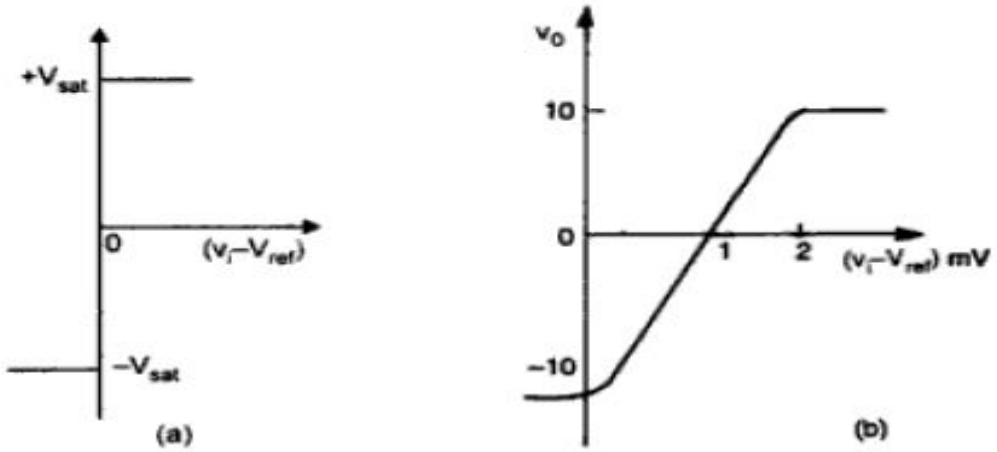
In practice the resistor R_1 is made slightly larger than the other resistors to ensure sufficient positive feedback for oscillations. The zener diodes, used

to limit the output of the inverting integrator, serve to stabilize the amplitude of oscillations.

UNIT-6 NON LINEAR CIRCUIT APPLICATIONS

6.1 COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output $\pm V_{sat}$ ($= V_{CC}$) as shown in the ideal transfer characteristics of Fig. 5.1 (a). However, a commercial op-amp has the transfer characteristics of Fig. 5.1 (b).

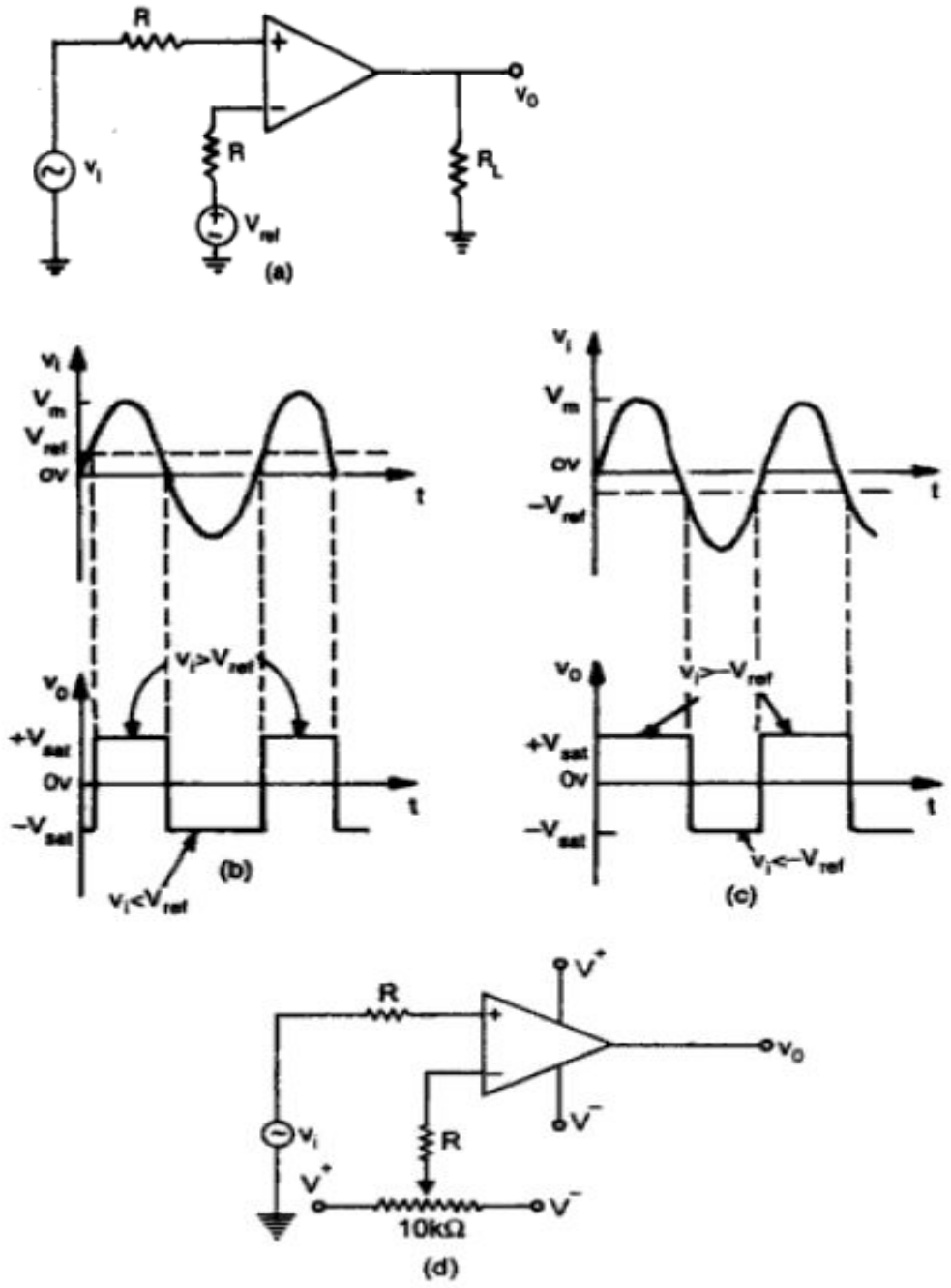


The transfer characteristics (a) ideal comparator
(b) practical comparator

It may be seen that the change in the output state takes place with an increment in input v_i of only 2 mV. This is the uncertainty region where output cannot be directly defined. There are basically two types of comparators:

Non-inverting comparator
Inverting comparator.

The circuit of Fig. 5.2 (a) is called a non-inverting comparator. A fixed reference voltage V_{ref} is applied to (–) input and a time varying



(a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} positive (c) V_{ref} negative (d) Practical noninverting comparator

signal v_i is applied to (+) input. The output voltage is at $-V_{sat}$ for $v_i < V_{ref}$. And v_o goes to $+V_{sat}$ for $v_i > V_{ref}$. The output waveform for a sinusoidal input signal applied to the (+) input is shown in Fig. 5.2 (b and c) for positive and negative V_{ref} respectively.

In a practical circuit V_{ref} is obtained by using a 10 kΩ potentiometer which forms a voltage divider with the supply voltages $V+$ and $V-$ with the wiper connected to (–) input terminal as shown in Fig. 5.2 (d). Thus a V_{ref} of desired amplitude and polarity can be obtained by simply adjusting the 10 kΩ potentiometer.

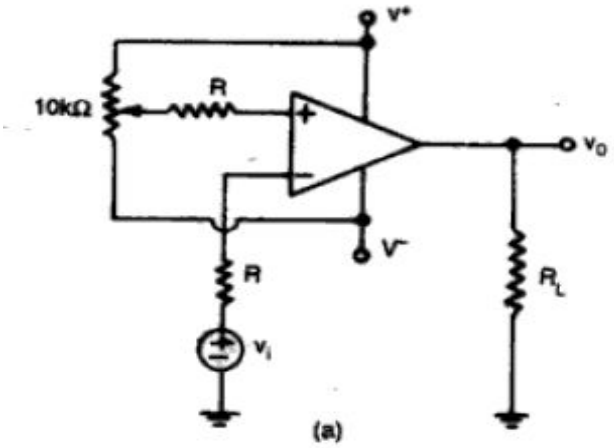
Figure 5.3 (a) shows a practical inverting comparator in which the reference voltage V_{ref} is applied to the (+) input and v_i is applied to (–) input. For a sinusoidal input signal, the output waveform is shown in Fig. 5.3 (b) and (c) for V_{ref} positive and negative respectively.

Output voltage levels independent of power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp as shown in Fig. 5.3 (d). The value of resistance R is chosen so the zener diodes operate at the recommended current. It can be seen that the limiting voltages of v_o are $(V_{Z1} + V_D)$ and $-(V_{Z2} + V_D)$ where V_D (~ 0.7 V) is the diode forward voltage.

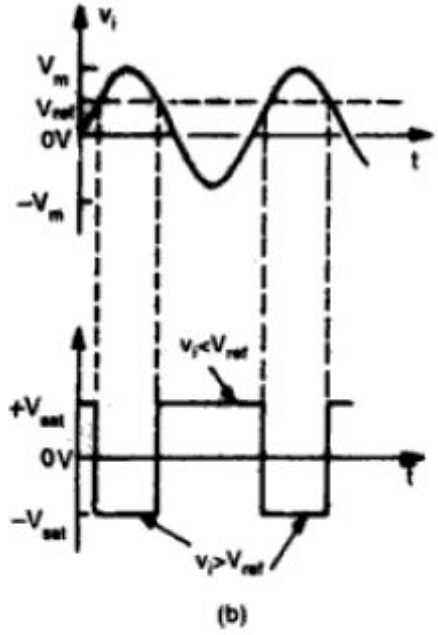
In the waveforms of Figs. 5.2 and 5.3, the output transitions are shown as taking place instantaneously. Practical circuits, however, take a certain amount of time to switch from one voltage level to another. The actual waveform will therefore exhibit slanted edges as well as delays at the points of input threshold crossing. These effects are more noticeable at high frequencies where the output switching times are comparable or even longer than the input period itself. Thus there is an upper limit to the operating frequency of any comparator.

If 741, the internally compensated op-amp is used as comparator, the primary limitation is the slew rate. Since 741C has slew rate equal to 0.5 V/μs, it takes $2 \times 13/0.5 \sim 50$ μs ($V_{sat} = \pm 13$V for 741) to swing from one saturation level to the other. In many applications, this is too long. To increase the response time, it is possible to use uncompensated op-amps such as 301, for comparator applications.

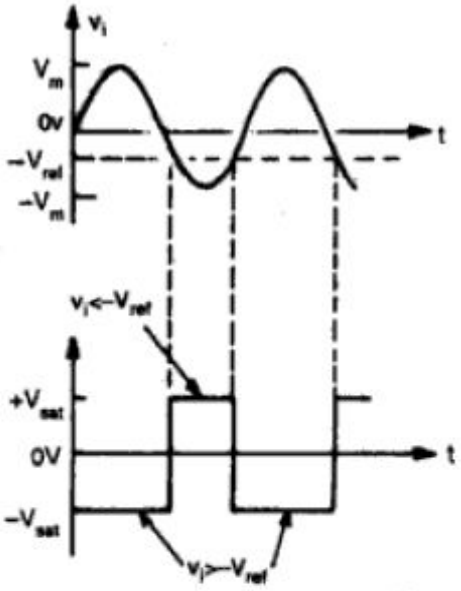
Although uncompensated op-amps make faster comparators than compensated op-amps, there are applications where even higher speeds are required. Also, for interfacing, it is often desired that the output logic levels be compatible with standard logic families such as TTL, CMOS, ECL. To accomodate these needs, monolithic voltage comparators are available. Some of the comparator chips available are the Fairchild μA 710 and 760, the National LM 111, 160 and 311. The response time for 311 is 200 ns whereas 710 is a high speed comparator with a response time of 40 ns. CMOS comparators are also available. Some examples are TLC 372 dual, TLC 374 quad (Texas Instruments), MC 14574 quad (Motorola).


V+
10kΩ
R
V0
V−
R
RL
Vi

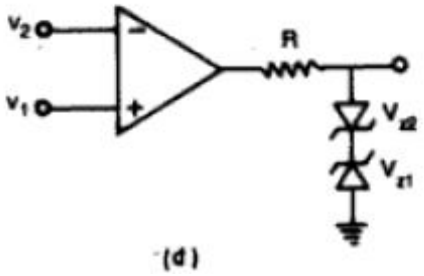
(a)


Vi
Vm
Vref
0V
−Vm
t
Vi<Vref
+Vsat
0V
−Vsat
t
Vi>Vref

(b)


Vi
Vm
0V
−Vref
−Vm
t
Vi<−Vref
+Vsat
0V
−Vsat
t
Vi>−Vref

(c)


V2
V1
R
Vz2
Vz1

(d)

(a) Inverting comparator. Input and output waveforms (b) $V_{ref} > 0$ (c) $V_{ref} < 0$ (d) Comparator with zener diode at the output

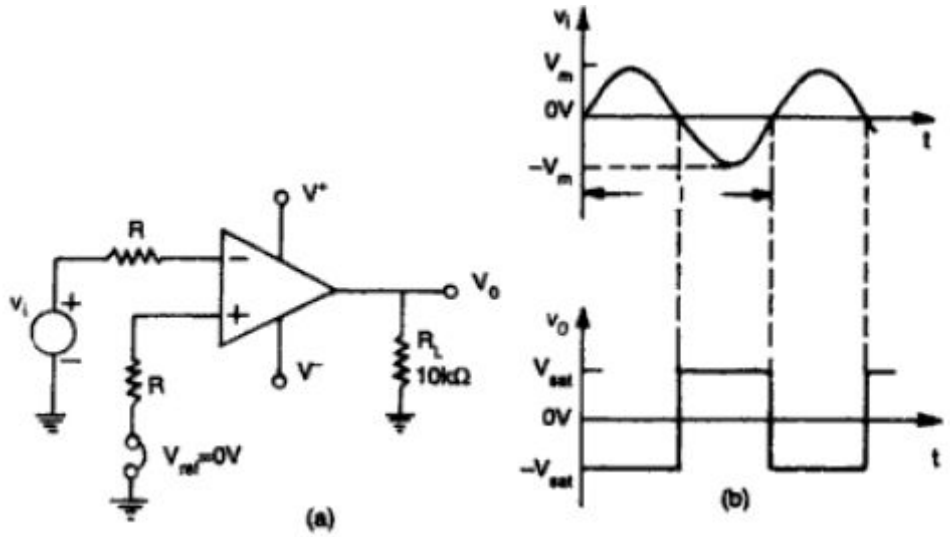
Applications of Comparator

Some important applications of comparator are:

- Zero crossing detector
- Window detector
- Time marker generator
- Phase meter.

Zero Crossing Detector

The basic comparators of Fig. 5.2 (a) and 5.3 (a) can be used as a zero crossing detector provided that V_{ref} is set to zero. An inverting zero-crossing detector is shown in Fig. 5.4 (a) and the output waveform for a sinusoidal input signal is shown in Fig. 5.4 (b). The circuit is also called a sine to square wave generator.



(a) Zero crossing detector (b) Input and output waveforms

6.2 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

If positive feedback is added to the comparator circuit, gain can be increased greatly. Consequently, the transfer curve of comparator becomes more close to ideal curve. Theoretically, if the loop gain $-\beta A_{OL}$ is adjusted to unity, then the gain with feedback, A_{Vf} becomes infinite. This results in an abrupt (zero rise time) transition between the extreme values of output voltage. In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations. So a value greater than unity is chosen. This also gives an output waveform virtually discontinuous at the comparison voltage. This circuit, however, now exhibits a phenomenon called hysteresis or backlash.

Figure 5.8 (a) shows such a regenerative comparator. The circuit is also known as Schmitt Trigger. The input voltage is applied to the (–) input terminal and feedback voltage to the (+) input terminal. The input voltage v_i triggers the output v_o every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). The hysteresis width is the difference between these two threshold voltages i.e. $V_{UT} - V_{LT}$. These threshold voltages are calculated as follows.

Suppose the output $v_o = +V_{sat}$. The voltage at (+) input terminal will be

$$V_{ref} + \frac{R_2}{R_1 + R_2}(V_{sat} - V_{ref}) = V_{UT}$$

This voltage is called upper threshold voltage V_{UT}. As long as v_i is less than V_{UT}, the output v_o remains constant at $+V_{sat}$. When v_i is just greater than V_{UT}, the output regeneratively switches to $-V_{sat}$ and remains at this level as long as $v_i > V_{UT}$ as shown in Fig. 5.8 (b).

For $v_o = -V_{sat}$, the voltage at the (+) input terminal is,

$$V_{ref} - \frac{R_2}{R_1 + R_2}(V_{sat} + V_{ref}) = V_{LT}$$

This voltage is referred to as lower threshold voltage V_{LT}. The input voltage v_i must become lesser than V_{LT} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$. A regenerative transition takes place as shown in Fig. 5.8 (c) and the output v_o returns from $-V_{sat}$ to $+V_{sat}$ almost instantaneously. The complete transfer characteristics are shown in Fig. 5.8 (d).

Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H and can be written as

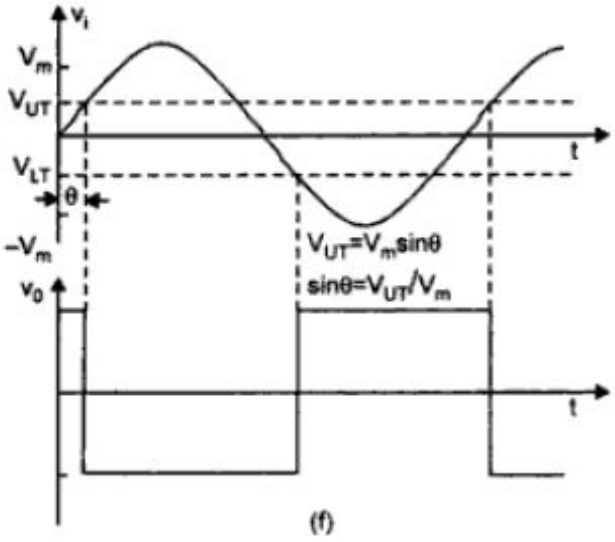
$$V_H = V_{UT} - V_{LT} = \frac{2 R_2 V_{sat}}{R_1 + R_2}$$

Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones. Further, note that if peak-to-peak input signal v_i were smaller than V_H then the Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction would never reset itself, that is, once the output has jumped to, say, $+V_{sat}$ it would remain at this level and never return

$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

If an input sinusoid of frequency $f = 1/T$ is applied to such a comparator, a symmetrical square wave is obtained at the output. The vertical edge of the output waveform however will not occur at the time the sine wave passes through zero [Fig. 5.8 (f)] but is shifted in phase by θ where $\sin \theta = V_{UT}/V_m$ and V_m is the peak sinusoidal voltage.

Special purpose Schmitt triggers are commercially available. T1–13, T1–14 and T1–132 chips with totem pole output and $V_{UT} = 1.7$ V, $V_{LT} = 0.9$ V are available. The T1–132 package is a quad two-input NAND Schmitt trigger. CMOS Schmitt triggers offer the advantage of high input impedance and low power consumption. Examples of CMOS inverting Schmitt trigger are the CD40106B and 744C14.



(f)

(f) Shift θ in the output waveform for $V_{UT} = -V_{LT}$

In the circuit of Schmitt trigger of Fig. 5.8 (a), $R_2 = 100\ \Omega$, $R_1 = 50\ k\Omega$, $V_{ref} = 0V$, $v_i = 1V_{pp}$ (peak-to-peak) sine wave and saturation voltage = ± 14V. Determine threshold voltages V_{UT} and V_{LT}.

$$V_{UT} = \frac{100}{50100} \times 14 = 28\ \text{mV}$$

$$V_{LT} = \frac{100}{50100} \times (-14) = -28\ \text{mV}$$

A Schmitt trigger with the upper threshold level V_{UT} = 0V and hysteresis width V_H = 0.2V converts a 1 kHz sine wave of amplitude $4V_{pp}$ into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

$$V_{UT} = 0$$

$$V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$$

So, $V_{LT} = -0.2$ V

In Fig. 5.9, the angle θ can be calculated as

$$-0.2 = V_m \sin(\pi + \theta) = -V_m \sin\theta = -2 \sin\theta$$

$$\theta = \text{arc sin } 0.1 = 0.1 \text{ radian}$$

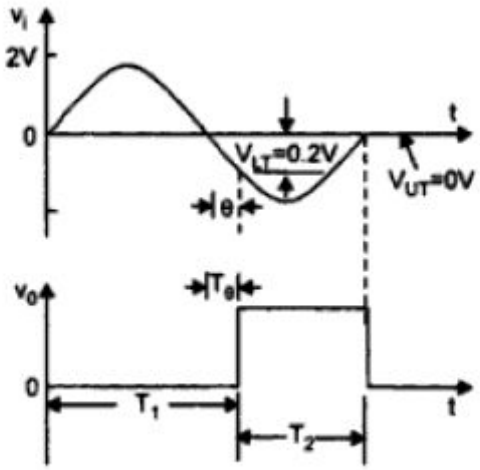
The period, $T = 1/f = 1/1000 = 1$ ms

$$wT_\theta = 2\pi\,(1000)\,T_\theta = 0.1$$

$$T_\theta = (0.1/2\pi) \text{ ms} = 0.016 \text{ ms}$$

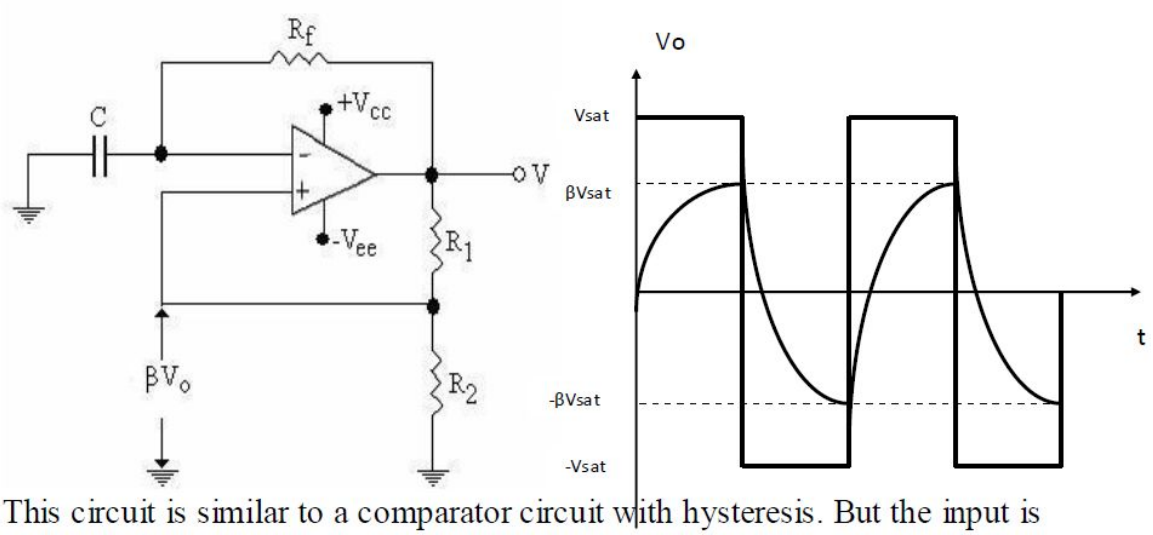
So, $T_1 = T/2 + T_\theta = 0.516$ ms

and $T_2 = T/2 - T_\theta = 0.484$ ms



(f)

ASTABLE MULTIVIBRATOR/FREE RUNNING OSCILLATOR/SQUARE WAVE GENERATOR



This circuit is similar to a comparator circuit with hysteresis. But the input is replaced by a capacitor.

ANALYSIS:

Let us assume the output vo to be at positive saturation

i.e. vo = + vsat

since R1and R2 divide the voltage vo,

voltage at non inverting terminal=v1=(R2/(R1+R2))(vo)

if ,

β = R2/(R1+R2) then v1= βV_o

now the capacitor charges due to the current flowing through the feedback resistor

when the capacitor charge exceeds v1 ,

vid=v1-v2

becomes negative and hence the output goes to negative saturation.

i.e vo=-vsat

now the capacitor discharges and further charges to a negative voltage of - βVsat

hence the output obtained results in a square wave.

TO OBTAIN FREQUNCY OF THE SQUARE WAVE:-

for a charging capacitor-

$vc = vf + (vi-vf)\, e^{-t/\tau}$

since T1=T2,

T= T1+T2 =2T1

hence T=t1/2

$V_c = [1-(1+\beta)]e^{-T1/2\tau}$

$\tau = R_fC$ is the time constant

since the capacitor charges and discharges through the same resisitor Rf,charging time constant equal to discharging time constant.

$e^{-T1/2\tau} = 1- \beta/1+ \beta$

$T1 = R_f C \log_e [1+ (2R_3/R_2)]$

$T=2T1=2R_fC \log_e [1+ (2R_3/R_2)]$

If R2=(0.86)R1

then , T=2RC

ASTABLE CONTROL

To get an unsymmetrical square wave the ckt is modified as shown below

When $V_O = +V_{sat}$

D_3 conducts (Forward biased)

$\beta V_{sat} = +V_{sat} - V_{sat}\,(1+\beta)\, e^{(-T1/R3C)}$

$T_1 = R_3C \ln [1 + 2R_2/R_1]$

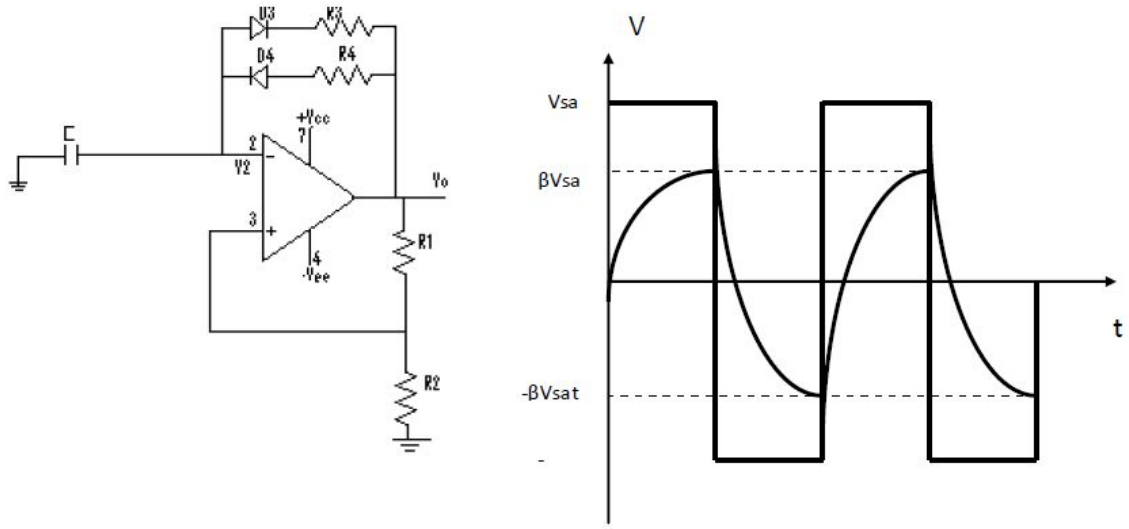
When $V_0= -V_{sat}$

D_4 is forward biased

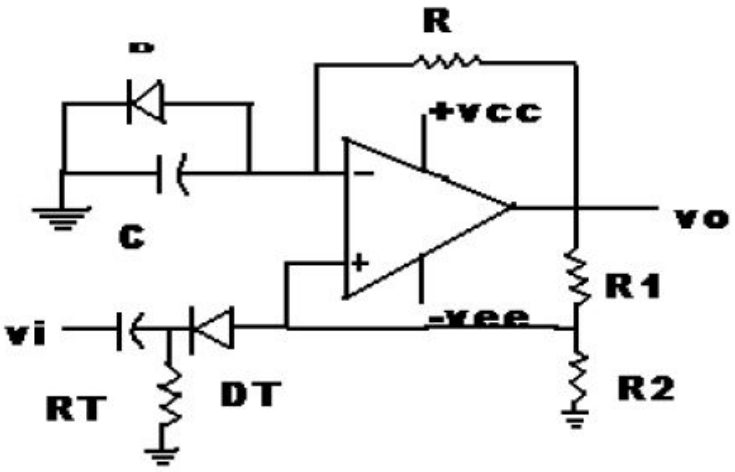
$\beta V_{sat} = -V_{sat} + V_{sat}\,(1+\beta)\, e^{(-T2/R4C)}$

$T_2 = R_4C \ln [1 + 2R_2/R_1]$

Therefore the total period is $(R_3+R_4)C \ln [1 + 2R_2/R_1]$



Monostable multivibrator/one shot Multivibrator:



The ckt shown above represents a monostable multivibrator which is also called as one shot multivibrator.

The circuit components CT and RT works as a differentiator and let us assume that we are giving a square wave as the input.Hence the output of the differentiator circuit would be spikes(alternating positive and negative).But since we have a diode DT connected in the manner as shown in the figure,it would allow only negative spikes to pass through it and not negative spikes.Thus the voltage V1 to the non-inverting input terminal would be the addition of negative spikes generated from the differentiator circuit and a part of output from the voltage divider circuit.

Let us assume Vo to be +Vcc to start with,thus

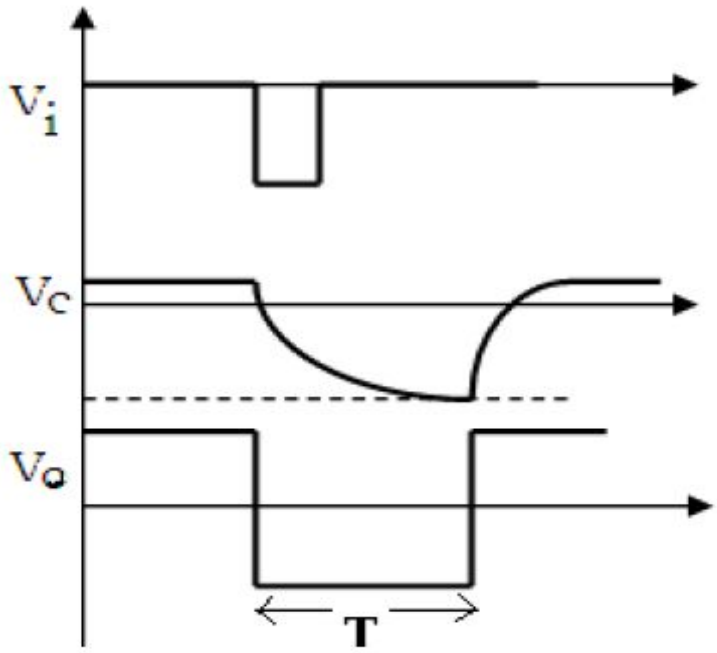
Vo=+Vsat

V1=Vut=βVsat

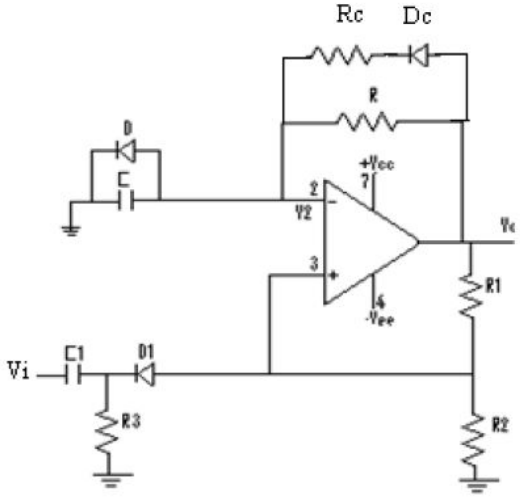
Where β=R2/(R1+R2)

Thus since the output is positive,diode D is forward viased .Hence the voltage across the capacitor is the voltage across the diode.When a negative spike is ther i.e.,during the transition from +ve value to a negative value in the square wave input,voltage V1,input to the no inverting input terminal would be –ve(since the magnitude of spikes generated will be usually very high).Thus V2 would be the diode voltage and the V1 becomes negative the moment negative spikes are applied and thus Vid=V1-V2 would become negative.Thus output switches from +Vsat to –Vsat.Thus now the diode D would be reverse biased and thus the capacitor charges by an aiming voltage of –Vsat.But the moment the capacitor voltage reaches –βvsat,Vid would become +ve since V1 now will be –ve(since Vo=-Vsat and we should also note spikes lasts long only for a short period of time),thus the the output would be equal to +Vsat and thus the voltage across the capacitor would be reduced again to the diode voltage.Thus the capacitor voltage be equal to the diode voltage during positive half cycle.

Recovery time:The time required by the capacitor to change it's value from LTP i.e.,-βVsat to Vd is termed as the recovery time.


V_i
V_C
V_o
T

The state during which the output will be high is termed as quasi state or unstable state. To reduce the recovery time Rc and Dc (series combination) is connected I parallel with R. During the Charging of the capacitor from Vd to Vlt, the diode is Dc is reverse biased and the charging is through R and during the discharging, From Vlt to Vd the Dc is forward biased, the effective resistance is R||Rc. So recovery time is reduced.



Expression for T.

Vc=Vf+(Vi-Vf)e^(-t/Rc)

From the graph,-BVsat=-Vsat+(Vd+Vsat)e^(-t/Rc)

Vsat(1-B)=(Vd+Vsat)E(-t/Rc)

1-B=((Vd/Vsat)+1)e^(-t/Rc)

e^(t/Rc)=((Vd/Vsat)+1)/(1-B)

T/Rc=ln(1+(Vd/Vsat))/(1-B)

Since Vd<<Vsat,

Ln(1/(1-B))

Thus,T=Rc ln(1/1-B)

Thus from the expression,it is clear that

a)when R1=R2,T=0.693Rc

b)when R2=R1/5,T=0.2Rc

From the graph it is clear that to get a perfect pulse,we shd have recovery time as small as possible.So.we connect a diode in series with Rc across R so that Rc=0.1R and thus the discharging time constant of the capacitor will be reduced and hence the desired task is achieved.

6.4 Active Filters:

Op-amps overcome most of the problems associated with the passive filter circuit. Not only will the high input impedance and low output impedance of the op-amp effectively isolate the frequency sensitive filter network from the following load, it can also provide useful current or voltage gain. More significantly, the op-amp can be designed into a *CR* only circuit in such a way as to provide a filter response virtually identical with that of a passive inductive filter network. This means that the use of inductors in filters is now unnecessary. Unlike the inductor, the op-amp does not possess a magnetic field which stores energy, rather it is designed to behave mathematically in the same way as the hole passive circuit it replaces. Any additional circuit energy is obtained from the separate power source used by the op-amp.

First order high-pass and low-pass filters

Examples of simple first order high- and low-pass active filters are shown in Figure 9.12. As expected, the frequency selective resistor-capacitor circuit elements decide the frequency response. The cut-off frequency is *f*c _ 1/2_*CR* at which the magnitude of the filter response is 3 dB less than that in the pass-band, and the higher frequency roll-off tends to 20 dB per decade. If a low value of *f*c is required, a general purpose Bi-FET operational amplifier should be suitable. This will allow the use of large resistance values without introducing any appreciable bias current off-set error. Resistor values up to

10 M_ may be used so avoiding the expense of a high value, close tolerance capacitor.

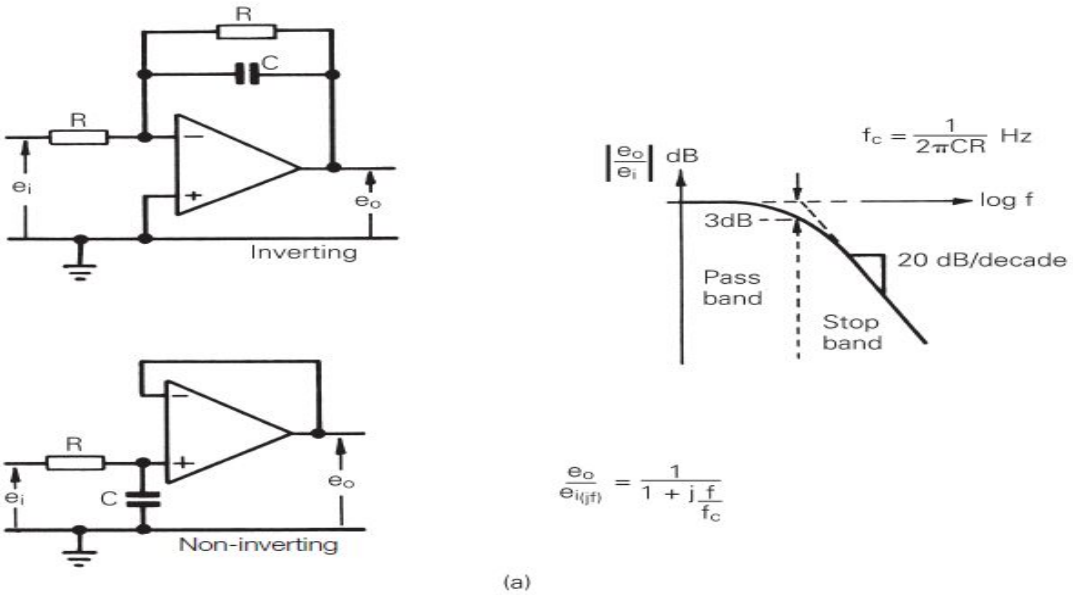
First order low-pass filters are often used to perform a running average of a signal having high frequency fluctuations superimposed upon a relatively slow mean variation; for this purpose it is simply necessary to make the filter time constant *CR* much greater than the period of the high frequency fluctuations. A practical point to remember is that all op-amp active high-pass filters show a band-pass characteristic. This is because their response eventually fails at frequencies which exceed the closed loop bandwidth of the op-amp.

Second order low-pass and high-pass filters

Examples of simple second order low-pass and high-pass active filter circuits are shown in Figure 9.13. The second order filter response has a 40 dB per decade roll-off in the stop-band. The sharpness of the response curve knee depends upon the choice of values for the components forming the frequency sensitive element of the filter. In Figure 9.13, the components are

proportioned to give a so-called Butterworth response (further details later in this chapter) and the cut-off frequency *fc* _ 1/[2√2(_*CR*)] hertz.

Figure 9.2 shows the ideal shape for a low-pass filter. It has a perfectly flat (horizontal) response from zero frequency up to the cut-off frequency where a vertical fall then occurs. In practice this perfectly rectangular shape is unattainable. Depending upon the intended role of the filter, it can be designed to approximate to the ideal response in varying ways and these are mentioned briefly below.



(a)

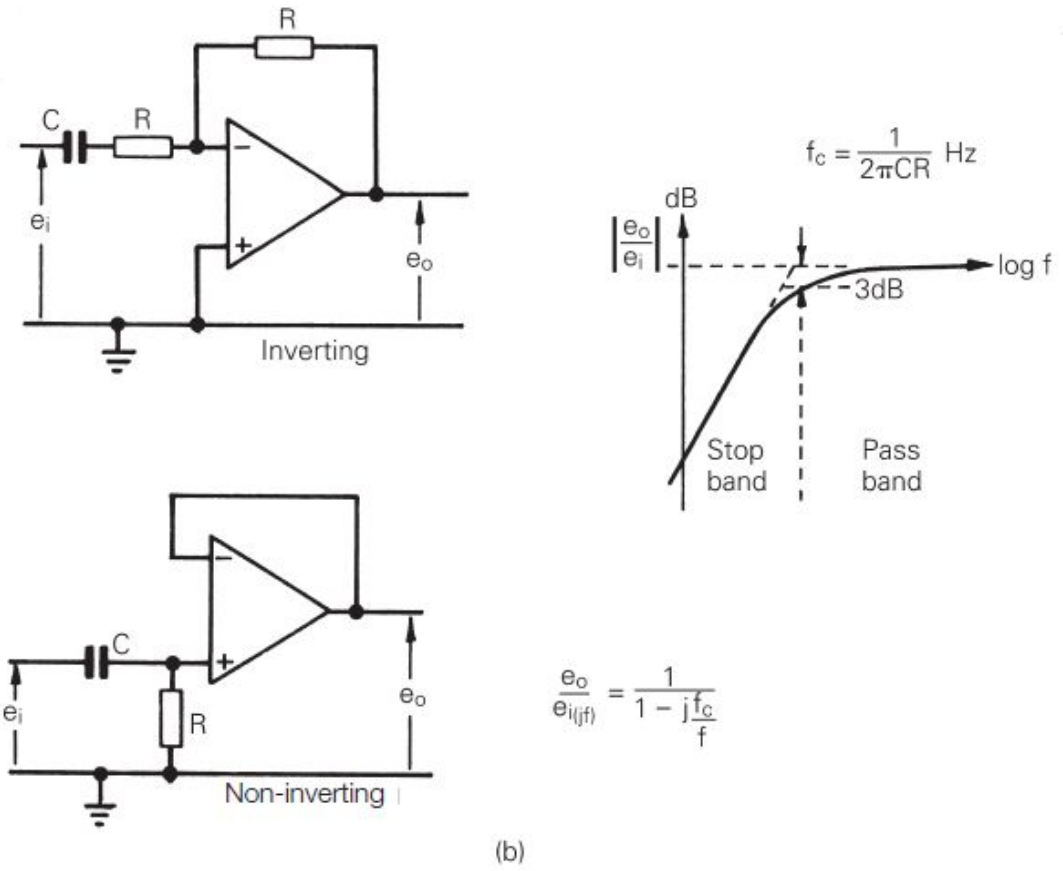
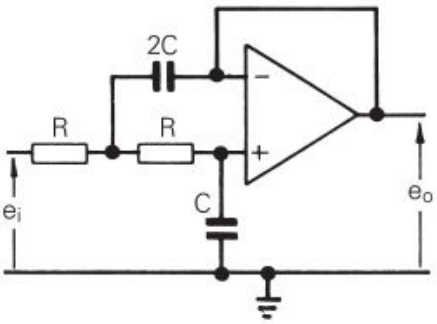
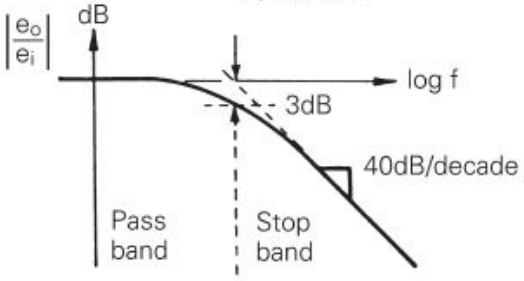


Figure 9.12 *First order low- and high-pass active filters. (a) First order low-pass response. (b) First order high-pass response*

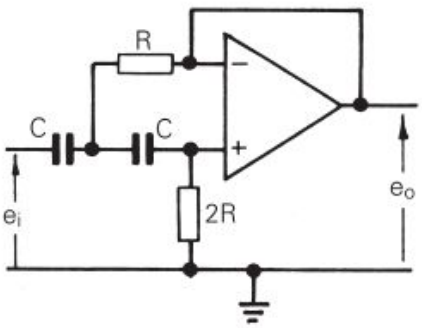


$$f_c = \frac{1}{2\sqrt{2}(\pi CR)} \text{ Hz}$$

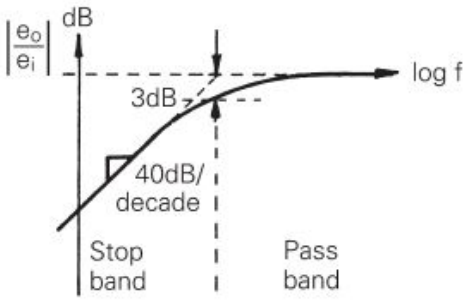


$$\text{Low pass } \frac{e_o}{e_{i(jf)}} = \frac{1}{1-\left(\frac{f}{f_c}\right)^2 + \sqrt{2}\left(j\frac{f}{f_c}\right)}$$

$$\left|\frac{e_o}{e_{i(jf)}}\right| = \frac{1}{\sqrt{\left\{\left[1-\left(\frac{f}{f_c}\right)^2\right]^2 + 2\left(\frac{f}{f_c}\right)^2\right\}}}$$



$$f_c = \frac{1}{2\sqrt{2}(\pi CR)} \text{ Hz}$$



$$\text{High pass } \frac{e_o}{e_{i(jf)}} = \frac{1}{1-\left(\frac{f_c}{f}\right)^2 - \sqrt{2}\left(j\frac{f_c}{f}\right)}$$

$$\left|\frac{e_o}{e_{i(jf)}}\right| = \frac{1}{\sqrt{\left\{\left[1-\left(\frac{f_c}{f}\right)^2\right]^2 + 2\left(\frac{f_c}{f}\right)^2\right\}}}$$

Second order low- and high-pass active filters

UNIT-7 VOLTAGE REGULATORS

Introduction and Series op-amp regulator:

A simple voltage regulator is shown in Figure. This uses an op-ampto drive the base of a power transistor, to turn on the transistor and pass currentfrom the input (*V*in) to the output (*V*out). The accuracy of the output voltagedepends upon both the gain of the op-amp and the transistor, as well as thereference voltage *V*ref. This reference voltage is applied to the non-invertinginput of the op-amp. A potential divider, comprising *R*1 and *R*2, applies afraction of the output voltage to the inverting input of the op-amp. The outputvoltage is stable when the feedback voltage equals the reference voltage.The output voltage equals the reference voltage (developed across *R*1) plus the voltage drop across *R*2. The current through *R*2 is *V*REF/*R*1, therefore:

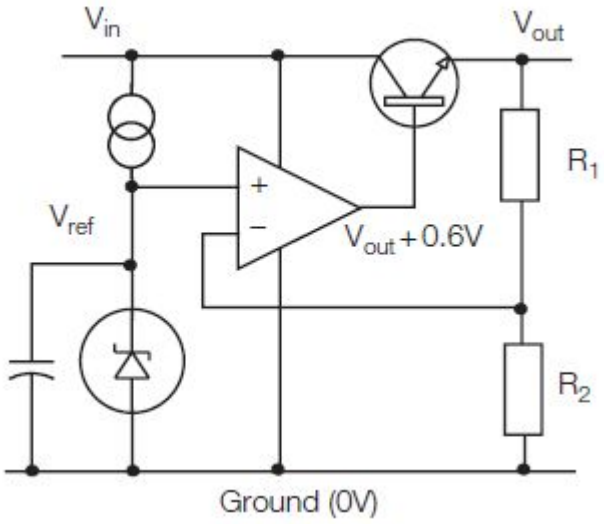
$$V_{OUT} = V_{REF} + R_2\left[\frac{V_{REF}}{R_1}\right]$$

This simplifies to:

$$V_{OUT} = V_{REF}\left[1 + \frac{R_2}{R_1}\right]$$

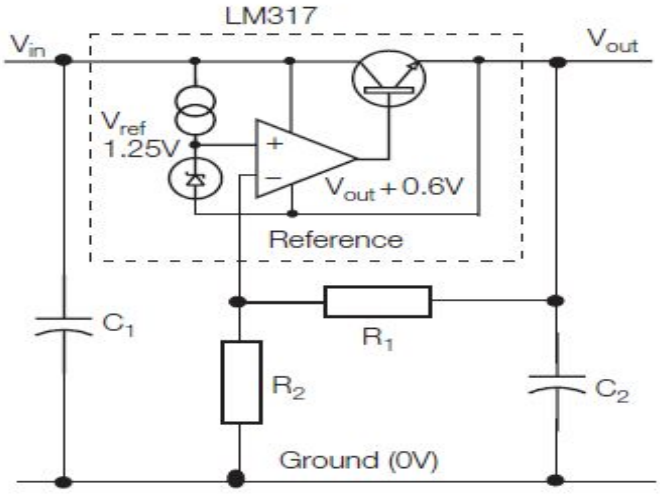
Integrated circuit voltage regulators are popular, because they have currentlimiting outputs and over-temperature shutdown circuits built into them. Onesuch regulator is the LM317, which is produced by a number of manufacturers.This uses external resistors to set the output voltage and a typical circuit is shown in Figure. The reference voltage is a band-gap referenceset at 1.25 V. Resistor *R*1 is usually set at 240 _, to give a nominal5 mA through the potential divider *R*1 and

*R*2. This level of current overcomesany errors due to small current leakage out of the LM317 referenceterminal. The output voltage is given by the equations above. Capacitors *C*1 and *C*2 connected from the input and output terminals to groundare necessary to prevent oscillation.



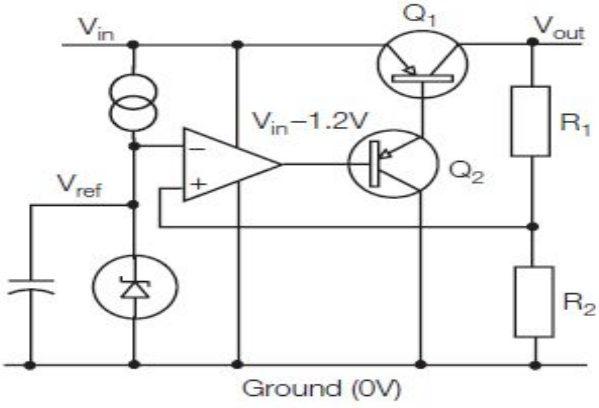
Simple voltage regulator

The disadvantage of the LM317 type of regulator is that the device needsat least 3 V between the input and the output in order to provide power tothe internal circuits. Fixed voltage regulators are slightly better in this regardbecause their internal circuits are able to use the higher potential differencebetween input and ground. However, in a fixed voltage regulator with anintegral output driving NPN transistor, the minimum potential differencebetween *V*in and *V*out must be about 1 V. This is because the base of theNPN transistor must be at least 0.6 V above the output voltage and a fractionof a volt will be dropped across the op-amp output stage.



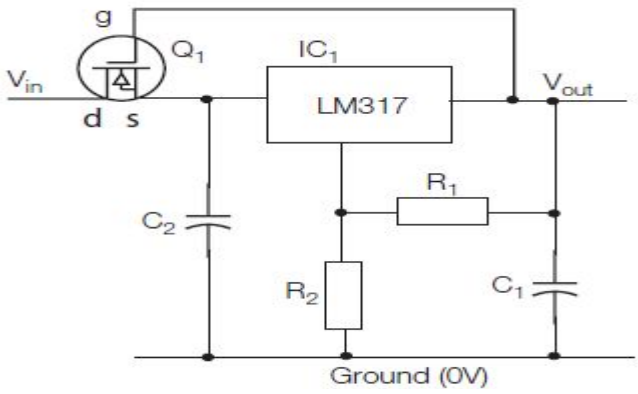
Standard LM317 voltage regulator circuit

A modification to the simple regulator circuit is given in Figure. Thisuses a PNP transistor *Q*1 to drive the output and a second PNP transistor *Q*2to buffer the op-amp output. The op-amp output is held at about *V*in _ 1.2 V.Note that the input terminals of the op-amp are reversed, compared to theregulators shown in Figures. If the voltage at the junction ofresistors*R*1 and *R*2 is higher than *V*ref, the output of the op-amp goes positive,reducing the base current through transistor *Q*2, which in turn reducesthe base drive to transistor *Q*1. This circuit arrangement allows the minimumvoltage between *V*in and *V*out to become very low (about 0.2 V). This is becausethe transistor base drive from the op-amp is relative to *V*in, instead of *V*out.The maximum voltage across a voltage regulator is usually limited to37 V _ 60 V.



Simple low drop-out (LDO) regulator

However, increasing the working voltage range of a regulator is possible usinga high voltage depletion mode MOSFET. The circuit shown in Figure 4.25 hasthe MOSFET *Q*1 preceding the regulator *IC*1. The drain of *Q*1 is connected tothe high voltage supply, the source is connected to *IC*1 input and the gate isconnected to *IC*1 output. A depletion mode MOSFET conducts between drainand source until a voltage that is about 3 V negative, with respect to the source,is applied to the gate. This means that if the regulator has more than about 3 Vdropped across it, the MOSFET conduction decreases and a greater proportionof the applied voltage is dropped across the MOSFET. However, heat dissipationlimits the current that can be supplied from such a circuit, because mostof the power is dissipated by the MOSFET. The LR8 high voltage regulator
from Supertex uses this technique to allow supply voltages of up to 450 V.



High voltage regulator

Current Source

The three terminal fixed voltage regulator can be used as a current source. Figure 6.4(a) shows the circuit where 7805 has been wired to supply a current of 1 ampere to a 10 Ω, 10 watt load.

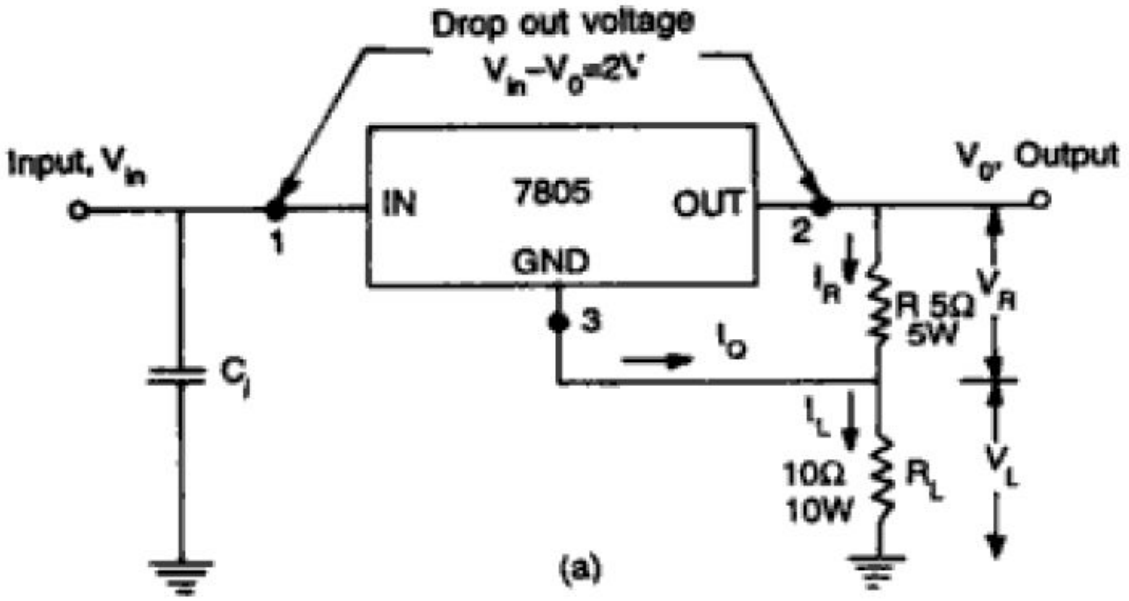
$$I_L = I_R + I_Q$$

where I_Q is the quiescent current and is about 4.2 mA for 7805.

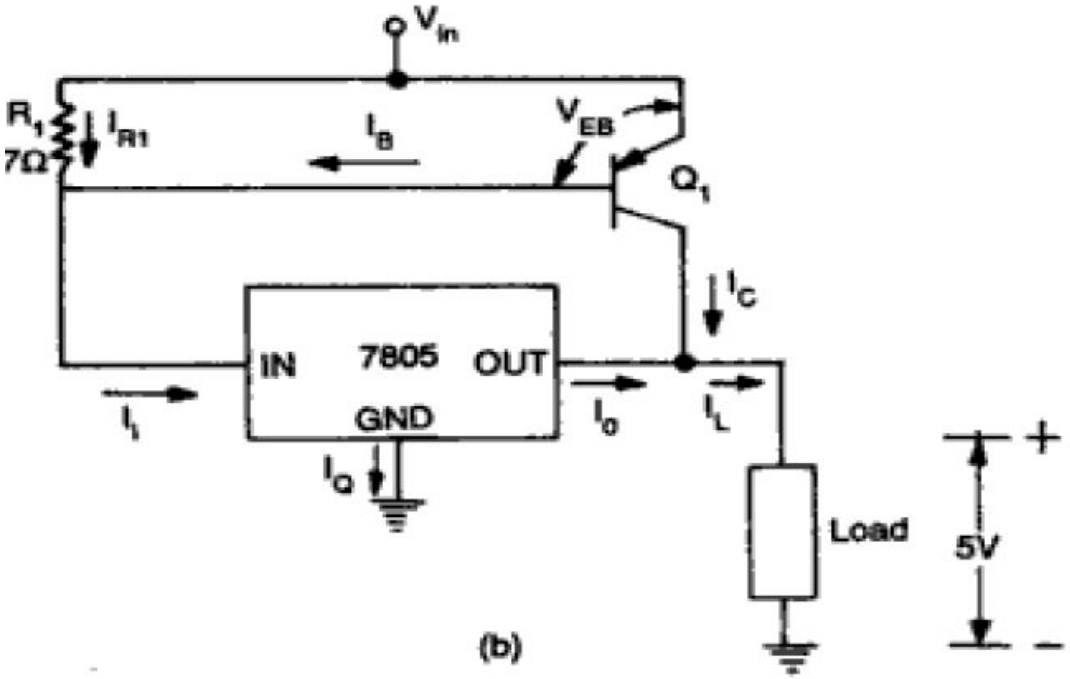
$$I_L = \frac{V_R}{R} + I_Q$$

Since I_L = 1A, $\frac{V_R}{R} \simeq 1A$ ($I_Q << I_L$)

Also V_R = 5 V (Voltage between terminal 2 and 3)



(a) IC 7805 as a current source



(b) Boosting a three terminal regulator

Fixed Regulator used as Adjustable Regulator

In the laboratory, one may need variable regulated voltages or a voltage that is not available as standard fixed voltage regulator. This can be achieved by using a fixed three terminal regulator as shown in Fig. 6.5. Note that the ground (GND) terminal of the fixed three terminal regulator is floating. The output voltage

$$V_o = V_R + V_{pot}$$

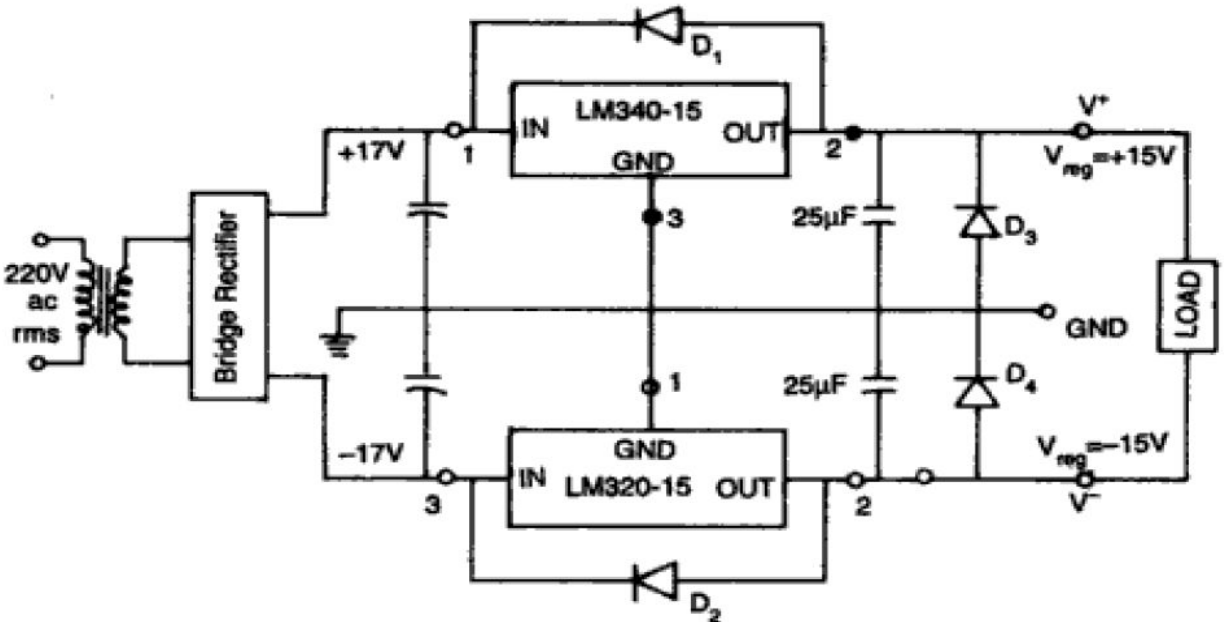
$$= V_R + (I_Q + I_{R1})\, R_2$$

$$= V_R + I_Q R_2 + \frac{V_R}{R_1} R_2$$

$$V_o = (1 + R_2/R_1)\, V_R + R_2 I_Q$$

where V_R is the regulated voltage difference between the OUT and GND terminals. The effect of I_Q is minimized by choosing R_2 small enough to minimize the term $I_Q R_2$. The minimum output voltage is the value of the fixed voltage available from the regulator. The LM117,

properly, both diodes will be reverse biased and will no longer have any effect on the circuit.



An op-amp draws less than 5 mA current, so a 100 mA supply can be used to drive a circuit consisting of 20 op-amps. LM 325H is a dual tracking ± 15V supply and is available in a 10-pin metal-can package and can furnish current upto 100 mA.

723 General purpose voltage regulator

The three terminal regulators discussed earlier have the following limitations:

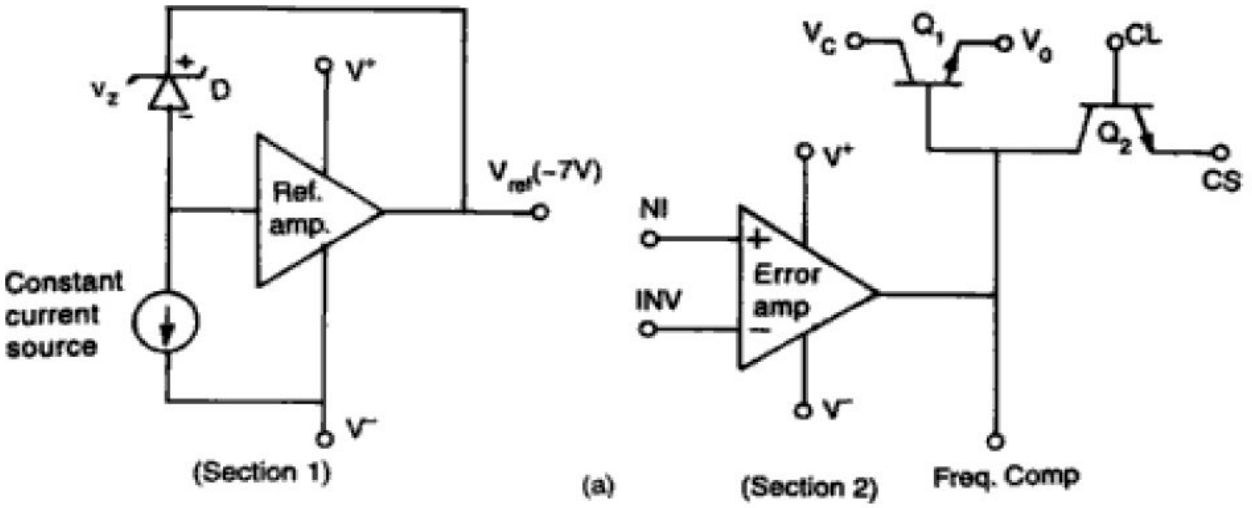
1. Not short circuit protection
2. Output voltage (positive or negative) is fixed.

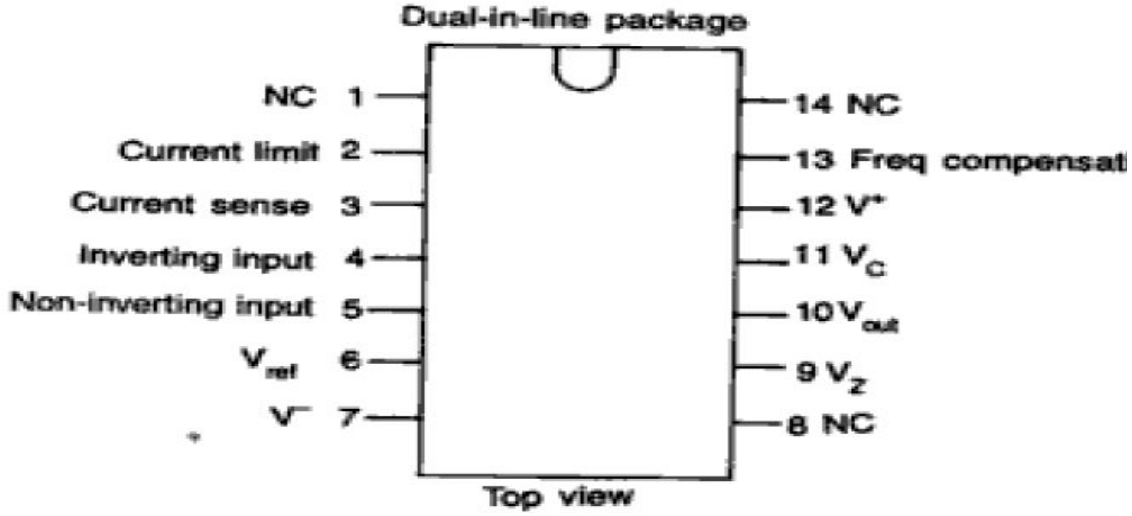
These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This IC is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short circuit current limits.

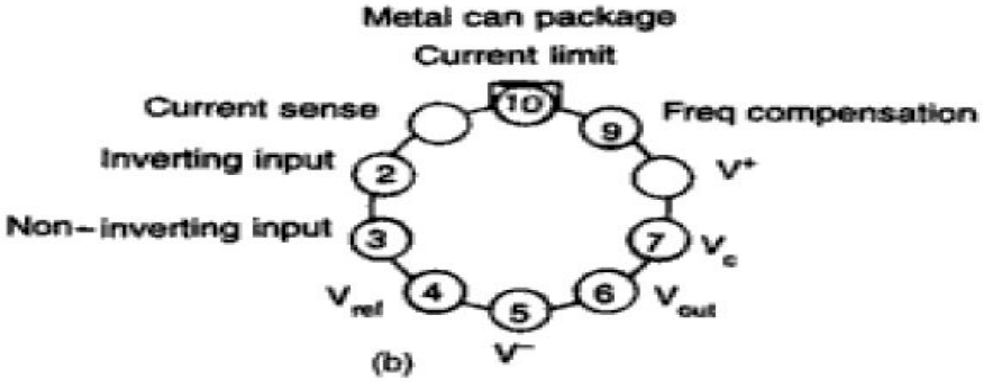
Figure 6.7 (a) shows the functional block diagram of a 723 regulator IC. It has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 volts at the terminal V_{ref}. The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2. The error amplifier compares a sample of the output voltage applied at the INV input terminal to the reference voltage V_{ref} applied at the NI input terminal.

The error signal controls the conduction of Q_1. These two sections are not internally connected but the various points are brought out on the IC package. 723 regulated IC is available in a 14-pin dual-in-line package or 10-pin metal-can as shown in Fig. 6.7(b). The important features and electrical characteristics are given in Table 6.2.







(a) Functional block diagram of 723 regulator

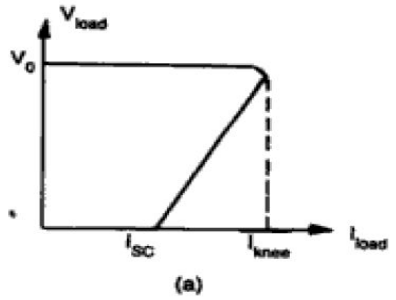
(b) Pin diagram for 14-pin DIP and 10-pin metal can

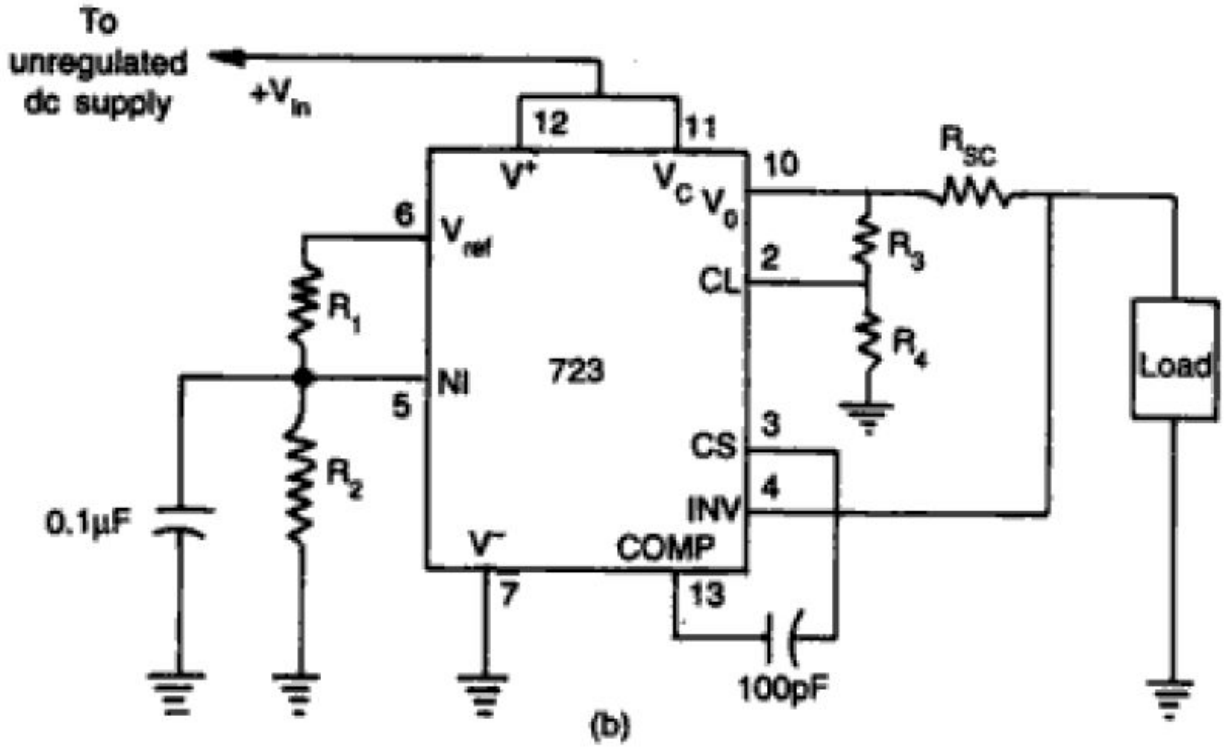
Current foldback:

In current limiting technique, the load current is maintained at a present value and when overload condition occurs, the output voltage V_o drops to zero. However, if the load is short circuited, maximum current does flow through the regulator. To protect the regulator, one must devise a method which will limit the short circuit current and yet allow higher currents to the load.

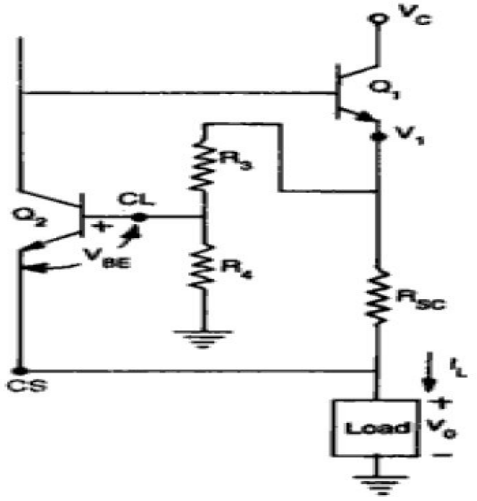
Current foldback is the method used for this. Figure 6.10(a) shows the current foldback characteristic curve. As current demand increases, the output voltage is held constant till a present current level (I_{knee}) is reached. If the current demand exceeds this level, both output voltage and output current decrease. The circuit in Fig. 6.10(b) shows the method of applying current foldback. In order to understand the operation of the circuit, consider the circuit of Fig. 6.10(c). The voltage at terminal CL is divided by $R_3 - R_4$ network. The current limit transistor Q_2 conducts only when the drop across the resistance R_{sc} is large enough to produce a base-emitter voltage of Q_2 to be at least

0.5 V. As Q_2 starts conducting, transistor Q_1 begins to turn off and the current I_L decreases. This reduces the voltage V_1 at the emitter of Q_1 and also the output voltage V_o. The voltage at the base of Q_2 (CL) will be $V_1R_4/(R_3 + R_4)$. Thus the voltage at the CL terminal drops by a smaller amount compared to the drop in voltage at CS terminal. This increases V_{BE} of Q_2 thereby increasing the conduction of Q_2, which in turn reduces the conduction of Q_1. That is, the current I_L further reduces. This process continues till $V_o = 0$V and V_1 is just large enough to keep 0.5V between CL and CS terminal. This point is I_{sc} and has been reduced by lowering both I_L and V_o.





(a) Current fold back characteristic curve (b) A low voltage regulator using current fold back

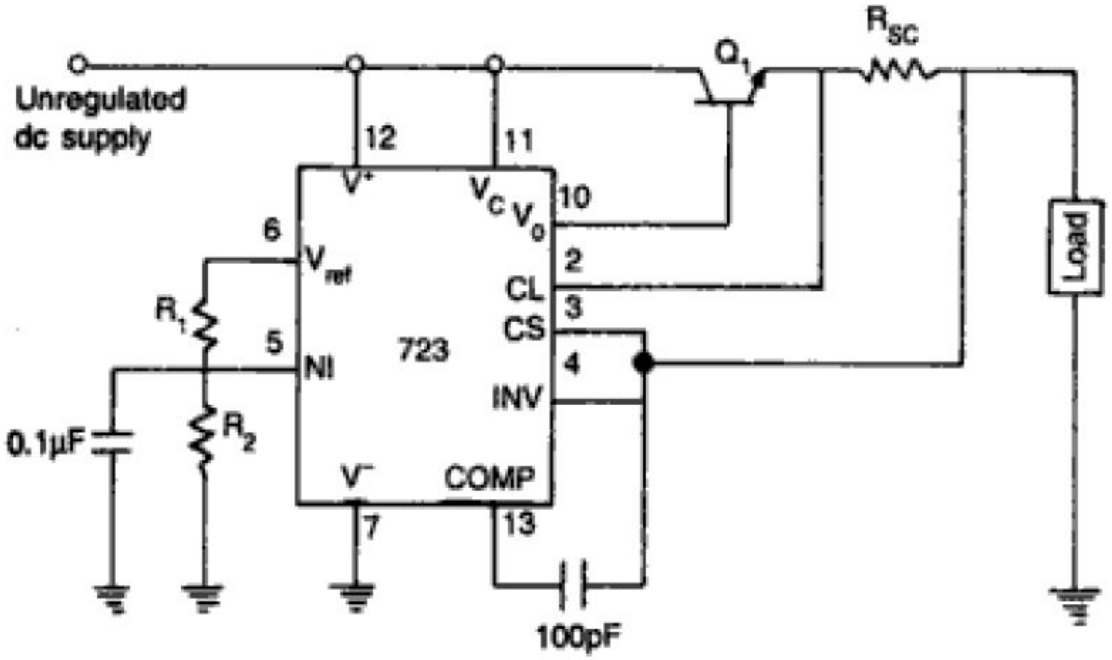


(c) Current fold back (partial schematic)

CURRENT BOOSTING

The maximum current that 723 IC regulator can provide is 140 mA. For many applications, this is not sufficient. It is possible to boost the current level simply by adding a boost transistor Q_1 to the voltage regulator as shown in Fig. 6.11. The collector current of the pass transistor Q_1 comes from the unregulated dc supply. The output current from V_o terminal drives the base of the pass transistor Q_1. This base current gets multiplied by the beta of the pass transistor, so that 723 has to provide only the base current. So,

$$I_{load} = \beta_{pass\ transistor} \times I_{o\ (723)}$$



Current boosted low voltage regulator

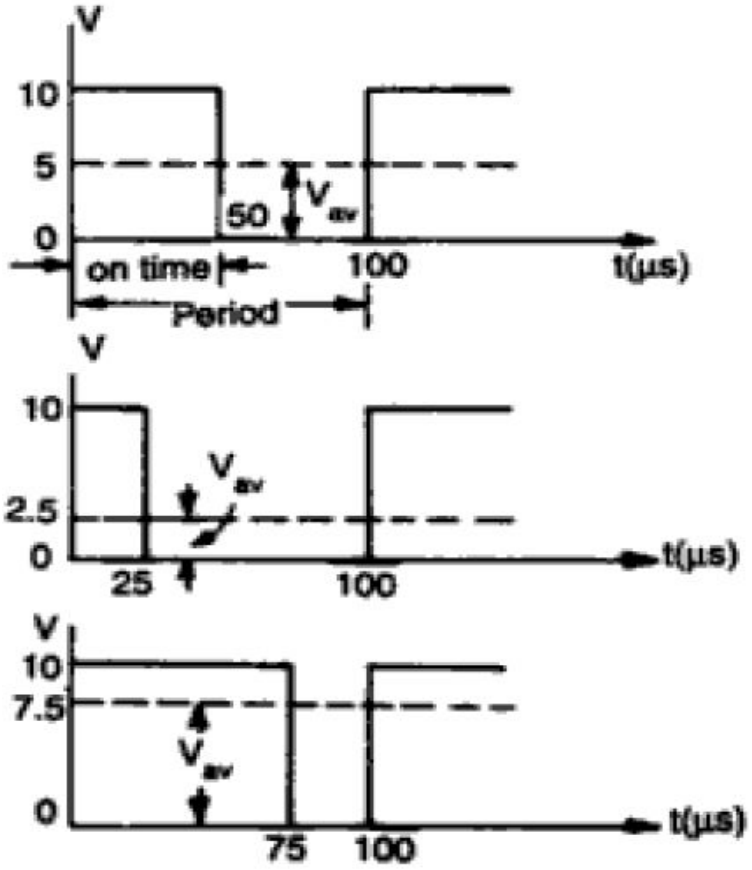
SWITCHING REGULATOR:

The regulated power supplies discussed so far are referred to as linear voltage regulator, since the series pass transistor operates in the linear region. The linear voltage regulator has the following limitations.

The input stepdown transformer is bulky and the most expensive component of the linear regulated power supply mainly because of low line frequency (50 Hz). Because of the low line frequency, large values of filter capacitors are required to decrease the ripple. The efficiency of a series regulator is usually very low (typically 50 percent). The input voltage must be greater than the output voltage. The greater the difference in input-output voltage, more will be the power dissipated in the series pass transistor which is always in the active region. A TTL system regulator (V_o = 5V) when operated at 10V dc input gives 50 percent efficiency and only 25 percent for 20V dc input. Another limitation is that in a system with one dc supply voltage (such as + 5V for TTL) if there is need for ± 15V for op-amp operation, it may not be economically and practically feasible to achieve this.

Switched mode power supplies overcome these difficulties. The switching regulator, also called switched mode regulator operate in a significantly different way from that of a conventional series regulator circuit discussed earlier. In series regulator, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady dc current flow. Whereas, in the case of switched-mode regulator, the pass transistor is used as a "controlled switch" and is operated at either cutoff or saturated state. Hence the power transmitted across the pass device is in discrete pulses rather than as a steady current flow. Greater efficiency is achieved since the pass device is operated as a low impedance switch. When the pass device is at cutoff, there is no current and dissipates no power. Again when the pass device is in saturation, a negligible voltage drop appears across it and thus dissipates only a small amount of average power, providing maximum current to the load. In either case, the power wasted in the pass device is very little and almost all the power is transmitted to the load. Thus efficiency in switched mode power supply is remarkably high–in the range of 70–90%.

Switched mode regulators rely on pulse width modulation to control the average value of the output voltage. The average value of a repetitive pulse waveform depends on the area under the waveform. If the duty cycle is varied as shown in Fig. 6.12, the average value of the voltage changes proportionally.



Pulse width modulation and average value

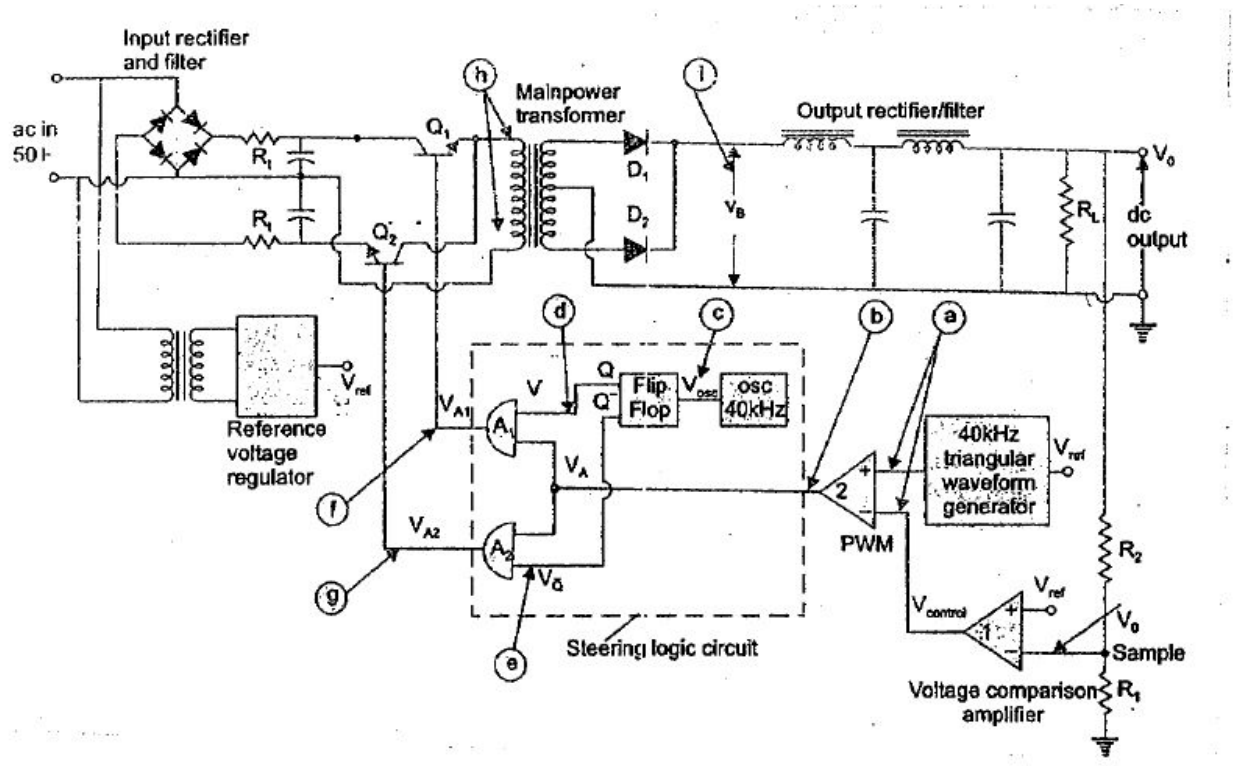
A switching power supply is shown in Fig. 6.13. The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. The thermistor R_t limits the high initial capacitor charge current. The reference regulator is a series pass regulator of the type shown in Fig. 6.1. Its output is a regulated reference voltage V_{ref} which serves as a power supply voltage for all other circuits. The current drawn from V_{ref} is usually very small (~ 10 mA), so the power loss in the series pass regulator does not affect the overall efficiency of the switched mode power supply (SMPS). Transistors Q_1 and Q_2 are alternately switched ***off*** and ***on*** at 20 kHz. These transistors are either fully ***on*** ($V_{CE\ sat}$ ~ 0.2V) or cut-off, so they dissipate very little power. These transistors drive the primary of the main transformer. The secondary is centre-tapped and full wave rectification is achieved by diodes D_1 and D_2. This unidirectional square wave is next filtered through a two stage LC filter to produce output voltage V_o.

The regulation of V_o is achieved by the feedback circuit consisting of a pulse-width modulator and steering logic circuit. The output voltage V_o is sampled by a R_1R_2 divider and a fraction $R_1/(R_1+R_2)$ is compared with a fixed reference voltage V_{ref} in comparator 1. The output of this voltage comparison amplifier is called $V_{control}$ and is shown in Fig. 6.14 (a). $V_{control}$ is applied to the (–) input terminal of comparator 2 and a triangular waveform of frequency 40 kHz (also shown in Fig. 6.14 (a)) is applied at the (+) input terminal. It may be noted that a high frequency triangular waveform is being used to reduce the ripple. The comparator 2 functions as a pulse width modulator and its output is a square wave v_A (Fig. 6.14 (b)) of period $T(f = 40$ kHz). The duty cycle of the square wave is $T_1/(T_1 + T_2)$ and varies with $V_{control}$ which in turn varies with the variation of v_o. The output v_A drives a steering logic circuit shown in the dashed block. It consists of a 40 kHz oscillator cascaded with a flip-flop to produce two complementary outputs v_Q and $v_{\overline{Q}}$ shown in Fig. 6.14 (d) and (e). The output v_{A1} and v_{A2} of AND gates A_1 and A_2 are shown in Fig. 6.10 (f) and (g). These waveforms are applied at the base of transistor Q_1 and Q_2. Depending upon whether transistor Q_1 or Q_2 is ***on***, the waveform at the input of the transformer will be a square wave as shown in Fig. 6.14 (h). The rectified output v_B is shown in Fig. 6.14 (i).

An inspection of Fig. 6.13 shows that the output current passes through the power switch consisting of transistors Q_1 and Q_2, inductor having low resistance and the load. Hence using a switch with low losses (transistor with small $V_{CE\,(sat)}$ and high switching speed) and a filter with high quality factor, the conversion efficiency can easily exceed 90%.

If there is a rise in dc output voltage V_o, the voltage control $V_{control}$ of the comparator 1 also rises. This changes the intersection of the $V_{control}$ with the triangular waveform and in this case decreases the time period T_1 in the waveform of Fig. 6.14 (b). This in turn decreases the pulse width of the waveform driving the main power transformer. Reduction in pulse width lowers the average value of the dc output V_o. Thus the initial rise in the dc output voltage V_o has been nullified.

So far we have discussed the operation of the SMPS. Now we shall be able to justify why SMPS has better efficiency than linear regulated power supply. We have noted that very high frequency signals (about 40 kHz or more) are being applied. The transistors Q_1 and Q_2 are acting as the switches and become alternately ***on*** and ***off*** at a frequency of 20 kHz (Fig. 6.14 (a)). Again the transistor Q_1 or Q_2 is ***on*** for very small duration and consumes negligibly small power since $V_{CE\,(sat)}$ (0.2V) is small. It may also be noted that the high operating frequency used for the switching transistors allows the use of smaller transformers, capacitors and inductors. This allows a decrease in size and cost.



UNIT-8

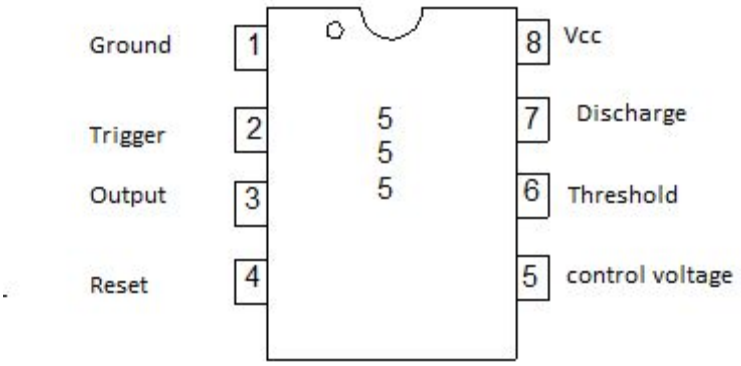
OTHER LINEAR IC APPLICATIONS

555 Timer:

-a stable device which will give accurate time delay. Hence called timers and since we use 3 5k resistors in the internal circuitry,it is called 555 timer.

-available in many forms, circular IC with 8 pins and usual 8 pin IC and 16 pin IC with dual in package.
Counter time:
Timer+ programmable binary counter,
-delay can be in the range of days.

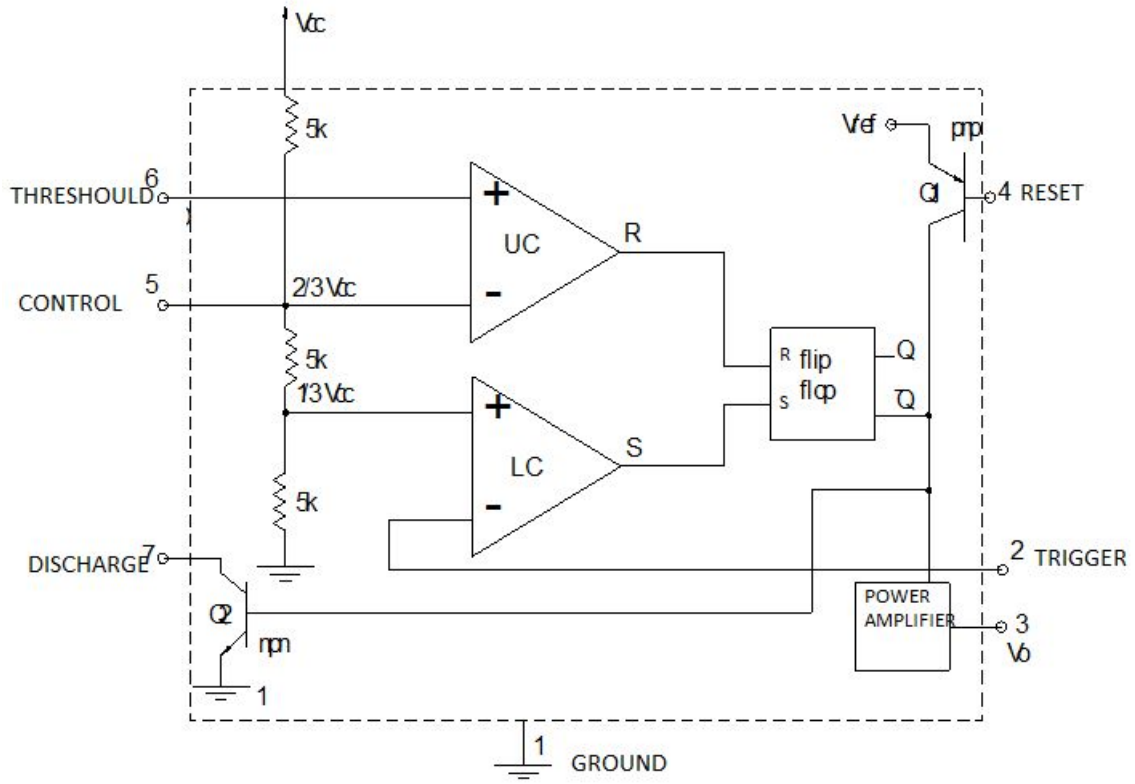
TERMINALS OF THE 555:



pin connections.

-since the range of Vcc that can be applied is very vast,we can use it for many applications.
-current it can handle is about 200mA
-compatible with TTL and CMOs.

INTERNAL BLOCK DIAGRAM OF 555 TIMER.



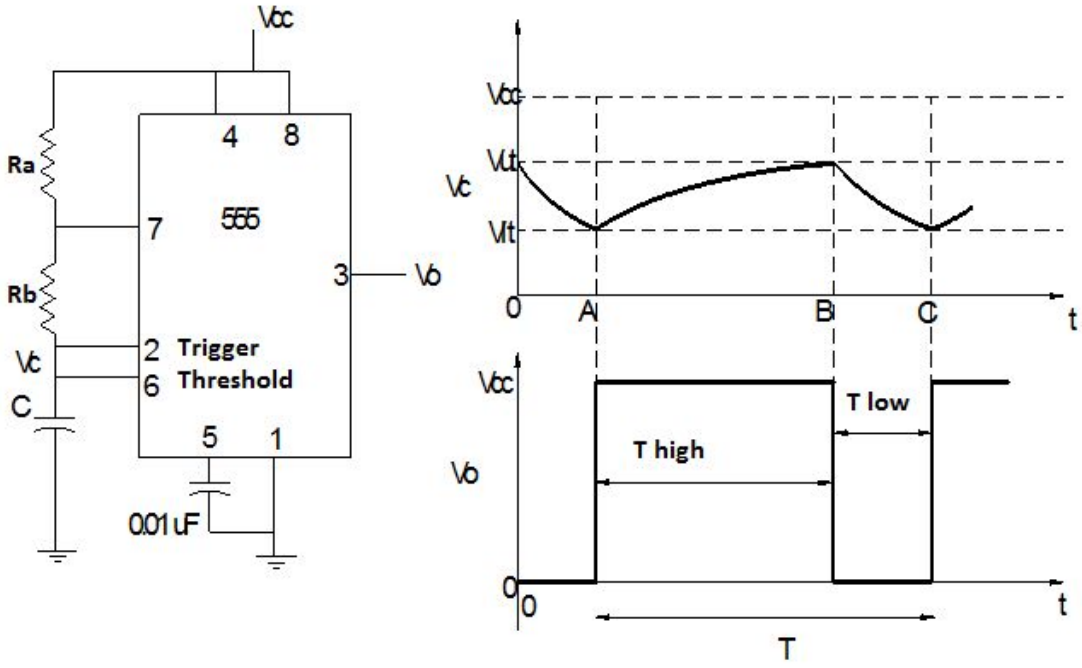
When the triggering pulse is less than (1/3)Vcc, Vid is positive, Output of comparator is +ve which is given to s-Q becomes 1 and thus the output will be 1.Hence called trigger.

We can change the reference voltage for comparison by connecting some other source at pin num 5.Voltage reference for lower comparator will be (Vref/2).

When we don't want different voltages as reference, usually we connect a by-pass capacitor of 0.01uf to eliminate the effect of noise signals.

When Q is zero, pin num 7 is activated, so discharging of capacitor takes place through the transistor.

ASTABLE MULTIVIBRATOR:



The above circuit shows 555 timer work in astable mode. Let us assume that the output is 1 which implies the output to the power amplifier/the inverter is zero., which means transistor is off and hence the capacitor starts charging towards Vcc, but the moment Vc reaches the ref voltage for upper comparator, the output of that comparator will reset the flip-flop. thus Q becomes zero and thus the transistor is on and the capacitor discharges through the transistor. And again while discharging when the capacitor discharges to (1/3)vcc, Q will be 1 and the capacitor starts charging.

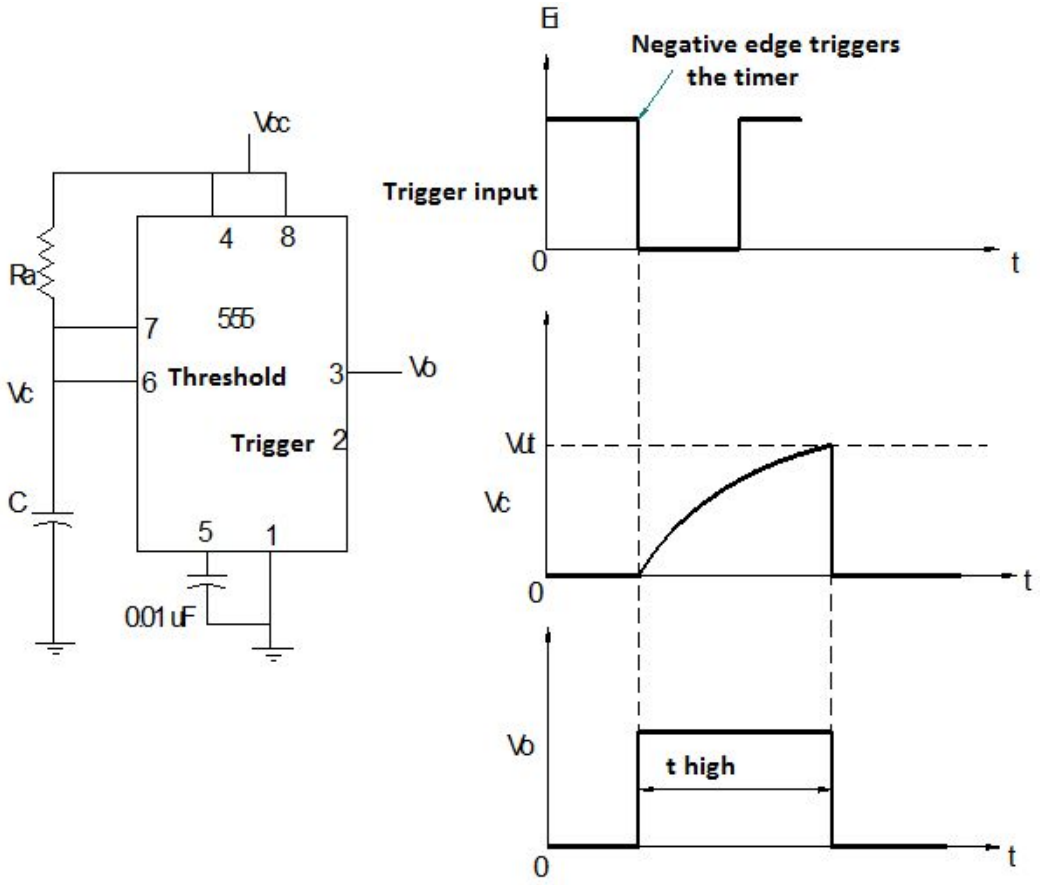
T=Thigh + Tlow.
Thigh=0.693(Ra+Rb)C.
Tlow =0.693RbC
Therefore, T=0.693(Ra+2Rb)C.
f=1.443/(Ra+2Rb)C-frequency of oscillation. Thus Th>Tl and thus it is not possible to generate a square wave.

Duty cycle in case of 555 timer=Tlow/T.Thus for the above ckt,duty cycle will always be less than 50%.
So we connect a diode across Rb in such a way that the positive is towards Vcc.Thus the capacitor will charge only through Ra since diode will be forward biased during charging.

Thus when the Ra and Rb both are same,we get a square wave.

Thus, the frequency of oscillation now will be f=1.44/(Ra+Rb)C.

MONOSTABLE MULTIVIBRATOR:



The working of a 555 timer in monostable mode is as shown in the fig., The trigger pulse is given to the pin num 2 of the timer.When there is a negative edge in the input,then the output of the lower comparator goes positive (high),thus setting the flip-flop ,thus the capacitor starts charging and when it reaches the refernce voltage of upper comparator(2/3)vcc,then output of the upper comparator goes high,thus Q will be zero and the capacitor starts discharging .Thus the output switches from high to low at that point which is clear from the above plot.
T=(Ln3)RC=1.11RC.

Tlow will be approximately zero since there is no resistor in the discharging path of the capacitor.Thus we get only one quasi state and hence called monostablemultivibrator or one shot multivibrator.

Phase-Locked Loops

INTRODUCTION

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

BASIC PRINCIPLES

The basic block schematic of the PLL is shown in Fig. 9.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO)

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency

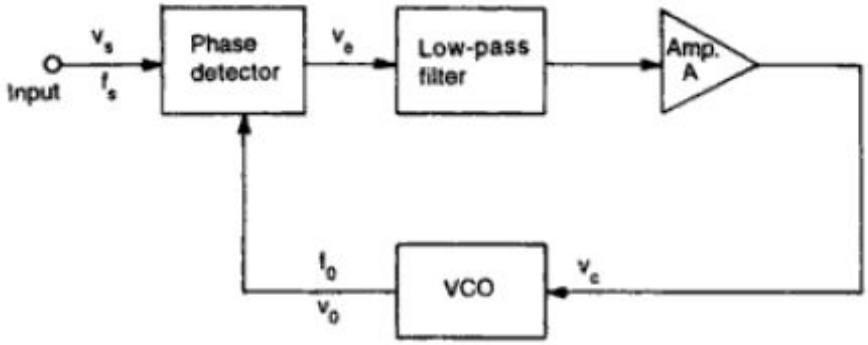
and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ components at its output. The high frequency component $(f_s + f_0)$ is removed by the low pass filter and the difference frequency

component is amplified and then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_0. Once this action starts, we say that the signal is in the capture range. The VCO continues to change

frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_0 to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Figure 9.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

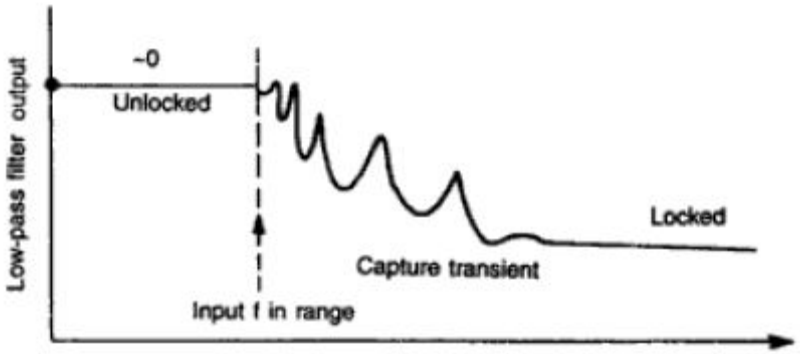
The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.



Block schematic of the PLL

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o, the VCO frequency.

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.



The capture transient

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

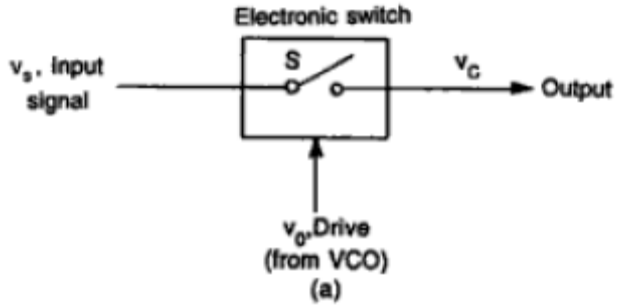
PHASE DETECTOR/COMPARATOR

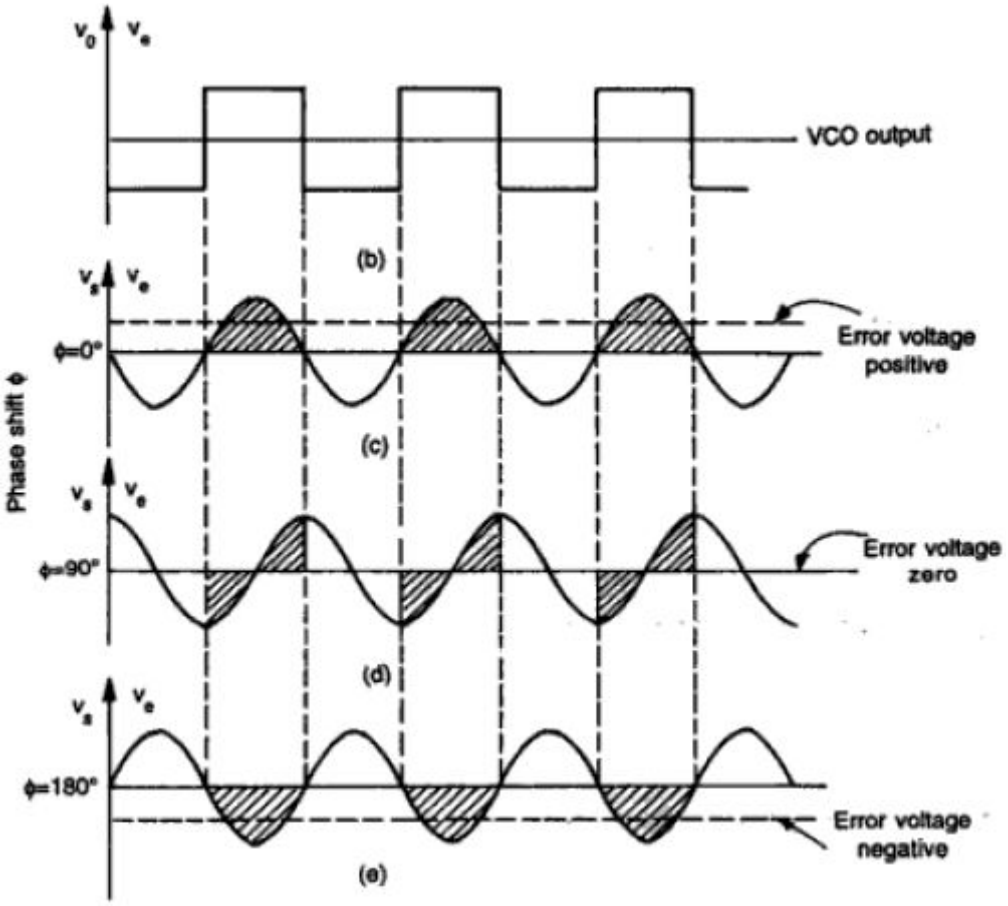
The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.

Analog Phase Detector

The principle of analog phase detection using switch type phase detector is shown in Fig. 9.3(a). An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) as shown in Fig. 9.3(b). The input signal is, therefore, chopped at a repetition rate determined by VCO frequency. Figure 9.3(c) shows the input signal v_s assumed to be in phase ($\phi = 0°$) with VCO output v_0. Since the switch S is closed only when VCO output is positive, the output waveform v_e will be half sinusoids (shown hatched). Similarly, the output waveform for $\phi = 90°$ and $\phi = 180°$ is shown in Fig. 9.3(d, e). This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged. The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in Fig. 9.3(c, d, e).

It may be seen that the error voltage is zero when the phase shift between the two inputs is 90°. So, for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.





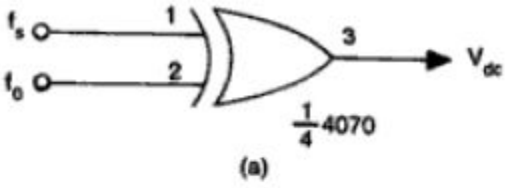
Phase detector for PLL (a) Basic scheme (b) VCO output waveform. Input and output waveform (hatched) of phase detector for (c) $\phi = 0$ (d) $\phi = 90°$ (e) $\phi = 180°$

Digital Phase Detector

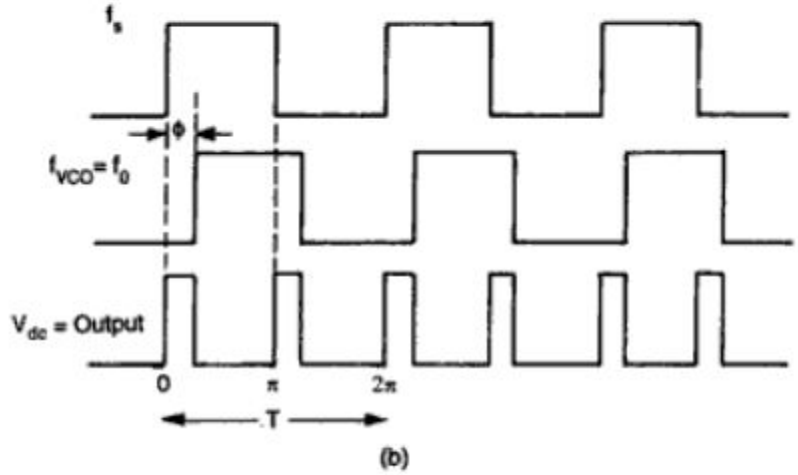
Figure 9.5(a) shows the digital type XOR (Exclusive–OR) phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR gate is high when only one of the inputs signals f_s or f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_o$ are shown

in Fig. 9.5(b). In this figure, f_s is leading f_o by ϕ degrees. The variation of dc output voltage with phase difference ϕ is shown in Fig. 9.5(c). It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout. The slope of the curve gives the conversion ratio k_ϕ of the phase detector. So, the conversion ration K_ϕ for a supply voltage V_{cc} = 5V is,

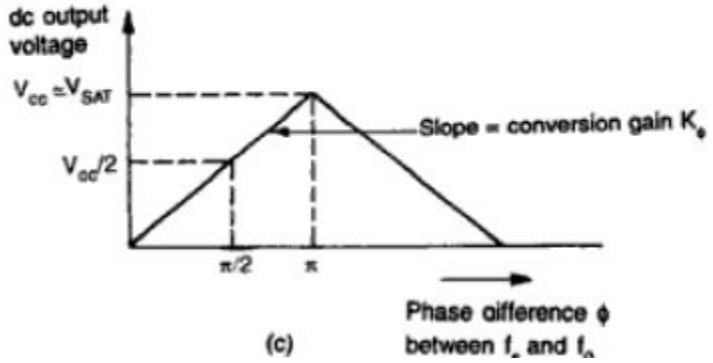
$$K_\phi = \frac{5}{\pi} = 1.59\ V/\text{rad}$$



(a)



(b)

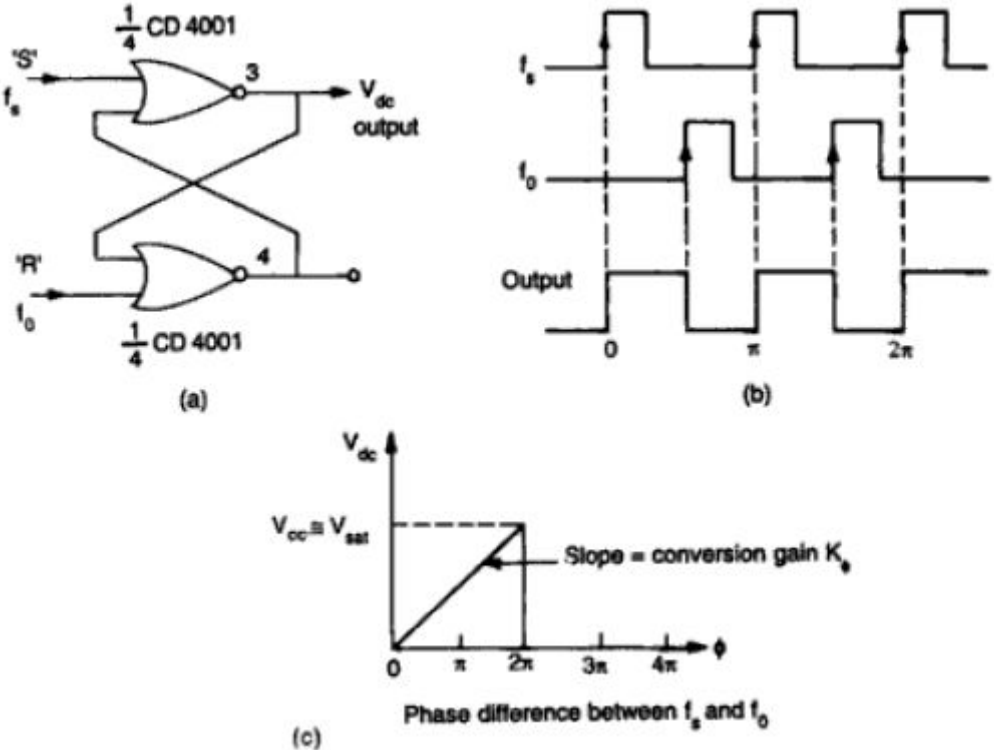


(c)

(a) Exclusive-OR phase detector (b) Input and output waveforms
(c) DC output voltage versus phase difference ϕ curve

Another type of digital phase detector is an edge-triggered phase detector as shown in Fig. 9.6(a). The circuit is an R-S flip-flop made by NOR gates, such as CD 4001. This circuit is useful when f_s (incoming signal) and f_o (VCO output) are both pulse waveforms with duty cycle less than 50 percent. The output of the R-S flip-flop changes its state on the leading edge of f_s and f_o as shown in Fig. 9.6(b). The variation of dc output voltage vs phase difference between f_s and f_o is shown in Fig. 9.6(c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear upto 360° compared to 180° in the case of Exclusive-OR detector.

Digital phase detector is also available in independent monolithic IC form. A typical example is MC4344/4044. This IC gives input/output transfer characteristics which is linear upto 4π radians or 720°.



(a) Edge-triggered phase detector using CD4001, Quad 2-input NOR gate (b) Input and output waveforms (c) dc output voltage vs phase difference ϕ

VOLTAGE CONTROLLED OSCILLATOR (VCO)

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 9.7(a, b). Referring to Fig. 9.7(b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{cc} and 0.5 V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{cc} to 0.25 V_{cc}. In Fig. 9.7(c), when the voltage on the capacitor C_T exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt

trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The output waveforms are shown in Fig. 9.7(c).

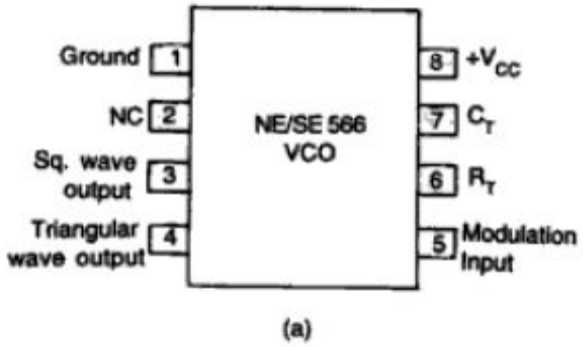
The output frequency of the VCO can be calculated as follows:

The total voltage on the capacitor changes from 0.25 V_{cc} to 0.5 V_{cc}. Thus $\Delta v = 0.25\ V_{cc}$. The capacitor chargers with a constant current source.

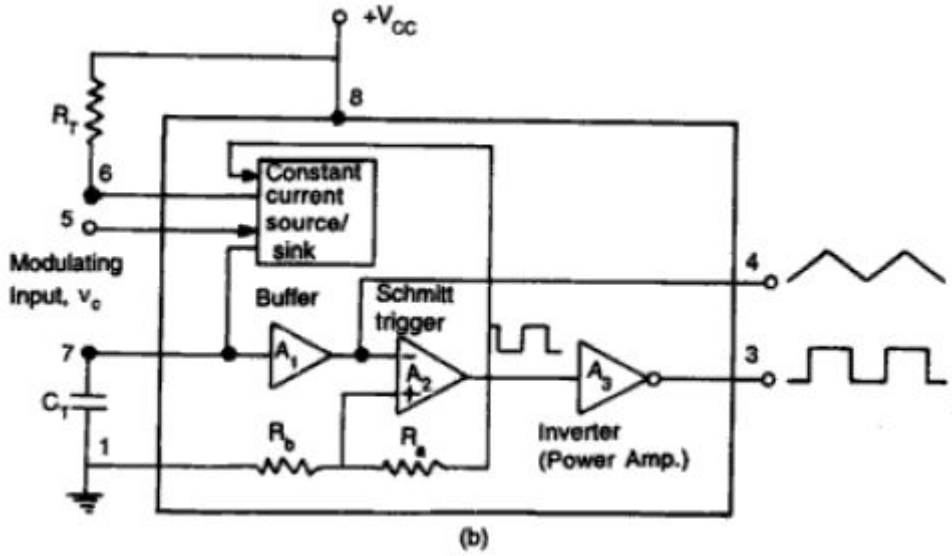
So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25\ V_{cc}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\ V_{cc} C_T}{i}$$



$$f_o = \frac{2(V_{cc} - (7/8)V_{cc})}{C_T R_T V_{cc}} = \frac{1}{4R_T C_T} = \frac{0.25}{R_T C_T}$$



Voltage controlled oscillator (a) Pin configuration (b) Block diagram

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_0}{\Delta v_c}$$

Here Δv_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o$$

$$= \frac{2(V_{cc} - v_c + \Delta v_c)}{C_T R_T V_{cc}} - \frac{2(V_{cc} - v_c)}{C_T R_T V_{cc}}$$

$$= \frac{2\,\Delta v_c}{C_T R_T V_{cc}}$$

or, $$\Delta v_c = \frac{\Delta f_o\, C_T R_T V_{cc}}{2}$$

Putting the value of $C_T R_T$ from Eq. (9.11)

$$\Delta v_c = \Delta f_o\, V_{cc}/8 f_o$$

or, $$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8 f_o}{V_{cc}}$$

MONOLITHIC PHASE-LOCKED LOOP

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However, a number of manufacturers have introduced monolithic PLLs too. Some of the important monolithic PLLs are SE/NE560 series introduced by Signetics and LM560 series by National Semiconductor. The SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. Since 565 is the most commonly used PLL, we will discuss some of the important features of this IC chip.

IC PLL 565

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in Fig. 9.9(a, b). The output frequency of the VCO (both inputs 2, 3 grounded) as given by Eq. (9.11) can be rewritten as,

$$f_o = \frac{0.25}{R_T C_T} \text{ Hz}$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and the

phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 kΩ.

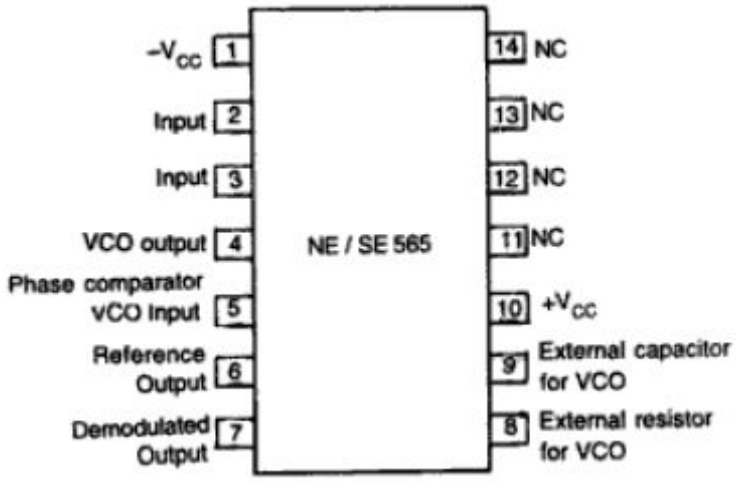
In Fig. 9.10, a complete diagram of LM565 (National Semiconductor) IC PLL is presented. The analog phase detector is comprised of the Q_1–Q_2, Q_3–Q_4 and Q_5–Q_6 differential amplifier pairs with Q_{37} together with R_3 (200 Ω) serving as a current sink bias source. Resistors R_1 and R_2 (each 7.2 kΩ) serve as the load for the phase detector. The output voltage of the phase detector is limited by the diode-connected transistors Q_7 and Q_8 to a maximum of ± 0.7 V which minimizes the

$$v_c = AK_\phi(\phi - \pi/2)$$

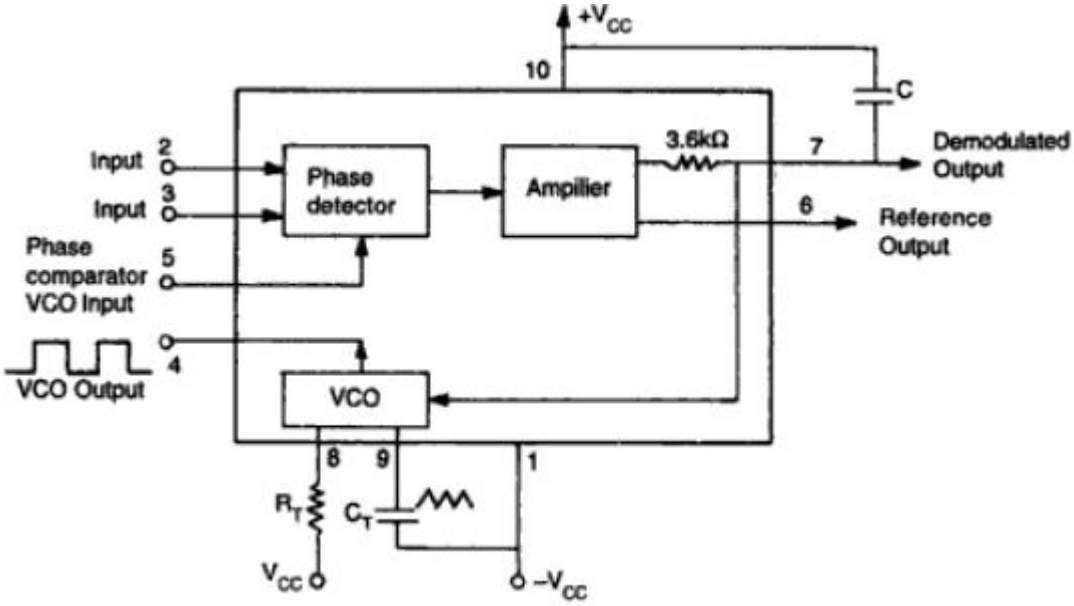
where A is the voltage gain of the amplifier. This v_c shifts VCO frequency from its free running frequency f_o to a frequency f given by,

$$f = f_o + K_v v_c$$

where K_v is the voltage to frequency transfer coefficient of the VCO. When PLL is locked-in to signal frequency f_s, then we have



Pin diagram



NE/SE565 PLL block diagram

$$f = f_s = f_o + K_v v_c$$

since, $$v_c = (f_s - f_o)/K_v = A K_\phi (\phi - \pi/2)$$

Thus, $$\phi = \pi/2 + (f_s - f_o)/K_v K_\phi A$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian (see in Fig. 9.4(c) and v_e (max) $= \pm K_\phi \pi/2$ from Eq. (9.6). The corresponding value of the maximum control voltage available to drive the VCO will be,

$$v_{c(max)} = \pm (\pi/2)\, K_\phi A$$

The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_o)_{max} = K_v\, v_{c(max)} = K_v K_\phi A\, (\pi/2)$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_o \pm (f - f_o)_{max}$$

$$= f_o \pm K_v K_\phi (\pi/2) A = f_o \pm \Delta f_L$$

where $2\,\Delta f_L$ will be the lock-in frequency range and is given by,

$$\text{lock-in range} = 2\,\Delta f_L = K_v K_\phi A\, \pi$$

or,

$$\Delta f_L = \pm K_v K_\phi A\, (\pi/2)$$

The lock-in range is symmetrically located with respect to VCO free running frequency f_o. For IC PLL 565,

$$K_v = \frac{8 f_o}{V} \quad \text{(from Eq. (9.15))}$$

where

$$V = +V_{cc} - (-V_{cc})$$

Again,

$$K_\phi = \frac{1.4}{\pi} \quad \text{(from Eq. (9.17))}$$

and

$$A = 1.4$$

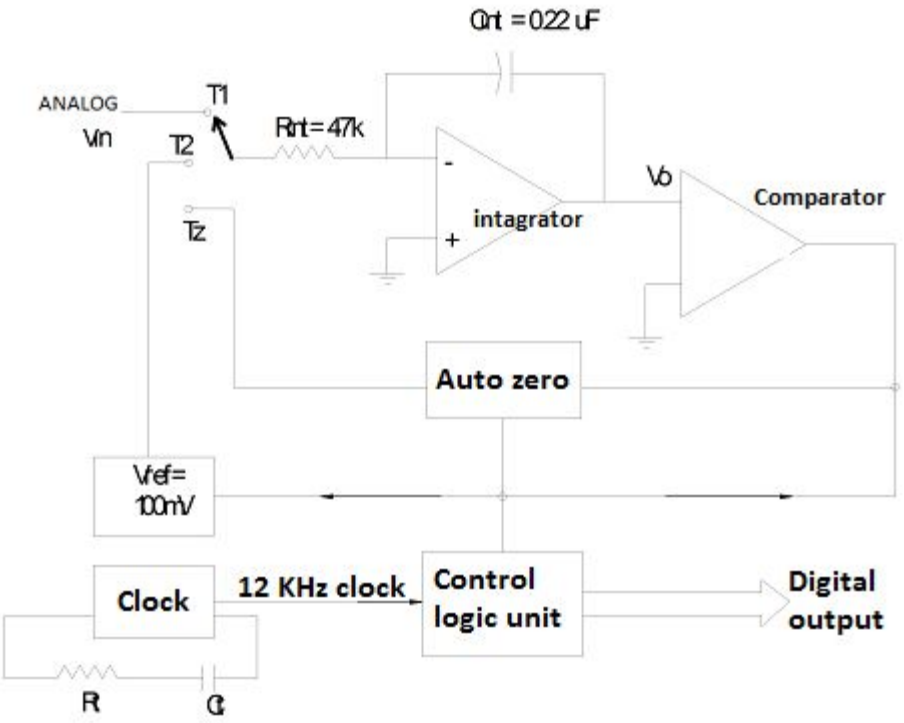
Hence the lock-in range from Eq. (9.28) becomes,

$$\Delta f_L = \pm 7.8\, f_o/V$$

ANALOG TO DIGITAL CONVERTERS

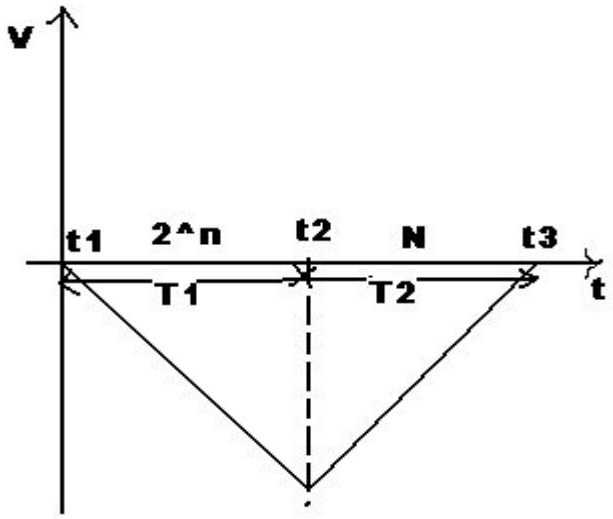
They are circuits which convert analog signals to digital signals. There are different catogories. 1.Slowest integrating ADC-conversion time is 300ms.-used in measuring slowly varying DC voltages. 2.Faster successive approximation ADC-conversion time-few microseconds, -used to digitalize audio signals. 3.Fastest flash ADC-normally used to digitalize video signals

Integrating type ADC consists of 2 op-amps ,one working as a integrator and the other working as a zero crossing detector.The output of the integrator is fed as the input to the zero crossing detector.thus ,it can be easily observed that whenever The output of the control logic changes switch position from Vin to Vref,ZCD changes it's output.



INTEGRATING ADC/DUAL SLOPE ADC.

When Vin is positive,integrator would give negative ramp and Vref would be negative at that time.Once the capacitor reaches the final integrated value,control logic will switch it's output from Vin to –Vref and thus the output of the integrator changes it's slope.It will count 2^n clock pulses during this time which is equivalent to N digital counts.
N=(Vi/Vref)2^n.,where n-number of bits and N-digital count.



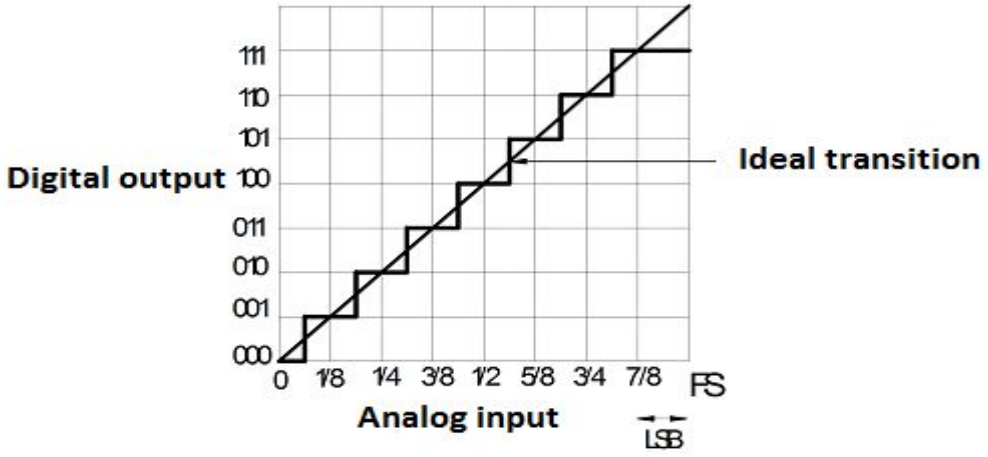
From the plot, it is clear that we will get 2 different slopes in the functioning of integrating type ADC..Thus it is also called as dual slope ADC.

ADC CHARACTERISTICS.

Resolution-Resolution is also defined as the ratio of change of input voltage, Vi needed to change the digital output by 1LSB.

Resolution=Vifs/((2^n)-1),where Vifs is the value of the full scale input voltage.
Digital output code=binary equivalent of D,D-num of LSBs in the digital output.
D=Vi/resolution.

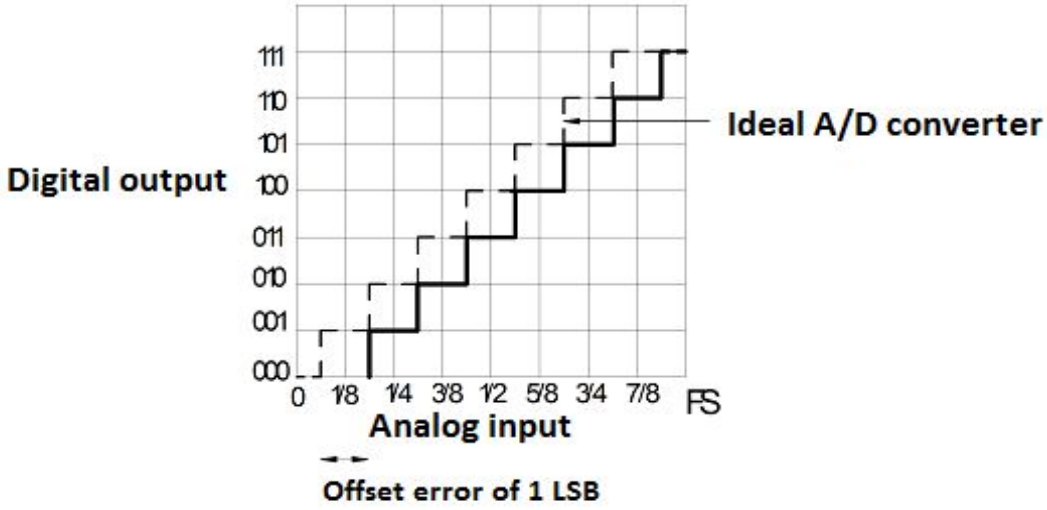
QUANTISATION ERROR.



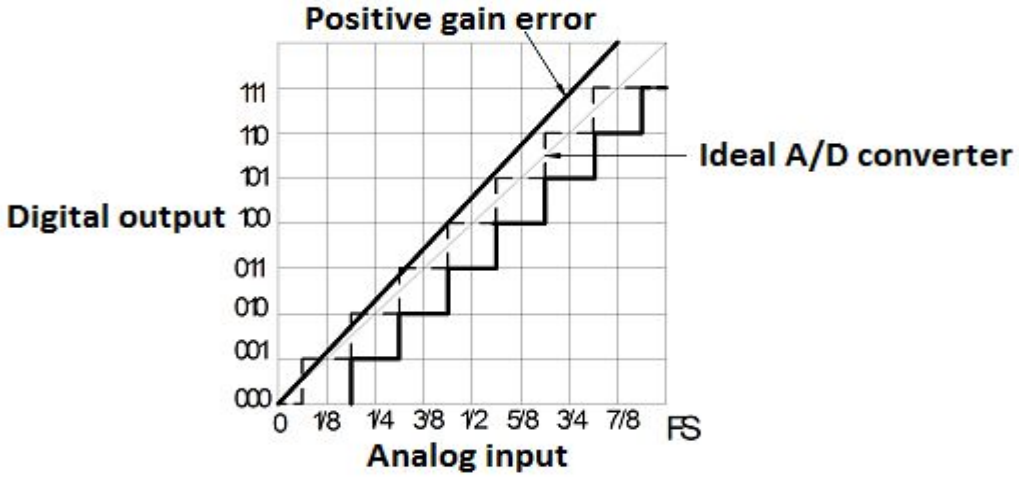
From the graph ,it is clear that there is a difference between actual transition and the actual transition which can be regarded as 0.5 LSB(positive or negative).And can be totally regarded as quantization error of 1 LSB,

OFFSET ERROR

In circuits, usually we get some output without application of any input which is referred to as offset error. To minimize, we first measure the output without applying any input and the most approximated output is got by subtracting the error output from the actual one got.



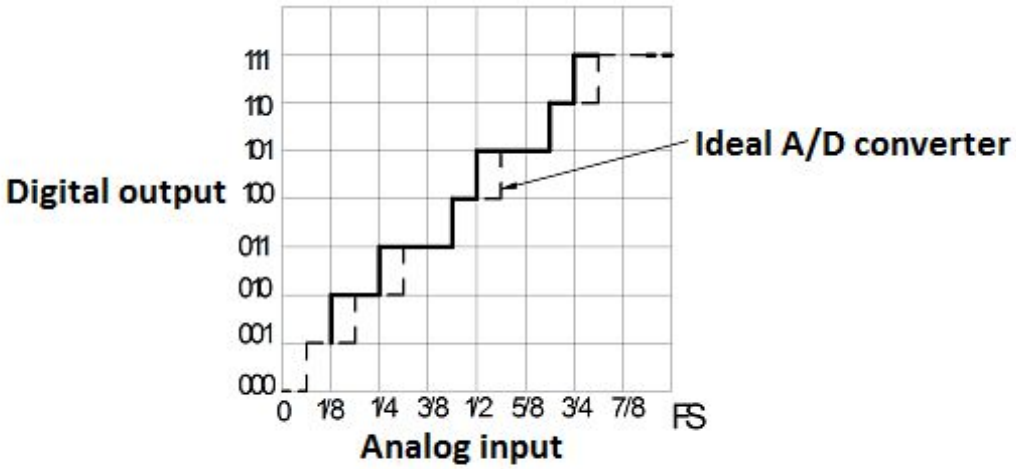
GAIN ERROR:



Gain error will be less during initial stages i.e., when the input is low and increases as the input increases which can be easily visualized from the above graph.

LINEARITY ERROR:

In this case,the initial and final values will be same and only the intermediate values changes and it can be easily visualised in the above graph.



FREQUENCY RESPONSE OF ADCs

Usually in ADCs, the error should not exceed total of 1 LSB, if it exceeds, it will be regarded as aperture error. And output depends on the amplitude peak and frequency of the input. The maximum frequency for which output is digitalized without any distortion is fmax=1/(2*pi*Tc*(2^n)).,where Tc-conversion time.

Digital to Analog converters

There are several circuit arrangements for digital-to-analogue converters (DACs). The three main classes of DACs are: decoder-based DACs, binary weighted DACs (including *R*–2*R* converters), and thermometer code DACs. The output from a DAC should be band limited to prevent switching spikes from appearing at the output. These spikes, or glitches, are usually at the clock frequency or higher.

Binary-weighted DACs

Since binary numbers represent digital words, individual bits have binary weights depending on their position within the digital word. A simple summing amplifier can be used to convert a digital word to its analogue value, by arranging for each bit to contribute a current equal to its binary weight. This principle is used in binary weighted DACs in two different implementations.

In the first implementation, the resistor values increase by a factor of two as the bit becomes less significant. The circuit of a binary-weighted resistor DAC is illustrated in Figure . When the value of the digital bits is at logic 1, the current through the binary-weighted resistance is diverted to flow through the feedback resistor, *R*f. When the digital bit is at logic 0, the current flows directly to ground.

The current flowing through the resistors in either position of the switch is constant. This is because the op-amp's inverting input is acting as a 'virtual earth' due to feedback, and is at earth potential. So, the potential on one side of each resistor is at *V*ref and the other side is at 0 V.

*I*4 _ *V*ref /2*R*

*I*3 _ *V*ref /4*R*

*I*2 _ *V*ref /8*R*

*I*1 _ *V*ref/16*R*

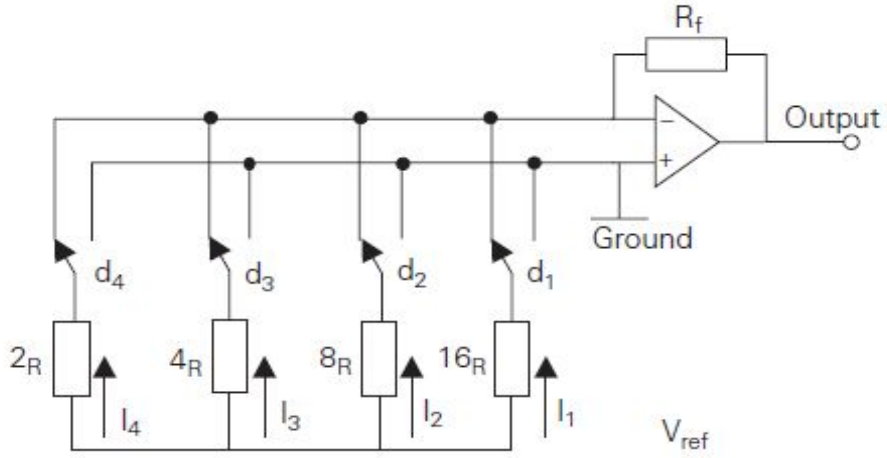
If the feedback resistor value is *R*, the buffer's output voltage range is 0 V to _15/16*V*ref.

The accuracy of a binary-weighted resistor DAC is dependent on the matching between different resistors used in the circuit. It is difficult to obtain a good match of resistors in an integrated circuit. When the range of resistor values is very large, matching them becomes the dominant problem. For example, with a 14-bit binary-weighted resistor DAC, the range of resistor values can vary by over four orders of magnitude. Therefore, the use of binary-weighted resistors can result in large mismatch errors.

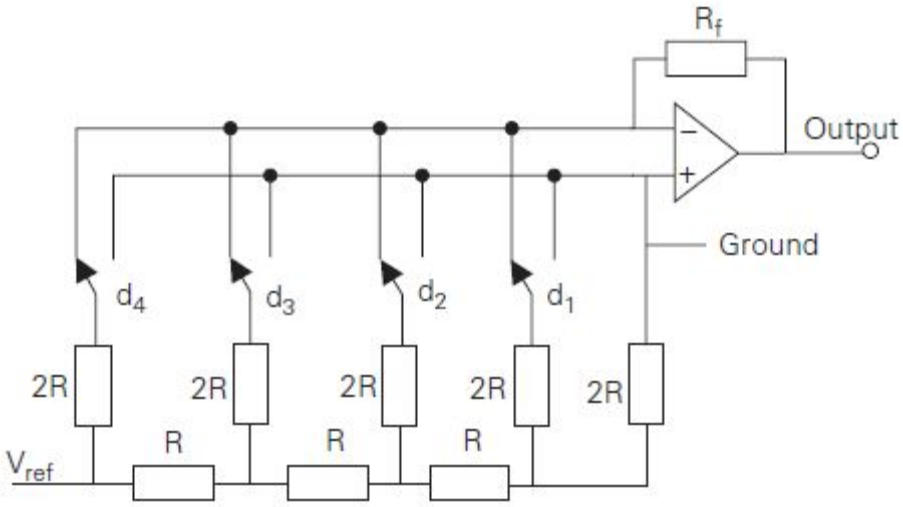
In the second implementation of binary weighting, only two different values of resistors are used to obtain the binary weighted currents. Using an *R*–2*R* network in conjunction with a summing amplifier and CMOS switches, it is possible to implement a binary-weighted DAC as given in Figure.

Depending on the CMOS switch position, the binary-weighted currents either flow to the feedback resistor or to ground. The currents flowing through the feedback resistor will contribute towards the output voltage. The bit values of the digital word determine the switch position. A logic 1 on the most significant bit causes the corresponding CMOS switch d4 to connect to the buffer's inverting input. Current *V*ref /2*R* will flow into the

buffer's summing node, thus generating an output voltage. A logic 1 on the next most significant bit operates CMOS switch d3 and causes current *V*ref/4*R* to flow into the summing node. The current is halved each time the binary value of the bit is halved, so the output voltage is proportional to the value of the digital word. The advantage of an *R*–2*R* network is that only two resistor values are required. Matching between a number of resistors, of values *R* and 2*R*, is much easier to achieve than by using binary-weighted values.



A binary-weighted resistor DAC (4 bit)



R–2R binary-weighted DAC