Electronic Circuits & Logic Design Laboratory

Subject Code: 10CSL38 IA Marks: 25
Hrs/Week: 03 Exam Hours: 03
Total Hours: 42 Exam Marks: 50

Part A

1. a. Design and construct a suitable circuit and demonstrate the working of positive clipper, double ended clipper and positive clamper using diodes.
   b. Demonstrate the working of the above circuits using a simulation package
2. a. Design and construct a suitable circuit and determine the frequency response, input Impedance, output impedance and bandwidth of a CE amplifier.
   b. Design and build the CE amplifier circuit using a simulation package and determine the voltage gain for two different values of supply voltage and for two different values of emitter resistance.
3. a. Design and construct a suitable circuit and determine the drain characteristics and transconductance characteristics of an enhancement mode MOSFET.
   b. Design and build CMOS inverter using a simulation package and verify its truth table.
4. a. Design and construct a Schmitt trigger circuit using op-amp for the given UTP and LTP values and demonstrate its working.
   b. Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working.
5. a. Design and construct a rectangular waveform generator (op-amp relaxation Oscillator) for a given frequency and demonstrate its working.
   b. Design and implement a rectangular waveform generator (Op-Amp relaxation Oscillator) using simulation package and demonstrate the changes in frequency when all resistor values are doubled.
6. Design and implement an Astable Multivibrator using 555 Timer for a given frequency and duty cycle.

Part B

7. a. Given a four variable expression, simplify using Entered Variable Map (EVM) and realize the simplified logic using 8:1 MUX.
   b. Design and develop the verilog/VHDL code for 8:1 MUX. Simulate and verify its working.
8. a. Realize a J-K Master/Slave FF using NAND gates and verify its truth table.
   b. Design and develop the verilog/VHDL code for DFF with positive edge triggering. Simulate and verify its working.
9. a. Design and implement a mod n ($a<8$) synchronous up counter using JK FF IC's and demonstrate its working.
   b. Design and develop the verilog/VHDL code for mod 8 up counter simulate and verify its working.
10. a. Design and implement ring counter using 4-bit shift register and demonstrate its working.
    b. Design and develop the verilog /VHDL code for switched tail counter. Simulate and verify its working.
11. Design and implement asynchronous counter using decade counter IC to count up from 0 to n ($n \leq 9$) and demonstrate its working.
12. Design a 4-bit R-2R ladder D/A converter using Op-Amp. Determine its accuracy and resolution.

Electronic Circuits Laboratory

1 a. CLIPPING AND CLAMPING CIRCUITS

AIM : Design and construct a suitable circuit and demonstrate the working of positive clipper, double ended clipper and positive clamper using diodes.

COMPONENTS REQUIRED: Diode (BY-127 / IN4007), Resistors-10 KΩ & 3.3kΩ, DC regulated power supply (for Vref), Signal generator (for V_i) and CRO.

CIRCUIT DIAGRAM OF POSITIVE CLIPPER

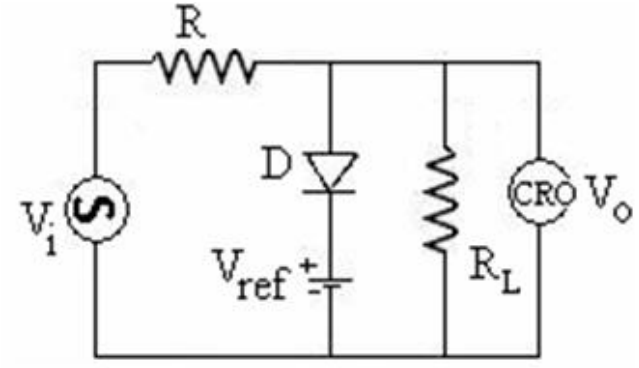
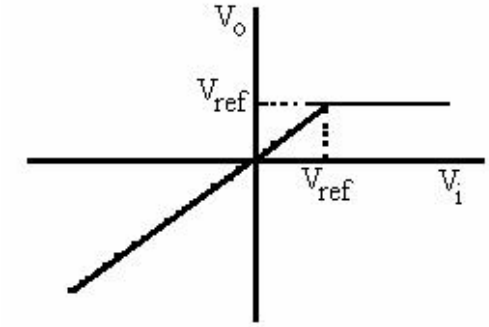


Fig.1 a Positive clipper Circuit



b. Transfer Characteristics

Clippers clip off a portion of the input signal without distorting the remaining part of the waveform. In the positive clipper shown above the input waveform above Vref is clipped off. If Vref = 0V, the entire positive half of the input waveform is clipped off.

Plot of input Vi (along X-axis) versus output Vo (along Y-axis) called transfer characteristics of the circuit can also be used to study the working of the clippers.

Choose R value such that $R = \sqrt{R_f R_r}$ where R_f = 100Ω and R_r = 100kΩ are the resistances of the forward and reverse diode respectively. Hence R = 3.3kΩ.

Let the output resistance R_L = 10kΩ. The simulations can be done even without R_L.

PROCEDURE:

1. Before making the connections check all components using multimeter.
2. Make the connections as shown in circuit diagram.
3. Using a signal generator (V_i) apply a sine wave of 1KHz frequency and a peak-to-peak amplitude of 10V to the circuit. (Square wave can also be applied.)
4. Keep the CRO in dual mode, connect the input (Vi) signal to channel 1 and output waveform (Vo) to channel 2. Observe the clipped output waveform which is as shown in fig. 2. Also record the amplitude and time data from the waveforms.
5. Now keep the CRO in X-Y mode and observe the transfer characteristic waveform.

   Note:

   1. Vary Vref and observe the variation in clipping level. For this use variable DC power supply for Vref.
   2. Change the direction of diode and Vref to realize a negative clipper.
   3. For double-ended clipping circuit, make the circuit connections as shown in fig.3 and the output waveform observed is as shown in figure 5.
   4. Adjust the ground level of the CRO on both channels properly and view the ouput in DC mode (not in AC mode) for both clippers and clampers.

WAVEFORMS

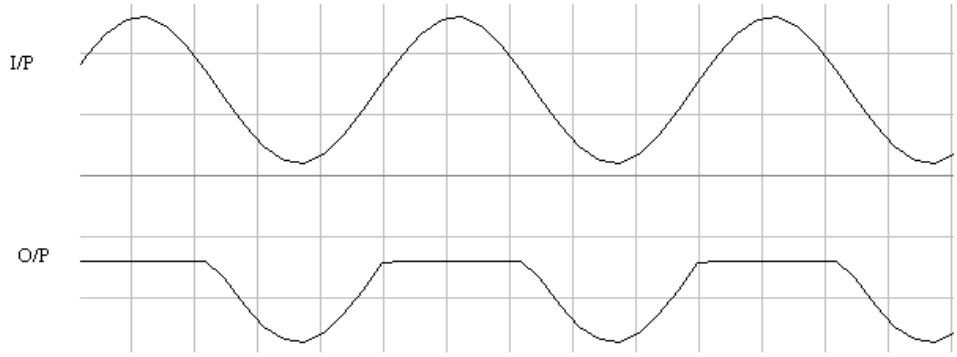


Fig. 2. Input and output waveform for positive Clipper

DOUBLE ENDED CLIPPER

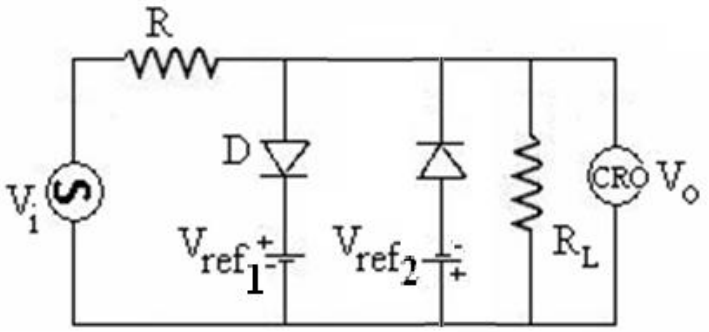
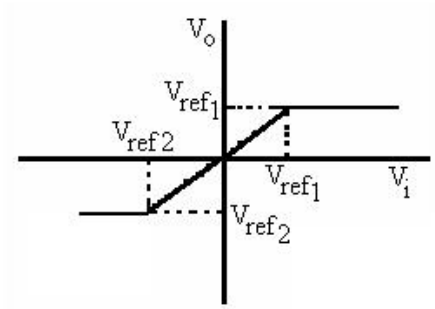


Fig.3 Double ended clipper Circuit



b. Transfer Characteristics

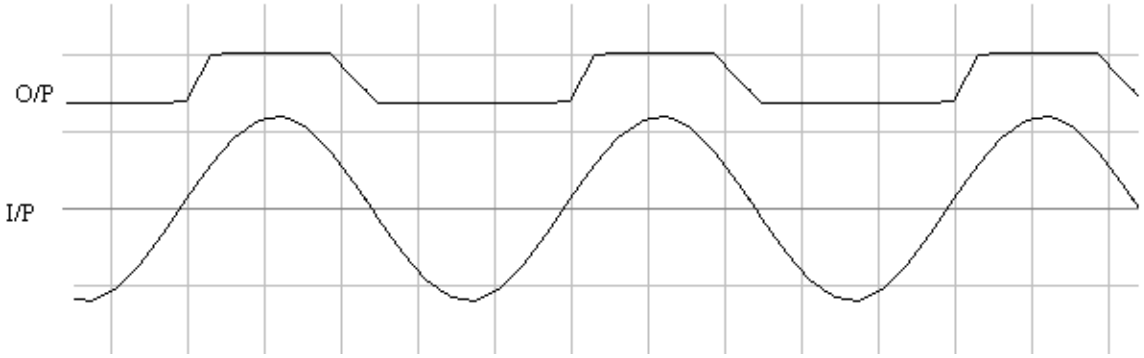


Fig. 4. Input and output waveform for double-ended clipping circuit

Note: The above clipper circuits are realized using the diodes in parallel with the load (at the output), hence they are called shunt clippers. The positive (and negative) clippers can also be realized in the series configuration wherein the diode is in series with the load. These circuits are called series clippers.

POSITIVE CLAMPER

COMPONENTS REQUIRED: Diode (BY-127), Resistor of 200 KΩ, Capacitor - 0.1 μF, DC regulated power supply, Signal generator, CRO

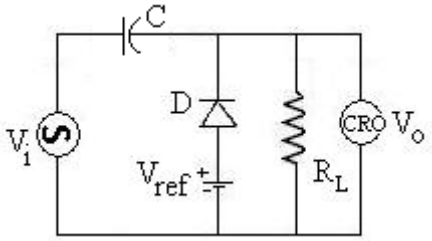


Fig. 5 Positive Clamper

The clamping network is one that will "clamp" a signal to a different DC level. The network must have a capacitor, a diode and a resistive element, but it can also employ an independent DC supply (V_{ref}) to introduce an additional shift. The magnitude of R and C must be chosen such that time constant ζ=RC is large enough to ensure the voltage across capacitor does not discharge significantly during the interval of the diode is non-conducting.

DESIGN:
Say for τ = 20msec (corresponding to a frequency of 50 Hz), then for RC >> τ, let C=0.1μF, then R ≥ 200KΩ.

PROCEDURE :

1. Before making the connections check all components using multimeter.
2. Make the connections as shown in circuit diagram (fig. 5).
3. Using a signal generator apply a square wave input (Vi) of peak-to-peak amplitude of 10V (and frequency greater than 50Hz) to the circuit. (Sine wave can also be applied)
4. Observe the clamped output waveform on CRO which is as shown in Fig. 6.

Note:

1. For clamping circuit with reference voltage V_{ref}, the output waveform is observed as shown in Fig. 7. For without reference voltage, Keep V_{ref} = 0V.
2. CRO in DUAL mode and DC mode. Also the grounds of both the channels can be made to have the same level so that the shift in DC level of the output can be observed.
3. For negative clampers reverse the directions of both diode and reference voltage.

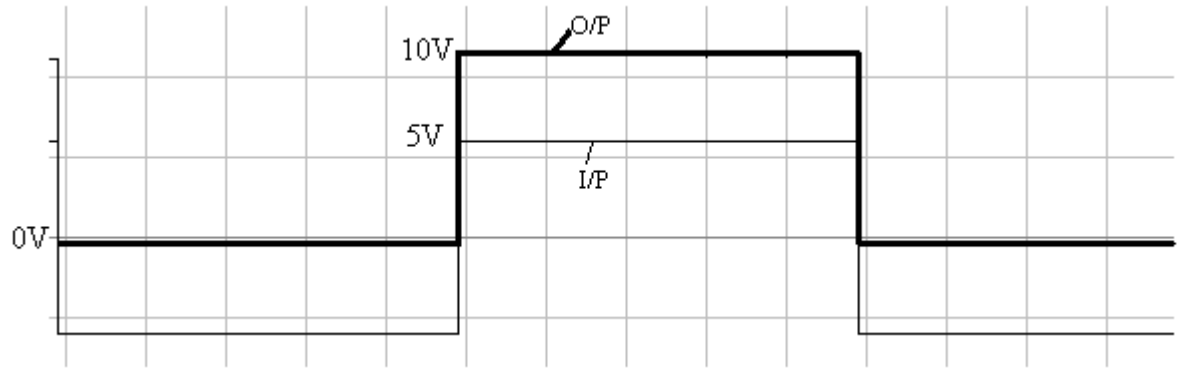


Fig. 6 Input and output waveform for positive clamper without reference voltage.

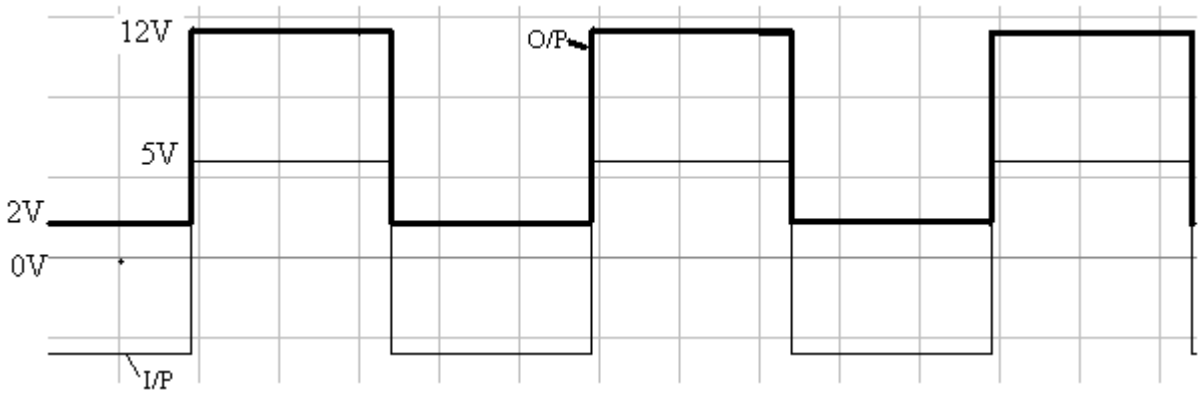


Fig. 7 Input and output waveform for positive clamper circuit with reference voltage = 2V

2 a. CE AMPLIFIER

AIM: Design and construct a suitable circuit and determine the frequency response, input impedance, output impedance and bandwidth of a CE amplifier..

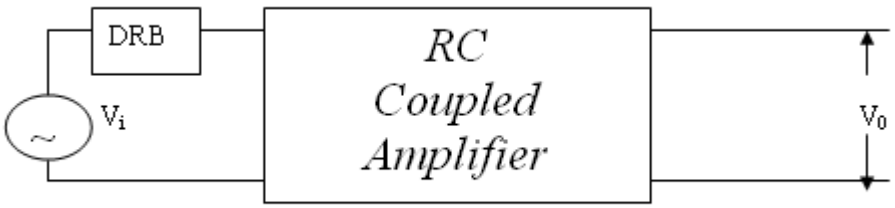
COMPONENTS REQUIRED: Transistor SL-100, Resistors -16 KΩ, 3.9 KΩ, 820Ω, 220 Ω, Capacitors - 0.47 μF, 100 μF, DC regulated power supply, Signal generator, CRO

PROCEDURE :

1. Before making the connections check all components using multimeter.
2. Make the connections as shown in circuit diagram.
3. Using a signal generator apply a sinusoidal input waveform of peak-to-peak amplitude 20mV (= V_{in}) to the circuit and observe the output signal on the CRO.
4. Vary the frequency of input from 50Hz to 1MHz range and note down corresponding output voltage V_O in the tabular column.
   Note: When the input frequency is being changed the input amplitude (i.e., around 20 mV) should remain constant.
   Adjust the amplitude of V_{in} (in mV) such that the output Vo does not get clipped (i.e., saturated) when the frequency is in the mid range say 1kHz.
5. After the frequency has been changed from 50 Hz to 1MHz and the readings are tabulated in a tabular column, calculate gain of the amplifier (in dB) using the formula,
   $$\text{Gain in dB} = 20 \log_{10} (V_o/V_{in})$$
6. Plot the graph of gain versus frequency on a semilog sheet and hence determine the bandwidth as shown in Fig. 3. Bandwidth = B = f_2-f_1

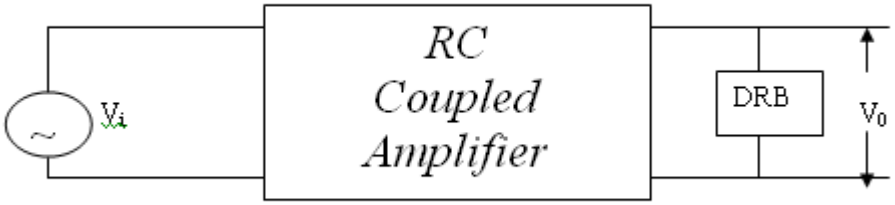
To find **input impedance**, set the input DRBI to a minimum value and DRBO to a maximum value (say, 10k) as shown in figure 2. Now apply an input signal using signal generator, say a sine wave whose peak-to-peak amplitude is 50mV with a frequency of 10 KHz. Observe the output on CRO. Note this value of output with DRBI = 0 as Vx.
Now increase the input DRBI value till the output voltage V_o = (1/2) Vx. The corresponding DRBI value gives input impedance.

To measure input impedence R_i



To find **output impedance**, set DRBO which is connected across the output to a maximum value as shown in figure 2, with the corresponding DRBI at the minimum position. Apply the input signal using signal generator, say a sine wave whose peak-to-peak amplitude is 50mV with a frequency of 10 KHz. Observe the output on CRO. Note this value of output with DRBI = 0 as Vx. Now decrease the DRBO value till the output voltage V_o = (1/2) Vx. The corresponding DRBO value gives output impedance.

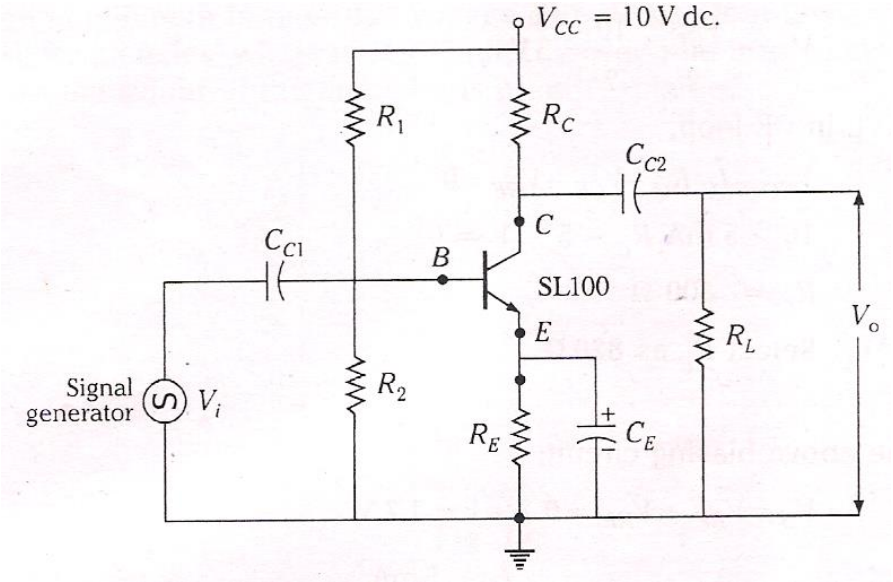
To measure output impedence R_0

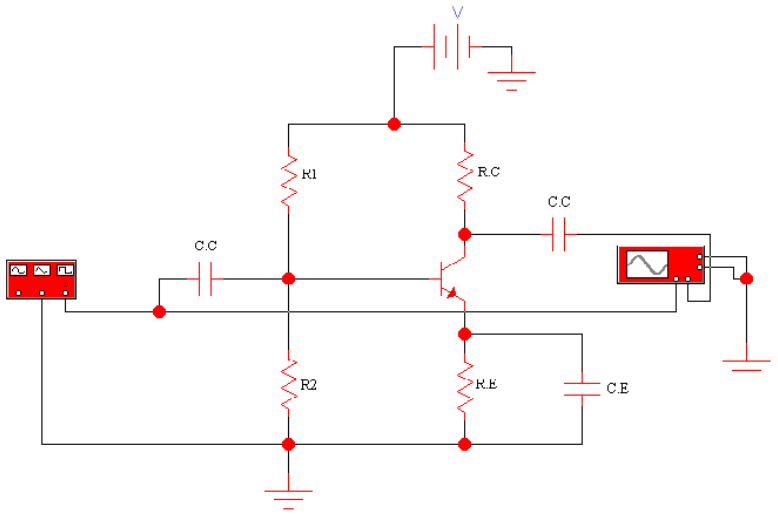


Note: DRBI is connected between the signal generator and the input coupling capacitor. DRBO is connected across the output (across the CRO terminals).
The ground symbol in the circuit diagram implies a common point. In some of the power supplies, there will be three terminals - +(plus), -(minus) and GND (ground). Never connect this GND terminal to the circuit.

TABULAR COLUMN

V_i = 50 mV (P-P)			
f in Hz	$V_{0\ P\text{-}P}$ volts	$A_V = \frac{V_0}{V_i}$	Power Gain = 20 $\log_{10} A_v$ in dB
50 Hz -- -- 1 MHz			





Values
$R_1 = 22k\Omega$
$R_2 = 4.7k\Omega$
$R_C = 1K\Omega$
$R_E = 270\Omega$
$R_L = 10k\ \Omega$
$C_{C1} = C_{C2} = 0.47\mu F$
$C_E = 47\mu F$

Fig. 1 : Transistor as a CE amplifier circuit diagram and actual connections (does not show R_L)

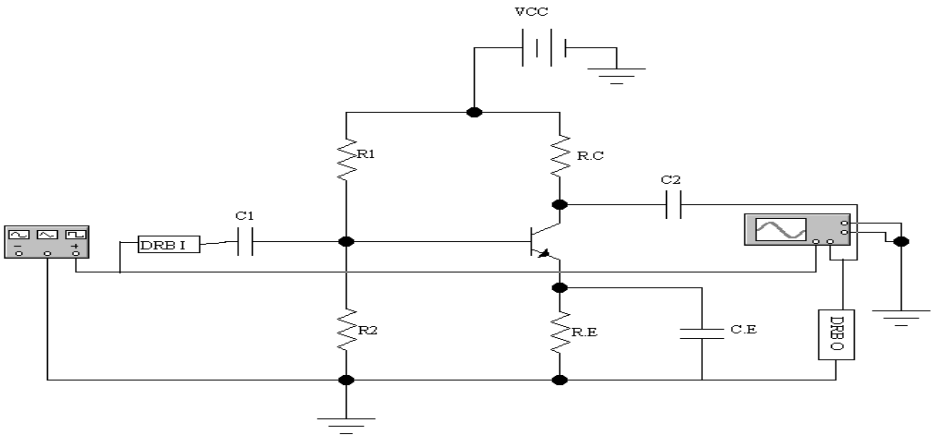
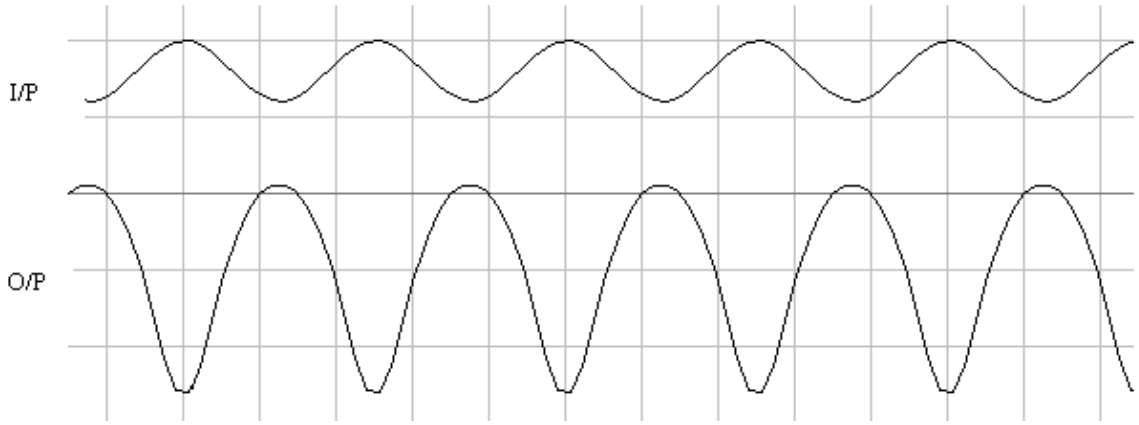


Fig. 2: CE Amplifier with DRBs connected at both input and output

WAVEFORMS:



FREQUENCY RESPONSE:

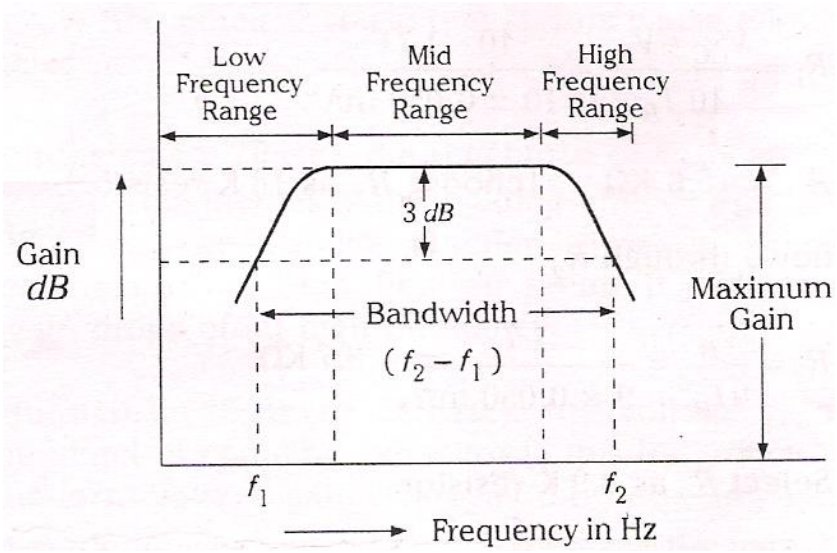


Fig. 3 Frequency response plotted on semilog graph (X-axis is log scale)

RESULT:

1. BANDWIDTH = …….Hz
2. INPUT IMPEDANCE = ……..Ω
3. OUTPUT IMPEDANCE = ……Ω

Note: Maximum gain occurs in mid frequency region. This is also called mid band gain.
Gain-bandwidth product = Midband gain x Bandwidth

THEORY:

The frequency response of an amplifier is the graph of its gain versus the frequency. Fig. 3 shows the frequency response of an ac amplifier. In the middle range of frequencies, the voltage gain is maximum. The amplifier is normally operated in this range of frequencies. At low frequencies, the voltage gain decreases because the coupling (C_C in Fig.1) and bypass (C_E) capacitors no longer act like short circuits; instead some of the ac signal voltage is attenuated. The result is a decrease of voltage gain as we approach zero hertz. At high frequencies, voltage gain decreases because the internal (parasitic) capacitances across the transistor junctions provide bypass paths for ac signal. So as frequency increases, the capacitive reactance becomes low enough to prevent normal transistor action. The result is a loss of voltage gain.

Cutoff frequencies (f_1 & f_2 in Fig. 3) are the frequencies at which the voltage gain equals 0.707 of its maximum value. It is also referred to as the half power frequencies because the load power is half of its maximum value at these frequencies.

DESIGN:

Given: $V_{CC} = 10V, I_C = 5mA \,\&\, \beta = 100$

To find R_E, let $V_{RE} = I_E R_E = \frac{1}{10} V_{CC} = 1V$, and $I_E \cong I_C$

Hence $R_E = \frac{V_{RE}}{I_E} = \frac{V_{RE}}{I_C} = \frac{1}{5m} = 200\Omega$. Choose $R_E = 220\Omega$.

To find R_C, R_C determines the Q-point. Choose R_C such that $V_{CE} = V_{CC}/2 = 5V$
Applying KVL to the CE loop (in Fig. 1), $V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$.
Substituting all the values we get $R_C = 800\Omega$. Choose $R_C = 820\Omega$(standard resistor value)

To find R_1: We have $V_B = V_{BE} + V_{RE} = 0.7 + 1 = 1.7V$ and $I_B = \frac{I_C}{\beta} = \frac{5m}{100} = 50\mu A$

Assuming that the biasing network (R_1 & R_2) is designed such that $10I_B$ flows through R_1, we have $V_{R_1} = 10I_B R_1 = V_{CC} - V_B$. Substituting the values of Vcc, V_B & I_B, $R_1 = 16.6k\ \Omega$.

Next to find R_2, we have $V_{R2} = 9I_B R_2 = V_B$. Hence $R_2 = \frac{V_B}{9I_B} = \frac{1.7}{9 \times 50\mu A} = 3.7K\Omega$. Choose $R_1 = 18k\Omega$ and choose $R_2 = 3.9k\Omega$

To find the bypass capacitor C_E: Let $X_{CE} = R_E/10$ at f = 100 Hz (remember C_E & R_E are in parallel). Hence $X_{CE} = \frac{1}{2\pi f C_E} = \frac{R_E}{10}$. Substituting all the values, C_E = 72.3 µF.

Choose C_E =100 µF and the coupling capacitors $C_{C1} = C_{C2} = 0.47$ µF.

3 a. CHARACTERISTICS OF AN ENHANCEMENT MODE MOSFET

AIM : Design and construct a suitable circuit and determine the drain characteristics and transconductance characteristics of an enhancement mode MOSFET.

COMPONENTS REQUIRED: MOSFET (1RF 740), Resistor (1kΩ), Voltmeters (0-30V range and 0-10V range), Ammeter (0- 25mA range) and Regulated power supply (2 nos. – variable power supply)

CIRCUIT DIAGRAM:

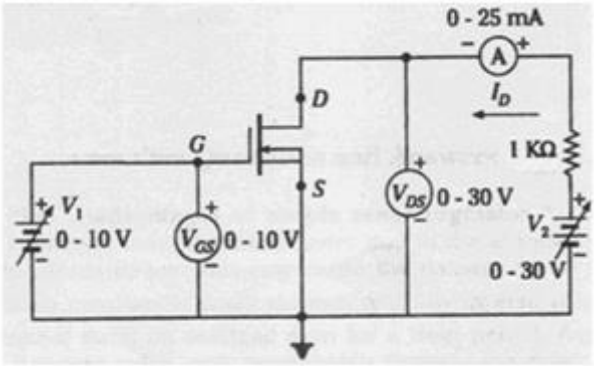


Fig.1a. Enhancement mode (positive gate voltage)

Sample Characteristics to be obtained

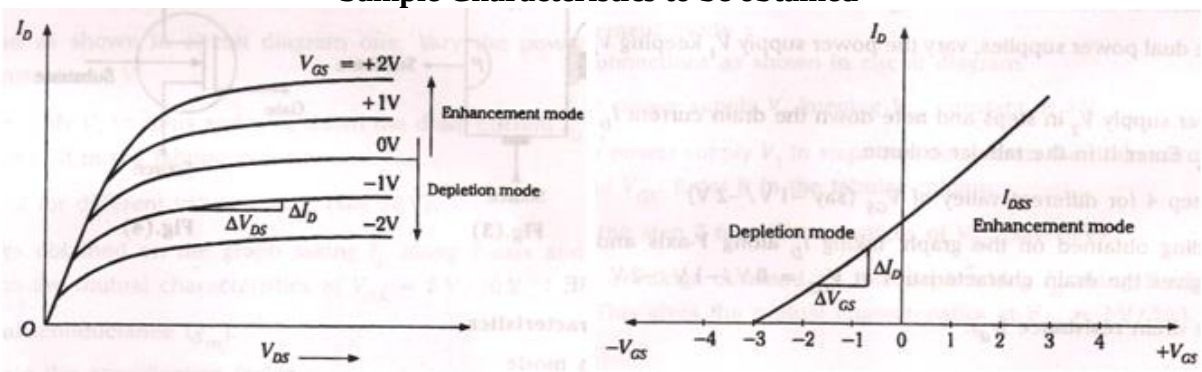


Fig. 2a. Drain Characteristics and b. Transconductance (or mutual/transfer) characteristics

PROCEDURE :

1. Make the connections as shown in the corresponding circuit diagram. Special care to be taken in connecting the voltmeters and ammeters according to the polarity shown in circuit diagram figures.
2. Repeat the procedure for finding drain and transconductance characteristics for both modes, that is for both depletion and enhancement modes.
3. Tabulate the readings in separate tabular columns as shown below.
4. Plot the drain characteristics (I_D versus V_{DS} for different values of gate voltages V_{GS}) of both modes (that is, depletion and enhancement) in one plot as shown below. (Take I_D along the Y-axis and V_{DS} along the X-axis in the plot)
5. From this plot of drain characteristics find the drain resistance $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$, which is shown in Fig. 2a.

6. Similarly plot the transconductance characteristics of both modes in one plot, with I_D along the Y-axis and V_{GS} along the X-axis in the graph for one value of V_{DS}, say V_{DS} = 5V.
7. From this plot find the mutual conductance or transconductance $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ (Fig. 2b).
8. Lastly find the amplification factor, $\mu = r_d \bullet g_m$

Procedure for finding the Transconductance Characteristics in both modes:

1. Switch on the power supplies, with both V_2 and V_1 at zero voltage.
2. Initially set $V_1 = V_{GS}$ = 0V. Now set $V_2 = V_{DS}$ = 5V (say). Vary the power supply V_1 i.e., V_{GS} and note down the corresponding current I_D (in mA) (Simultaneously note down the V_{GS} value from the voltmeter connected at the gate terminal).
3. Repeat the above procedure for a different value of V_{DS}, say 10V.

Note: In the above procedure V_{DS} (i.e., the power supply V_2) is kept constant and the power supply V_1 ($=V_{GS}$) is varied.

Drain Characteristics :

1. Initially set $V_1 = V_{GS}$ =3.5V (say), slowly vary V_2 and note down the corresponding current I_D. Simultaneously note down in the tabular column the voltmeter reading V_{GS}.
2. Repeat the above procedure for different values of V_{GS} and note down the current I_D for corresponding $V_1 = V_{DS.}$
3. Plot the graph of I_D versus V_{DS} for different values of gate voltages.

Note: In the above procedure V_{DS} (i.e., the power supply V_2) is varied and the power supply V_1 ($=V_{GS}$) is kept constant.

READINGS TABULATED IN TABULAR COLUMN

Enhancement mode readings

Drain Characteristics

V_{GS}= V		**V_{GS}= V**	
V_{DS}	**I_D (ma)**	**V_{DS}**	**I_D(ma)**

Transconductance Characteristics

V_{DS}= 5V		**V_{DS}=10 V**	
V_{GS}	**I_D (ma)**	**V_{GS}**	**I_D (ma)**

4 a. SCHMITT TRIGGER

AIM : Design and construct a Schmitt trigger circuit using op-amp for the given UTP and LTP values and demonstrate its working..

COMPONENTS REQUIRED : IC μA 741, Resistor of 10KΩ, 90KΩ, DC regulated power supply, Signal generator, CRO

DESIGN :

From theory of Schmitt trigger circuit using op-amp, we have the trip points,

$$UTP = \frac{R_1 V_{ref}}{R_1 + R_2} + \frac{R_2 V_{sat}}{R_1 + R_2} \text{ where } V_{sat} \text{ is the positive saturation of the opamp} = 90\% \text{ of } V_{cc}$$

$$\& \; LTP = \frac{R_1 V_{ref}}{R_1 + R_2} - \frac{R_2 V_{sat}}{R_1 + R_2}$$

Hence given the LTP & UTP values to find the R_1, R_2 & V_{ref} values, the following design is used.

$$UTP + LTP = \frac{2R_1 V_{ref}}{R_1 + R_2} \quad \text{------(1)}$$

$$UTP - LTP = \frac{2R_1 V_{sat}}{R_1 + R_2} \quad \text{------(2)}$$

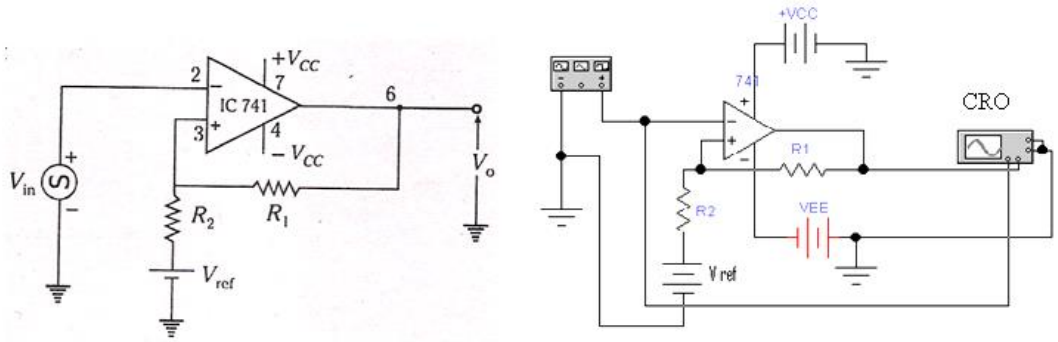
Let $V_{sat} = 10\text{V}$, UTP $= 4\text{V}$ & LTP $= 2\text{V}$, then equation (2) yields $R_1 = 9R_2$

Let $R_2 = 10K\Omega$, then $R_1 = 90K\Omega$

From equation (1) we have $V_{ref} = \frac{(UTP + LTP)(R_1 + R_2)}{2R_1} = 3.33V$

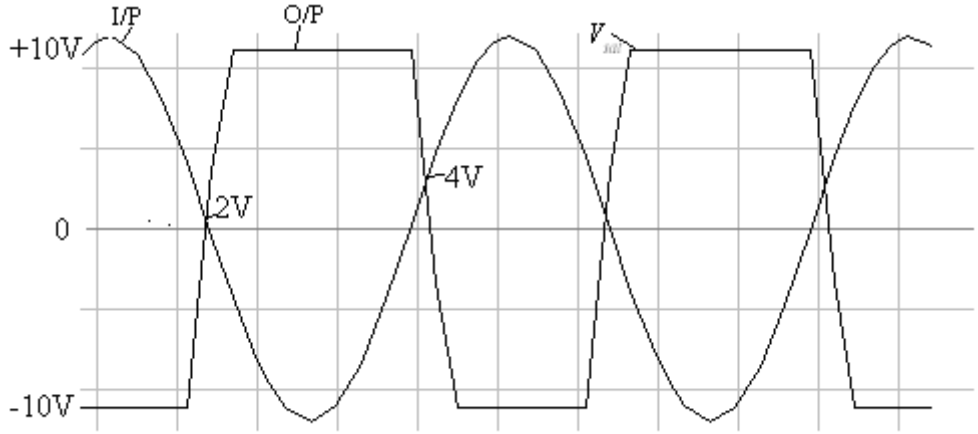
PROCEDURE :

1. Before doing the connections, check all the components using multimeter.
2. Make the connection as shown in circuit diagram.
3. Using a signal generator apply the sinusoidal input waveform of peak-to-peak amplitude of 10V, frequency 1kHz.
4. Keep the CRO in dual mode; apply input (V_{in}) signal to the channel 1 and observe the output (V_o) on channel 2 which is as shown in the waveform below. Note the amplitude levels from the waveforms.
5. Now keep CRO in X-Y mode and observe the hysteresis curve.

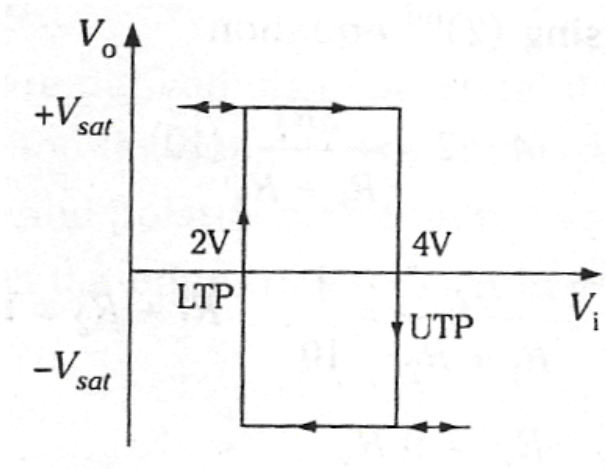


Circuit Diagram and actual connections of Schmitt Trigger Circuit

Waveforms:



CRO in DUAL mode



CRO in X-Y mode showing the Hysteresis curve

THEORY:

Schmitt Trigger converts an irregular shaped waveform to a square wave or pulse. Here, the input voltage triggers the output voltage every time it exceeds certain voltage levels called the upper threshold voltage V_{UTP} and lower threshold voltage V_{LTP}. The input voltage is applied to the inverting input. Because the feedback voltage is aiding the input voltage, the feedback is positive. A comparator using positive feedback is usually called a Schmitt Trigger. Schmitt Trigger is used as a squaring circuit, in digital circuitry, amplitude comparator, etc.

5 a. OP-AMP AS A RELAXATION OSCILLATOR

AIM : Design and construct a rectangular waveform generator (op-amp relaxation oscillator) for a given frequency and demonstrate its working...

COMPONENTS REQUIRED:

Op-amp µA 741, Resistor of 1KΩ, 10KΩ, 20 kΩ Potentiometer, Capacitor of 0.1 µF, Regulated DC power supply, CRO

DESIGN :

The period of the output rectangular wave is given as $T = 2RC\ln\left(\frac{1+\beta}{1-\beta}\right)$-------(1)

Where, $\beta = \frac{R_1}{R_1 + R_2}$ is the feedback fraction

If $R_1 = R_2$, then from equation (1) we have T = 2RC ln(3)

Another example, if R_2=1.16 R_1, then T = 2RC ----------(2)

Example: Design for a frequency of 1kHz (implies $T = \frac{1}{f} = \frac{1}{10^3} = 10^{-3} = 1ms$)

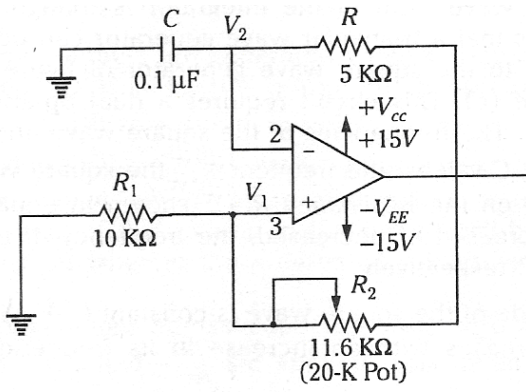
Use R_2=1.16 R_1, for equation (2) to be applied.
Let R_1 = 10kΩ, then R_2 = 11.6kΩ (use 20kΩ potentiometer as shown in circuit figure)
Choose next a value of C and then calculate value of R from equation (2).

Let C=0.1µF (i.e., 10^{-7}), then $R = \frac{T}{2C} = \frac{10^{-3}}{2\times10^{-7}} = 5K\Omega$

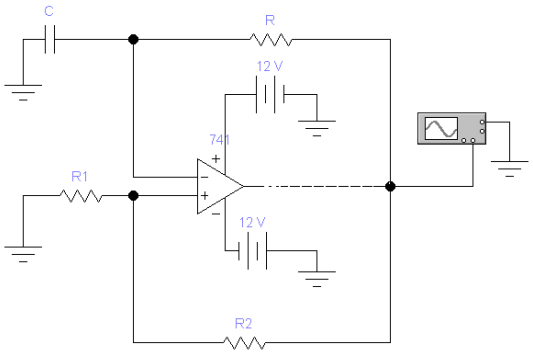
The voltage across the capacitor has a peak voltage of $V_c = \frac{R_1}{R_1 + R_2}V_{sat}$

PROCEDURE :

1. Before making the connections check all the components using multimeter.
2. Make the connections as shown in figure and switch on the power supply.
3. Observe the voltage waveform across the capacitor on CRO.
4. Also observe the output waveform on CRO. Measure its amplitude and frequency.

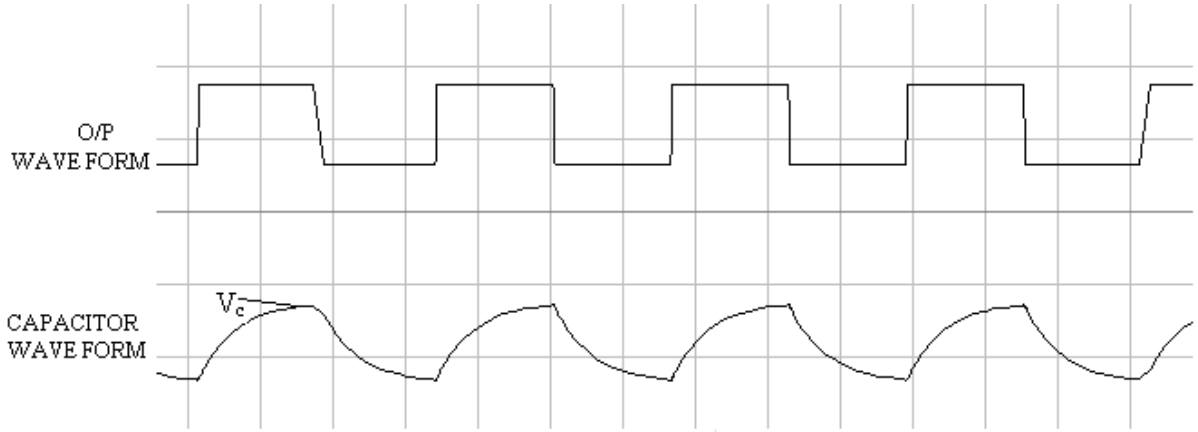


Circuit Diagram & actual connections



Values
C=0.1µF
R_1 = 10kΩ, R_2 = 11.6 kΩ,R = 4.7k/5.1kΩ

WAVEFORMS



RESULT:
The frequency of the oscillations = ……Hz.

THEORY:

Op-Amp Relaxation Oscillator is a simple Square wave generator which is also called as a Free running oscillator or Astable multivibrator or Relaxation oscillator. In this figure the op-amp operates in the saturation region. Here, a fraction (R2/(R1+R2)) of output is fed back to the noninverting input terminal. Thus reference voltage is (R2/(R1+R2)) Vo. And may take values as +(R2/(R1+R2)) Vsat or - (R2/(R1+R2)) Vsat. The output is also fed back to the inverting input terminal after integrating by means of a low-pass RC combination. Thus whenever the voltage at inverting input terminal just exceeds reference voltage, switching takes place resulting in a square wave output.

6. ASTABLE MULTIVIBRATOR USING 555 TIMER

AIM : Design and implement an astable multivibrator using 555 Timer for a given frequency and duty cycle.

COMPONENTS REQUIRED: 555 Timer IC, Resistors of 3.3KΩ, 6.8KΩ, Capacitors of 0.1 μF, 0.01 μF, Regulated power supply, CRO.

DESIGN : Given frequency (f) = 1KHz and duty cycle = 60% (=0.6)
The time period T =1/f = 1ms = T_{on} + T_{off}
Where T_{on} is the time the output is high and T_{off} is the time the output is low.
From the theory of astable multivibrator using 555 Timer(refer Malvino), we have

$T_{off} = 0.693\ R_B\ C$ ------(1)

$T_{on} = 0.693\ (R_A + R_B)C$ ------(2)

$T = T_{on} + T_{off} = 0.693\ (R_A + 2\ R_B)\ C$

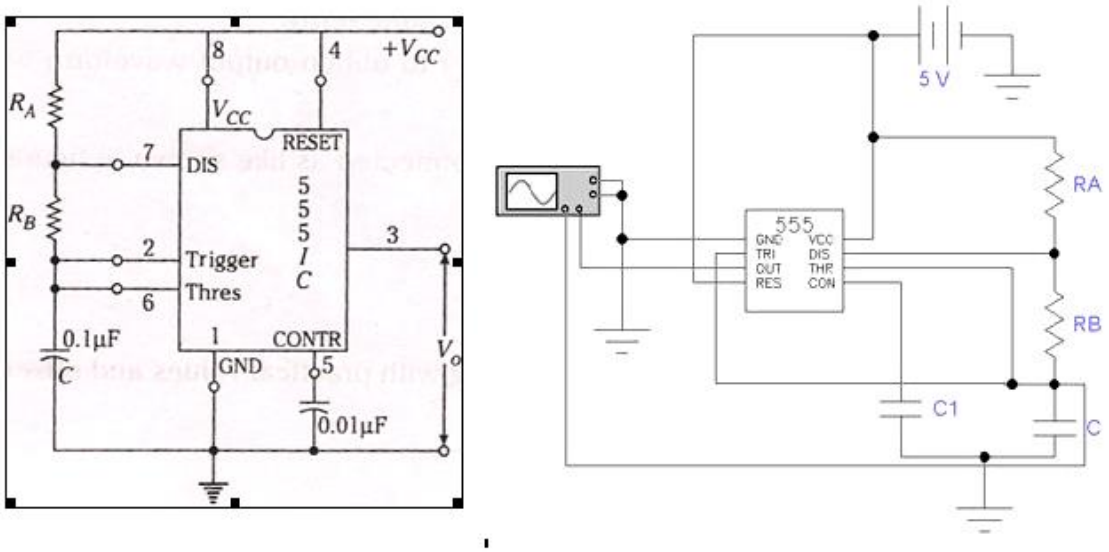
Duty cycle = T_{on} / T = 0.6. Hence T_{on} = 0.6T = 0.6ms and T_{off} = T – T_C = 0.4ms.
Let C=0.1μF and substituting in the above equations,

R_B = 5.8KΩ (from equation 1) and R_A = 2.9KΩ (from equation 2 & R_B values).

The Vcc determines the upper and lower threshold voltages (observed from the capacitor voltage waveform) as $V_{UT} = \frac{2}{3}V_{CC}$ & $V_{LT} = \frac{1}{3}V_{CC}$.

Note: The duty cycle determined by R_A & R_B can vary only between 50 & 100%. If R_A is much smaller than R_B, the duty cycle approaches 50%.

Example 2: frequency = 1kHz and duty cycle =75%, R_A = 7.2kΩ & R_B =3.6kΩ, choose R_A = 6.8kΩ and R_B = 3.3kΩ.



Circuit Diagram and actual connections

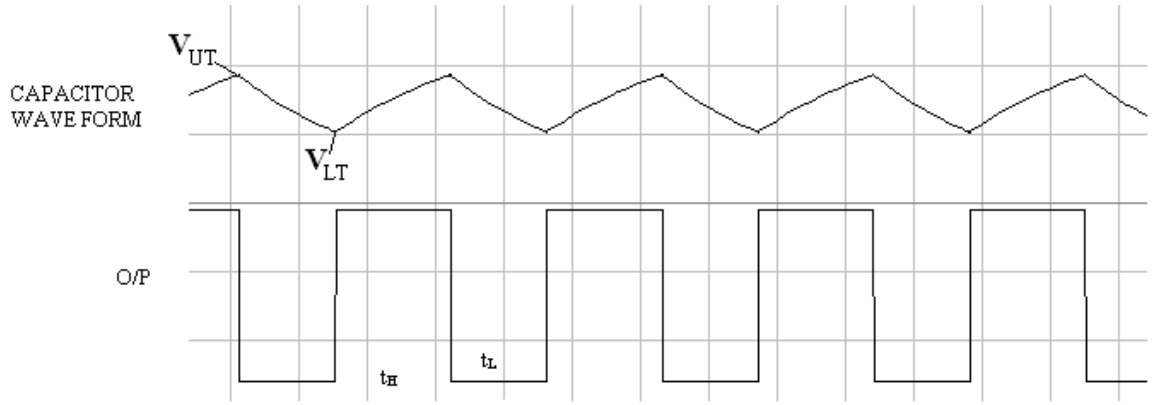
PROCEDURE :

1. Before making the connections, check the components using multimeter.
2. Make the connections as shown in figure and switch on the power supply.
3. Observe the capacitor voltage waveform at 6^{th} pin of 555 timer on CRO.
4. Observe the output waveform at 3^{rd} pin of 555 timer on CRO (shown below).
5. Note down the amplitude levels, time period and hence calculate duty cycle.

RESULT:

The frequency of the oscillations = …….Hz.

WAVEFORMS



THEORY:

Multivibrator is a form of oscillator, which has a non-sinusoidal output. The output waveform is rectangular. The multivibrators are classified as: **Astable or free running multivibrator**: It alternates automatically between two states (low and high for a rectangular output) and remains in each state for a time dependent upon the circuit constants. It is just an oscillator as it requires no external pulse for its operation. **Monostable or one shot multivibrator**: It has one stable state and one quasi stable. The application of an input pulse triggers the circuit time constants. After a period of time determined by the time constant, the circuit returns to its initial stable state. The process is repeated upon the application of each trigger pulse. **Bistable Multivibrators**: It has both stable states. It requires the application of an external triggering pulse to change the output from one state to other. After the output has changed its state, it remains in that state until the application of next trigger pulse. Flip flop is an example.

LOGIC DESIGN LABORATORY

7. a) Given a four variable expression, simplify using Entered Variable Map (EVM) and realize the simplified logic using 8:1 MUX.

a) E.g.,

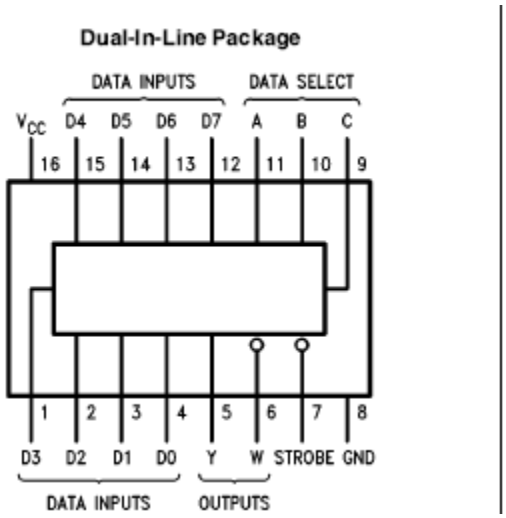
Simplify the function using MEV technique

f(a,b,c,d)=∑m(2,3,4,5,13,15)+dc(8,9,10,11)

Decimal	LSB	f	MEV map entry
0}0	0000	0	0------Do
1	0001	0	
1}2	0010	1	1------D1
9	0011	1	
2}4	0100	1	1-----D2
5	0101	1	
3}6	0110	0	0-----D3
7	0111	0	
4}8	1000	X	X-----D4
9	1001	X	
5}10	1010	X	X-----D5
11	1011	X	
6}12	1100	0	d----D6
13	1101	1	
7}14	1110	0	d----D7
15	1111	1	

Components Used: IC 74LS151, Patch Chords, Power chords, Trainer kit.

Pin Diagram of Ics Used:



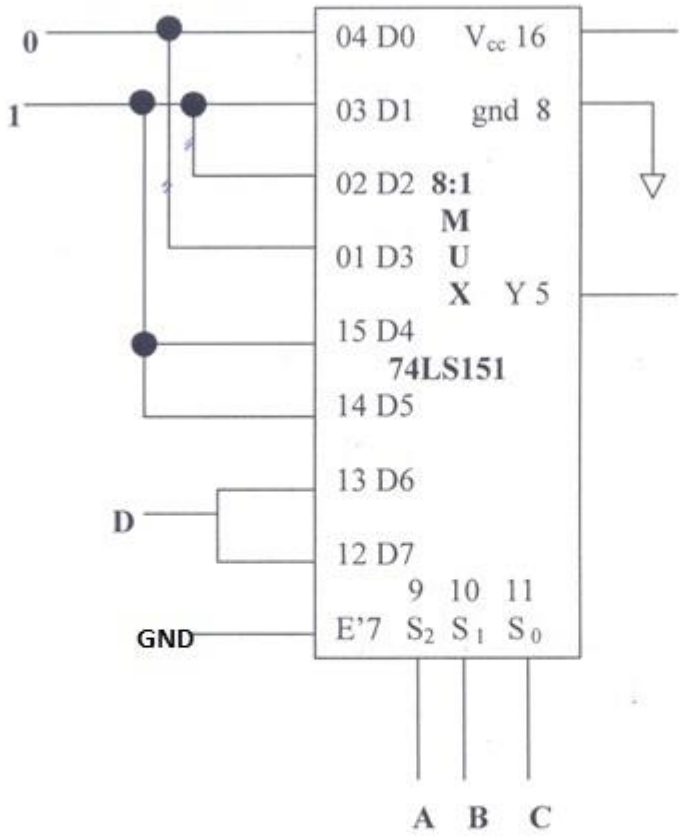
Theory:

Map Entered Variable Method:

Rules for entering values in a MEV K Map:

Rule No.	MEV f		Entry in MEV Map	Comments
1.	0	0	0	If function equals 0 for both values of MEV, enter 0 in appropriate cell of MEV Map
	1	0		
2	0	1	1	If function equals 1 for both values of MEV, enter 1.
	1	1		
3.	0	0	MEV	If function equals MEV enter MEV
	1	1		
4.	0	1	------	If the function is compliment of MEV enter MEV.
	1	0	MEV	
5.	0	-	-	If function equals don't care for both values of MEV, enter -
	1	-		
6.	0	-	0	If f=0 for MEV=0 and f=0 for MEV=1, enter 0.
	1	0		
7.	0	0	0	If f=0 for MEV=0 and f=- for MEV=1, enter 0.
	1	-		
8.	0	-	1	If f=-for MEV=0 and f=1 for MEV=1, enter 1.
	1	1		
9.	0	1	1	If f=1 for MEV=0 and f=- for MEV=-, enter -.
	1	-		

Circuit Diagram:



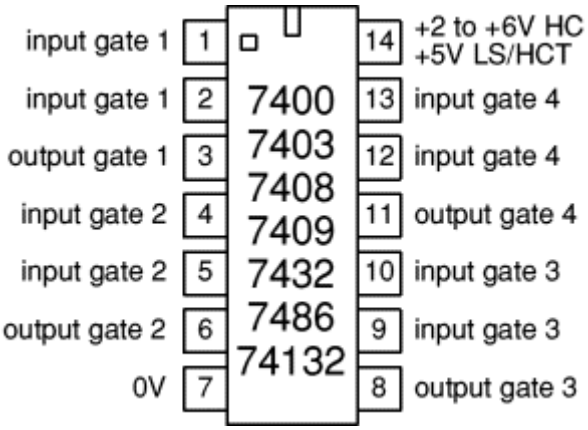
Procedure:

(1) Verify all components and patch chords whether they are in good condition not.
(2) Make connection as shown in the circuit diagram.
(3) Give supply to the trainer kit.
(4) Provide input data to circuit via switches.
(5) Verify truth table sequence and observe outputs.

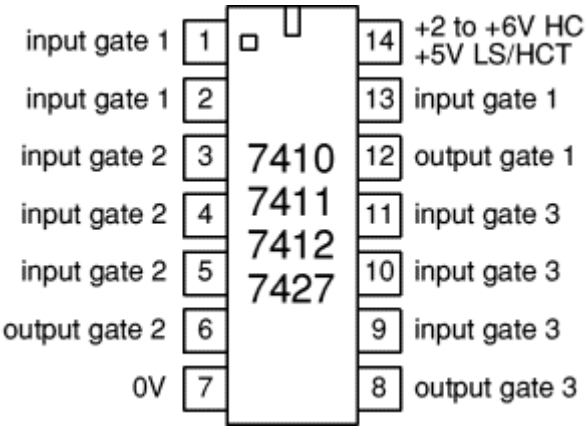
8a. Realize a J-K Master/Slave FF using NAND gates and verify its truth table.

Components used: IC 74LS00, IC 74LS10, IC 74LS20, Power chords, Patch chords, Trainer kit.

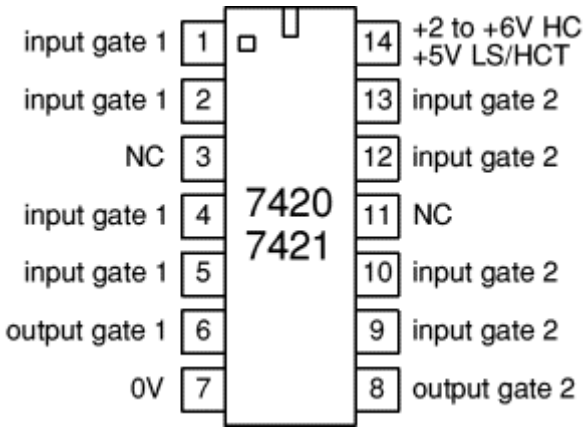
Pin Details of the ICs: 7400



IC-7410



IC-7420



Theory:

The circuit below shows the solution. To the RS flip-flop we have added two new connections from the Q and Q' outputs back to the original input gates. Remember that a NAND gate may have any number of inputs, so this causes no trouble. To show that we have done this, we change the designations of the logic inputs and of the flip-flop itself. The inputs are now designated J (instead of S) and K (instead of R). The entire circuit is known as a *JK flip-flop*.

In most ways, the JK flip-flop behaves just like the RS flip-flop. The Q and Q' outputs will only change state on the falling edge of the CLK signal, and the J and K inputs will control the future output state pretty much as before. However, there are some important differences.

Since one of the two logic inputs is always disabled according to the output state of the overall flip-flop, the master latch cannot change state back and forth while the CLK input is at logic 1. Instead, the enabled input can change the state of the master latch *once*, after which this latch will not change again. This was not true of the RS flip-flop.

If both the J and K inputs are held at logic 1 and the CLK signal continues to change, the Q and Q' outputs will simply change state with each falling edge of the CLK signal. (The master latch circuit will change state with each *rising* edge of CLK.) We can use this characteristic to advantage in a number of ways. A flip-flop built specifically to operate this way is typically designated as a *T* (for *Toggle*) flip-flop. The lone T input is in fact the CLK input for other types of flip-flops.

The JK flip-flop *must* be edge triggered in this manner. Any level-triggered JK latch circuit will oscillate rapidly if all three inputs are held at logic 1. This is not very useful. For the same reason, the T flip-flop must also be edge triggered. For both types, this is the only way to ensure that the flip-flop will change state only once on any given clock pulse.

Because the behavior of the JK flip-flop is completely predictable under all conditions, this is the preferred type of flip-flop for most logic circuit designs. The RS flip-flop is only used in applications where it can be guaranteed that both R and S cannot be logic 1 at the same time.

At the same time, there are some additional useful configurations of both latches and flip-flops. In the next pages, we will look first at the major configurations and note their properties. Then we will see how multiple flip-flops or latches can be combined to perform useful functions and operations.

Master Slave Flip Flop:

The control inputs to a clocked flip flop will be making a transition at approximately the same times as triggering edge of the clock input occurs. This can lead to unpredictable triggering.

A JK master flip flop is positive edge triggered, where as slave is negative edge triggered. Therefore master first responds to J and K inputs and then slave. If J=0 and K=1, master resets on arrival of positive clock edge. High output of the master drives the K input of the slave. For the trailing edge of the clock pulse the slave is forced to reset. If both the inputs are

high, it changes the state or toggles on the arrival of the positive clock edge and the slave toggles on the negative clock edge. The slave does exactly what the master does.
Function Table:

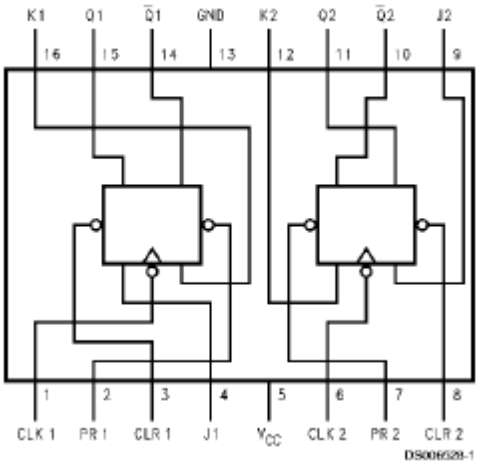
Clk	J	K	Q	--- Q	comment
	0	0	Q_0	---- Q_0	No change
	0	1	0	1	Reset
	1	0	1	0	Set
	1	1	Q_0	Q_0	toggle

9. a) Design and implement a mod n (n<8) synchronous up counter using JK FF IC's and demonstrate its working.

Components used: IC 74LS76, IC 74LS08, Patch chords, power chords, and Trainer kit.

Pin diagram of 7476

Dual-In-Line Package

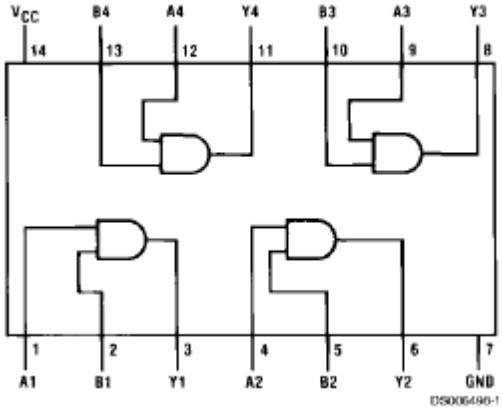


Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	⊓	L	L	Q_0	$\overline{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	Toggle	

IC:7408

Dual-In-Line Package



Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

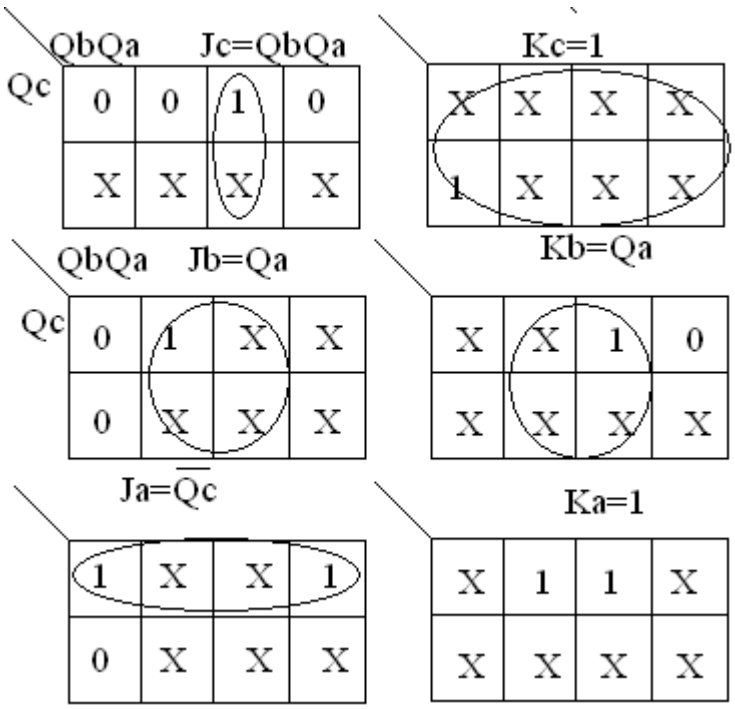
Theory:

The ripple counter requires a finite amount of time for each flip flop to change state. This problem can be solved by using a synchronous parallel counter where every flip flop is triggered in synchronism with the clock, and all the output which are scheduled to change do so simultaneously.

The counter progresses counting upwards in a natural binary sequence from count 000 to count 100 advancing count with every negative clock transition and get back to 000 after this cycle.

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

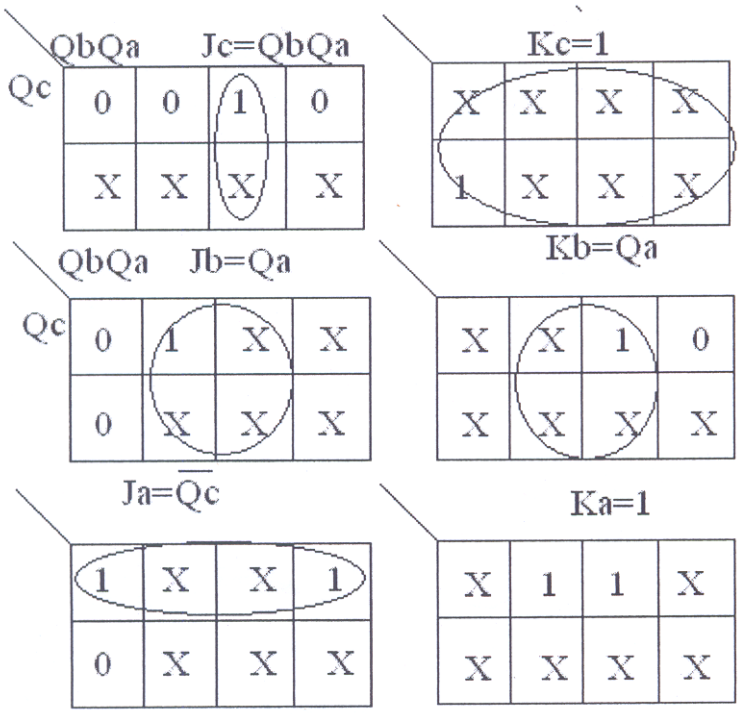
Circuit Diagram:



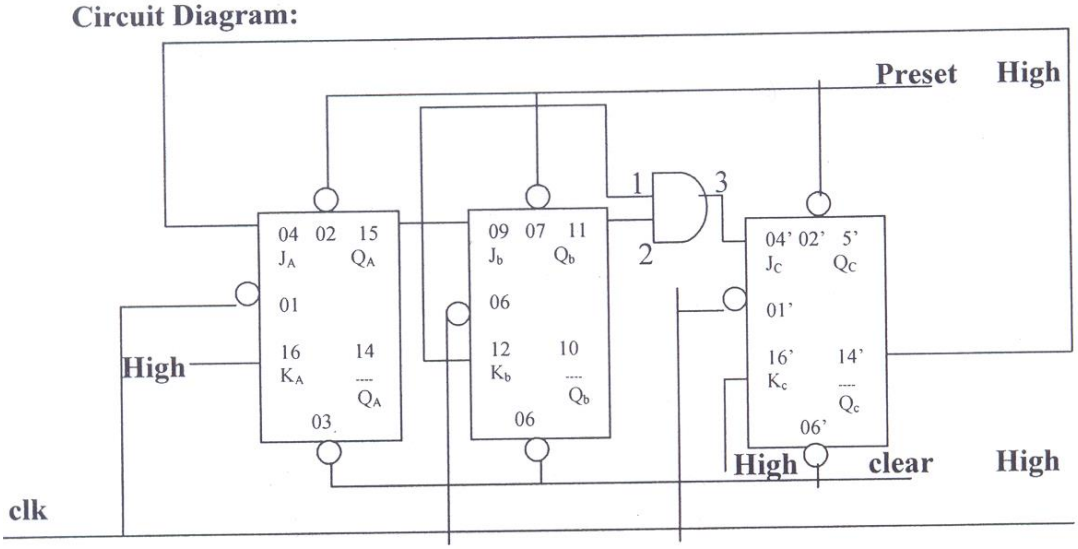
Transition Table:

Present State			Nert State			Jc	Kc	Jb	Kb	Ja	Ka
Qc	Qb	Qa	Qc+1	Qb+1	Qa+1						
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	0	0	0	x	1	0	x	0	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

K-Maps:



Circuit Diagram:



Procedure:

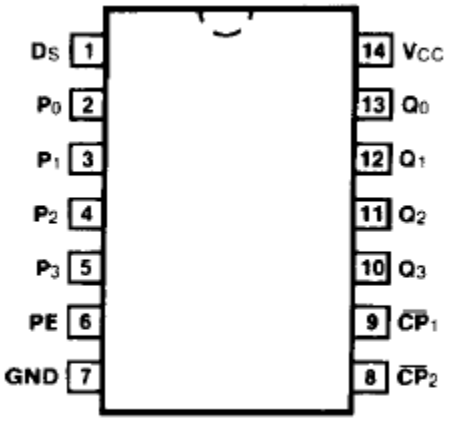
(1) Verify all components and patch chords whether they are in good condition or not.
(2) Make connection as shown in the circuit diagram.
(3) Give supply to the trainer kit.
(4) Provide input data to circuit via switches.
(5) Verify truth table sequence and observe outputs.

10a) Design and implement ring counter using 4-bit shift register and demonstrate its Working.

Components used: IC 74LS95, Patch chords, Power chords, Trainer Kit.

Pin Diagram of ICs:

IC-7495

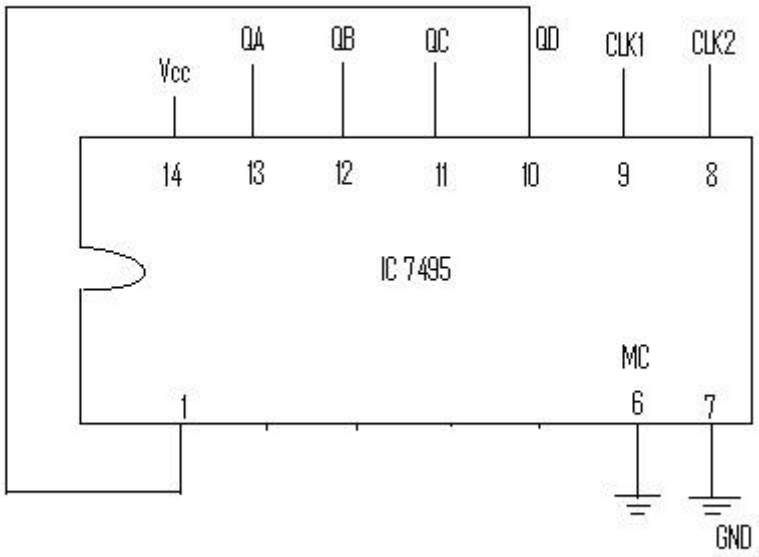


Theory:
Ring Counter is a basic register with direct feedback such that contents of the register simply circulate around the register when the clock is running. Here last output Q_d in a shift register is connected back to the serial input.

Function Table:

Clk	Qa	Qb	Qc	Qd
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

Circuit Diagram:



Procedure:

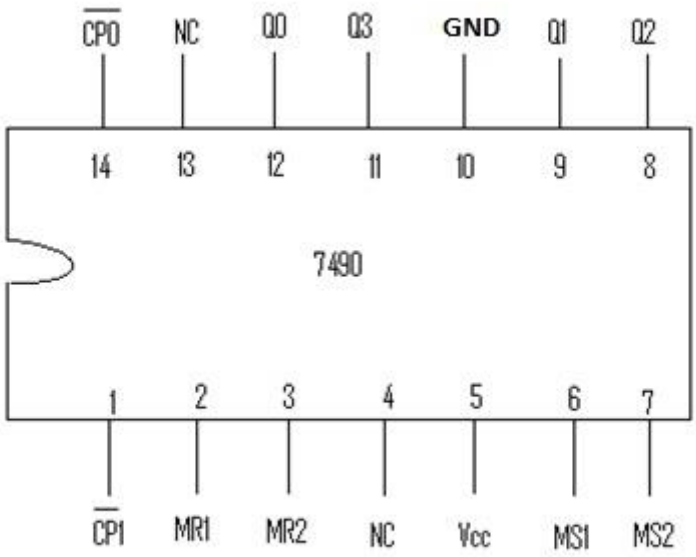
1) Verify all components and patch chords whether they are in good condition r not.
2) Make connection as shown in the circuit diagram.
3) Give supply to the trainer kit.
4) Provide input data to circuit via switched.
5) Verify truth table sequence and observe outputs.

Note: Do not connect 1 and 10. Put 1 to ground, press clock to get low every where in output. Then remove 1 from ground and before connecting it to 10 press clock once, we will get red at Q_a. Then fix the 1 to 10 and press clock to get output.

11. Design and implement asynchronous counter using decade counter IC to count up from 0 to n (n≤9) and demonstrate its working.

Components used: IC 74LS90, Patch chords, Power chords and Trainer kit.

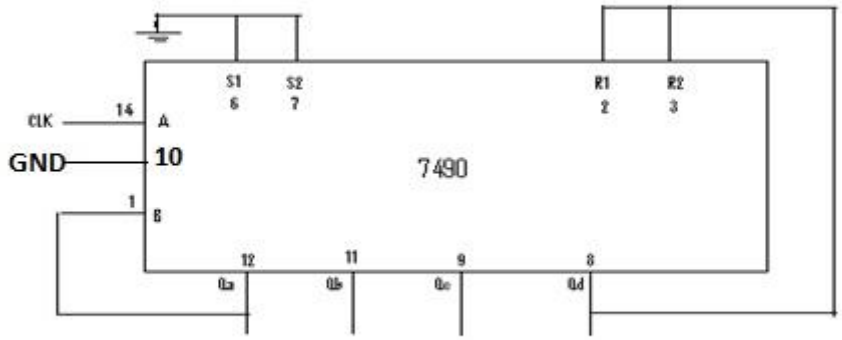
Pin Diagram of 7490



Theory:

Asynchronous counter is a counter in which the clock signal is connected to the clock input of only first stage flip flop. The clock input of the second stage flip flop is triggered by the output of the first stage flip flop and so on. This introduces an inherent propagation delay time through a flip flop. A transition of input clock pulse and a transition of the output of a flip flop can never occur exactly at the same time. Therefore, the two flip flops are never simultaneously triggered, which results in asynchronous counter operation.

Circuit Diagram:



Function Table:

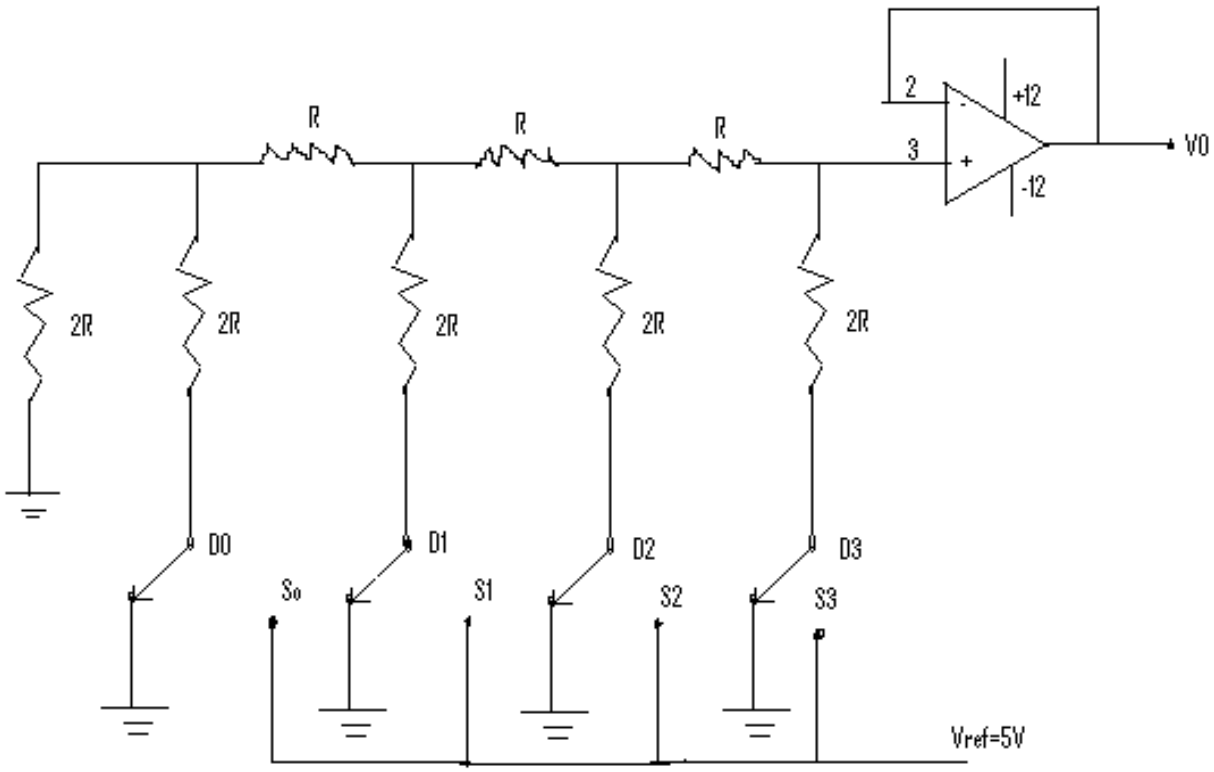
Clock	Q_a	Q_b	Q_c	Q_d
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
8	0	1	1	1
9	1	0	0	0

12. Design a 4-bit R-2R ladder D/A converter using Op-Amp. Determine its accuracy and resolution.

Aim: To study the operation of 4-bit DAC using R-2R ladder network.

Components required: Resistors, DMM, OP-741, Connecting wires, IC Trainer kit.

Circuit diagram:



Vref=5V

$V_0=(8D_3+4D_2+2D_1+1D_0)Vref/2^4$

Smallest increment or change in the output voltage=$VR/2^4*(2R/3R)$

Accuracy=Error Voltage

Full scale o/p Voltage

Resolution= $(1/16)*V_i$

Tabular column:

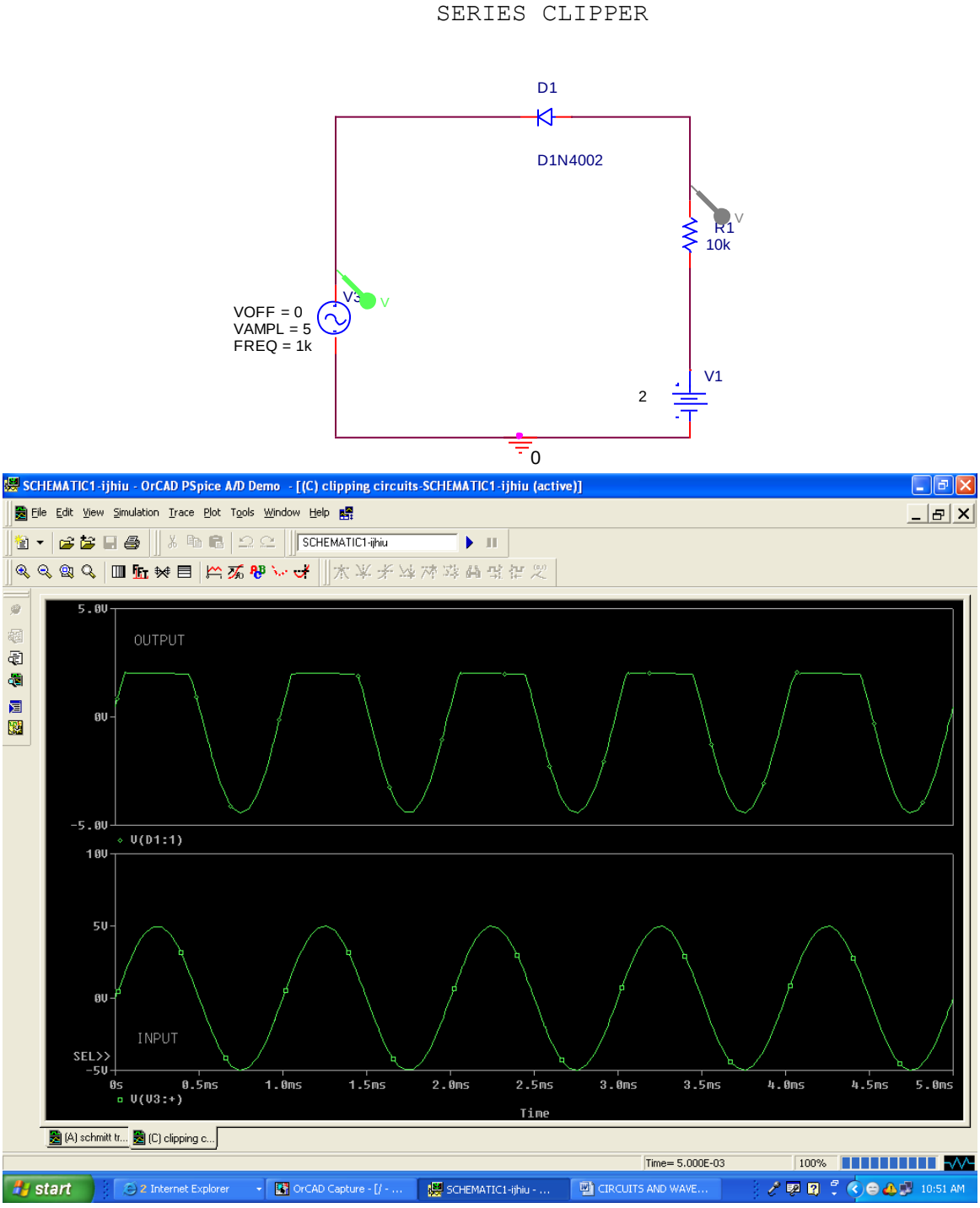
Decimal eqiuvalent	Digital inputs D3 D2 D1 D0	Analog output voltage	
		Theoratical value	Practical value
0	0 0 0 0		
1	0 0 0 1		
2			
3			
.			
.			
15	1 1 1 1		

Procedure:

1) Make connections as shown in the circuit diagram
2) In different digital inputs measure the analog output voltage using multimeter.
3) Tabulate the results compare the theoretical output values with the practical ones.

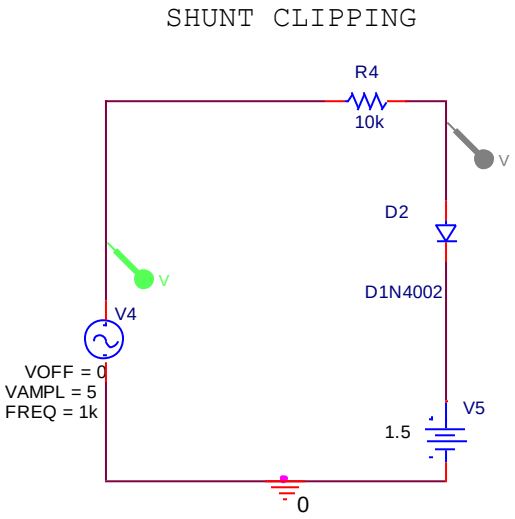
Electronics Circuits with PSPICE

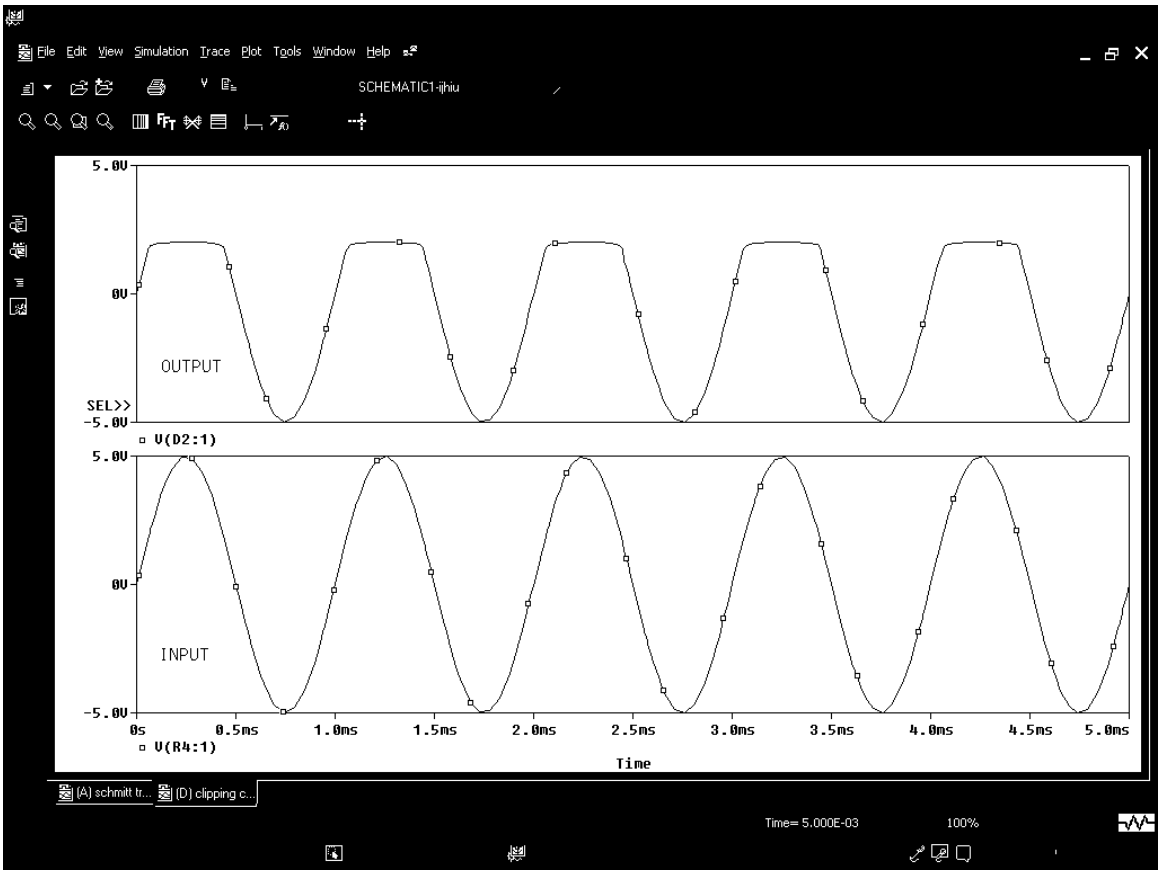
1. b. Demonstrate the working of the above circuits using a simulation package



Type of analysis: TIME DOMAIN (TRANSIENT)

Run to time: 5msec step size: 0.01msec

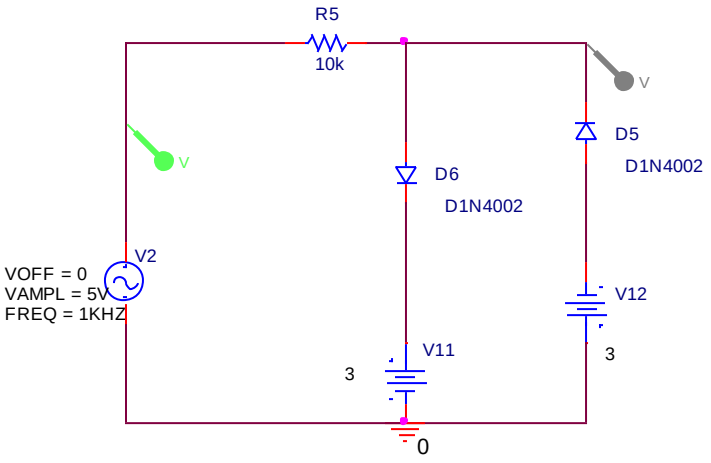


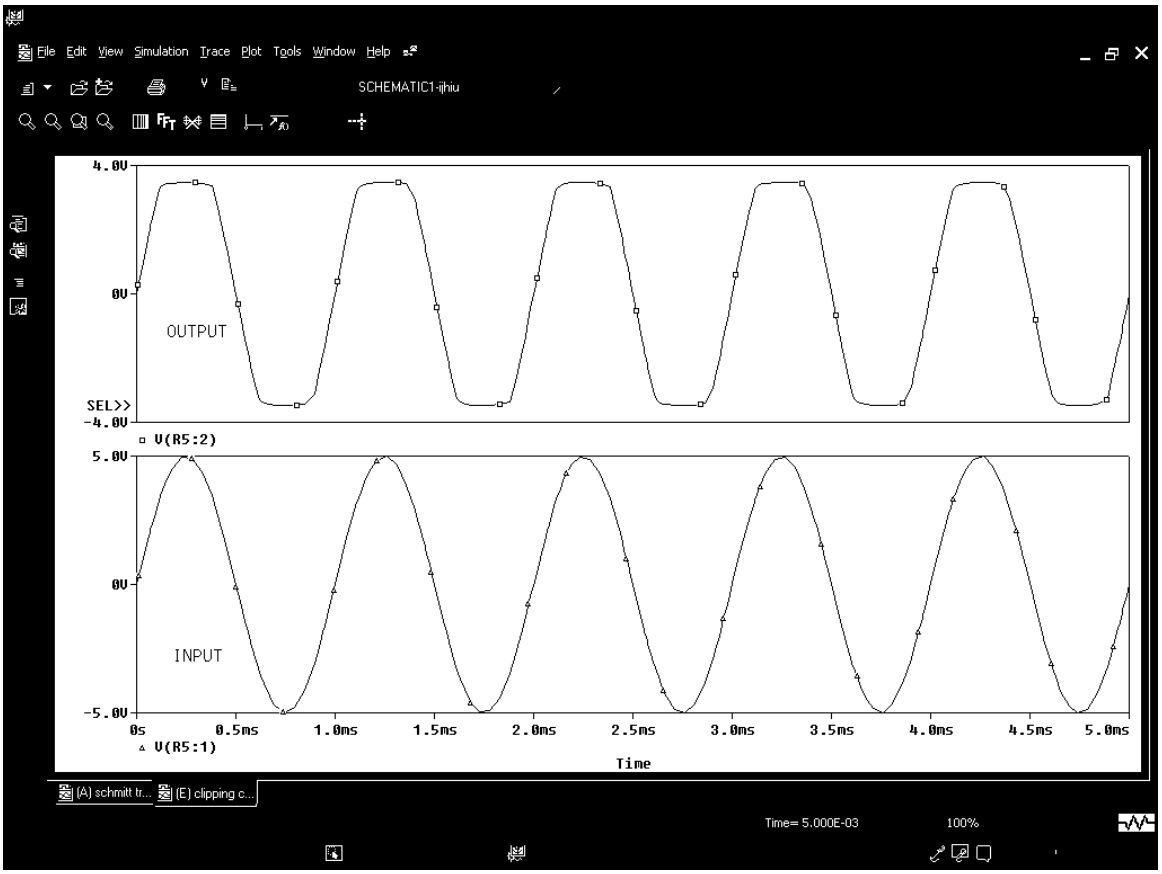


Type of analysis: TIME DOMAIN (TRANSIENT)

Run to time: 5msec step size: 0.01msec

DOUBLE ENDED CLIPPER

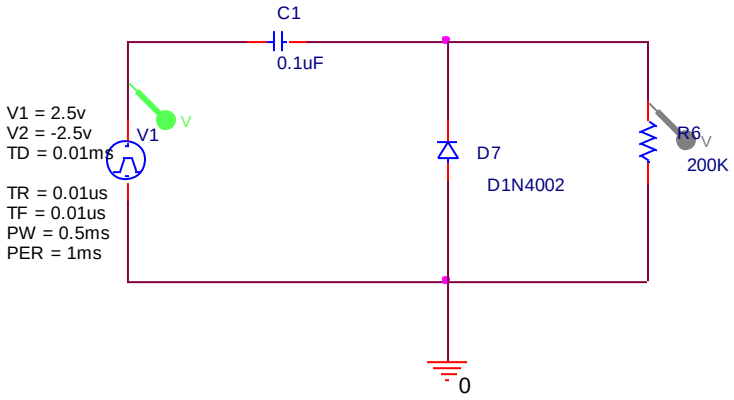




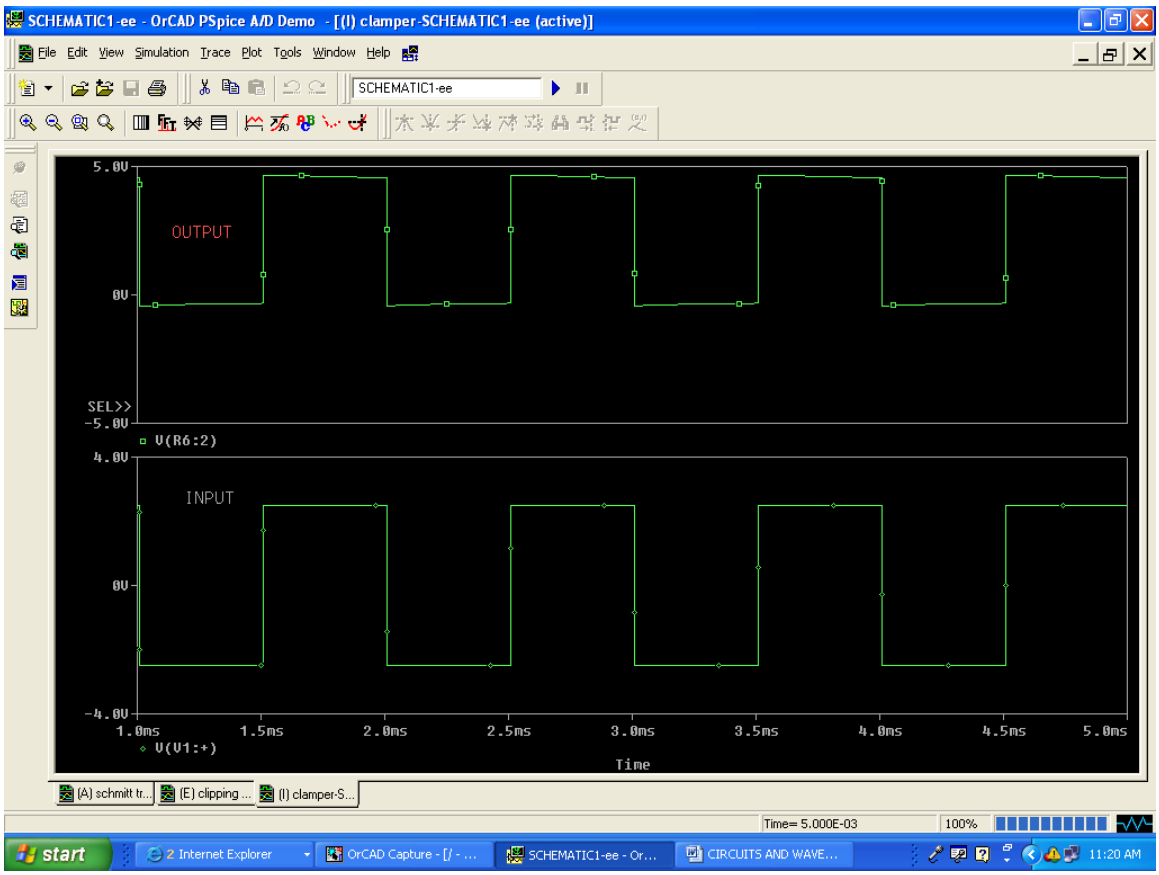
Type of analysis: TIME DOMAIN (TRANSIENT)

Run to time: 5msec step size: 0.01msec

WITHOUT
REFERENCE
VOLTAGE



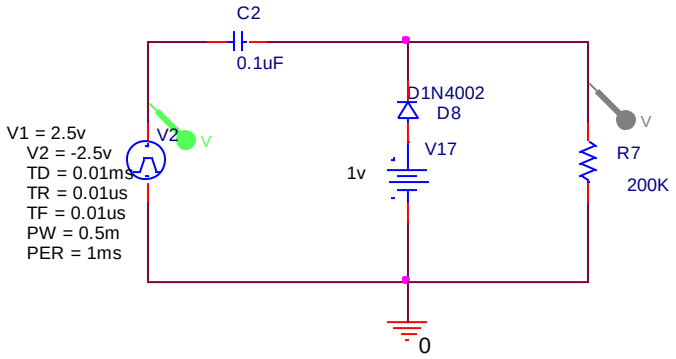
POSITIVE CLAMPER WITHOUT REFERENCE



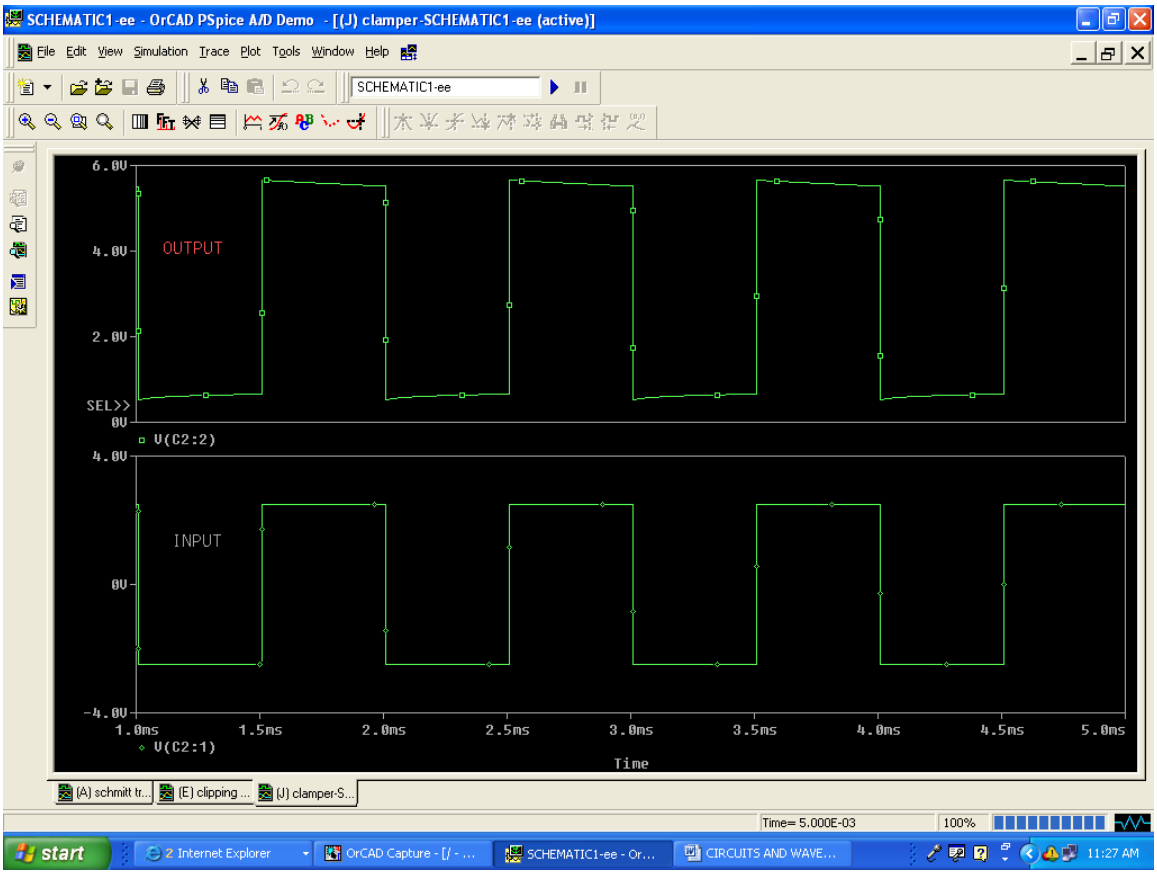
Type of analysis: TIME DOMAIN (TRANSIENT)

Run to time: 5msec step size:0.01msec

WITH
REFERENCE
VOLTAGE



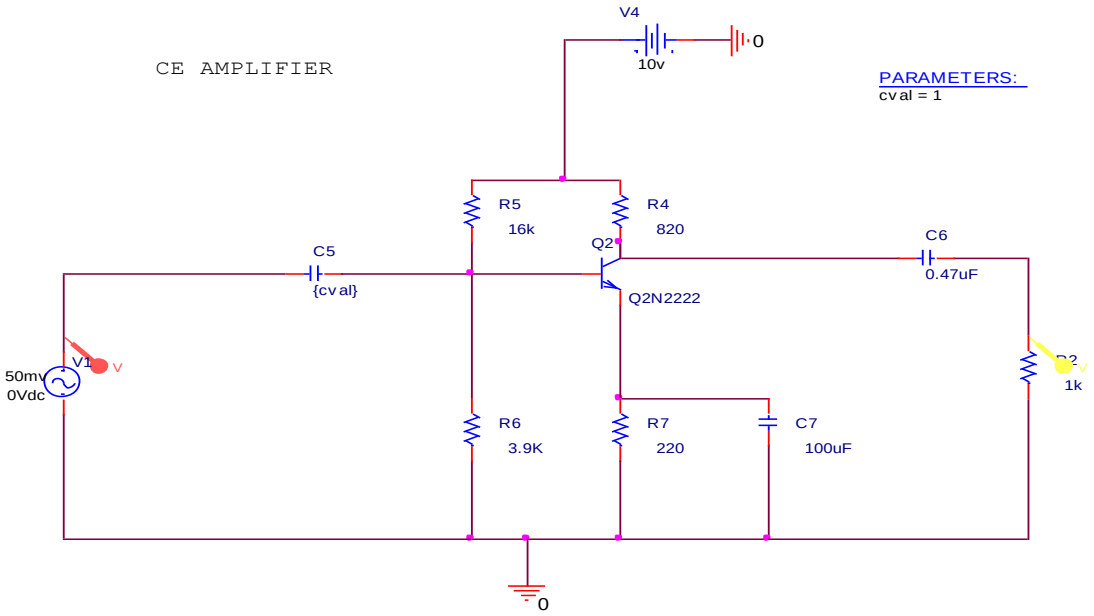
POSITIVE CLAMPER WITH REFERENCE

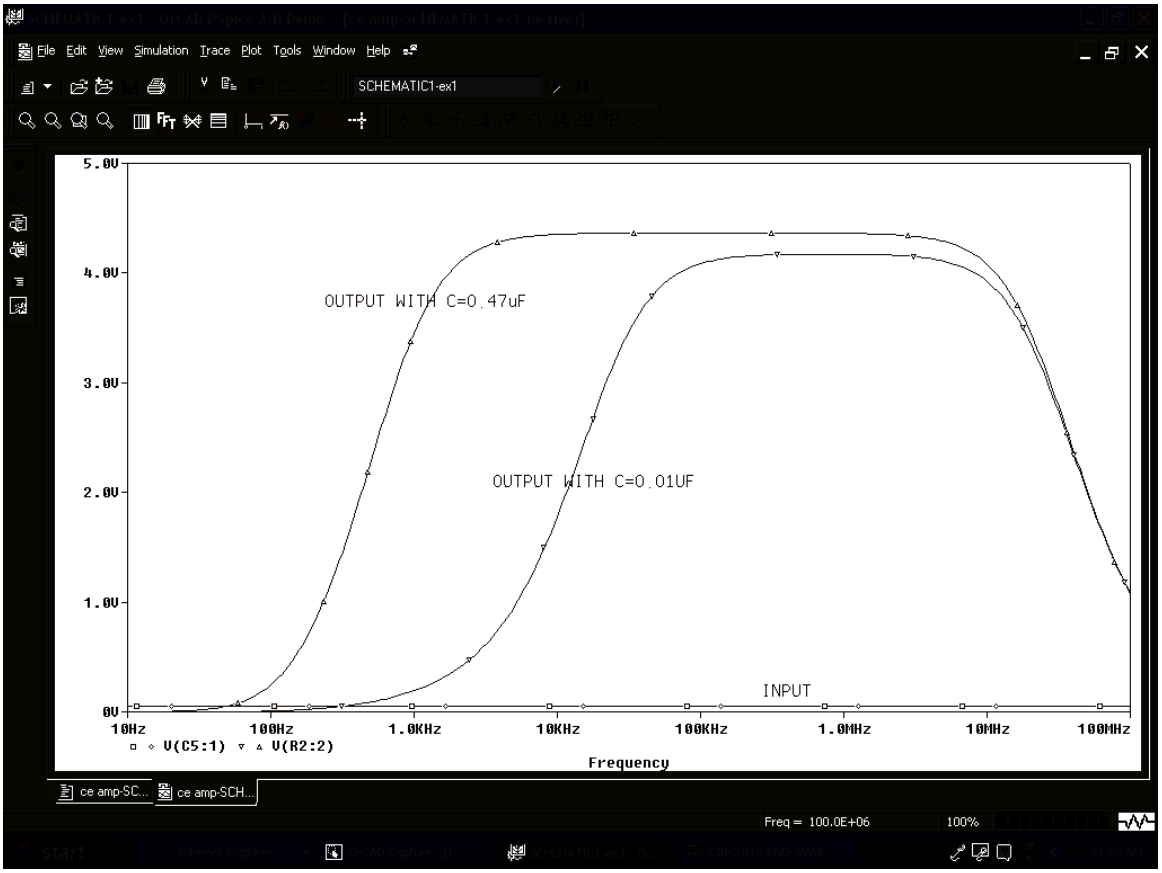


Type of analysis: TIME DOMAIN (TRANSIENT)

Run to time: 5msec step size:0.01msec

2b. Design and build the CE amplifier circuit using a simulation package and determine the voltage gain for two different values of supply voltage and for two different values of emitter resistance.

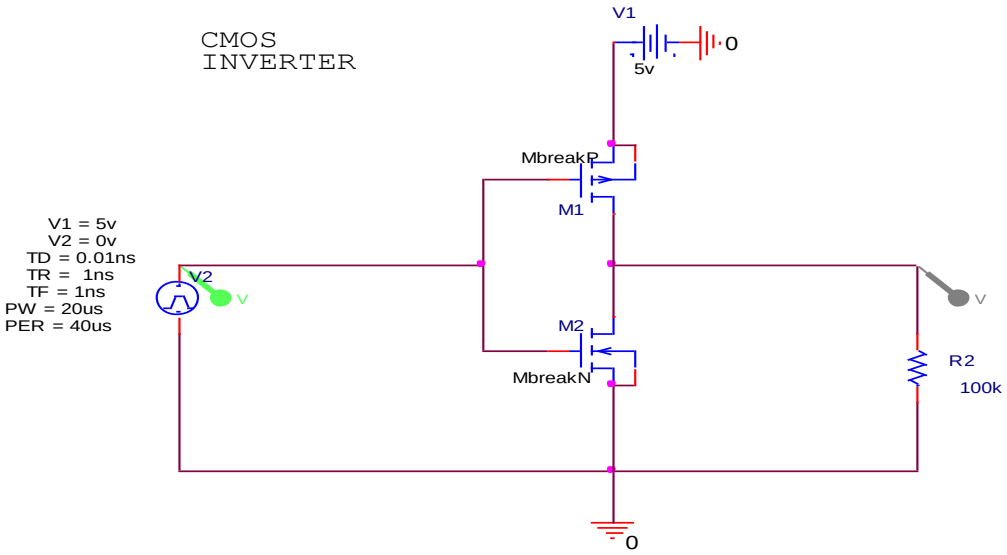


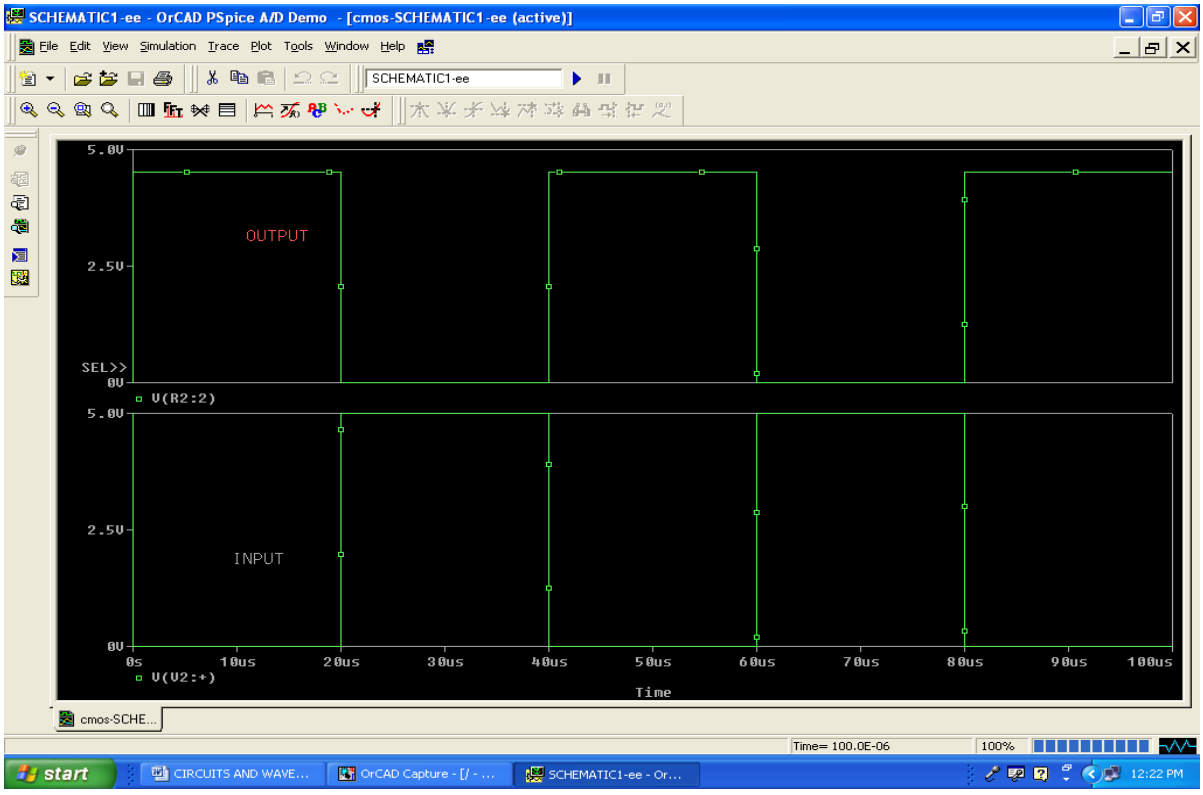


Type of analysis: Ac Sweep, Sweep type: logarithmic

Start frequency:10hz End frequency:10meg points per decade:40

3b. Design and build CMOS inverter using a simulation package and verify its truth table.

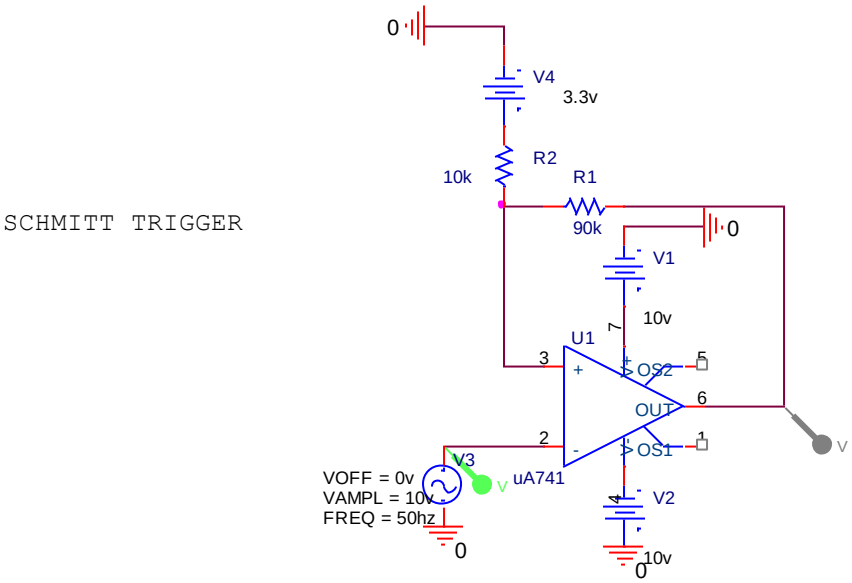


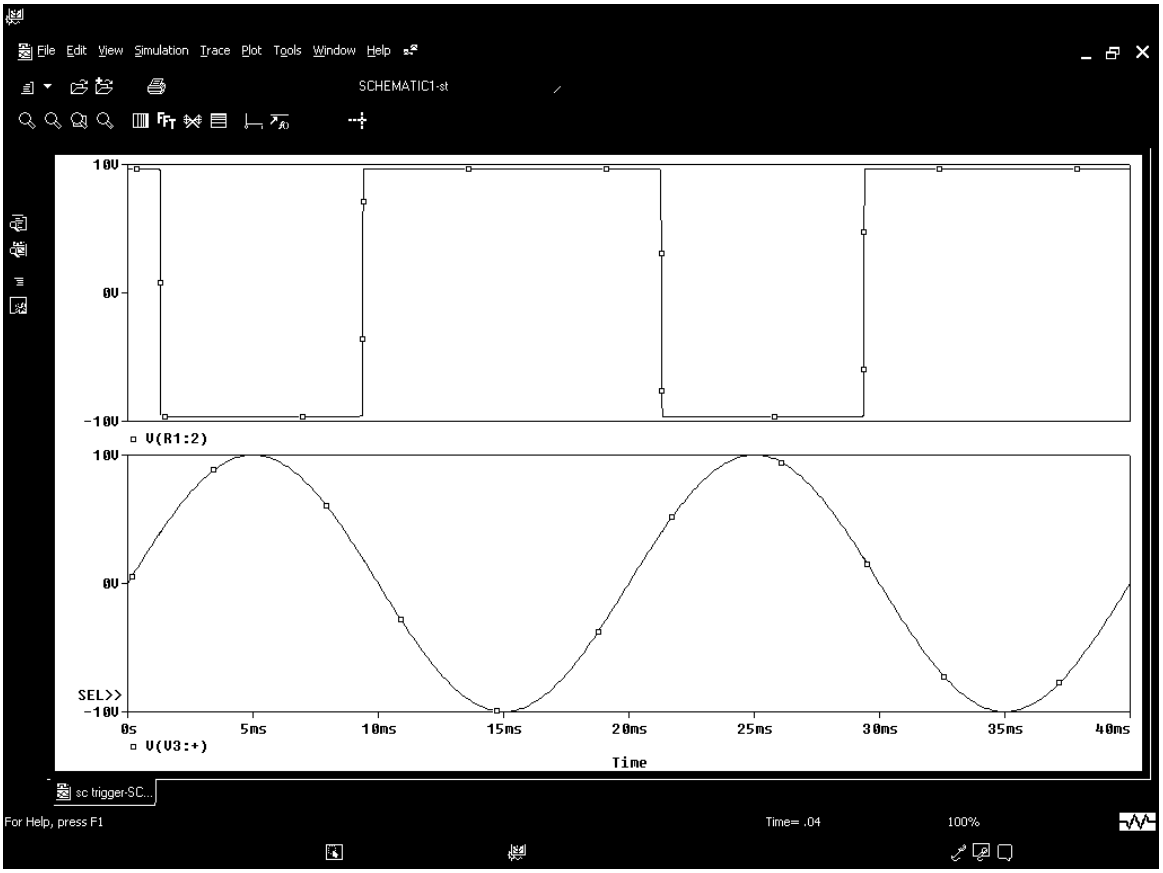


Type of analysis: TIME DOMAIN (TRANSIENT)

Run to time: 100usec step size:0.1usec

4b. Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working..

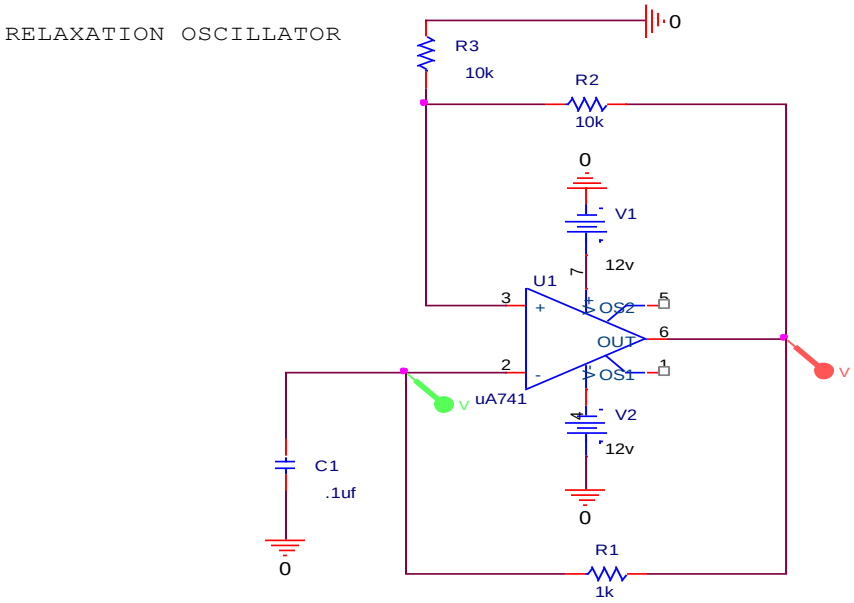




Type of analysis: TIME DOMAIN (TRANSIENT)

Run to time: 40msec step size:0.1msec

5b. Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and demonstrate the changes in frequency when all resistor values are doubled.



TYPE OF ANALYSIS : TIME DOMAIN
RUN TO TIME : 4ms MAXIMUM STEP SIZE : 0.01ms

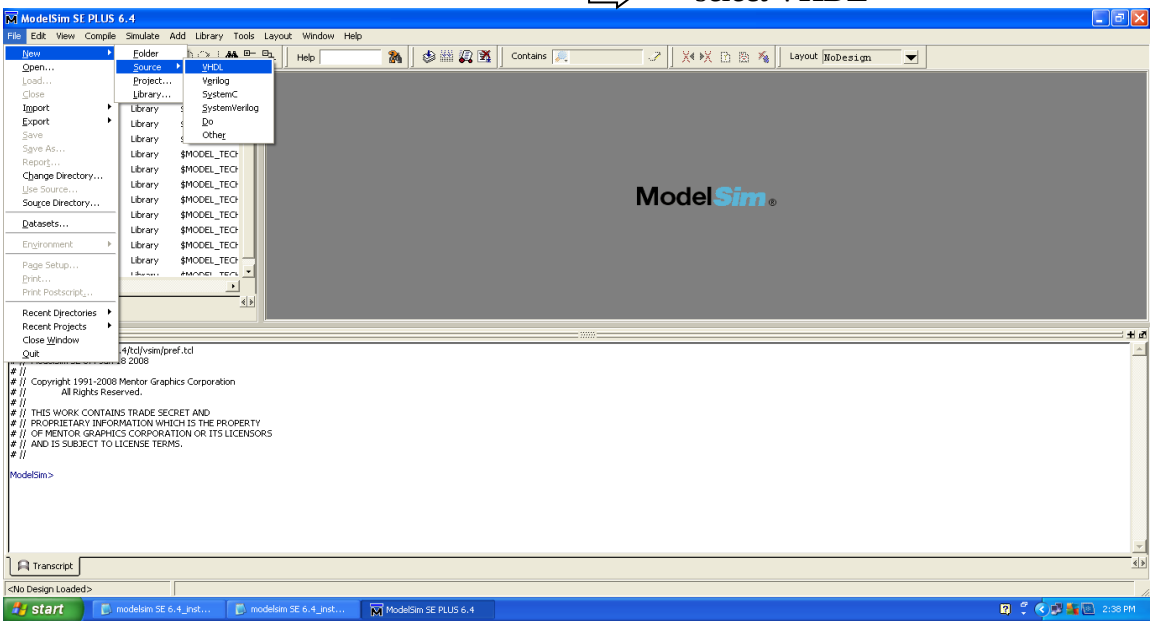
Logic Design with Model Sim Software (VHDL)

Steps to write VHDL code and to simulate in Model Sim

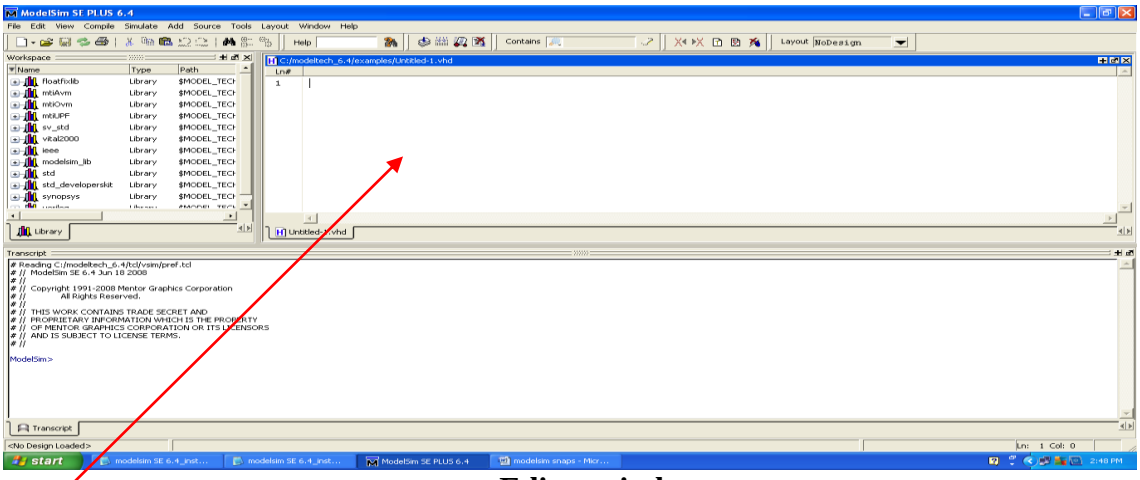
1. Double click on ModelSim icon on your desktop.
2. Goto **File menu**, select **New**,

   ↳ select **source**

   ↳ select **VHDL**

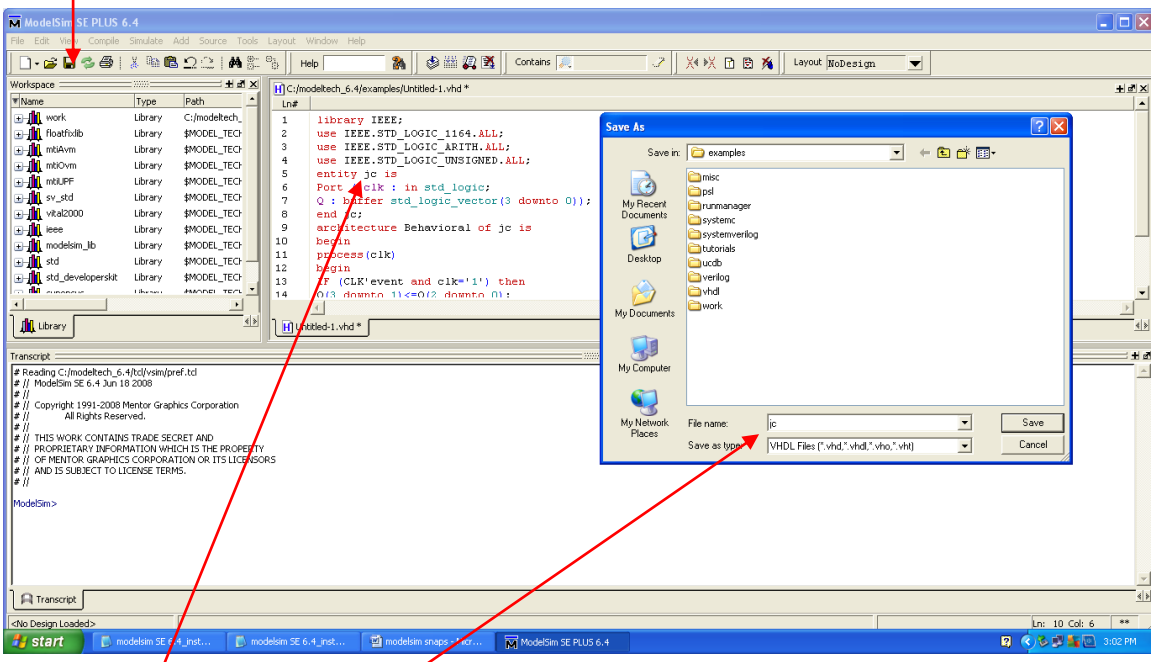


3. **You will get text editor where you can type VHDL code and save.**

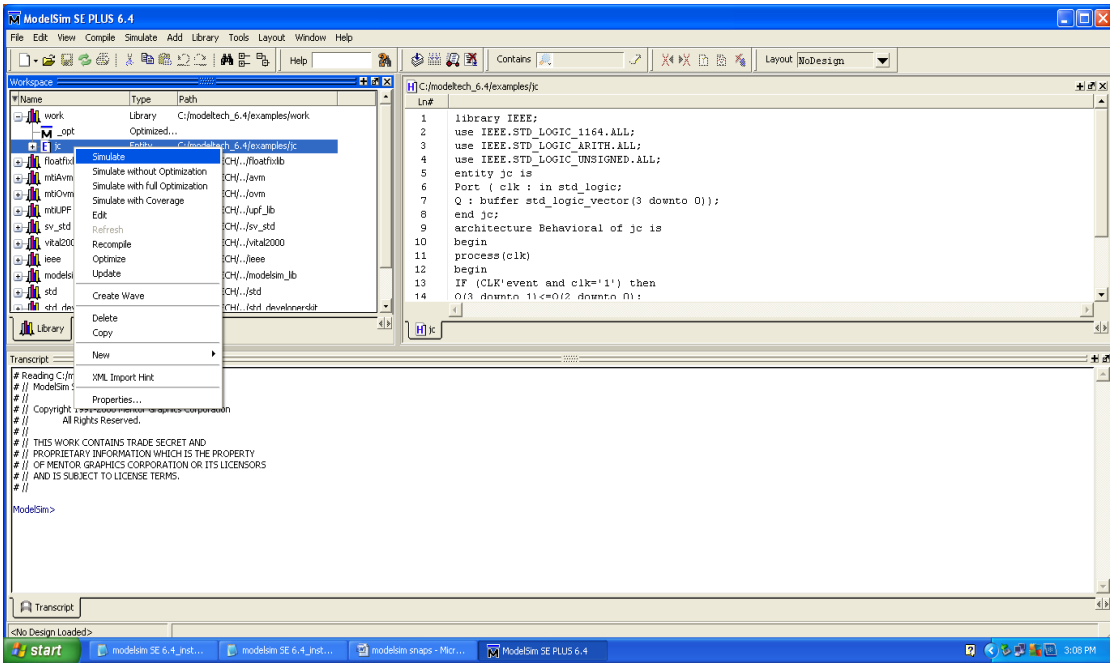


Editor window

Click on save button

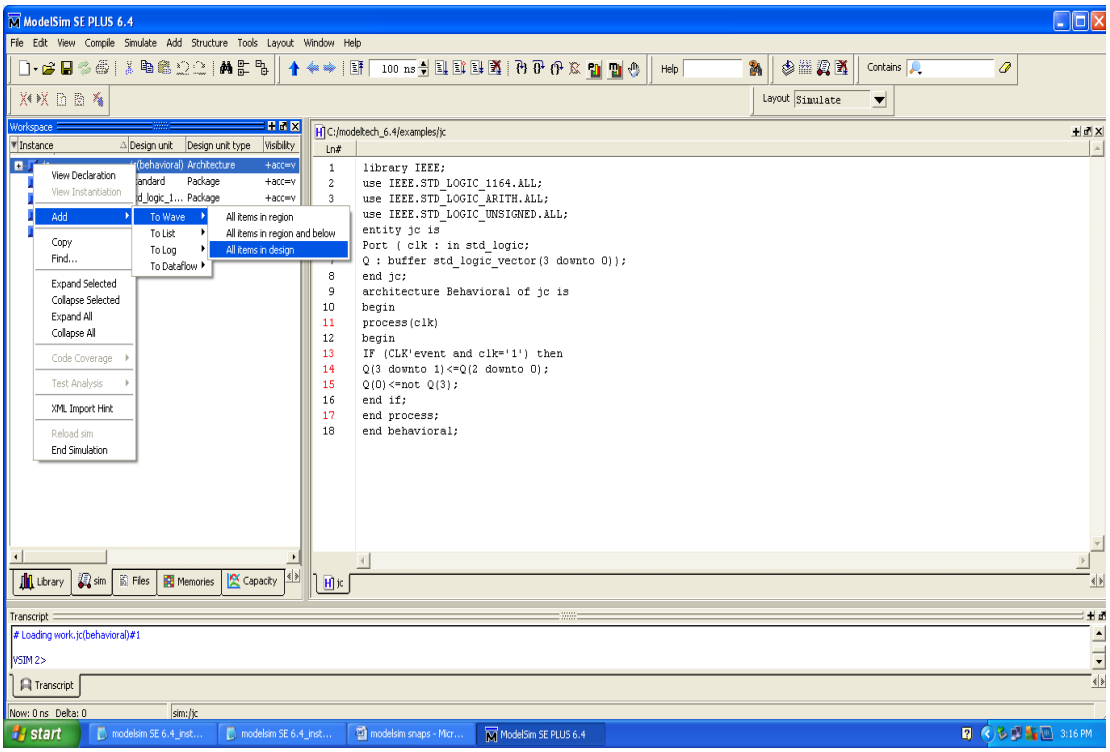


4. After saving click on **View** and select **Workspace.**
5. Click on **work, right click** on your **file,** choose **simulate** option**.**

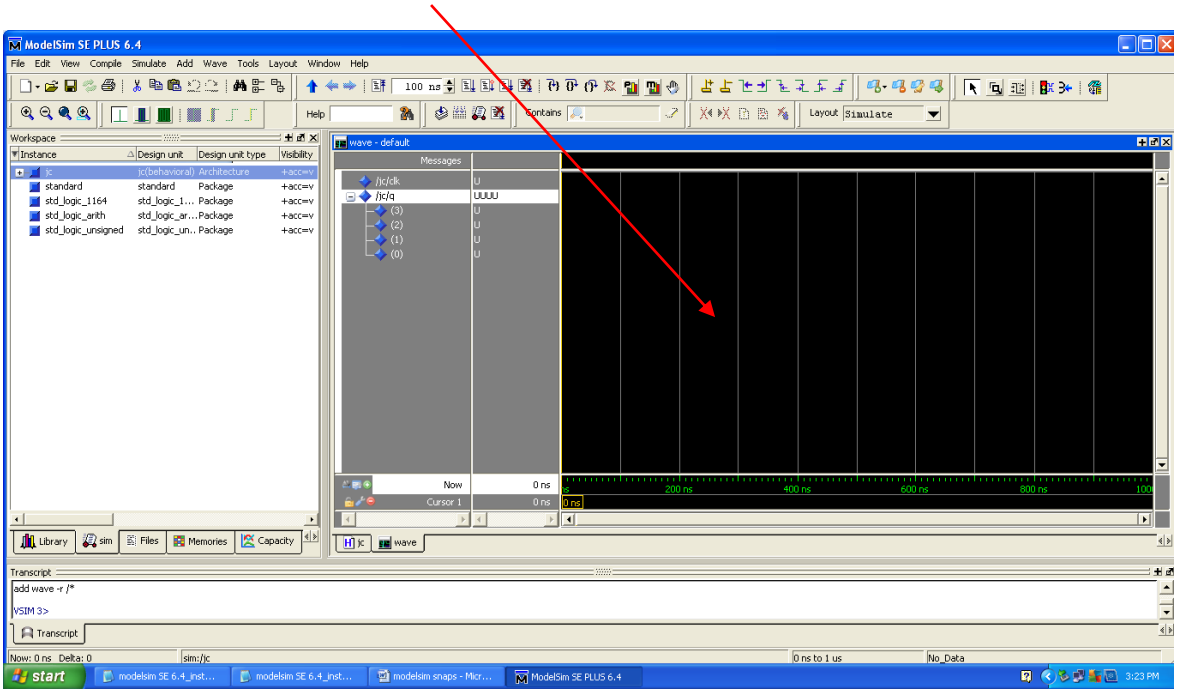


6. Select **work space instance, right click on file,**

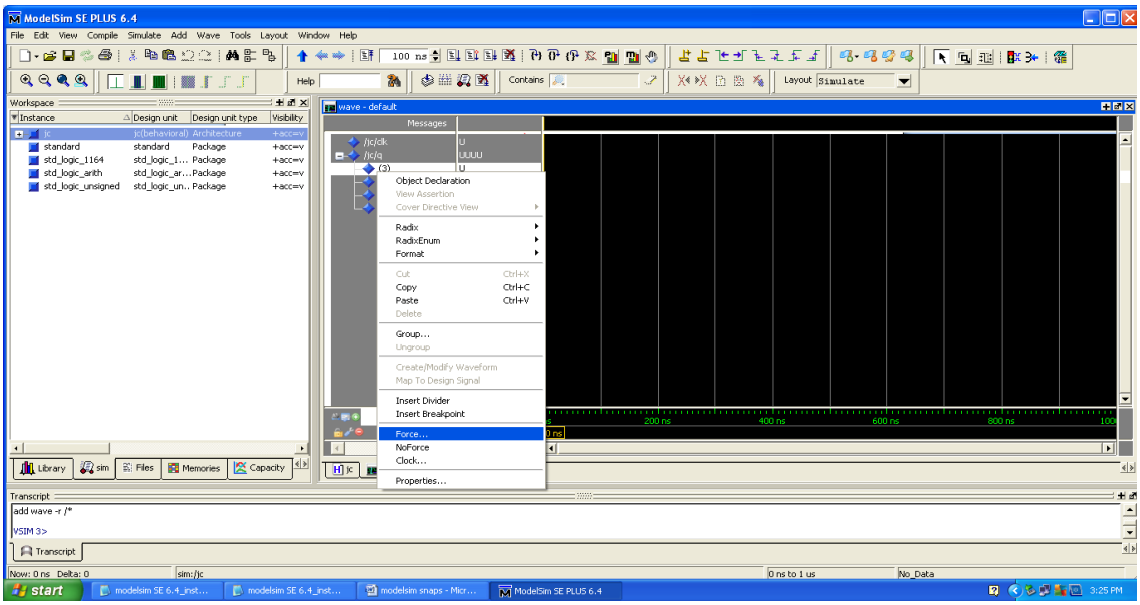
ADD ⇨ To wave ⇨ All items in design

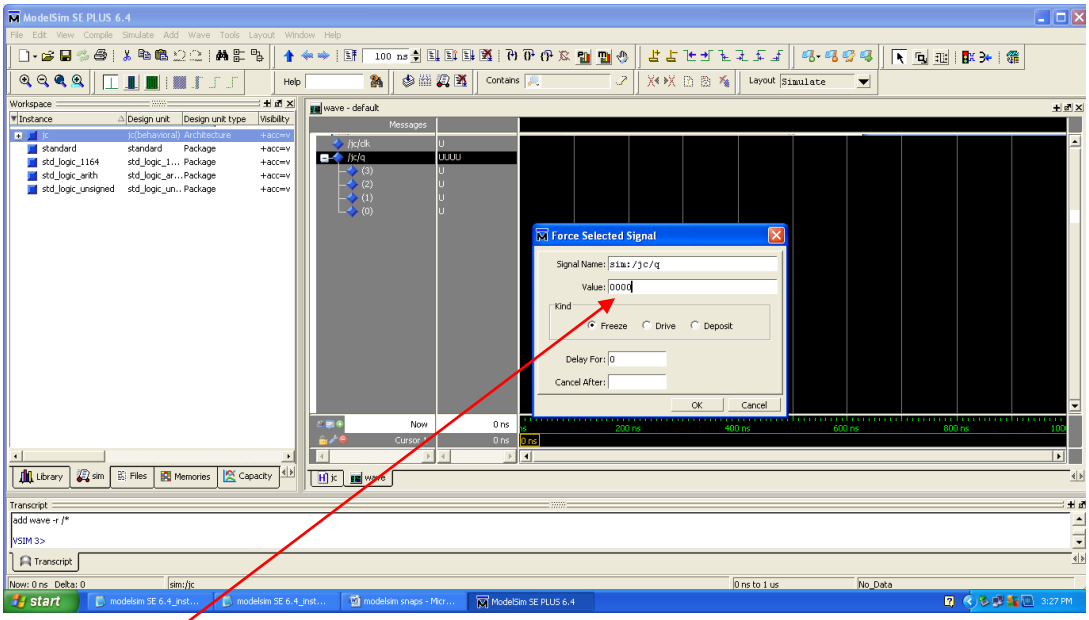


You will get waveform window

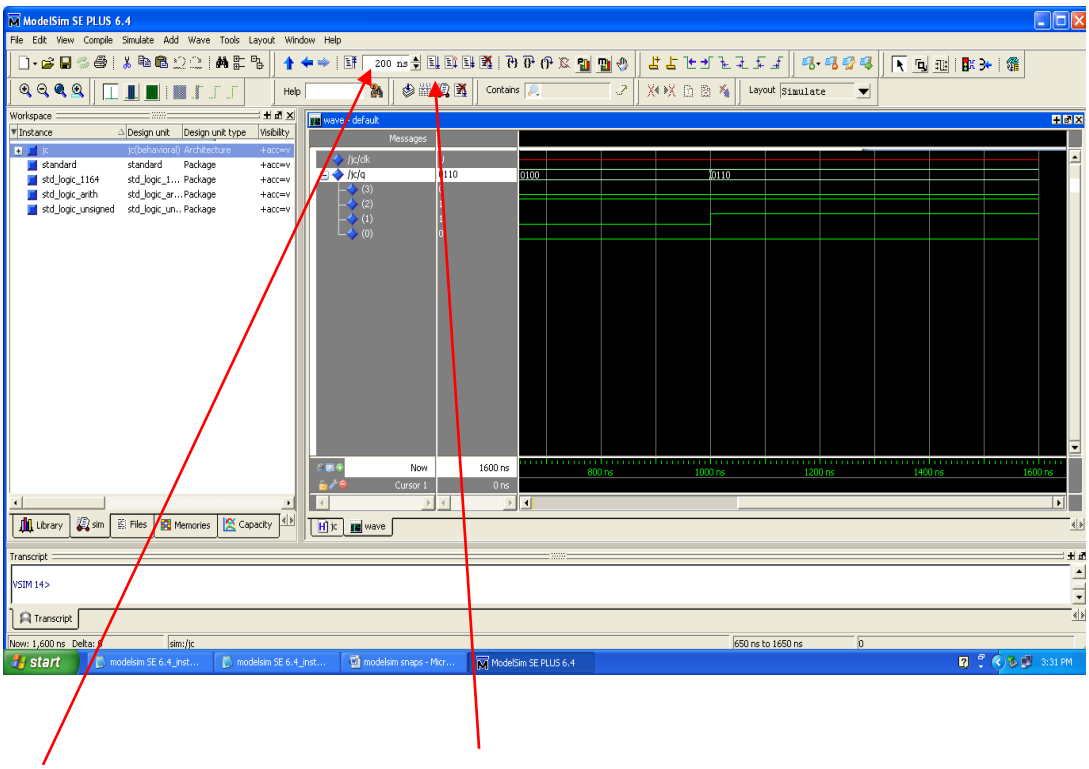


To assign the values**, right click on entity** and select **Force.**





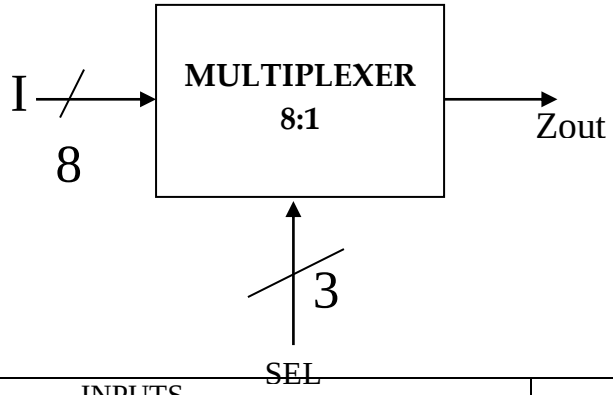
Assign the values for all the bits and click **OK.**



Set the **time** delay

Click on **Run** button

7b. Design and develop the verilog/VHDL code for 8:1 MUX. Simulate and verify its working.



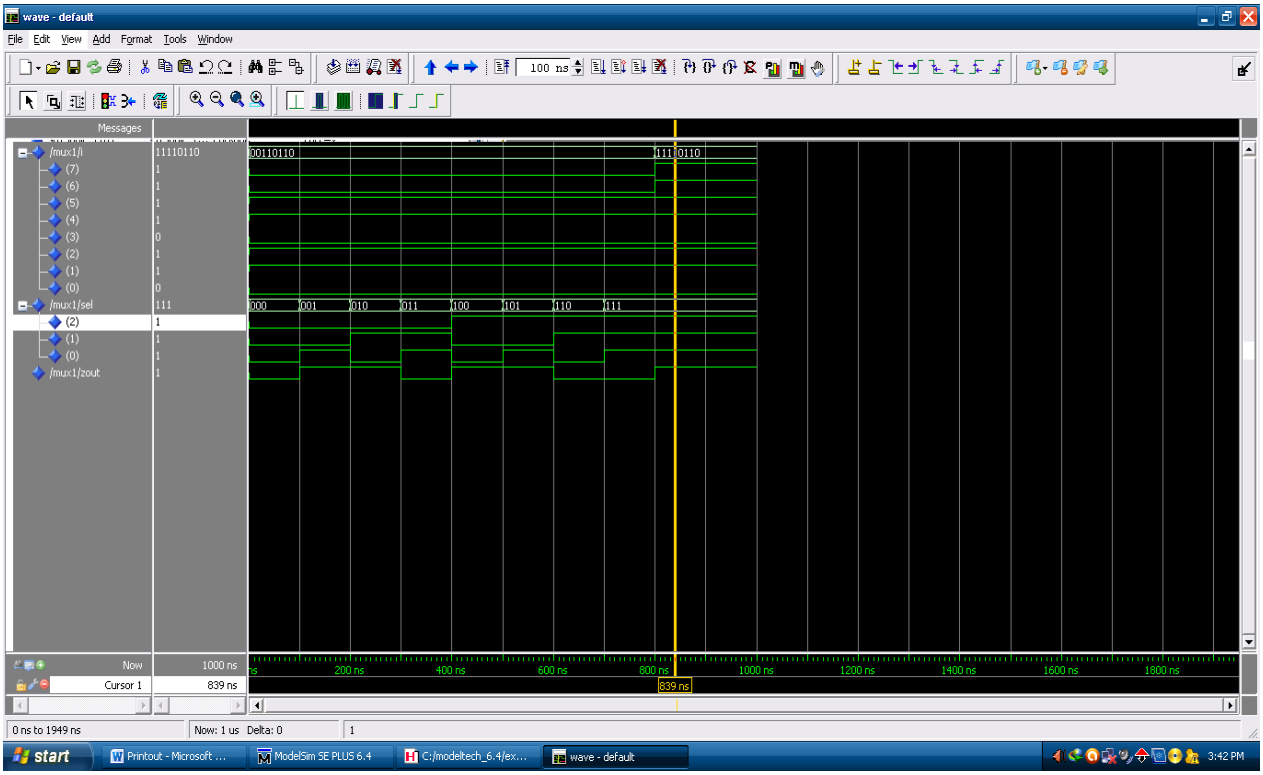
TruthTable

INPUTS			OUTPUTS
SEL (2)	SEL (1)	SEL (0)	Zout
0	0	0	I(0)
0	0	1	I(1)
0	1	0	I(2)
0	1	1	I(3)
1	0	0	I(4)
1	0	1	I(5)
0	1	1	I(6)
1	1	1	I(7)

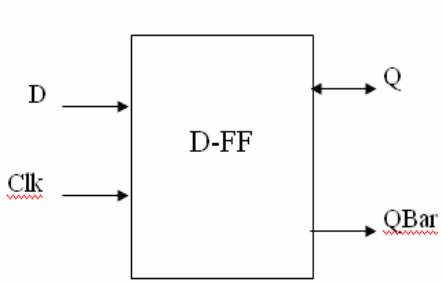
-- VHDL code for 8 to 1 mux (Behavioral modeling).

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mux1 is
   Port ( I : in std_logic_vector(7 downto 0);
          sel : in std_logic_vector(2 downto 0);
          zout : out std_logic);
end mux1;

architecture behavioral of mux1 is
begin
        zout <=   I(0) when sel="000" else
                  I(1) when sel="001" else
                  I(2)  when sel="010" else
                  I(3)  when sel="011" else
                  I(4)  when sel="100" else
                  I(5)  when sel="101" else
                  I(6)  when sel="110" else
                  I(7);
end behavioral;
```

Output:



8b. Design and develop the verilog/VHDL code for DFF with positive edge triggering. Simulate and verify its working.



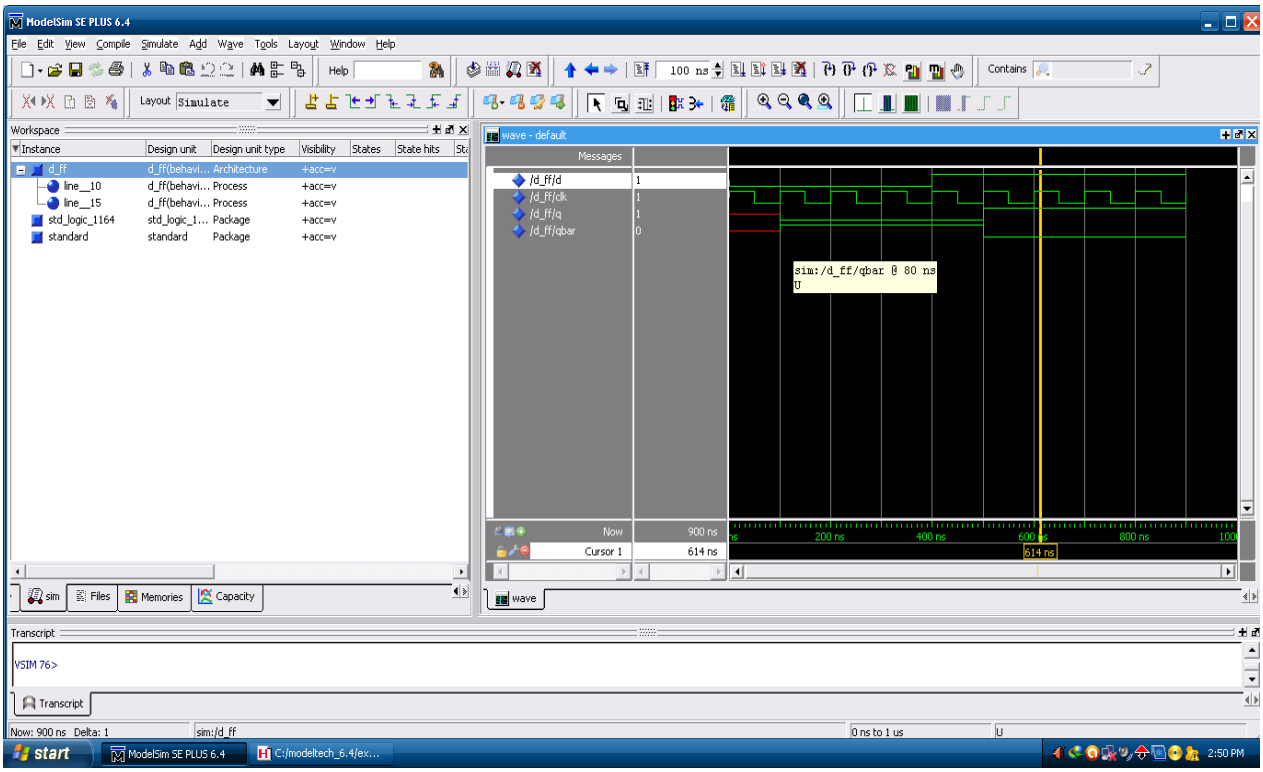
TruthTable

INPUT	OUTPUTS	
D	Q	QBar
0	0	1
1	1	0

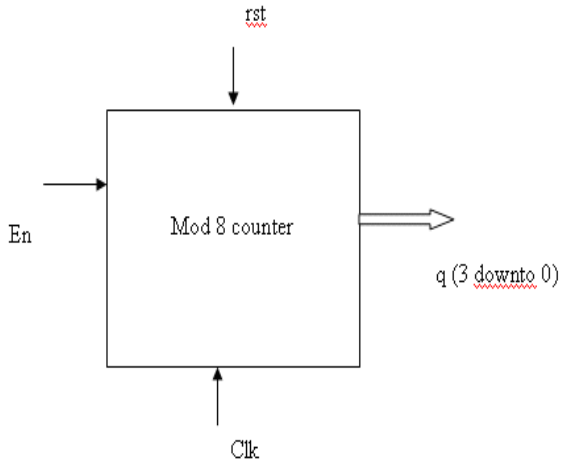
```
--VHDL code for D Flip Flop Counter.

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity d_ff is
    Port ( D,Clk : in std_logic;
           Q : inout std_logic;
           Qbar : out std_logic);
end d_ff;

architecture behavioral of d_ff is
begin
    process(clk)
```

```
    begin
      if rising_edge(clk) then
      Q<= D;
      end if;
    end process;
  Qbar<= not Q;

end behavioral;
```

Output:



9b. Design and develop the verilog/VHDL code for mod 8 up counter simulate and verify its working.



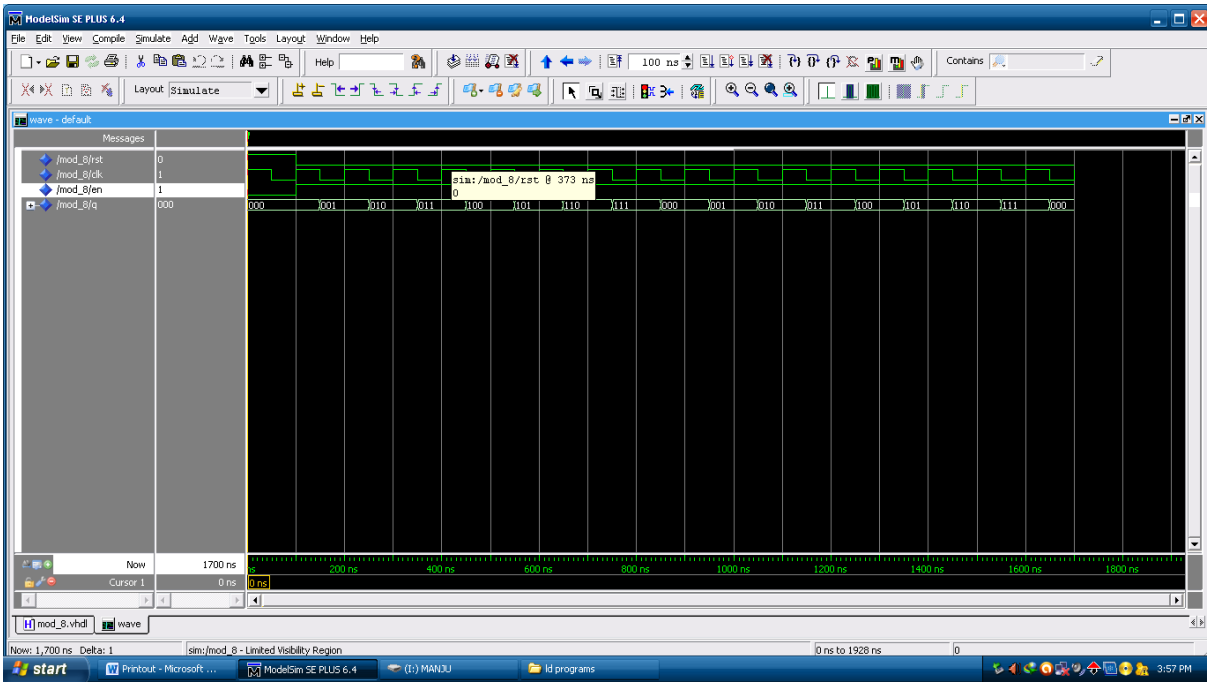
Truth Table

rst	Clk	En	Q
1	X	0	0000
0	1	1	0001
0	1	1	0010
0	1	1	0011
0	1	1	0100
0	1	1	0101
0	1	1	0110
0	1	1	0111

--VHDL code for Mod-8 Counter.

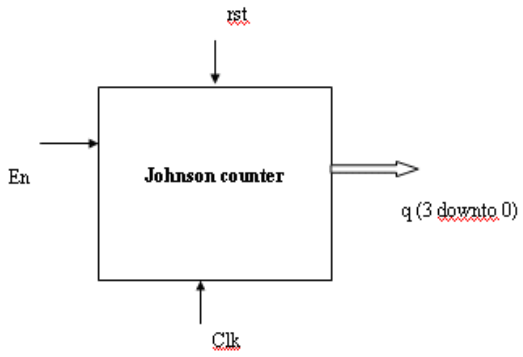
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mod_8 is
        Port ( rst, clk, en: in std_logic;
                q : inout std_logic_vector(3 downto 0));
end mod_8;

architecture behavioral of mod_8 is
   begin
        process(clk,rst) is
        begin
                if rst='1' then q<="0000";
                elsif rising_edge(clk) then
                   if en='1' then
                   Q<=Q+1;
                   end if;
                   if Q="0111" then
                   Q<= "0000";
                   end if;
               end if;
            end process;
end behavioral;
```

Output:



10b. Design and develop the verilog /VHDL code for switched tail counter.Simulate and verify its working.

Truth Table



rst	clk	en	Q
1	0	0	0000
0	1	1	0001
0	1	1	0000
0	1	1	1000
0	1	1	1100
0	1	1	1110
0	1	1	1111
0	1	1	0111
0	1	1	0011

--VHDL code for Johnson counter.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity jc is
    Port ( clk, en, rst : in std_logic;
           q : inout std_logic_vector(3 downto 0));
end jc;
```

```
architecture behavioral of jc is
begin
   Process(clk,rst)
   begin
      if rst='1' then q<="0001";
      elsif rising_edge (clk) then
          if en='1' then
          q<=(not q(0)) & q(3 downto 1);
          end if;
      end if;
   end process;

end behavioral;
```

Output: