17333

Seat No.

Instructions – (1) All Questions are *Compulsory*.

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data, if necessary.

(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. a) **Attempt any <u>SIX</u> of the following:**   **12**

    i) State two advantages of digital system over analog system.

    ii) Define with respect to digital ICs:

       1) Fan-in

       2) Noise immunity.

    iii) State any two boolean laws.

    iv) Draw symbol, logical expression and truth table of EX-OR gate.

    v) Convert $(57)_{10}$ into binary equivalent.

    vi) Derive AND gate and OR gate using NAND gates only.

    vii) Draw the truth table of digital comparator IC 7485.

    viii) Define the following specifications of A to D converter:

       i) Resolution

       ii) Conversion time.

b) **Attempt any <u>TWO</u> of the following:**   **8**

    i)   Subtract using 1's complement method:

        1) $(11011)_2 - (1010)_2$

        2) $(10111)_2 - (11000)_2$

    ii)   State and prove Demorgan's theorems.

    iii) Convert the following:

        1) $(11001)_2 = (\ ?\ )_{10}$

        2) $(10101)_2 = (\ ?\ )_8$

        3) $(37)_8 = (\ ?\ )_2$

        4) $(5AC) = (\ ?\ )_2$

2.   **Attempt any <u>FOUR</u> of the following:**   **16**

    a) Derive NOT gate and AND gate using NOR gates only.

    b) Simplify the following Boolean expressions using Boolean laws:

       i) $A\overline{B} + \overline{A}B + AB + \overline{A}\,\overline{B}$

       ii) $(A+B)\cdot(A+\overline{B})\cdot(\overline{A}+B)$

    c) Perform the following binary operations.

       i) 111.01×110

       ii) $11001 \div 101$

    d) Design a half subtractor circuit using K-map.

    e) Minimize the following boolean expression using K-map.

       $Y = \Sigma m(1,3,5,7,8,10,14)$

       Draw the logical diagram of minimized expression using logic gates.

    f) Draw the block diagram of octal to binary encoder and write its truth table.

Marks

3. **Attempt any FOUR of the following:** 16

   a) Implement the logical expression using gates.

   $$Y = \overline{A}\,\overline{B} + \overline{A}\,C + B\,\overline{C}$$

   b) Draw logic diagram of 1:4 demultiplexer. Write truth table of it.

   c) Design 16:1 multiplexer using 4:1 multiplexers only.

   d) Convert the following boolean expression into its standard forms:

   i) $Y = A\,\overline{B} + A\,C + \overline{B}\,C$

   ii) $Y = (A + \overline{B}) \cdot (A + C) \cdot (B + \overline{C})$

   e) What are the different triggering methods used in flip flops?

   f) What is race around condition in JK flip flop and how it can be eliminated?

4. **Attempt any FOUR of the following:** 16

   a) Draw the logical diagram of MOD-12 counter and describe its operation. Write its truth table.

   b) State any four specifications of A to D converter.

   c) Draw the logic circuit diagram of clocked SR flip flop using NAND gates. Write its truth table.

   d) Explain the function of preset and clear terminals in JK flip flop. Write truth table of it.

   e) Classify memories. Compare RAM and ROM on two points.

   f) Draw the circuit diagram of weighted resistor type D to A converter. Describe its working.

Marks

5. **Attempt any <u>FOUR</u> of the following:** 16

a) Perform the following BCD arithmetic:

  i) $(65)_{10} + (52)_{10}$

  ii) $(74)_{10} - (36)_{10}$

b) Draw the logic diagram of D type flip flop using NAND gates. Write its truth table.

c) Design a circuit using basic logic gates to realize the following function.

$$Y = \overline{A}B + AC + \overline{B}C$$

d) Draw the logical circuit diagram of 3 bit asynchronous up counter and describe its operation.

e) Draw the block diagram of BCD to seven segment decoder using IC 7447. Write truth table of it.

f) Draw the block diagram of SISO shift register and describe the operation.

6. **Attempt any <u>TWO</u> of the following:** 16

a) i) State the applications of multiplexer. 2

  ii) Design full adder circuit using K-map. Draw designed diagram using logic gates. 6

b) i) Compare combinational and sequential logic circuits on two points. 2

  ii) State the applications of shift registers. 2

  iii) Draw the block diagram of 4 bit PIPO shift register and describe its operation with truth table and timing diagram. 4

c) i) Draw the circuit diagram of successive approximation type A to D converter and describe its working. 4

  ii) A D to A converter has a full scale analog output of 12V with 4 bit binary inputs. Find the voltage corresponding to each analog step. 4

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3 Hours / 100 Marks