17320

21314

3 Hours/100 Marks

Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*

(2) Illustrate your answers with ***neat*** *sketches* ***wherever*** *necessary.*

(3) Figures to the ***right*** *indicate* ***full*** *marks.*

(4) Use of Non-programmable Electronic Pocket Calculator is ***permissible****.*

(5) Mobile Phone, Pager and any other Electronic Communication devices are ***not permissible*** *in Examination Hall.*

MARKS

1. Attempt **any ten** of the following : **20**

a) Convert given numbers :

i) $(110100)_2 = (...)_{Gray}$ ii) $(1111)_{Gray} = \cdots_B$

b) Draw the logic circuit diagram of 1 bit memory cell using NAND gate.

c) State the necessity of multiplexers.

d) Differentiate between RAM and ROM (any 2 points).

e) Subtract $(32)_{10}$ from $(85)_{10}$ using 2's complement binary arithmetic.

f) Give two applications of A/D converter.

g) Draw OR and AND gate using NAND gate only.

h) Classify memories on the basis of principle of operation.

i) Write truth table and the expressions of half subtractor.

j) Perform $(52)_{10} - (89)_{10}$ using 9's and 10's complement method.

k) Draw the truth table of following IC's

i) IC – 7432 ii) IC – 7486

l) Draw circuit diagram of 4 : 1 multiplexer.

m) Give various methods of D/A converter.

n) State the applications of Flip-Flops.

P.T.O.

MARKS

2. Attempt **any four** of the following : **16**

a) Perform the following operations :

i) $(11100)_2 \div (100)_2$ ii) $(1010.11)_2 \times (11)_2$

b) Design 32 : 1 multiplexer using 16 : 1 multiplexer and 2 : 1 multiplexer.

c) Draw the circuit diagram of S – R Flip-Flop using NAND gate and describe its working.

d) Simplify the following expression using Boolean laws.

i) $y = (A + B)(A + C)$ ii) $y = ABC + A\bar{B}C + AB\bar{C}$

e) How many bits are required for a resolution of 5 mV and full scale voltage in 15 V ?

f) Identify the following circuit as combinational circuit or sequential circuit.

i) 3 – bit ring counter ii) Full adder

iii) Clocked J-K F/F iv) 4 : 1 MUX

3. Attempt **any four** of the following : **16**

a) State and prove De-Morgan's 1st and 2nd theorem.

b) Describe the operation of single digit BCD adder using IC – 7483 with circuit diagram.

c) State the working principle of J–K Flip-Flop with neat diagram.

d) Minimize the following expression using K-map.

i) $f(w, x, y) = \sum m\,(0, 1, 2, 4, 6, 7)$

ii) $f(A, B, C, D) = \prod M\,(0, 2, 7, 8, 9, 10, 13)$

e) Describe with circuit diagram the working operation of static RAM cell.

f) Study the given circuit as shown in fig. no. 1 initial o/p condition is $Q_A Q_B Q_C = 010$, write truth table of output $Q_A Q_B Q_C$.

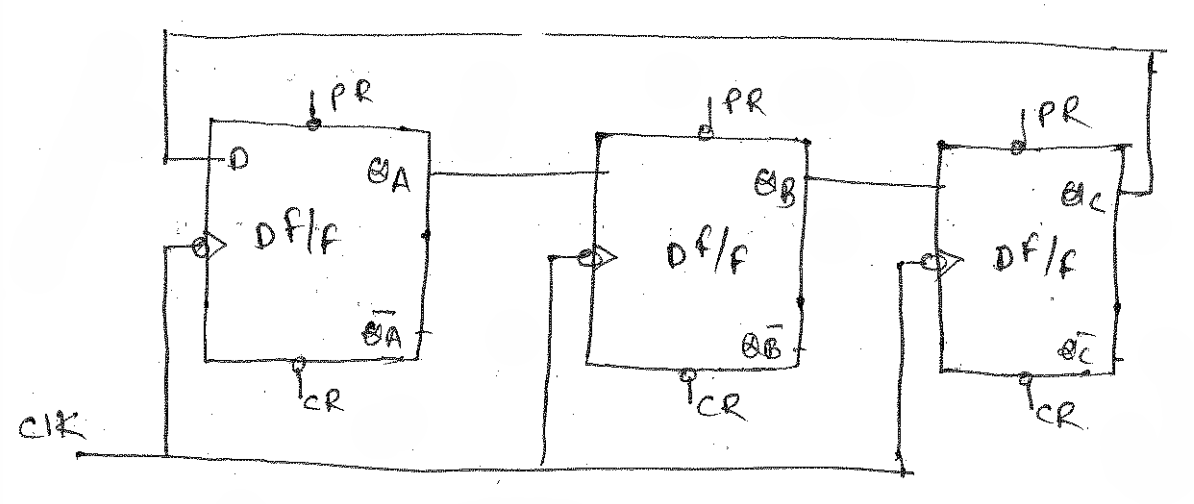

Fig No. 1

MARKS

4. Attempt **any four** of the following : **16**

   a) Encode the following decimal number in BCD code and excess-3 code.
      i) $(48)_{10}$ ii) $(228)_{10}$

   b) Describe R-2R ladder network method of D/A conversion with neat circuit diagram.

   c) Explain the operation of TTL logic using NAND gate.

   d) Design a full subtractor circuit using K-map with truth tables.

   e) For 3 bit synchronous up-counter.
      i) Draw circuit diagram (use T-Flip Flop)
      ii) Write truth table

   f) Draw block diagram of decimal to BCD encoder with its truth table.

5. Attempt **any four** of the following : **16**

   a) Compare combinational and sequential logic circuits. (any four points)

   b) Draw pinout diag. of 2716 EPROM and state its operation.

   c) Explain race around condition in J-K Flip-Flop.

   d) Describe the working of dual slope A/D converter.

   e) Compare TTL and CMOS logic families.

   f) In the given fig. 2, the control signal S_2S_3 of 1 : 4 demux changes from 00 through 11. Write its truth table.

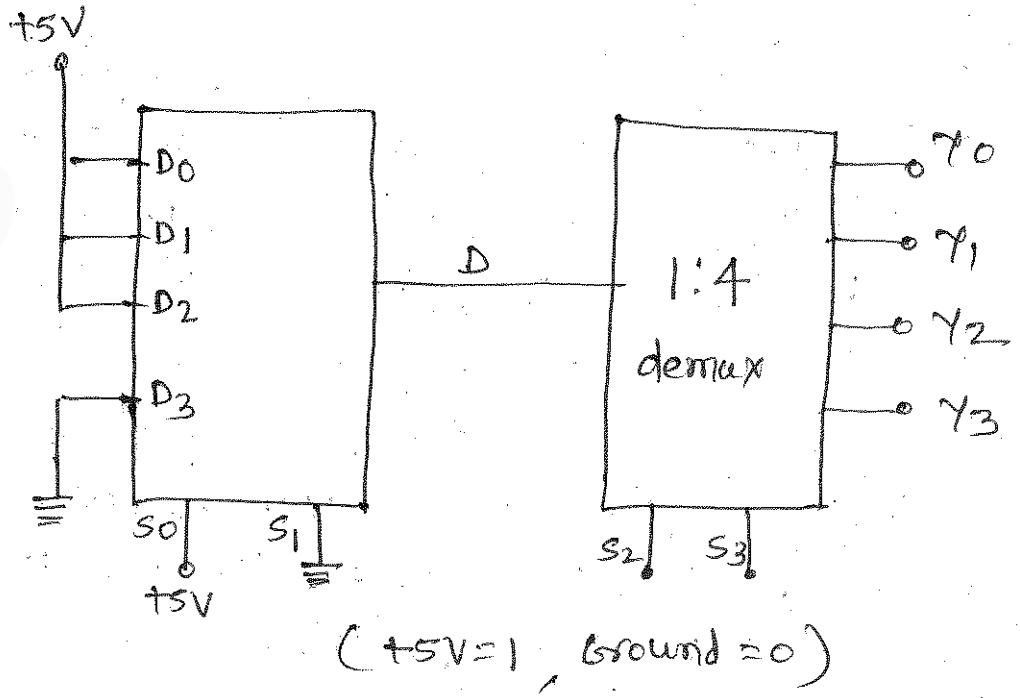

Fig. No. 2

MARKS

6. Attempt **any four** of the following : **16**

a) Add $(147)_{10}$ and $(284)_{10}$ in BCD code.

b) Explain the operation of 1 : 4 de-multiplexer using logic gate.

c) Describe operation of SIPO shift register with circuit diagram.

d) A RAM IC has 12 address lines and 8 data lines. If its first location has address 9000H what will be the address of the last location ?

e) Describe the working principle of successive approximation method ADC with block diagram.

f) For a given logical diagram, derive Boolean expression for output Y by simplifying it as much as possible.

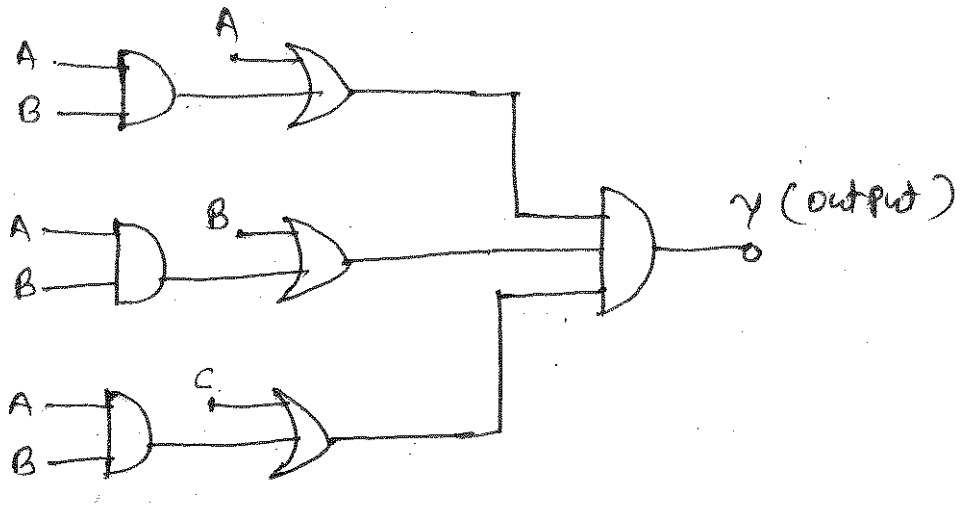

Fig. No. 3
